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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AS3715

Dual Power Path PMIC

General Description

The AS3715 is a compact System PMU supporting two Li-Ion batteries and up to 14 power rails.

The device offers advanced power management functions. All necessary ICs and peripherals in a battery powered mobile device are supplied by the AS3715. It features 3 DCDC buck converters, one DCDC buck controller, a 5V HDMI booster, a HV backlight boost controller with 3 current sinks as well as 8 LDOs (2 low noise). The different regulated supply voltages are programmable via the serial control interface. 3-4MHz operation with 0.47uH coils is reducing cost and PCB space.

AS3715 contains a linear or switch mode Li-Ion battery charger with constant current and constant voltage operation. The maximum charging current is 1.5A. An internal battery switch and an optional external switch are separating the battery during charging or whenever an external power supply is present. In addition a second external battery path can be controlled. With these switches it is also possible to operate with no or deeply discharged batteries.

A dual USB input current limiter can be used to control the current taken form the USB supplies or charger inputs. Additional features are a 30V OV protection and JEITA compliant battery temperature supervision with selectable NTC beta values.

The single supply voltage may vary from 2.7V to 5.5V.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits and Features

Following the general description are key benefits and features for AS3715.

Figure 1:
Added Value of Using AS3715

Benefits	Features
Compact design due to small coils for IO and memory voltage generation	• DCDC step down regulators (3-4MHz) - Output (0.6V-3.3V; 2x1A, 1x2A)
High current generation with external power stages to minimize PMIC power dissipation	• DCDC step down controller - DVM (0.6V-1.5V; 1x5A)
Multiple independent voltage rails for general purpose IO supplies	• 8 universal LDOs - 6x universal IO range(0.8-3.3V; 0.3A) - 2x analog (1.2-3.3V; 0.25A)

Benefits	Features
Backlight boost controller for multiple display configurations or fixed voltage supplies	• Current mode boost controller with two current sinks. • Constant voltage operation and over-voltage protection • 3 programmable current sinks (max. 40mA) • Possible external PWM dimming input (DLS, CABC)
Self-contained Li-Ion battery charger with dual battery and USB path control.	• 1.5A max charging current • Dual battery control • Dual charger input with current limiters • Soft-, Trickle-, Constant Current and Constant Voltage operation (3.5 .. 4.44V) • Linear and switch mode charging • Charger timeout and JEITA temperature supervision • NTC beta selection
Save supervision in HW which works also without a processor.	• Supervisor with interrupt generation and selectable warning levels - Automatic battery monitoring - Automatic temperature monitoring - Power supply supervision for DCDC
Flexible multi-purpose IOs for general control tasks.	• General Purpose IOs - ADC input - Wake-up/stand-by input - PWM input/output - Low battery and power good status
Enables the processor to check the actual system state in detail.	• ADC with internal and external sources
Flexible and fast adaptation to different processors/applications.	• OTP programmable Boot and Power-down sequence
Power saving control according to the processor needs.	• Stand-by function with programmable sequence and voltages
Self-contained start-up and control dual battery and dual USB operation. Safety shutdown feature.	• Control Interface - I^2C control lines with watchdog - ONKEY with 4/8s emergency shut-down - POR with RESET I/O
Dedicated packages for specific applications. Optimization for PCB cost or size.	• Package - 81-ball WL-CSP 0.4mm pitch

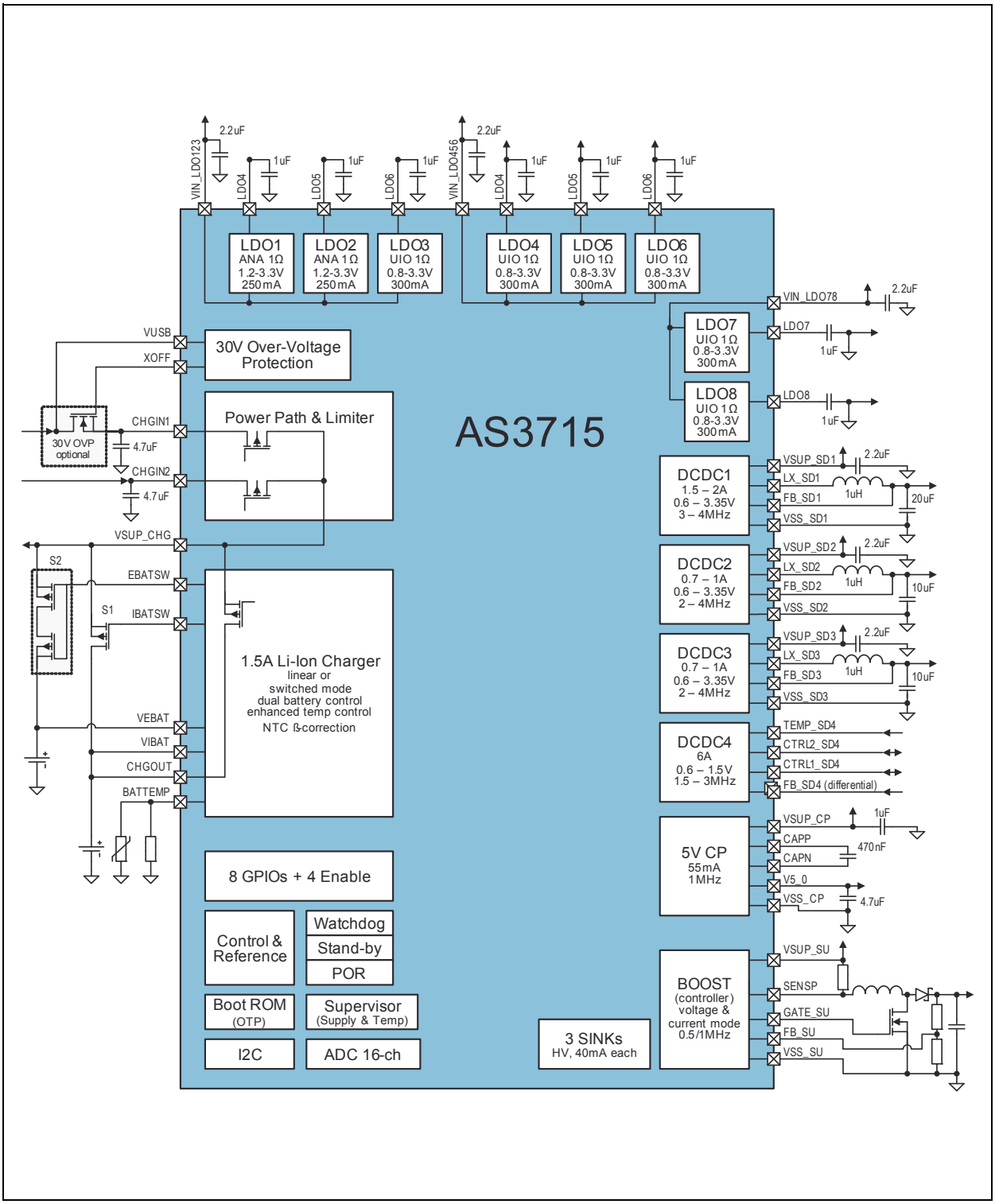
Applications

The device is suitable for digital still cameras, outdoor action cameras, digital movie cameras, general Li-Ion battery powered mobile devices.

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
Block Diagram for AS3715



Block Diagram: Shows the main function blocks of the AS3715.

Pin Assignments

Figure 3:
Pin Assignment

	1	2	3	4	5	6	7	8	9
A	VSS_SU	SENSEN_SU	LDO6	LDO5	LDO4	CHGIN1	VSUP_CHG	CHGIN2	CHGOUT
B	FB_SD4_N	GATE_SU	VIN_LDO456	GPIO8	EN2	CHGIN1	VSUP_CHG	CHGIN2	CHGOUT
C	CTRL1_SD4	TEMP_SD4	VSUP_SU	FB_SD4_P	FB_SU	EN1	IBATSW	XOFF	VSUP_SD3
D	CAPN	VSS_CP	VEBAT	CTRL2_SD4	SENSEP_SU	EN4	EBATSW	FB_SD3	LX_SD3
E	V5_0	CAPP	VSUP_CP	VIBAT	BATTEMP	VUSB	EN3	FB_SD2	VSS_SD3
F	V2_5	LDO3	CREF	GPIO7	GPIO6	SDA	VSS_ANA	VSSA	VSS_SD2
G	LDO2	VIN_LDO123	GPIO5	GPIO2	GPIO1	CURR3	FB_SD1	VSUP_SD2	LX_SD2
H	LDO1	GPIO3	SCL	ONKEY	VIN_LDO78	CURR2	LX_SD1	VSUP_SD1	VSUP_SD1
J	GPIO4	XRES	VSUP_GPIO	LDO7	LDO8	CURR1	LX_SD1	VSS_SD1	VSS_SD1

Pin Assignment: Shows the top view pin assignment of the AS3715

Figure 4:
Pin Description

Pin #	Pin Name	I/O	Description	Max. Voltage	If not used
F6	SDA	DI	SPI digital input in SPI mode; Data IO in I²C mode.	VSUP	Open
H3	SCL	DI	SPI clock input in SPI mode; SCK input in I²C mode.	VSUP	Open
H4	ONKEY	DI	Input pin to startup with pull-down	5.5V	Define level
J2	XRES	DIO	IO pin for reset during active state	VSUP	Define level
F1	V2_5	AO	Output voltage of low power LDO V2_5	2.6V	Mandatory
F3	CREF	AIO	Bypass capacitor for the internal voltage reference; connect 100nF	1.8V	Mandatory
J3	VSUP_GPIO	S	Supply pin for GPIOs (connect to other VSUP pins)	5.5V	Mandatory
F7	VSS_ANA	AIO	Analog sense GND input (connect to VSSA on PCB)	-	Mandatory
G5	GPIO1	DIO	General purpose input/output pin	VSUP	Open
G4	GPIO2	DIO	General purpose input/output pin	VSUP	Open
H2	GPIO3	DIO	General purpose input/output pin	VSUP	Open
J1	GPIO4	DIO	General purpose input/output pin	VSUP	Open
G3	GPIO5	DIO	General purpose input/output pin	VSUP	Open
F5	GPIO6	DIO	General purpose input/output pin / optional current sink	VSUP	Open
F4	GPIO7	DIO	General purpose input/output pin / optional current sink	VSUP	Open
B4	GPIO8	DI	General purpose input/output pin	VSUP	Open
C6	EN1	DI	Input pin to startup with pull-down	5.5V	Open
B5	EN2	DI	Input pin to startup with pull-down	5.5V	Open
E7	EN3	DI	Input pin to startup with pull-down	5.5V	Open
D6	EN4	DI	Input pin to startup with pull-down	5.5V	Open
G2	VIN_LDO123	S	Supply pad for LDOs	5.5V	Mandatory
B3	VIN_LDO456	S	Supply pad for LDOs	5.5V	Mandatory
H5	VIN_LDO78	S	Supply pad for LDOs	5.5V	Mandatory
H1	LDO1	AO	Output voltage of LDO - PMOS_1	3.3V	Open

Pin #	Pin Name	I/O	Description	Max. Voltage	If not used
G1	LDO2	AO	Output voltage of LDO - PMOS_1	3.3V	Open
F2	LDO3	AO	Output voltage of LDO - PMOS_1	3.3V	Open
A5	LDO4	AO	Output voltage of LDO - PMOS_0.6	3.3V	Open
A4	LDO5	AO	Output voltage of LDO - PMOS_0.6	3.3V	Open
A3	LDO6	AO	Output voltage of LDO - PMOS_0.6	3.3V	Open
J4	LDO7	AO	Output voltage of LDO - PMOS_0.6	3.3V	Open
J5	LDO8	AO	Output voltage of LDO - PMOS_1	3.3V	Open
H9	VSUP_SD1	S	System supply voltage input of SD1 (connect to other VSUP pins)	5.5V	Mandatory
H8	VSUP_SD1	S	System supply voltage input of SD1 (connect to other VSUP pins)	5.5V	Mandatory
J7	LX_SD1	AIO	LX node of Stepdown1	VSUP	Open
H7	LX_SD1	AIO	LX node of Stepdown1	VSUP	Open
G7	FB_SD1	AI	Analog Feedback pin of SD1	3.6V	Open
J9	VSS_SD1	AIO	Power GND pin of Stepdown1	-	Mandatory
J8	VSS_SD1	AIO	Power GND pin of Stepdown1	-	Mandatory
G8	VSUP_SD2	S	System supply voltage input of SD2 (connect to other VSUP pins)	5.5V	Mandatory
G9	LX_SD2	AIO	LX node of Stepdown2	VSUP	Open
E8	FB_SD2	AI	Analog Feedback pin of SD2	3.6V	Open
F9	VSS_SD2	AIO	Power GND pin of Stepdown2	-	Mandatory
C9	VSUP_SD3	S	System supply voltage input of SD3 (connect to other VSUP pins)	5.5V	Mandatory
D9	LX_SD3	AIO	LX node of Stepdown3	VSUP	Open
D8	FB_SD3	AI	Analog Feedback pin of SD3	3.6V	Open
E9	VSS_SD3	AIO	Power GND pin of Stepdown3	-	Mandatory
C4	FB_SD4_P	AIO	Positive Feedback of SD1	3.6V	Open
B1	FB_SD4_N	AIO	Negative Feedback of SD1	3.6V	Open
C1	CTRL1_SD4	AIO	Bidirectional control pin of SD0, phase 1	VSUP	Open
D4	CTRL2_SD4	AIO	Bidirectional control pin of SD0, phase 2	VSUP	Open
C2	TEMP_SD4	AIO	Temperature control pin of power stage for SD1	VSUP	Open

Pin #	Pin Name	I/O	Description	Max. Voltage	If not used
E3	VSUP_CP	S	System supply voltage input of CP (connect to other VSUP pins)	5.5V	Mandatory
E2	CAPP	AIO	Flying cap of charge pump	VSUP	Open
D1	CAPN	AIO	Flying cap of charge pump	VSUP	Open
E1	V5_0	AIO	Output voltage of charge pump	-	Open
D2	VSS_CP	AIO	Power GND pin of 5V charge pump	-	Mandatory
C3	VSUP_SU	S	System supply voltage input of SU (connect to other VSUP pins)	5.5V	Mandatory
D5	SENSEP_SU	AI	SU positive sense resistor input	VSUP	Open
A2	SENSEN_SU	AI	SU negative sense resistor input	VSUP	Open
C5	FB_SU	AI	Analog Feedback pin of SU	3.6V	Open
B2	GATE_SU	AO	SU ext. NMOS gate driver output	VSUP	Open
A1	VSS_SU	AIO	Power GND pin of SU	-	Mandatory
J6	CURR1	AIO	Current sink 1 terminal	30V	Open
H6	CURR2	AIO	Current sink 2 terminal	30V	Open
G6	CURR3	AIO	Current sink 3 terminal	30V	Open
D7	EBATSW	AO	External battery switch gate driver	VSUP	Open
C7	IBATSW	AO	Internal battery switch gate driver	VSUP	Open
C8	XOFF	AO	External OV NMOS gate driver	15V	Open
A6	CHGIN1	S	Charger adapter input (protected)	5.5V	Open
B6	CHGIN1	S	Charger adapter input (protected)	5.5V	Open
A8	CHGIN2	S	2nd Charger adapter input	5.5V	Open
B8	CHGIN2	S	2nd Charger adapter input	5.5V	Open
A7	VSUP_CHG	S IO	Current limiter output, Charger input	VSUP	Open
B7	VSUP_CHG	S IO	Current limiter output, Charger input	VSUP	Open
A9	CHG_OUT	AO	Charger output (liner, switched)	5.5V	Open
B9	CHG_OUT	AO	Charger output (liner, switched)	5.5V	Open
E6	VUSB	S	Charger adapter input (unprotected)	30V	Open
E4	VIBAT	S	Internal Li-Ion battery terminal	5.5V	Open
D3	VEBAT	S	External Li-Ion battery terminal	5.5V	Open

Pin #	Pin Name	I/O	Description	Max. Voltage	If not used
E5	BATTEMP	AIO	Li-Ion battery charger NTC input	3.6V	Open
F8	VSSA	AIO	Analog GND input	-	Mandatory

Pin Description: This table shows the pin description for the CSP package including information of the I/O type, protection and handling if the function block is not used.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
	Supply Voltage to Ground 30V pins	-0.5	32	V	Applicable for pins VUSB, CURR1/2/3
	Supply Voltage to Ground 15V pins	-0.5	17	V	Applicable for pins XOFF
	Supply Voltage to Ground 5V pins	-0.5	7.0	V	Applicable for pins VSUP_SDx, VSUP_GPIO, VSUP_ANA, VIN_LDOx, LDOx, GPIOx, LX_SDx, GATE_SU, FB_SU, SENSEP/N XRES, SCL, SDA, ONKEY, ENx, VIBAT, VEBAT, E/IBATSW, CTRLx_SD4
	Supply Voltage to Ground 3V pins	-0.5	5.0	V	Applicable for pins V2_5, CREF, FB_SDx, TEMP_SD4, BATTEMP
	Voltage Difference between Ground Terminals	-0.3	0.3	V	Applicable for pins VSSx, VSSA
	Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC JESD78
Continuous Power Dissipation (T_A = +70°C)					
P_T	Continuous power dissipation		1.2	W	P_T [(1)] for WL-CSP81 package (R_{THJA} ~ 45K/W)
Electrostatic Discharge					
	Electrostatic Discharge HBM		±1.5	kV	Norm: JEDEC JESD22-A114F

Symbol	Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions					
T_A	Operating Temperature	-40	+85	°C	
R_{THJA}	Junction to Ambient Thermal Resistance			°C/W	R_{THJA} typ. 45K/W
T_J	Junction Temperature		+125	°C	
	Storage Temperature Range	-55	+125	°C	
T_{BODY}	Package Body Temperature		+260	°C	Norm IPC/JEDEC J-STD-020 (2)
	Humidity non-condensing	5	85	%	
	Moisture Sensitive Level	1			Represents an unlimited floor life time

Note(s) and/or Footnote(s):

1. Depending on actual PCB layout and PCB used.
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices".

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
AS3715 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VUSB	Charger HV input		0	5	30	V
CHGINx	Charger input		0	5	5.5	V
VIBAT, VEBAT	Battery Voltage		2.5	3.6	5.5	V
VSUPx	Supply Voltage		2.5	3.6	5.5	V
VINLDO123	Supply Voltage for LDO1, 2 & 3		2.7	3.6	5.5	V
VINLDO456	Supply Voltage for LDO4, 5 & 6		1.7	3.6	5.5	V
VINLDO78	Supply Voltage for LDO7 & 8		1.7	3.6	5.5	V
V2_5	Voltage on Pin V2_5		2.4	2.5	2.6	V
I_{low_power}	Low Power current	@ VSUPx = 4.2V		220		µA
I_{power_off}	Power-OFF current	All regulators OFF, V2_5 ON, supplied via VIBAT only		13		µA

Electrical Characteristics: VSUPx=+2.7V...+5.5V, TA =-40°C...+85°C. Typical values are at VSUPx=+3.6V, TA=+25°C, unless otherwise specified.

Typical Operating Characteristics

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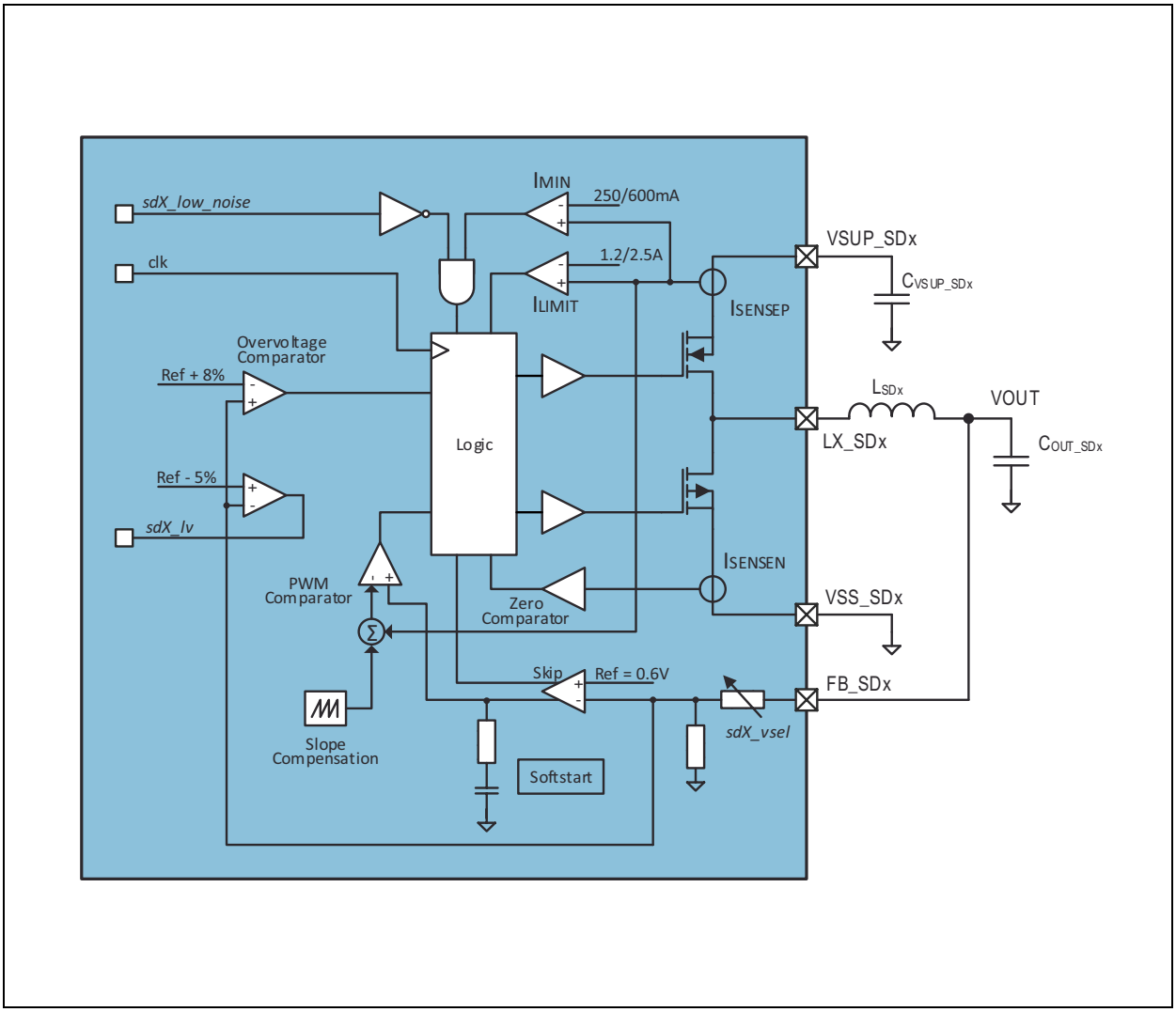
Detailed Description – Power Management Functions

DCDC Step-Down Converter

Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 2A (SD1), and 1A for (SD2, SD3), with an output capacitor of only 8-12µF. The implemented current limitation protects the DCDC and the coil during overload condition.

Figure 7:
Step Down DC/DC Converter Block Diagram



DCDC Step Down Converter Block Diagram: Shows the internal structure of the DCDC bucks.

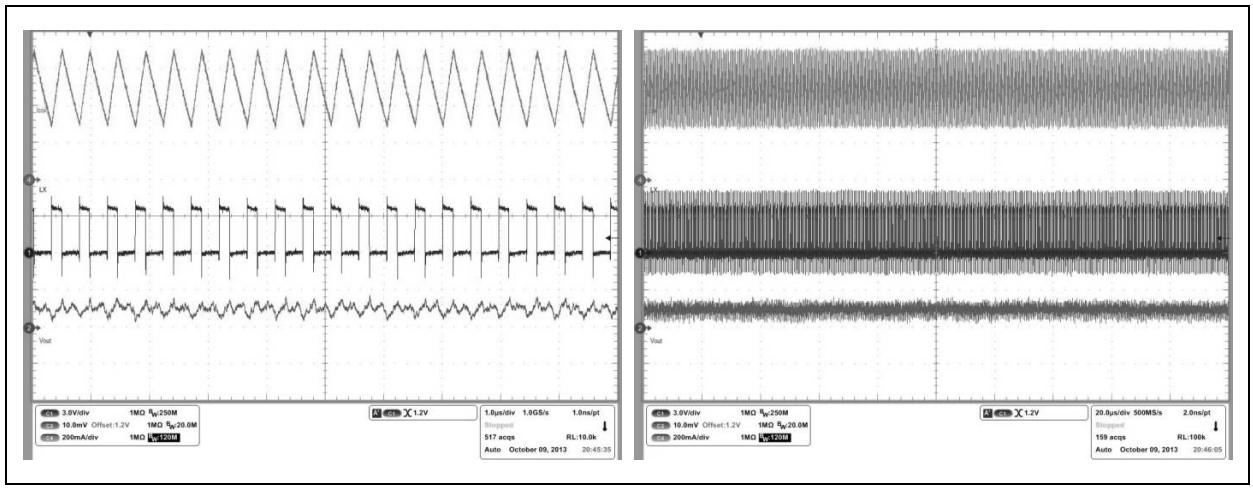
Mode Settings

Low Ripple, Low Noise Operation:

Bit settings: *sdX_low_noise*=1

In this mode there is no minimum coil current necessary before switching OFF the PMOS. As long as the load current is superior to the ripple current the device operates in continuous mode.

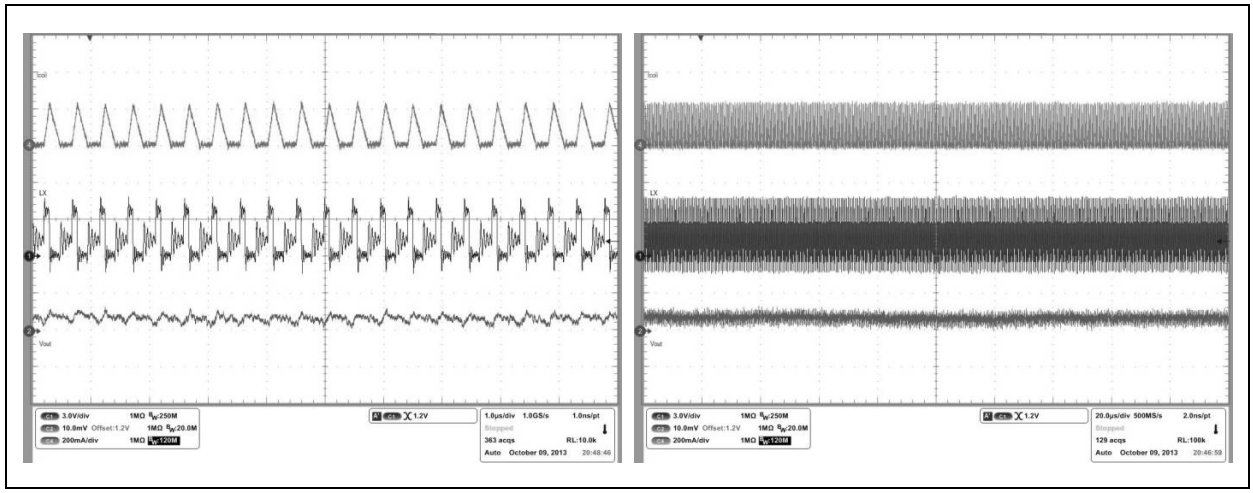
Figure 8:
DC/DC Buck Continuous Mode



DC/DC Buck Continuous Mode: Shows the DC/DC switching waveforms of for SD3 at about 500mA.

When the load current gets lower, the discontinuous mode is triggered. As result, the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to tmin_on to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences.

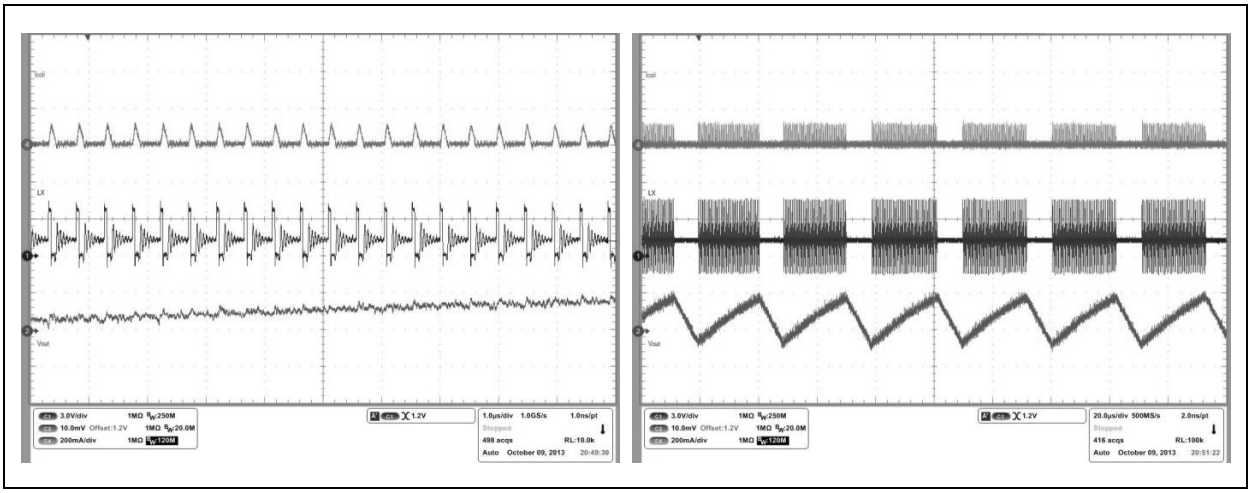
Figure 9:
DC/DC Buck Dis-continuous Mode



DC/DC Buck Dis-continuous Mode: Shows the DC/DC switching waveforms of for SD3 at about 60mA.

Only in the case the load current gets so small that less than the minimum ON-time of the PMOS would be needed to keep the loop in regulation the regulator will enter low power mode operation and skip pulses during this time. The crossover point is about ~1% of the DCDC current limit.

Figure 10:
DC/DC Buck Dis-continuous & Low Power Mode



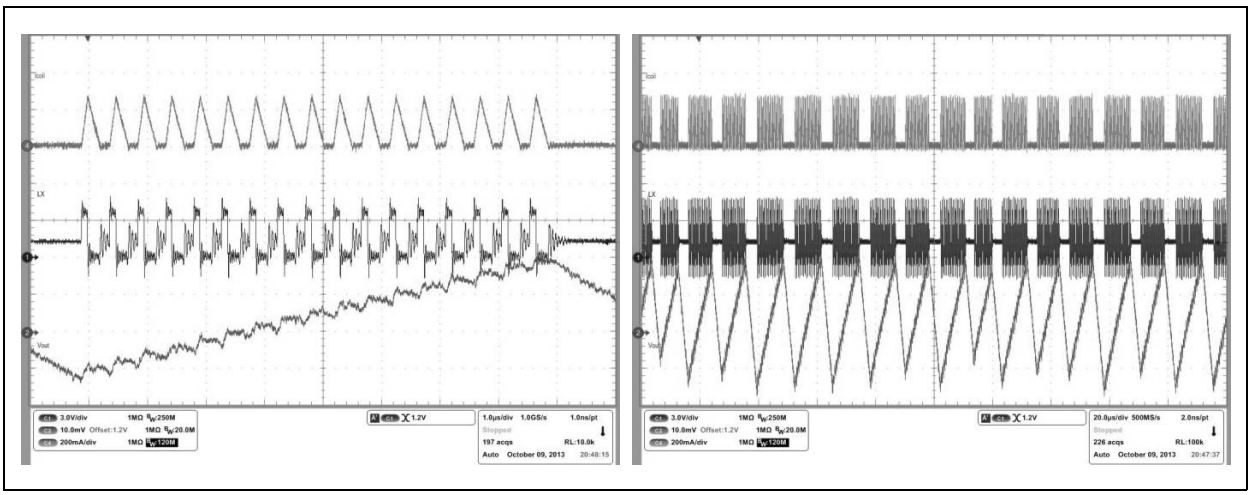
DC/DC Buck Dis-continuous & Low Power Mode: Shows the DC/DC switching waveforms of for SD3 at about 10mA.High efficiency operation (default setting).

Bit settings: *sdX_low_noise*=0

In this mode there is a minimum coil current necessary before switching OFF the PMOS. As a result there are less pulses necessary at low output loads, and therefore the efficiency at low output load is increased. As drawback this mode increases the ripple up to higher output currents.

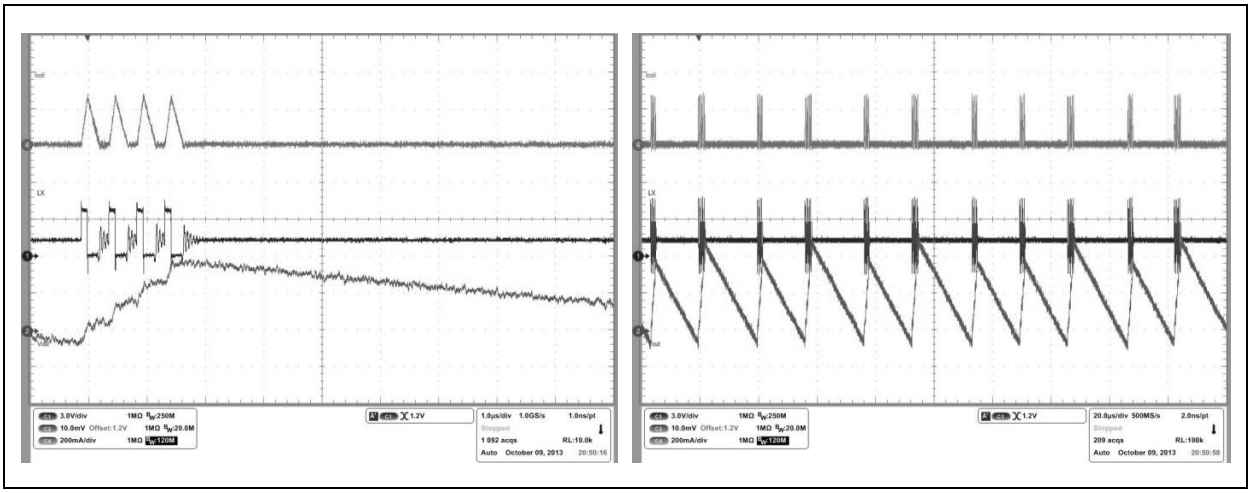
The crossover point to low power mode is already reached at reasonable high output currents (~10% of the DCDC current limit).

Figure 11:
DC/DC Buck Dis-continuous Mode & High Efficiency 1/2



DC/DC Buck Dis-continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 60mA with the low_noise bit deactivated.

Figure 12:
DC/DC Buck Dis-continuous Mode & High Efficiency 2/2



DC/DC Buck Dis-continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 10mA with the low_noise bit deactivated.

It's possible to switch between these two modes during operation.

Power Save Operation (Automatically Controlled):

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/under-shoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

DVM (Dynamic Voltage Management)

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down controllers, but only for one at a time. (see *dvm_time* and *sd_dvm_select* description)

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a bigger output capacitor to guarantee the stability of the regulator. The mode is enabled by setting *sdX_fast* =1.

Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency for SD1 can be set to 3 or 4MHz. SD2 and SD3 have a 2, 3 or 4MHz mode. This mode is selected by setting *sdX_freq* and *sdX_fsel* to the appropriate values.

100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

Step-Down Converter Configuration Modes

The step down dc/dc converters have two configuration modes to deliver different output currents for the applications. The operating mode is selected by setting the bit *sd2_slave*, *sd3_slave* (the default is set by the Boot-OTP)

Parameter

Figure 13:
DC/DC Buck Converter Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage	Pin VSUP_SDx	2.7		5.5	V
V_{OUT}	Regulated output voltage		0.6125		3.35	V
V_{OUT_tol}	Output voltage tolerance	min. 30mV	-3		+3	%
I_{LOAD_SD23}	Load current SD2, 3	VSD2, 3 <1.8V	0		1	A
		VSD2, 3 >1.8V	0		0.7	A
I_{LOAD_SD1}	Load current SD1	VSD1 <1.8V	0		2	A
		VSD1 >1.8V	0		1.2	A
I_{LIMIT}	Current limit	SD2, 3		1.2		A
		SD1		2.5		A
R_{PSW}	P-Switch ON resistance incl. bonds, substrate, etc	SD2, SD3; VSUP_SDx=3.0V		250	500	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		SD1, VSUP_SDx=3.0V		120	200	mΩ
R_{NSW}	N-Switch ON resistance incl. bonds, substrate, etc	SD2, SD3; VSUP_SDx=3.0V		160	500	mΩ
		SD1; VSUP_SDx=3.0V		63	200	mΩ
f_{SW}	Switching frequency	sdX_frequ=1; sdX_fsel=1; fclk_int =4MHz		4		MHz
		sdX_frequ=0; sdX_fsel=1; fclk_int =4MHz		3		MHz
		sdX_frequ=0; sdX_fsel=0; fclk_int =4MHz (SD2/3 only)		2		MHz
ηeff	Efficiency	see figures below				%
I_{VDD}	Current consumption	Operating current without load		60		µA
R_{DISCHG}	Pull-down resistance	SD1 disabled		100		Ω
		SD2 or SD3 disabled		200		Ω

DC/DC Buck Converter Parameter: Shows the key electrical parameter of the internal DC/DC buck converters.

Figure 14:
DC/DC Buck Converter External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{OUT\_SD2;3}$	Output capacitor	Ceramic X5R or X7R	8			µF
	Output capacitor, sd2_fast=1 or sd3_fast=1	Ceramic X5R or X7R	18			µF
C_{OUT_SD1}	Output capacitor	Ceramic X5R or X7R	12			µF
	Output capacitor, sd1_fast=1	Ceramic X5R or X7R	27			µF
$C_{VSUP\_SD1;2;3}$	Input capacitor	Ceramic X5R or X7R		2.2		µF
$L_{SD1-SD3}$	Inductor	4/3MHz operation	0.5	1		µH
		4/3MHz; VOUT≤1.8V	0.3	0.47		µH

DC/DC Buck Converter External Components: Shows the external component parameter of the internal DC/DC buck converters.

Figure 15:
DC/DC Buck SD1 3.7V Efficiency vs. Iout

DC/DC Buck SD1 Efficiency: Shows efficiency of the internal SD1 buck converter @ 0.6V, 1.2V & 3.4V with VSUP=3.7V, 2.7MHz operation with TFM252010 1uH coils and T_A=+25°C .

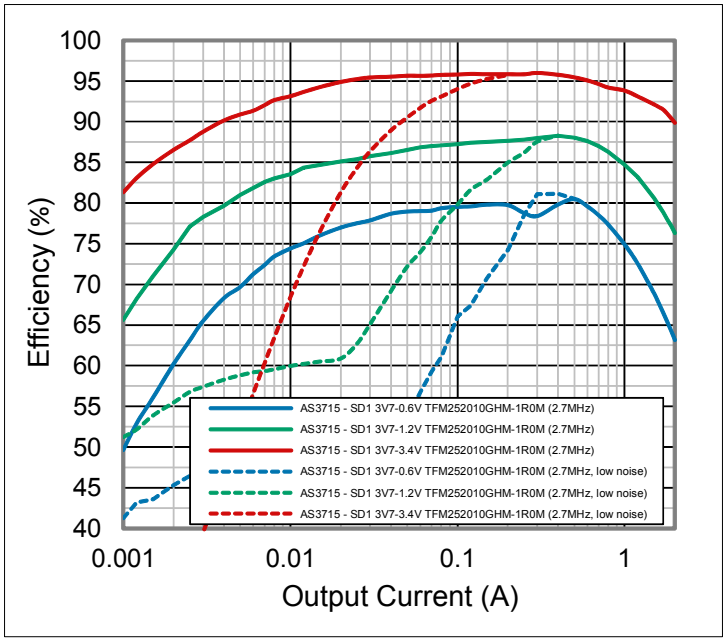
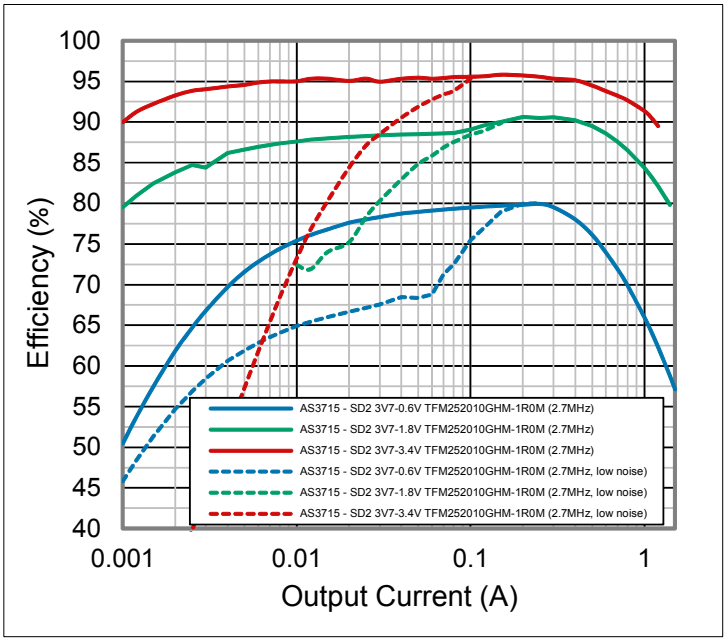


Figure 16:
DC/DC Buck SD2/3 3.7V Efficiency vs. Iout

DC/DC Buck SD2/3 Efficiency: Shows efficiency of the internal SD2/3 buck converter @ 0.6V, 1.8V & 3.4V with VSUP=3.7V, 2.7MHz operation with TFM252010 1uH coils and T_A=+25°C.

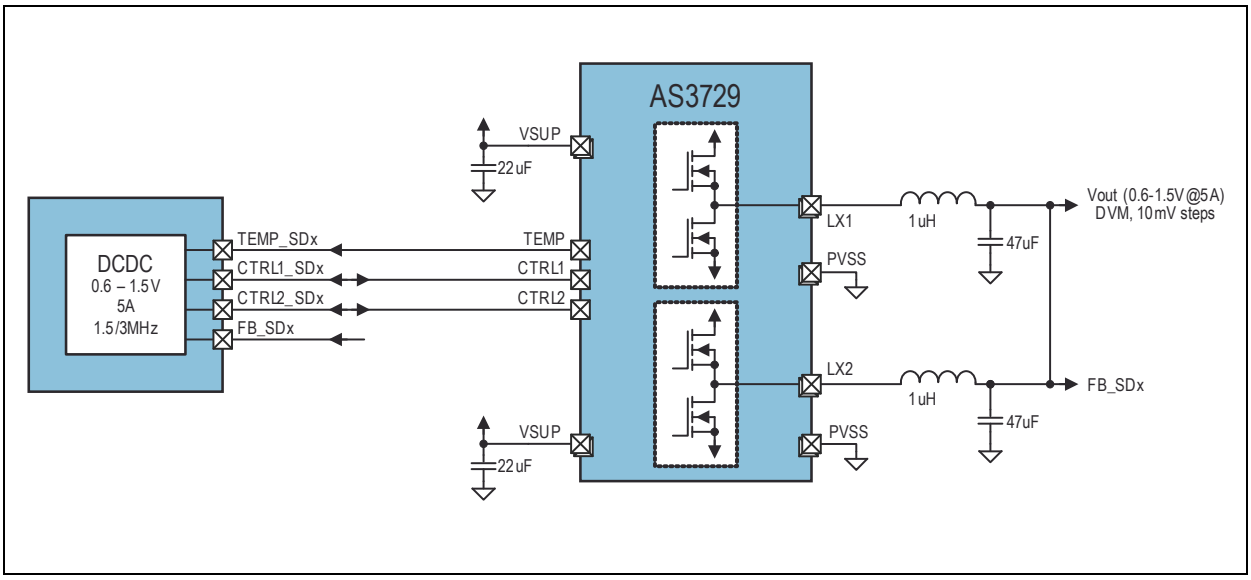


DCDC Step-Down Controller

Description

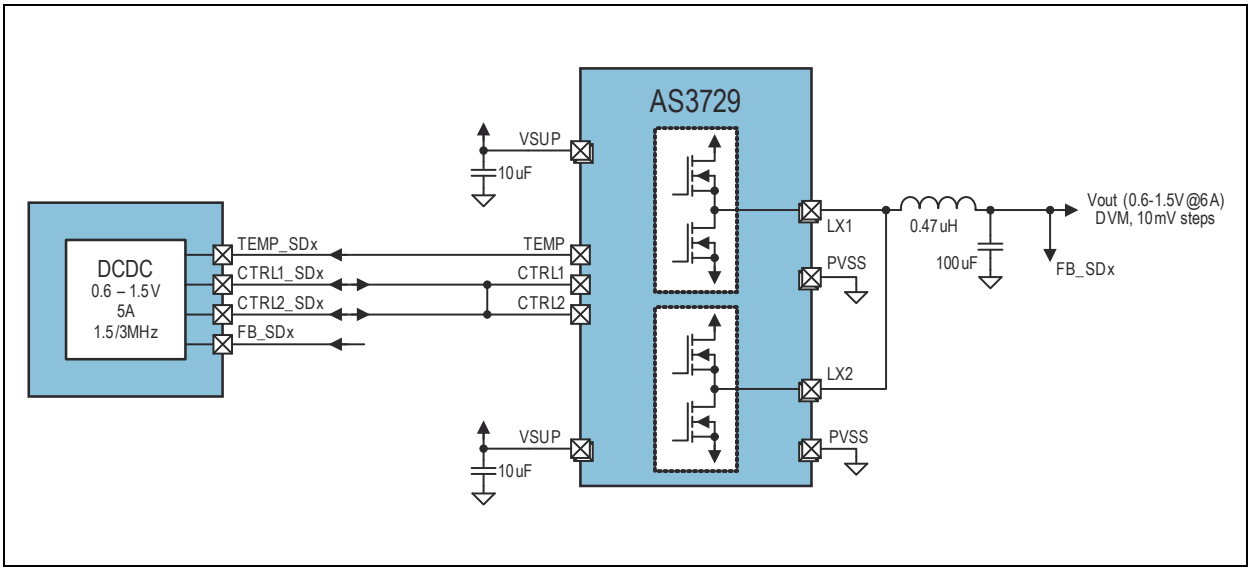
The Step-Down controller SD4 is a dual phase controller using an external power-stage incorporating 2 phases to achieve higher output currents. The maximum output current is 5A with having 2.5A per phase when using the AS3729 power stage. This allows the use of low profile coils without compromising on performance.

Figure 17:
SD4 DC/DC Buck Controller 5A Block Diagram



SD4 DC/DC Buck Controller: Shows basic connection of the SD4 controller to the external power stage (AS3729) for 5A output current.

Figure 18:
SD4 DC/DC Buck Controller 5A Combined Mode



SD4 DC/DC Buck Controller: Shows basic configuration of the SD4 controller to the external power stage (AS3729) for 5A output current using a single coil in combined mode.

Mode Settings

Low Ripple, Low Noise Operation:

Bit settings: *sdX_low_noise*=1

In this mode there is no minimum coil current necessary before switching OFF the PMOS. As long as the load current is superior to the ripple current the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. As result, the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to tmin_on to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences.

Only in the case the load current gets so small that less than the minimum ON-time of the PMOS would be needed to keep the loop in regulation the regulator will enter low power mode operation. The crossover point is about ~1% of the DCDC current limit.

High efficiency Operation (Default Setting):

Bit settings: *sdX_low_noise*=0

In this mode there is a minimum coil current necessary before switching OFF the PMOS. As a result there are less pulses necessary at low output loads, and therefore the efficiency at low output load is increased. As drawback this mode increases the ripple up to a higher output current.

The crossover point to low power mode is already reached at reasonable high output currents (~10% of the DCDC current limit).

It's possible to switch between these two modes during operation.

Low Power Operation (sdX_low_power=1):

In this mode the controller is only running on a single phase (phase 1). Only one output stage of the external power stage is used to reduce the power consumption for e.g. a stand-by mode operation.

Power Save Operation (Automatically Controlled):

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/under-shoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

Force PWM Mode Operation:

Even in the case the load current gets so small that less than the minimum ON-time of the PMOS would be needed to keep the loop in regulation the regulator will still stay on the fixed switching frequency without entering low power mode. To guarantee a stable output voltage also negative coil currents are possible. This mode guarantees the lowest possible ripple and a fixed frequency over all load conditions for powering noise sensitive RF circuits, but is compromising on the efficiency. The mode is enabled by setting *sdX_force_pwm* =1.

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a bigger output capacitor to guarantee the stability of the regulator. The mode is enabled by setting *sdX_fast* =1.

100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

DVM (Dynamic Voltage Management)

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down controllers, but only for one at a time. (see *dvm_time* and *sd_dvm_select* description)

Parameter

Figure 19:
DC/DC Buck Controller Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage	Pin VSUP_SDx	2.5		5.5	V
V_{OUT}	Regulated output voltage		0.61		1.5	V
V_{OUT_tol}	Output voltage tolerance	min. 20mV	-2		+2	%
I_{VDD}	Current consumption	Dual phase without load		136		uA
f_{SW}	Switching frequency	fclk_int = 4MHz		2.7	3	MHz

DC/DC Buck Controller Parameter: Shows the key electrical parameter of the DC/DC buck controller.

Figure 20:
DC/DC Buck Controller External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External Components 5A						
AS3729	# power stages		1			
C_{OUT_SD4}	Output capacitor	Ceramic X5R or X7R, high performance	40	47		µF
		Ceramic X5R or X7R, cost optimized	20	22		µF
C_{VSUP_SD4}	Input capacitor	Ceramic X5R or X7R	6	10		µF
L_{SD4}	Inductor	4A rated, 3MHz operation, low Ron	0.3	0.47		µH
External Components 8A (HV)						
AS3728	# power stages		1			
C_{OUT_SD4}	Output Capacitor	Ceramic X5R or X7R / 6.3V high performance	64	82		µF
		Ceramic X5R or X7R / 6.3V cost optimized	32	47		µF
C_{HVSUP_SD4}	HV Input Capacitor	Ceramic X5R or X7R / 25V	10	22		µF
C_{BOOT_SD4}	Boost Capacitor	Ceramic X5R or X7R / 6.3V		100		nF
C_{5VVSUP_SD4}	5V Supply Capacitor	Ceramic X5R or X7R / 6.3V		1		µF
L_{SDx_SD4}	Inductor	5A rated, 1MHz operation, low R_{ON}	0.5	1		µH

DC/DC Buck Controller External Components: Shows the external component parameter of the DC/DC buck controller.

Figure 21:
SD4 3.7V Eff vs. Iout Coil Comparison

DC/DC Buck SD4 Efficiency: Shows efficiency of the SD4 buck controller with AS3729 power stage for different coils @ 1.2V in dual phase and combined mode with VSUP=3.7V, 1.35MHz operation and T_A=+25°C.

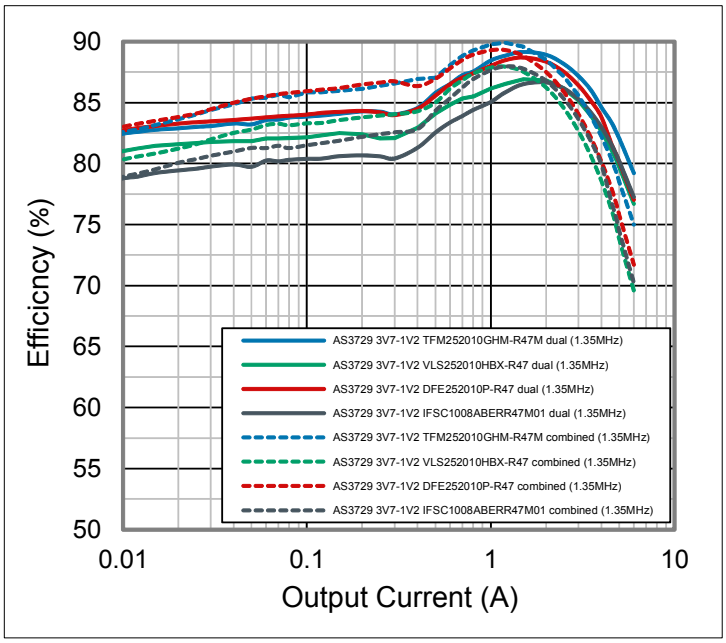
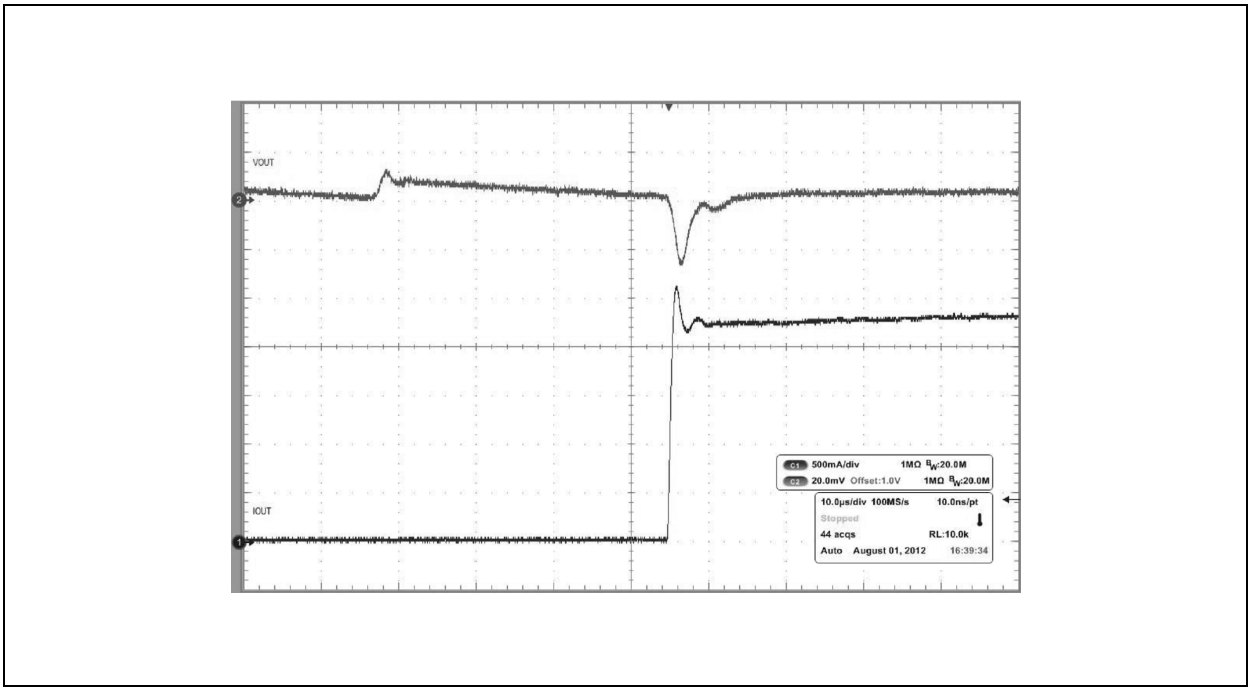
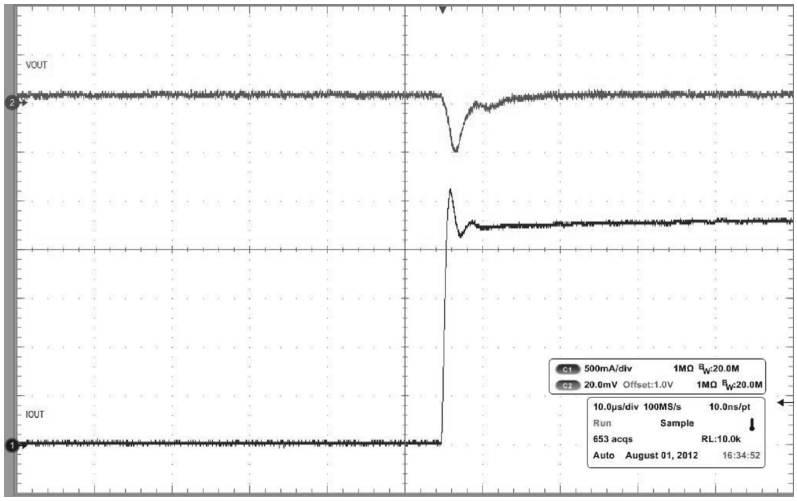


Figure 22:
DC/DC Buck SD4 Load Transient Fast Mode



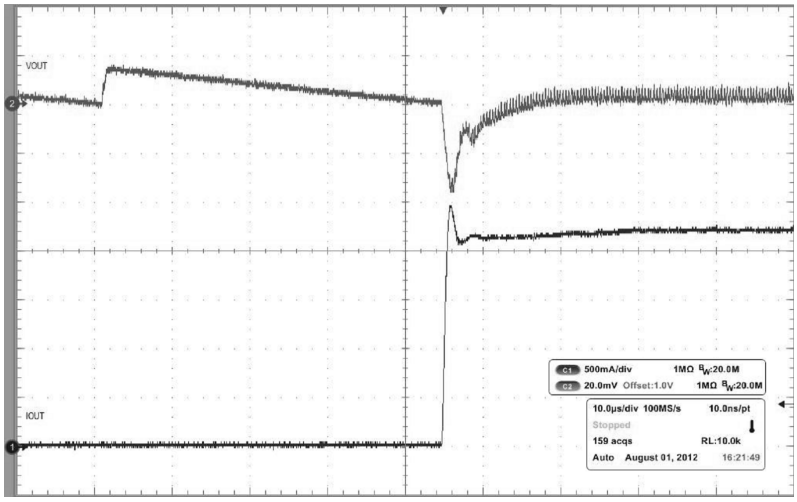
DC/DC Buck SD4 Load Transient: Shows the response of the SD4 buck controller to a load transient from 0 to 2.3A @ 1.2V with VSUP=3.7V, 3MHz operation, fast=1, C_{OUT}=88uF and T_A=+25°C.

Figure 23:
DC/DC Buck SD4 Low Noise Load Transient Fast Mode



DC/DC Buck SD4 Low Noise Load Transient: Shows the response of the SD4 buck controller to a load transient from 0 to 2.3A @ 1.2V with VSUP=3.7V, 3MHz operation, fast=1, C_{OUT}=88uF, low_noise=1 and T_A=+25°C.

Figure 24:
DC/DC Buck SD4 Load Transient



DC/DC Buck SD4 Load Transient: Shows the response of the SD4 buck controller to a load transient from 0 to 2.3A @ 1.2V with VSUP=3.7V, 3MHz operation, fast=0, C_{OUT}=44uF and T_A=+25°C.