Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AS3722

Multi-Phase DCDC Controller PMIC

General Description

The AS3722 is a compact System PMU supporting up to 20 high current rails.

The device offers advanced power management functions. All necessary ICs and peripherals in a battery powered mobile device are supplied by the AS3722. It features 4 DCDC buck converters as well as 11 low noise LDOs. The different regulated supply voltages are programmable via the serial control interface. 3-4MHz operation with 0.47uH coils is reducing cost and PCB space.

AS3722 further features 3 DCDC buck controller which are ideal to support processor currents ranging from 5A up to 32A depending on the used power stages. The multi-phase topology operating on 3MHz ensures fast load transient responses and reduces the footprint for external components.

The single supply voltage may vary from 2.7V to 5.5V.

Ordering Information and *Content Guide* appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3722, Multi-Phase DCDC Controller PMIC are listed below:

Figure 1:
Added Value of Using AS3722

Benefits	Features
• Compact design due to small coils for IO and memory voltage generation	• 4 DCDC step down regulators (3-4MHz) • Output (0.6V-3.35V; 1x5A, 1x2A, 2x1.5A)
• High current generation with external power stages to minimize PMIC power dissipation	• 3 DCDC step down controller • DVM (0.6V-1.5V; 1x6A, 1x12A, 1x24A)

• Multiple independent voltage rails for general purpose IO supplies	• 11 universal LDOs
	  • 9x universal IO range(0.8-3.3V; 0.3A)
	  • 1x low output range (0.6-1.5V; 0.3A)
	  • 1x extended input range (0.8-1.2V; 0.3A)

• Ultra low-power oscillator and no external caps needed	• RTC
	  • 1µA total power consumption
	  • Programmable alarm
	  • Auto wake-up, repeating alarms
	  • 32kHz output to peripherals

Benefits	Features

• Safe supervision in HW which works also without a processor	• Supervisor with interrupt generation and selectable warning levels
	  • Automatic battery monitoring
	  • Automatic temperature monitoring
	  • Automatic over-current monitoring
	  • Power supply supervision for DCDC

• Flexible multi-purpose IOs for general control tasks	• General Purpose IOs
	  • ADC input
	  • Wake-up/stand-by input
	  • PWM input/output
	  • Low battery and power good status

• Enables the processor to check the actual system state in detail	• ADC with internal and external sources
• Flexible and fast adaptation to different processors/applications	• OTP programmable Boot and Power-down sequence
• Power saving control according to the processor needs	• Stand-by function with programmable sequence and voltages

• Self-contained start-up and control for single and multi-cell battery applications. Safety shutdown feature	• Control Interface
	  • I2C/SPI control lines with watchdog
	  • ONKEY with 4/8s emergency shut-down
	  • POR with RESET I/O
	  • 5V pre-regulator enable

• Dedicated packages for specific applications. Optimization for PCB cost or size	• Package
	  • 124-pin CTBGA (8x8mm), 0.5mm pitch
	  • 108-pin WL-CSP (4.8x3.6mm), 0.4mm pitch

Applications

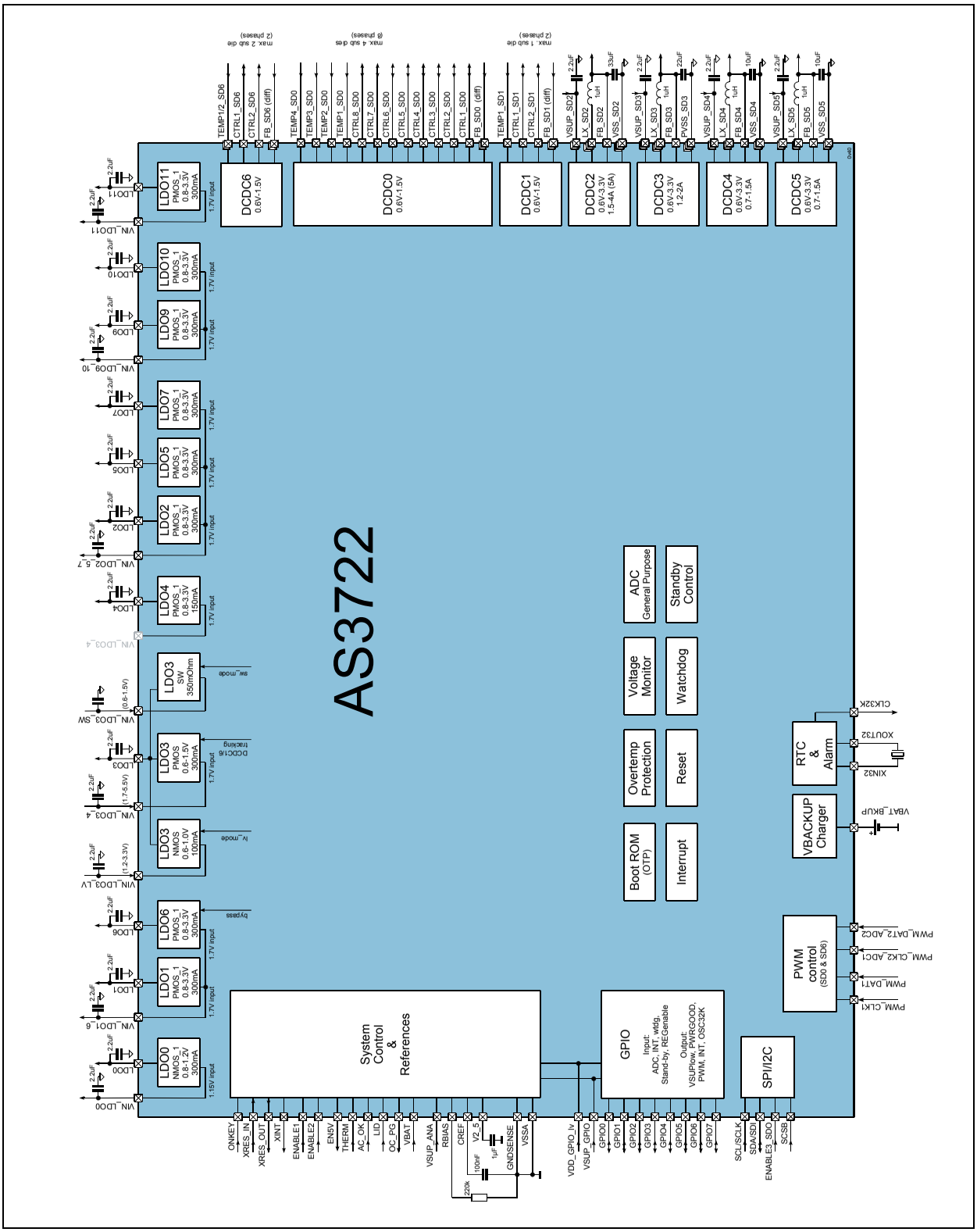
The device is suitable for:

- Mobile Phones
- Tablet PCs
- NetBooks
- Portable Media Players
- Portable Navigation Devices
- Mobile Internet Devices

Block Diagram

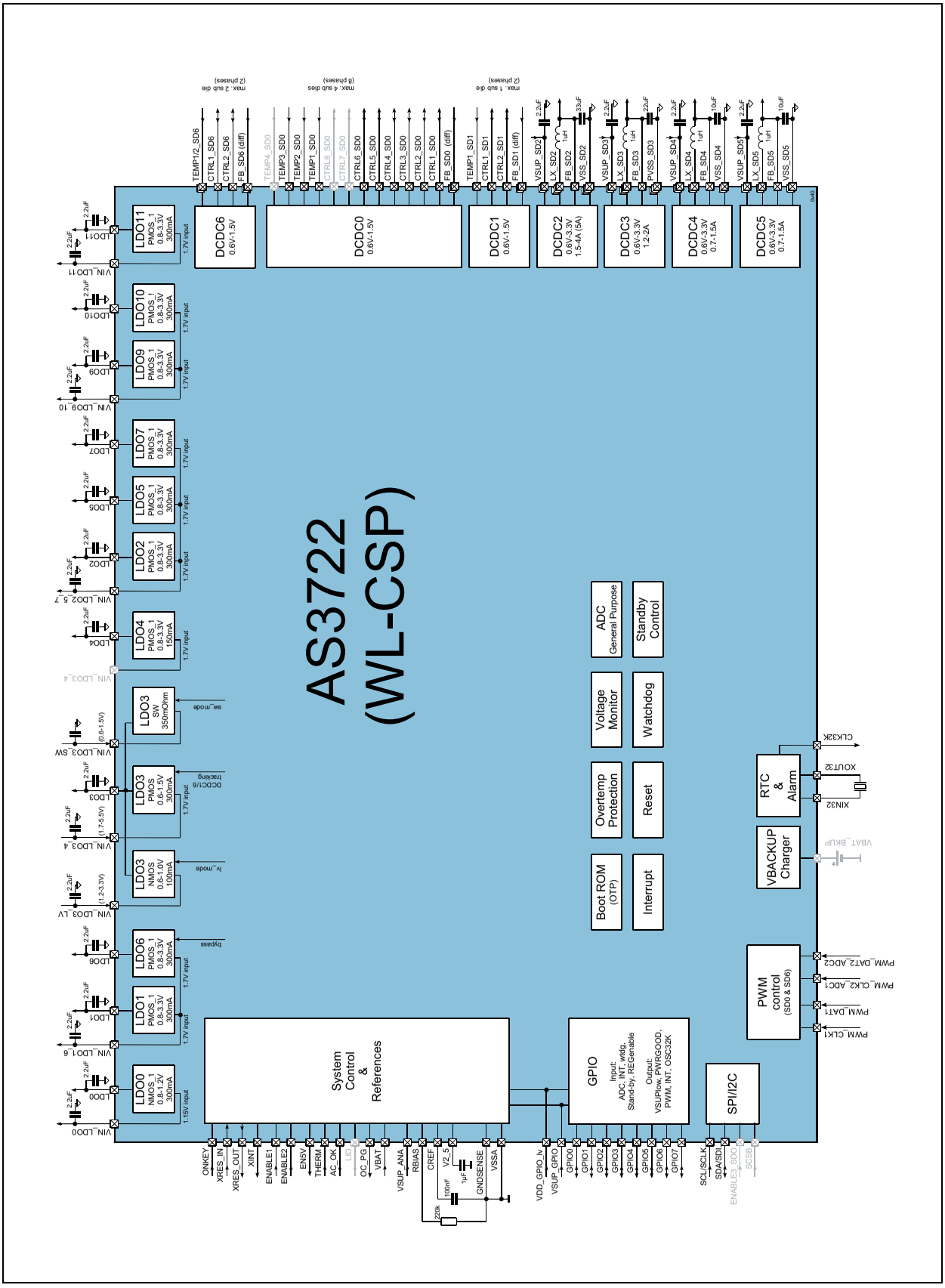
The functional blocks of this device are shown below:

Figure 2:
AS3722 Block Diagram (CTBGA)



Block Diagram: Shows the main function blocks of the AS3722 including basic external components.

Figure 3:
AS3722 Block Diagram (WL-CSP)



Block Diagram: Shows the main function blocks of the AS3722 in WL-CSP package.

Pin Assignment

Figure 4:
Pin Assignment (CTBGA124)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSSA	LDO4	VIN_ LDO3_ 4	VIN_ LDO3_ SW	LDO9	VIN_ LDO9_ 10	LDO6	VIN_ LDO1_ 6	LDO2	LDO5	LDO7	VIN_ LDO2_ 5_7	LDO0	VSSA
B	VIN_ LDO11		GPIO4	GPIO6	LDO11	VIN_ LDO3_ LV	LDO3	LDO10	LDO1	ONKEY	PWM_ CLK2_ ADC1	PWM_ DAT2_ ADC2		VIN_ LDO0
C	XINT	GPIO5											CTRL1 _SD6	CTRL2 _SD6
D	CLK 32K	GPIO7			GPIO2	GPIO0	LID	THERM	PWM_ CLK1	PWM_ DAT1			CTRL1 _SD1	CTRL2 _SD1
E	OC_PG	ENABLE 3_SDO		GPIO3							ENABL E2		CTRL1 _SD0	CTRL2 _SD0
F	VSS_ GPIO	VDD_ GPIO_ LV		SDA_ SDI			VSSA	ENABL E1			FB_ SD6_P		CTRL3 _SD0	CTRL4 _SD0
G	XIN32K	XOUT 32K		SCL_ SCLK		GPIO1			FB_ SD1_P		FB_ SD6_N		CTRL5 _SD0	CTRL6 _SD0
H	VSUP_ ANA	V2_5		VBAT_ BKUP		SCSB			FB_ SD1_N		FB_ SD0_P		CTRL7 _SD0	CTRL8 _SD0
J	FB_SD 5	RBIAS		CREF			VSSA	XRES_ IN			FB_ SD0_N		TEMP2 _SD0	TEMP 1_SD0
K	FB_SD 2	FB_SD 3		GND SENSE							TEMP4 _SD0		TEMP3 _SD0	TEMP _SD1
L	VSUP_ SD3	VSUP_ SD3			XRES_ OUT	EN5V	VBAT	AC_OK	VSUP_ GPIO	FB_SD 4			TEMP2 _SD6	TEMP 1_SD6
M	LX_ SD3	LX_ SD3											VSS_ SD4	VSS_ SD4
N	LX_ SD3		VSS_ SD3	VSS_ SD2	LX_ SD2	VSUP_ SD2	LX_ SD2	VSS_ SD2	VSS_ SD5	LX_ SD5	VSUP_ SD5	VSUP_ SD4		LX_ SD4
P	VSSA	VSS_ SD3	VSS_ SD3	VSS_ SD2	LX_ SD2	VSUP_ SD2	LX_ SD2	VSS_ SD2	VSS_ SD5	LX_ SD5	VSUP_ SD5	VSUP_ SD4	LX_ SD4	VSSA

Pin Assignment: Shows the top view pin assignment of the AS3722 in the CTBGA124.

Figure 5:
Ball Assignment (WL-CSP108)

	1	2	3	4	5	6	7	8	9	10	11	12
A	PWM_ DAT2_ ADC1	ONKEY	LDO7	LDO5	LDO6	LDO1	LDO9	LDO3	LDO4	GPIO0	GPIO5	XINT
B	PWM_ CLK2_ ADC1	THERM	VIN_LDO 0	VIN_LDO 2_5_7	LDO2	VIN_LDO 1_6	VIN_LDO 9_10	VIN_LDO 3_SW	VIN_LDO 11	GPIO4	CLK32K	GPIO7
C	CTRL1_ SD6	ENABLE 1	XRES_IN	LDO0	PWM_ DAT1	PWM_ CLK1	VIN_LDO 3_LV	LDO11	GPIO3	VSUP_ GPIO	OC_PG	SCL_ SCLK
D	CTRL2_ SD6	CTRL1_ SD1	ENABLE2	AC_OK	CTRL2_ SD1	LDO10	VIN_LDO 3_4	GPIO2	VBAT	VDD_ GPIO_LV	SDA_SDI	V2_5
E	CTRL5_ SD0	CTRL2_ SD0	CTRL1_ SD0	CTRL3_ SD0	CTRL4_ SD0	VSSA	GPIO1	EN5V	XOUT 32K	XIN32K	CREF	VSUP_ ANA
F	TEMP2_ SD0	CTRL6_ SD0	VSUP_ GPIO	TEMP1_ SD0	TEMP3_ SD0	FB_SD0_ P	GPIO6	XRES_ OUT	VSSA	FB_SD5	RBIAS	FB_SD2
G	FB_SD6 _N	FB_SD6 _P	TEMP_ SD1	FB_SD1_ P	FB_SD1 _N	VSSA	VSSA	LX_SD2	LX_SD2	FB_SD3	VSS_ SD3	VSS_ SD3
H	TEMP1_ SD6	FB_SD4	FB_SD0_ N	VSUP_ SD4_5	LX_SD5	VSS_ SD5	VSS_ SD2	VSUP_ SD2	LX_SD2	VSS_ SD2	LX_SD3	VSUP_ SD3
J	TEMP2_ SD6	VSS_ SD4	LX_SD4	VSUP_ SD4_5	LX_SD5	VSS_ SD5	VSS_ SD2	VSUP_ SD2	LX_SD2	VSS_ SD2	LX_SD3	VSUP_ SD3

Ball Assignment: Shows the top view pin assignment of the AS3722 in the WL-CSP108.

Pin Description

Figure 6:
Pin Description

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
F4	D11	SDA_SDI	DI	SPI digital input in SPI mode; Data IO in I2C mode.	VSUP	Open
G4	C12	SCL_SCLK	DI	SPI clock input in SPI mode; SCK input in I2C mode.	VSUP	Open
E2		ENABLE3_SDO	DIO	SPI digital output in SPI mode	VSUP	Define level
H6		SCSB	DI	SPI chip-select in SPI mode; connect to VSS in I2C mode.	VSUP	VSS
B14	B3	VIN_LDO0	S	Supply pad for LDOs	5.5V	Mandatory
A8	B6	VIN_LDO1_6	S	Supply pad for LDOs	5.5V	Mandatory
A6	B7	VIN_LDO9_10	S	Supply pad for LDOs	5.5V	Mandatory
A3	D7	VIN_LDO3_4	S	Supply pad for LDOs	5.5V	Mandatory
A12	B4	VIN_LDO2_5_7	S	Supply pad for LDOs	5.5V	Mandatory
A4	B8	VIN_LDO3_SW	S	Supply pad for LDO3 switch function	3.6V	Mandatory
B1	B9	VIN_LDO11	S	Supply pad for LDOs	5.5V	Mandatory
A13	C4	LDO0	AO	Output voltage of LDO - NMOS_0.6	VIN_LDO0	Open
B9	A6	LDO1	AO	Output voltage of LDO - PMOS_1	VIN_LDO1_6	Open
A9	B5	LDO2	AO	Output voltage of LDO - PMOS_1	VIN_LDO2_5_7	Open
B6	C7	VIN_LDO3_LV	S	Supply pad for LDO3 NMOS function	3.6V	Open
A2	A9	LDO4	AO	Output voltage of LDO - PMOS_0.6	VIN_LDO3_4	Open
A10	A4	LDO5	AO	Output voltage of LDO - PMOS_0.6	VIN_LDO2_5_7	Open
A7	A5	LDO6	AO	Output voltage of LDO - PMOS_0.6	VIN_LDO1_6	Open
A11	A3	LDO7	AO	Output voltage of LDO - PMOS_0.6	VIN_LDO2_5_7	Open

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
B7	A8	LDO3	AO	Output voltage of LDO - PMOS_1	VIN_LDO8	Open
A5	A7	LDO9	AO	Output voltage of LDO - PMOS_1	VIN_LDO9_10	Open
B8	D6	LDO10	AO	Output voltage of LDO - PMOS_1	VIN_LDO9_10	Open
B5	C8	LDO11	AO	Output voltage of LDO - PMOS_1	VIN_LDO11	Open
B10	A2	ONKEY	DI	Input pin to startup (no pullup/pull down)	5.5V	Define level
F8	C2	ENABLE1	DI	Input pin for transition into and out of deep-sleep mode	VSUP	Define level
E11	D3	ENABLE2	DI	Input pin for control of DCDC0	VSUP	Define level
D8	B2	THERM	DI	Input pin for thermal event	5.5V	Define level
J8	C3	XRES_IN	DI	Input pin for reset during active and stand-by state	VSUP	Define level
L5	F8	XRES_OUT	DO	Push pull to VDD_GPIO_lv	VSUP	Open
L8	D4	AC_OK	DI	Pin to indicate, that the AC adaptor is present	5.5V	Define level
D7		LID	DI	Input pin to indicates LID status of Device	5.5V	Define level
C1	A12	XINT	DO	Push-Pull or open drain output for interrupt detection	VSUP	Open
L9	C10, F3	VSUP_GPIO	S	Supply pin for GPIOs (connect to other VSUP pins)	5.5V	Mandatory
F2	D10	VDD_GPIO_lv	S	Supply pin for GPIOs (connect to typical 1.8V or 3.3)	VSUP	Mandatory
F1		VSS_GPIO	AIO	Analog GND input	-	Mandatory
D6	A10	GPIO0	DIO	General purpose input/output pin	VSUP	Open
G6	E7	GPIO1	DIO	General purpose input/output pin	VSUP	Open

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
D5	D8	GPIO2	DIO	General purpose input/output pin	VSUP	Open
E4	C9	GPIO3	DIO	General purpose input/output pin	VSUP	Open
B3	B10	GPIO4	DIO	General purpose input/output pin	VSUP	Open
C2	A11	GPIO5	DIO	General purpose input/output pin	VSUP	Open
B4	F7	GPIO6	DIO	General purpose input/output pin	VSUP	Open
D2	B12	GPIO7	DIO	General purpose input/output pin	VSUP	Open
H2	D12	V2_5	AO	Output voltage of low power LDO V2_5	3.6V	Mandatory
J4	E11	CREF	AIO	Bypass capacitor for the internal voltage reference; connect 100nF	V2_5	Mandatory
J2	F11	RBIAS	AIO	External resistor; always connect a resistor of 220kΩ (±1%) to VSSA	V2_5	Mandatory
H4		VBAT_BKUP	AIO	Backup battery input	3.6V	Open
A1	G7	VSSA	AIO	Analog GND input	-	Mandatory
A14	G6	VSSA	AIO	Analog GND input	-	Mandatory
J7	E6	VSSA	AIO	Analog GND input	-	Mandatory
P1	F9	VSSA	AIO	Analog GND input	-	Mandatory
P14		VSSA	AIO	Analog GND input	-	Mandatory
F7		VSSA	AIO	Analog GND input	-	Mandatory
D1	B11	CLK32K	DO	32kHz clk output push/pull to VDD_GPIO_lv	VSUP	Open
G1	E10	XIN32K	AIO	Connect to 32kHz crystal oscillator	V2_5	Open
G2	E9	XOUT32K	AIO	Connect to 32kHz crystal oscillator	V2_5	Open
K4		GNDSENSE	AIO	Analog sense GND input (connect to VSSA on WL-CSP)	-	Mandatory

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
E1	C11	OC_PG	DO	Digital Output open drain to indicate over-current/ power_good	VSUP	Open
H1	E12	VSUP_ANA	S	System supply voltage input (connect to other VSUP pins)	5.5V	Mandatory
N6	H8	VSUP_SD2	S	System supply voltage input of Stepdown2 (connect to other VSUP pins)	5.5V	Mandatory
P6	J8	VSUP_SD2	S	System supply voltage input of Stepdown2 (connect to other VSUP pins)	5.5V	Mandatory
N5	G8	LX_SD2	AIO	LX node of Stepdown2	VSUP	Open
N7	G9	LX_SD2	AIO	LX node of Stepdown2	VSUP	Open
P5	H9	LX_SD2	AIO	LX node of Stepdown2	VSUP	Open
P7	J9	LX_SD2	AIO	LX node of Stepdown2	VSUP	Open
N4	H7	VSS_SD2	AIO	Power GND pin of Stepdown2	-	Mandatory
N8	J7	VSS_SD2	AIO	Power GND pin of Stepdown2	-	Mandatory
P4	H10	VSS_SD2	AIO	Power GND pin of Stepdown2	-	Mandatory
P8	J10	VSS_SD2	AIO	Power GND pin of Stepdown2	-	Mandatory
K1	F12	FB_SD2	AIO	Analog Feedback pin of SD2	3.6V	Open
L1	H12	VSUP_SD3	S	System supply voltage input of Stepdown3 (connect to other VSUP pins)	5.5V	Mandatory
L2	J12	VSUP_SD3	S	System supply voltage input of Stepdown3 (connect to other VSUP pins)	5.5V	Mandatory
M1	H11	LX_SD3	AIO	LX node of Stepdown3	VSUP	Open
M2	J11	LX_SD3	AIO	LX node of Stepdown3	VSUP	Open
N1		LX_SD3	AIO	LX node of Stepdown3	VSUP	Open

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
N3	G11	VSS_SD3	AIO	Power GND pin of Stepdown3	-	Mandatory
P2	G12	VSS_SD3	AIO	Power GND pin of Stepdown3	-	Mandatory
P3		VSS_SD3	AIO	Power GND pin of Stepdown3	-	Mandatory
K2	G10	FB_SD3	AIO	Analog Feedback pin of SD3	3.6V	Open
N12	H4	VSUP_SD4	S	System supply voltage input of Stepdown4 (connect to other VSUP pins)	5.5V	Mandatory
P12	J4	VSUP_SD4	S	System supply voltage input of Stepdown4 (connect to other VSUP pins)	5.5V	Mandatory
L10	H2	FB_SD4	AIO	Analog Feedback pin of SD4	3.6V	Open
N14	J3	LX_SD4	AIO	LX node of Stepdown4	VSUP	Open
P13		LX_SD4	AIO	LX node of Stepdown4	VSUP	Open
M13	J2	VSS_SD4	AIO	Power GND pin of Stepdown4	-	Mandatory
M14		VSS_SD4	AIO	Power GND pin of Stepdown4	-	Mandatory
N11	H4	VSUP_SD5	S	System supply voltage input of Stepdown5 (connect to other VSUP pins)	5.5V	Mandatory
P11	J4	VSUP_SD5	S	System supply voltage input of Stepdown5 (connect to other VSUP pins)	5.5V	Mandatory
J1	F10	FB_SD5	AIO	Analog Feedback pin of SD5	3.6V	Open
N10	H5	LX_SD5	AIO	LX node of Stepdown5	VSUP	Open
P10	J5	LX_SD5	AIO	LX node of Stepdown5	VSUP	Open
P9	H6	VSS_SD5	AIO	Power GND pin of Stepdown5	-	Mandatory
N9	J6	VSS_SD5	AIO	Power GND pin of Stepdown5	-	Mandatory
H11	F6	FB_SD0_P	AIO	Positive Feedback of SD0	3.6V	Open

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
J11	H3	FB_SD0_N	AIO	Negative Feedback of SD0	3.6V	Open
E13	E3	CTRL1_SD0	AIO	Bidirectional control pin of SD0, phase 1	VSUP	Open
E14	E2	CTRL2_SD0	AIO	Bidirectional control pin of SD0, phase 2	VSUP	Open
F13	E4	CTRL3_SD0	AIO	Bidirectional control pin of SD0, phase 3	VSUP	Open
F14	E5	CTRL4_SD0	AIO	Bidirectional control pin of SD0, phase 4	VSUP	Open
G13	E1	CTRL5_SD0	AIO	Bidirectional control pin of SD0, phase 5	VSUP	Open
G14	F2	CTRL6_SD0	AIO	Bidirectional control pin of SD0, phase 6	VSUP	Open
H13		CTRL7_SD0	AIO	Bidirectional control pin of SD0, phase 7	VSUP	Open
H14		CTRL8_SD0	AIO	Bidirectional control pin of SD0, phase 8	VSUP	Open
J14	F4	TEMP1_SD0	AIO	Temperature control pin of subdie1 for SD0	VSUP	Open
J13	F1	TEMP2_SD0	AIO	Temperature control pin of subdie2 for SD0	VSUP	Open
K13	F5	TEMP3_SD0	AIO	Temperature control pin of subdie3 for SD0	VSUP	Open
K11		TEMP4_SD0	AIO	Temperature control pin of subdie4 for SD0	VSUP	Open
G9	G4	FB_SD1_P	AIO	Positive Feedback of SD1	3.6V	Open
H9	G5	FB_SD1_N	AIO	Negative Feedback of SD1	3.6V	Open
D13	D2	CTRL1_SD1	AIO	Bidirectional control pin of SD1, phase 1	VSUP	Open
D14	D5	CTRL2_SD1	AIO	Bidirectional control pin of SD1, phase 2	VSUP	Open

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
K14	G3	TEMP_SD1	AIO	Temperature control pin of subdie1 for SD1	VSUP	Open
F11	G2	FB_SD6_P	AIO	Positive Feedback of SD6	3.6V	Open
G11	G1	FB_SD6_N	AIO	Negative Feedback of SD6	3.6V	Open
C13	C1	CTRL1_SD6	AIO	Bidirectional control pin of SD6, phase 1	VSUP	Open
C14	D1	CTRL2_SD6	AIO	Bidirectional control pin of SD6, phase 2	VSUP	Open
L14	H1	TEMP1_SD6	AIO	Temperature control pin of subdie1 for SD6	VSUP	Open
L13	J1	TEMP2_SD6	AIO	Temperature control pin of subdie2 for SD6	VSUP	Open
D9	C6	PWM_CLK1	DI	PWM input pin for DVM control of SD0	VSUP	Define level
D10	C5	PWM_DAT1	DI	PWM input pin for DVM control of SD0	VSUP	Define level
B11	B1	PWM_CLK2_ ADC1	DI	PWM input pin for DVM control of SD6 or ADC input pin	VSUP	Define level
B12	A1	PWM_DAT2_ ADC2	DI	PWM input pin for DVM control of SD6 or ADC input pin	VSUP	Define level
L7	D9	VBAT	S	High Voltage Supply pin for RTC, and voltage detection	30V	Connect to VSUP
L6	E8	EN5V	DO	Enable pin for external 5V HV stepdown to supply VSUP rails	V2_5	Open

Pin Description: This table shows the pin description for the CTBGA as well as the WL-CSP package including information of the I/O type, protection and handling if the function block is not used.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
	Supply Voltage to Ground 30V pins	-0.5	32	V	Applicable for pin VBAT
	Supply Voltage to Ground 5V pins	-0.5	7.0	V	Applicable for pins VSUP_SDx, VSUP_ANA, ONKEY, VSUP_GPIO, VIN_LDOx, LDO6 (switch mode), THERM, AC_OK, LID
	5V pins with protection to VSUP	-0.5	VSUP_x	V	Applicable for pins SCL_SCLK, SDA_SDI, SCSB, SDO, XINT, VDD_GPIO_LV, GPIOx, CLK32K, OC_PG, LX_SDx, CTRLx, XRES_IN/OUT, ENABLEx, PWMx
	Supply Voltage to Ground 3V pins	-0.5	5.0	V	Applicable for pins V2_5, VBAT_BKUP, VIN_LDO3_LV/SW
	3V pins with protection to VIN_LDOx	-0.5	5.0 or VIN_LDOx	V	Applicable for pins LDOx
	3V pins with protection to VSUP	-0.5	5.0 or VSUP_x	V	Applicable for pins TEMPx, FB_SDx
	3V pins with protection to V2_5	-0.5	V2_5	V	Applicable for pins CREF, RBIAS, XIN32K, XOUT32K, EN5V
	Voltage Difference between Ground Terminals	-0.3	0.3	V	Applicable for pins VSSx, VSSA, GNDSENSE
I_{SCR}	Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC JESD78

Symbol	Parameter	Min	Max	Units	Comments
Continuous Power Dissipation (T_A = 70°C)					
P_T	Continuous power dissipation		1.4	W	P_T[(1)] for CTBGA124 package (R_{THJA} ~ 38K/W)
P_T	Continuous power dissipation		1.3	W	P_T[(1)] for WL-CSP108 package (R_{THJA} ~ 40K/W)
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±1.5		kV	Norm: JEDEC JESD22-A114F
Temperature Ranges and Storage Conditions					
T_A	Operating Temperature	-40	85	°C	
T_J	Junction Temperature		125	°C	
T_{STRG}	Storage Temperature Range	-55	125	°C	
T_{BODY}	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020[(2)]
RH_{NC}	Relative Humidity non-condensing	5	85	%	
MSL	Moisture Sensitivity Level	3			for CTBGA, represents a max. floor life time of 168h
		1			for WL-CSP, represents an unlimited max. floor life time
Bump Temperature (CTBGA Soldering)					
T_{PEAK}	Soldering Profile	235	245	°C	Peak Temperature
t_{WELL}		30	45	s	Well Time above 217°C

Note(s) and/or Footnote(s):

1. Depending on actual PCB layout and PCB used
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices"

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 8:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT	Battery Voltage		2.5	3.6	30	V
VSUPx	Supply Voltage		2.5	3.6	5.5	V
VBAT_BKUP	Backup-Battery Voltage		2.5	3	3.6	V
VDD_GPIO_lv	Alternative GPIO Supply Voltage		1.7	1.8	3.6	V
VINLDO0	Supply Voltage for LDO0		1.15	3.6	5.5	V
VINLDO1-11	Supply Voltage for LDO1 to LDO11		1.7	3.6	5.5	V
VINLDO3_LV	Supply Voltage for LDO3 NMOS		1.2		3.6V	V
VINLDO3_SW	Supply Voltage for LDO3 switch		0.6		1.5V	V
V2_5	Voltage on Pin V2_5		2.4	2.5	2.6	V
$I_{quiescent}$	Quiescent current	@ VSUPx = 3.8V, no regulator enabled only V2_5 on, digital part, bias and references running		310		µA
I_{low_power1}	Low Power current	as above but, low_power=1		265		µA
I_{low_power2}	Low Power current	As above, but low_power=1; clk_div=1		160		µA
I_{power_off}	Power-Off current	All regulators off V2_5 on		10		µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital Input Pin Characteristics						
V_{IL}	Low Level input voltage	ONKEY, XRES_IN	–0.3		0.4	V
V_{IH}	High Level input	XRES_IN, ENABLEx	1.4		V_{VSUP_GPIO}	V
V_{IH_noprot}	High Level input	ONKEY, THERM, AC_OK, LID	1.4		5.5V	V
Digital Output Pin Characteristics						
V_{OL}	XRES_OUT Low-Level Output Voltage	XRES_OUT; XINT, OC_PG at 2.0mA			0.2 x $V_{VDD\_GPIO\_lv}$	V
V_{OH}	XRES_OUT High-Level Output Voltage	XRES_OUT; XINT (if on push pull mode), OC_PG, SDO at -1.0mA	0.8 x $V_{VDD\_GPIO\_lv}$			V
V_{OL_EN5V}	Low-Level Output Voltage	EN_5V at 0.1mA			0.2 x V_{V2_5}	V
V_{OH_EN5V}	High-Level Output Voltage	EN_5V at -0.1mA	0.8 x V_{V2_5}			V
$I_{LEAKAGE}$	Leakage current	high impedance			10	µA
R_{PULLUP}	Internal pull-up to VDD_GPIO_lv	XINT=2V, VDD_GPIO_LV=3V (XINT in open-drain mode)	33		91	kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GPIO Pin Characteristics						
V_{IL}	Low level input voltage	digital input	-0.3		0.4	V
V_{IH}	High level input voltage	digital input	1.4		$V_{VDD\_GPIO\_lv}$ or V_{VSUP_GPIO}	V
V_{OL}	Low level output voltage	GPIO, I_{OL}=+2mA; digital output			0.2 x $V_{VDD\_GPIO\_lv}$ or V_{VSUP_GPIO}	V
V_{OH}	High level output voltage	GPIO, I_{OH}=–1mA; digital push-pull output	0.8 x$V_{VDD_GPIO_lv}$ or V_{VSUP_GPIO}		$V_{VDD\_GPIO\_lv}$ or V_{VSUP_GPIO}	V
$I_{LEAKAGE}$	Leakage current	high impedance			10	µA
$R_{pull-up}$	Pull-up resistance	if enabled; VSUP_GPIO=3.6V		300		kΩ
$R_{pull-down}$	Pull-down resistance	if enabled; VSUP_GPIO=3.6V		300		kΩ
R_{NMOS}	NMOS resistance	VSUP_GPIO>=3.3V			50	Ω

Electrical Characteristics: VSUPx=+2.7V...+5.5V, TA = -40°C...85°C. Typical values are at VSUPx=+3.6V, TA= 25°C, unless otherwise specified.

Typical Operating Characteristics

This page is intentionally left blank.

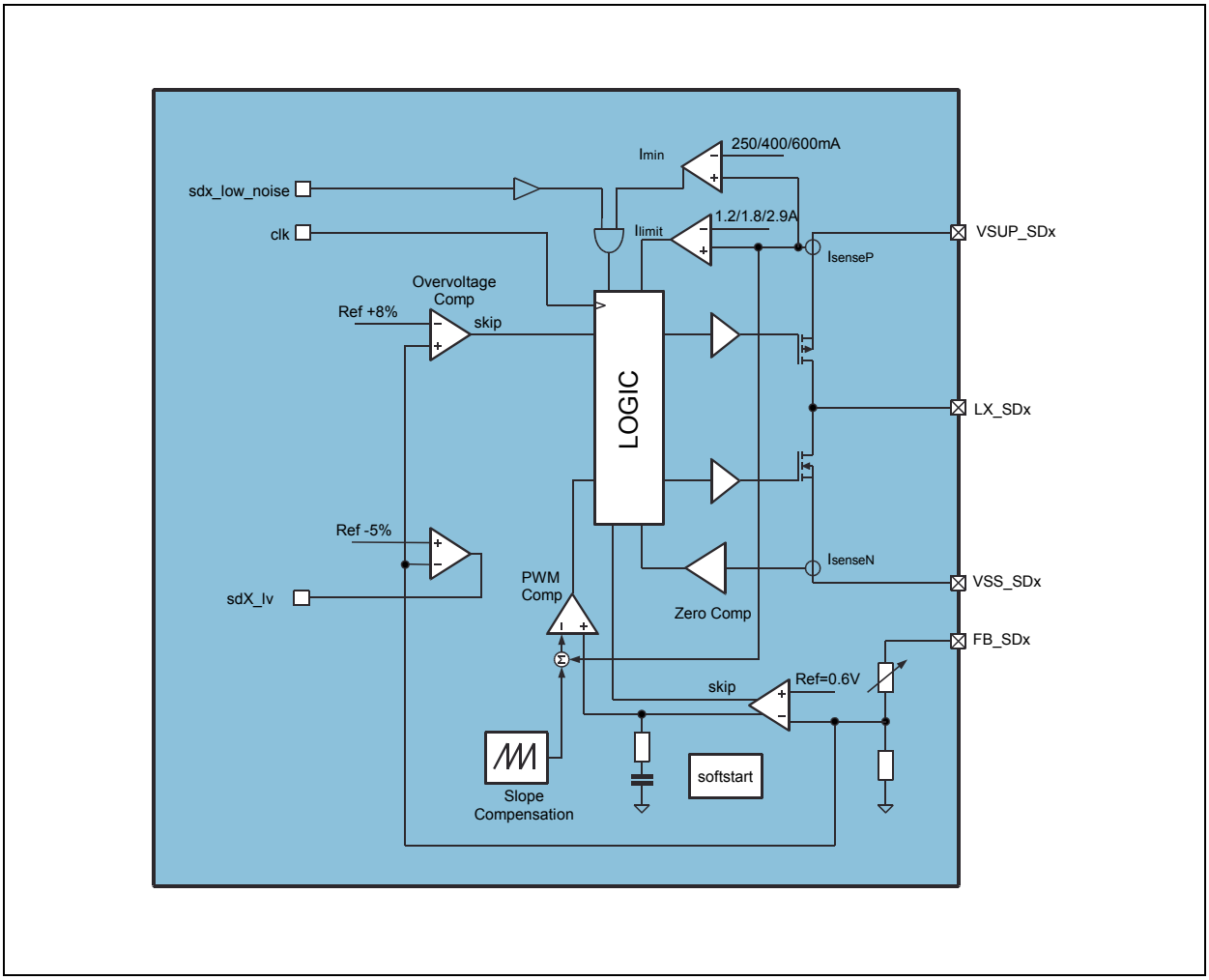
Detailed Descriptions-Power Management Functions

DCDC Step-Down Converter

Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 1.5A (SD4, SD5), 2A (SD3) and 5A for SD2, with an output capacitor of only 8-27µF. The implemented current limitation protects the DCDC and the coil during overload condition.

Figure 9:
Step Down DC/DC Converter Block Diagram



DCDC Step Down Converter Block Diagram: Shows the internal structure of the DCDC bucks.

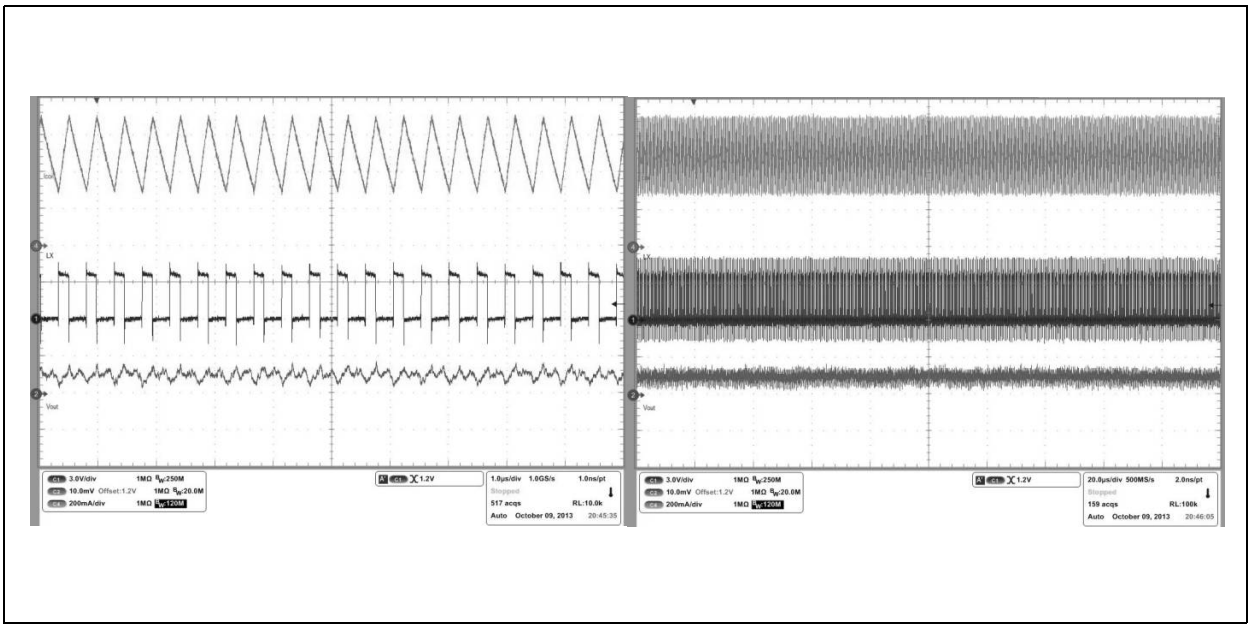
Mode Settings

Low Ripple, Low Noise Operation

Bit settings: *sdX_low_noise*=1

In this mode there is no minimum coil current necessary before switching off the PMOS. As long as the load current is superior to the ripple current the device operates in continuous mode.

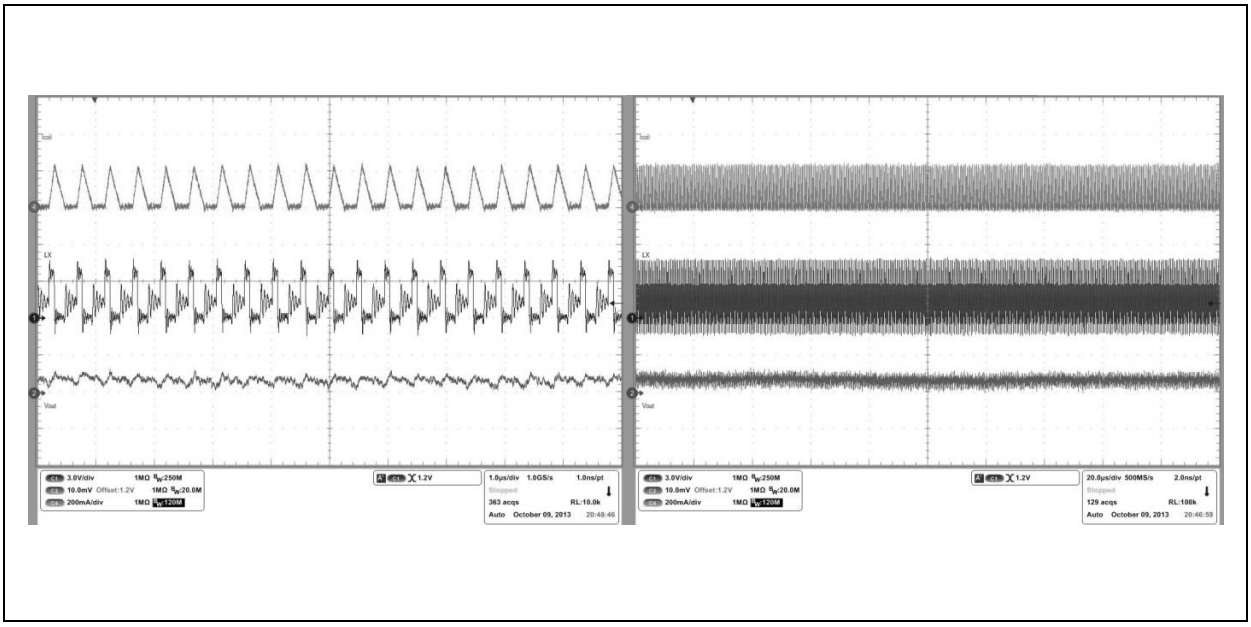
Figure 10:
DC/DC Buck Continuous Mode



DC/DC Buck Continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 500mA.

When the load current gets lower, the discontinuous mode is triggered. As result, the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to tmin_on to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences.

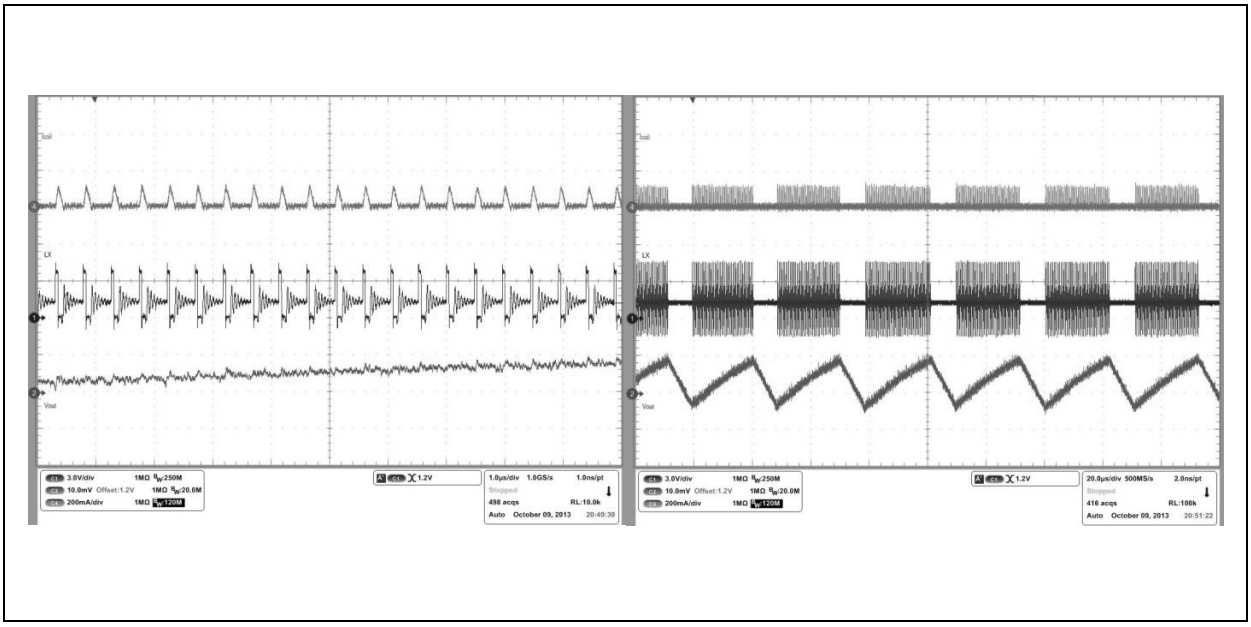
Figure 11:
DC/DC Buck Dis-Continuous Mode



DC/DC Buck Dis-Continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 60mA.

Only in the case the load current gets so small that less than the minimum on-time of the PMOS would be needed to keep the loop in regulation the regulator will enter power save operation and skip pulses during this time. The crossover point is about ~1% of the DCDC current limit.

Figure 12:
DC/DC Buck Dis-Continuous & Low Power Mode



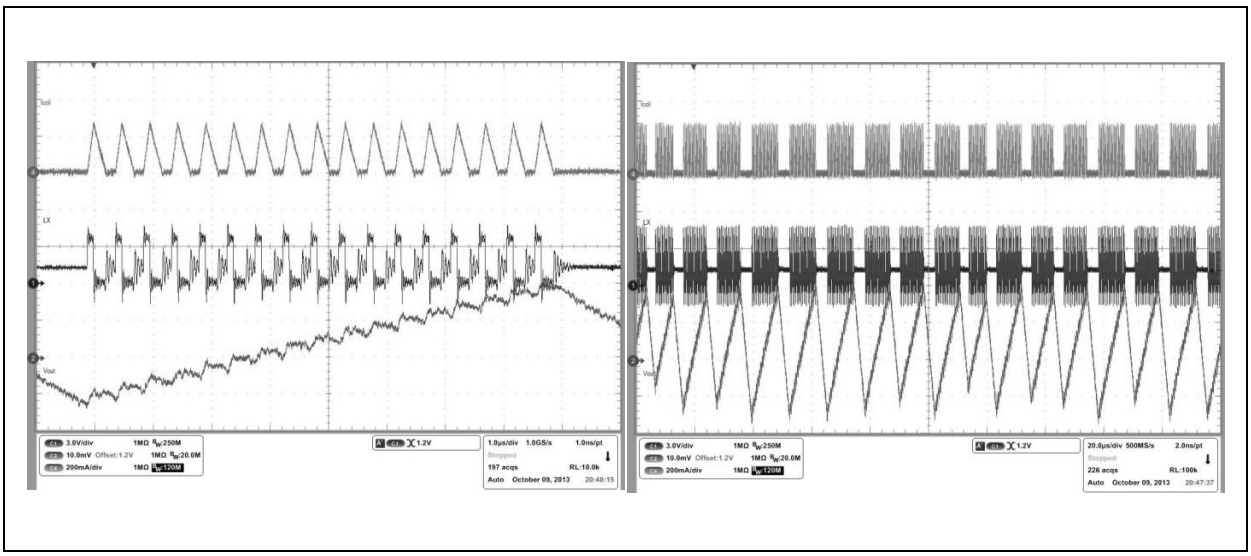
DC/DC Buck Dis-Continuous & Low Power Mode: Shows the DC/DC switching waveforms of for SD5 at about 10mA.High efficiency operation (default setting):

Bit settings: *sdX_low_noise*=0

In this mode there is a minimum coil current necessary before switching off the PMOS. As a result there are less pulses necessary at low output loads, and therefore the efficiency at low output load is increased. As drawback this mode increases the ripple up to higher output currents.

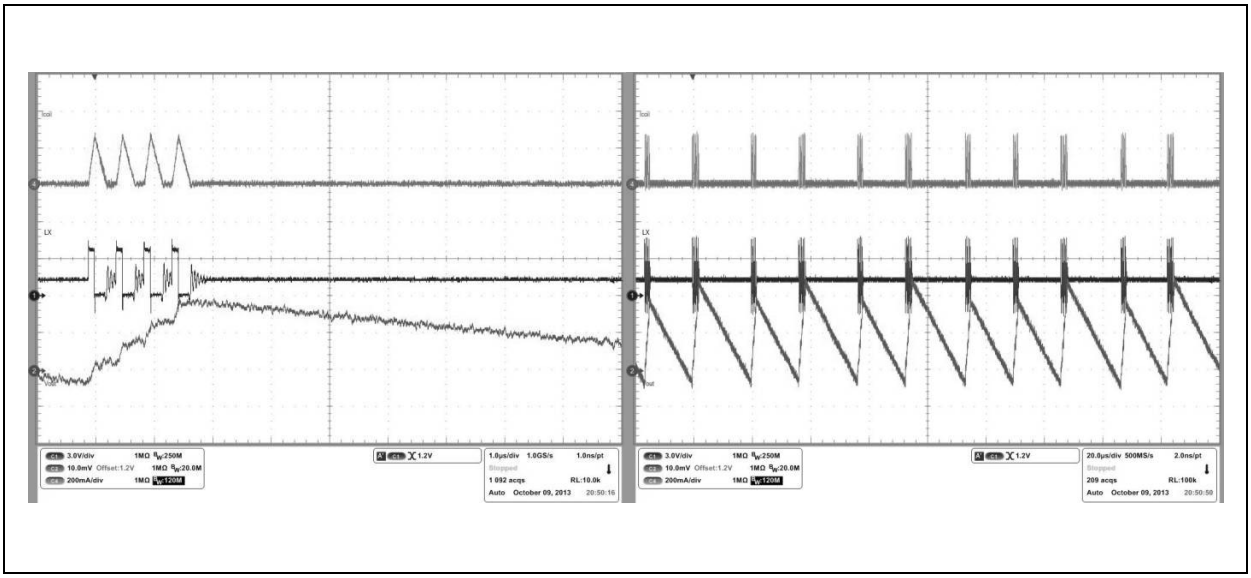
The crossover point to power save operation is already reached at reasonable high output currents (~10% of the DCDC current limit).

Figure 13:
DC/DC Buck Dis-Continuous Mode & High Efficiency 1/2



DC/DC Buck Dis-Continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 60mA with the low_noise bit deactivated.

Figure 14:
DC/DC Buck Dis-Continuous Mode & High Efficiency 2/2



DC/DC Buck Dis-Continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 10mA with the low_noise bit deactivated.

It's possible to switch between these two modes during operation.

Power Save Operation (Automatically Controlled)

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/under-shoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a bigger output capacitor to guarantee the stability of the regulator. The mode is enabled by setting *sdX_fast* =1.

Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency for SD2, SD3, SD4 and SD5 can be set to 3 or 4MHz. This mode is selected by setting *sdX_freq* to the appropriate value.

100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

Step-Down Converter Configuration Modes

The step down dc/dc converters have two configuration modes to deliver different output currents for the applications. The operating mode is selected by setting the bit *sd3_slave*, *sd4_slave* and *sd5_slave* (the default is set by the Boot-OTP). It's not allowed to set *sd3_slave* and *sd4_slave* at the same time.

Figure 15:
DC/DC Buck Converter Normal Operation

DC/DC Buck Normal Operation: Shows the internal DC/DC buck converters in normal operation independent from each other; no slave mode set

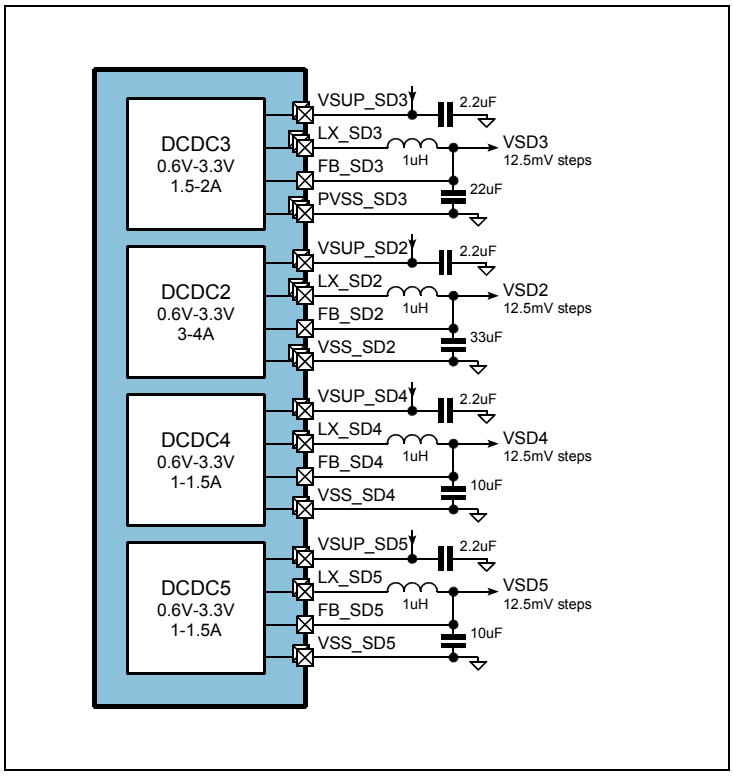


Figure 16:
DC/DC Buck Converter SD4+SD5 (2-3A) Mode

DC/DC Buck Slave Operation: Shows the internal DC/DC buck converters with SD5 operating as slave of SD4 to increase the output current. (*sd5_slave* = 1)