Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# AS3900

## 27MHz Low Power Star Network Transceiver

## 1 General Description

The AS3900 is a low power FSK transceiver ideal for battery-operated short range devices (SRD) applications in which a limited amount of data (data rate up to 210 kbit/s) need to be transferred. The device can be configured as transceiver, transmitter only or receiver only system and operates in one channel in the worldwide ISM band at 27 MHz.

The frequency of the external oscillator determines the operating frequency. Use of 27 MHz is in particular advantageous for communication in close proximity of the human body due to the low absorption of the signal by tissue because of the low specific absorption rate at 27 MHz. The device incorporates a serial digital interface (SDI), which enables bidirectional communication with external system components.

The integrated real-time-clock, sophisticated wake-up functionality, and link manager enable current efficient control of all communication events and eliminate the need for an expensive microcontroller.

The AS3900 supports data transfer in burst mode (bidirectional, controlled by link manager), semi-continuous (bidirectional, controlled by microcontroller) and continuous mode (unidirectional, controlled by microcontroller) and requires only a small number of external components.

## 2 Key Features

- FSK transceiver
- Operating frequency 27.12 MHz (ISM - band)
- Integrated real-time-clock (RTC) based on 32.768kHz XTAL
- FM deviation selectable (±106 kHz, ±53 kHz)
- Data transfer in burst mode and (semi-)continuous mode
- Data rate adjustable to 26.5, 53, 106, 212 kbit/s
- Low average current consumption in Tx and Rx mode
- Output power adjustable to 0, +5, +10 dBm
- Integrated OOK based wake-up system
- Link manager for control of star network with up to 8 clients
- Bidirectional serial digital interface (SDI)

**Main Characteristics**

- Operating temperature range -40ºC to +85ºC
- Operating supply voltage 2.2V to 3.6V (Functional down to 2.0V)
- Rx current consumption 3.8 mA (typ.)
- Tx current consumption 4.9 mA@0dBm, 7.6 mA @10dBm
- Maximum output power 10 dBm (delivered to matching network and antenna)
- Receiver sensitivity –88 dBm @ 106 kbit/s
- Polling mode average current consumption typ. 2.5µA
- Power down current consumption max. 700nA
- Typ. communication range using small antenna 1.2m@0dBm, 2.5m@10dBm
- QFN 28 pin (5x5) package

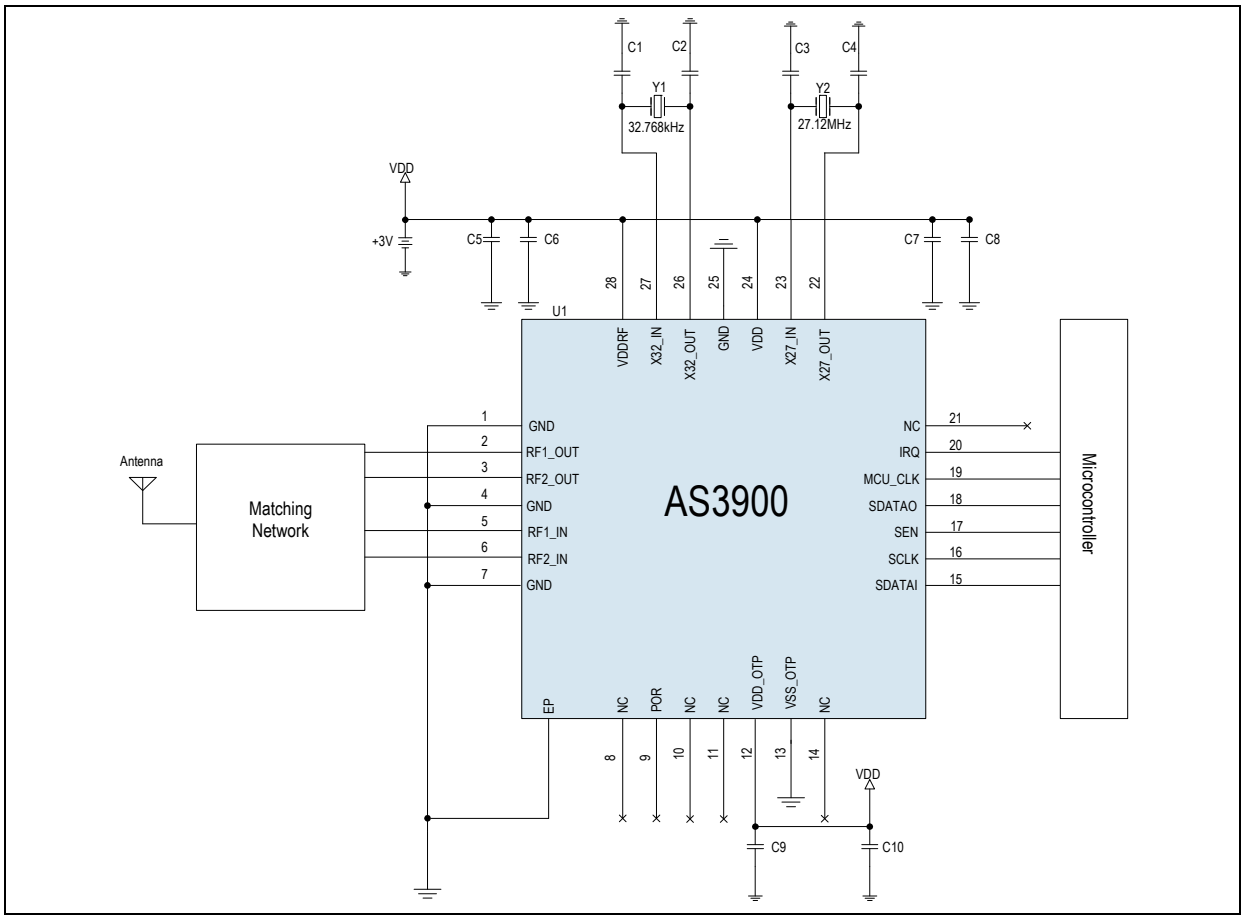
**Additional Features**

- Reliable pairing and synchronization of master and clients
- Automatic 16 bit CRC computation in burst mode
- Auto-acknowledgement and re-transmit
- Programmable timers to assign variable communication cycle times
- Reliable system start due to internal POR
- Programmable microcontroller clock frequency
- Separate interrupt request line
- Battery level detector
- Digital RSSI value accessible in register
- User programmable Identification with OTP memory (24 bits)

## 3 Applications

The AS3900 is ideal for reliable low-power short-range data exchange, data transfer among devices in close proximity of human body (Body Area Networks), simple control networks (home, industry), and interactive remote controls. A typical application can be designed in combination with a microcontroller, an antenna and a few additional passive components.

*Figure 1. Typical Application Diagram of Low Power Star Network Transceiver AS3900*



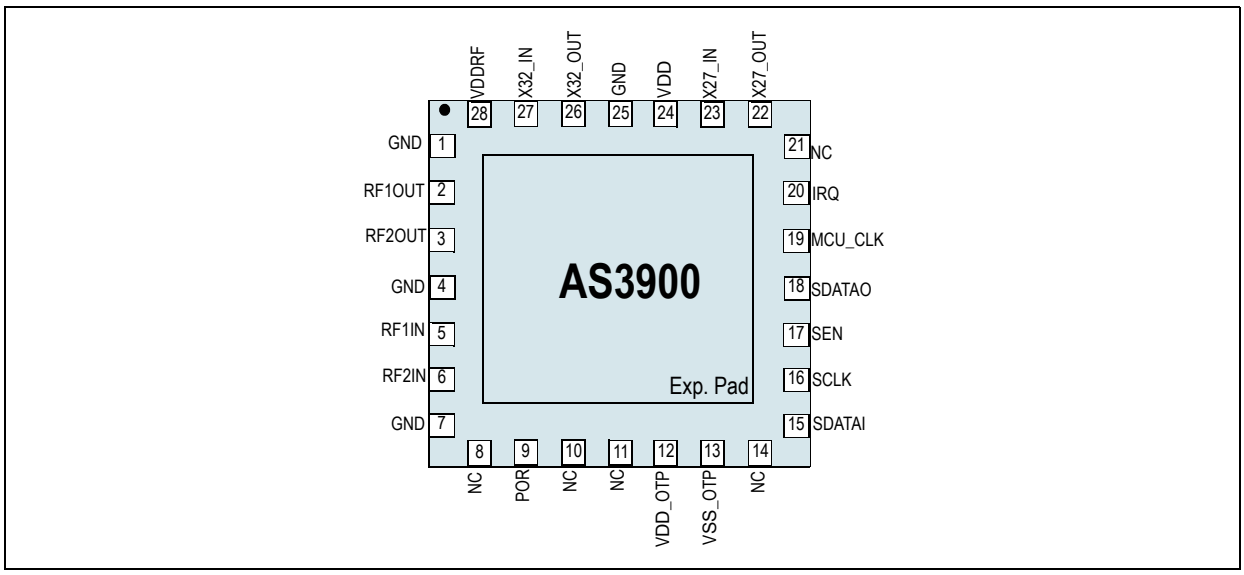

**Abbreviations**

| | |
|---|---|
| ACK: | Acknowledgement |
| ACP: | Acknowledgement Plus Data |
| BER: | Bit Error Rate |
| CRC: | Cyclic Redundancy Check |
| FSK | Frequency Shift Keying |
| I/Q: | In-Phase/Quadrature |
| ISM | Industrial, Scientific and Medical |
| LNA | Low Noise Amplifier |
| MCU | Microcontroller |
| NAK | Negative Acknowledge Character |
| NAR | Negative Acknowledge Return |
| OOK | On Off Keying |
| OTP | One Time Programmable |
| PER | Packet Error Rate |
| PA | Power Amplifier |
| PRBS | Pseudorandom Binary Sequence |
| RSSI | Received Signal Strength Indication |
| POR | Power on Reset |
| REG | Register, MAIN Register |
| SREG | SHADOW Register |
| RTC | Real Time Clock |
| RF | Radio Frequency |
| RX | Receive – Receive Mode |
| SRD | Short Range Devices |
| TX | Transmit, -Transmit Mode |
| XREF | Reference Crystal Oscillator |
| XTAL | Crystal Oscillator |

# Contents

# 4 Pin Assignment

*Figure 2. AS3900 Pin Assignment (Top View)*




## 4.1 Pin Description

*Table 1. QFN 28 pin Package*

| Pin Name | Pin Number | Pin Type | Description |
|---|---|---|---|
| GND | 1 | S | **Negative RF Supply Voltage.** Ground reference point for VDDRF. |
| RF1OUT | 2 | AO | **Transmitter Positive Output.** Analog Push/Pull Output of Power Amplifier for positive amplitude. Output Impedance can be programmed to 12.5Ω or 25Ω. Transmitter can be programmed to single ended or true-differential analog outputs. |
| RF2OUT | 3 | AO | **Transmitter Negative Output.** Analog Push/Pull Output of Power Amplifier for negative amplitude. Output Impedance can be programmed to 12.5Ω or 25Ω. Transmitter can be programmed to single ended or differential analog outputs. In single ended mode RF2OUT is connected to GND. |
| GND | 4 | S | **Negative RF Supply Voltage.** Ground reference point for RF outputs and inputs. |
| RF1IN | 5 | AI | **Receiver Positive Input**. Positive analog input of differential Low Noise Amplifier. |
| RF2IN | 6 | AI | **Receiver Negative Input.** Negative analog input of differential Low Noise Amplifier. |
| GND | 7 | S | **Negative RF Supply Voltage.** Ground reference point for RF outputs and inputs. |
| NC | 8 | | Not connected. Leave the pin floating. |
| POR | 9 | DO | **Power On Reset output:** Digital Output that indicates hardware reset of the device.<br>Reset Low: VDD > 1.35V |
| NC | 10 | | Not connected. Leave the pin floating. |
| NC | 11 | | Not connected. Leave the pin floating. |
| VDD_OTP | 12 | S | **Positive OTP Supply Voltage.** 2.2V to 3.6V for operation mode. For fuse mode apply a minimum supply voltage of 3.3V. Buffer capacitors of 10µF and 100nF are needed for fuse mode. |

*Table 1. QFN 28 pin Package*

| Pin Name | Pin Number | Pin Type | Description |
|---|---|---|---|
| VSS_OTP | 13 | S | **Negative OTP Supply Voltage**. Ground reference for VDD_OTP. Decouple point for buffer capacitors of VDD_OTP. |
| NC | 14 | | Not connected. Leave the pin floating. |
| SDATAI | 15 | DI | **Serial Digital Interface DATA input.** Serial Data Input for writing registers. The bits are clocked in on the falling edge of SCLK. |
| SCLK | 16 | DI | **Serial Digital Interface Clock.** A serial clock provides the SCLK for accessing data from the AS3900. Write and read operation is provided by the SCLK. |
| SEN | 17 | DI | **Serial Digital Interface Enable.** CMOS digital input. Falling edges on SEN ends a read or write operation and frames the serial data transfer. |
| SDATAO | 18 | DO | **Serial Digital Interface DATA output.** Serial Data Output for reading registers. The bits are clocked out on the rising edge of SCLK and can be read from the microcontroller on the falling edge of SCLK. |
| MCU_CLK | 19 | DO | **Microcontroller Clock Output.** Programmable Clock for microcontroller that is derived from the 27MHz crystal oscillator. System frequency for microcontroller can be adjusted between 188kHz and 3.39MHz. |
| IRQ | 20 | DO | **Interrupt Output.** Digital CMOS Output for external interrupt input at microcontroller. If an interrupt condition is met a HIGH level is applied on the IRQ pin. The IRQ level is set to low level after the internal interrupt registers are read manually. An interrupt can be triggered on the rising edge of the IRQ pin. |
| NC | 21 | | Not connected. Leave the pin floating. |
| X27_OUT | 22 | AO | **27MHz oscillator output.** Analog output for 27.12MHz crystal oscillator. |
| X27_IN | 23 | AI | **27MHz oscillator input.** Analog input for 27.12MHz crystal oscillator |
| $V_{DD}$ | 24 | S | **Positive Digital Supply Voltage.** 2.2V to 3.6V. Decoupling capacitors (1µF, 100nF and 100pF) are recommended. |
| GND | 25 | | **Negative Digital Supply Voltage.** Ground reference point for VDD. Decouple point for capacitors. |
| X32_OUT | 26 | AO | **32kHz oscillator output.** Analog output for 32.768kHz crystal oscillator. |
| X32_IN | 27 | AI | **32kHz oscillator input.** Analog input for 32.768kHz crystal oscillator |
| $V_{DD}$RF | 28 | S | **Positive RF Supply Voltage.** 2.2V to 3.6V. Decoupling capacitors (1µF, 100nF and 100pF) are recommended. |

# 5 Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Detailed Description are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Table 2. Absolute Maximum Ratings*

| Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|
| DC supply voltage ($V_{DD}$) | -0.5 | 5.0 | V | |
| Input pin voltage($V_{IN}$) | -0.5 | 5.0 | V | |
| Input current (latchup immunity) ($I_{scr}$) | -100 | 100 | mA | Norm: Jedec 78 |
| ESD for digital pins (ESDD) | ±2 | | kV | Norm: MIL 883 E method 3015 (Human Body Model) |
| ESD for analog pins (ESDA) | ±2.0 | | kV | Norm: MIL 883 E method 3015 (Human Body Model) |
| ESD for RF pins (ESDRF) | ±1.5 | | kV | Norm: MIL 883 E method 3015 (Human Body Model) |
| Total power dissipation ($P_t$) (all supplies and outputs) | | 30 | mW | TX: 8mA*3.6V=29mW |
| Storage temperature ($T_{strg}$) | -55 | 125 | ºC | |
| Package body temperature ($T_{body}$) | | 260 | ºC | The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”. The lead finish for Pb-free leaded packages is matte tin (100% Sn). |
| Humidity non-condensing | 5 | 85 | % | |

# 6 Electrical Characteristics

VDDRF=VDD=VDD_OTP= 2.2V to 3.6V; TAMB= -45 to +85ºC; Typical values at VDD=3.0V and TAMB=25ºC; Unless otherwise specified.

*Table 3. Electrical Characteristics*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Operating Conditions** | | | | | | |
| VDDRF | Positive analog supply voltage | Functional down to 2.0V | 2.2 | | 3.6 | V |
| GND | Negative analog supply voltage | | 0 | | 0 | V |
| VDD | Positive digital supply voltage | Functional down to 2.0V | 2.2 | | 3.6 | V |
| GND | Negative digital supply voltage | | 0 | | 0 | V |
| VDD_OTP | Positive OTP supply voltage | Buffer Capacitor connected here for FUSE Mode. In Fuse Mode a minimum supply voltage of 3.3V is needed. Functional down to 2.0V | 2.2 | | 3.6 | V |
| VSS_OTP | Negative OTP supply voltage | Buffer Capacitor connected here for FUSE Mode | 0 | | 0 | V |
| A - D | Difference of supplies | VDDRF – VDD<br>GNDRF – VSS | -0.1 | | 0.1 | V |
| $f_{clk}$ | System clock frequency | | | 27.12 | | MHz |
| **Current Consumption** | | | | | | |
| $I_{PD}$ | POWER-DOWN mode | | | | 700 | nA |
| $I_{SB}$ | STANDBY mode | Timers running<br>Wakeup Receiver listens every 1s | | 2.5 | | µA |
| $I_{SL}$ | SLEEP mode | Timers running<br>no data transmission | | 1.8 | | µA |
| $I_{WRX}$ | WAKEUP RX mode | | | 2.5 | | mA |
| $I_{WTX}$ | WAKEUP TX mode, 10dBm | | | 5.1 | | mA |
| $I_{RX}$ | RX mode | | | 3.8 | | mA |
| $I_{TX10}$ | TX mode, 10dBm | | | 7.6 | | mA |
| $I_{TX5}$ | TX mode, 5dBm | | | 5.5 | | mA |
| $I_{TX0}$ | TX mode, 0dBm | | | 4.9 | | mA |
| **DC/AC Characteristics for Digital Inputs and Outputs** | | | | | | |
| **CMOS Input** | | | | | | |
| $V_{IH}$ | High level input voltage | | 0.7 * VDD | | | V |
| $V_{IL}$ | Low level input voltage | | | | 0.3 * DVDD | V |
| $I_{LEAK}$ | Input leakage current | | | | 1 | µA |
| **CMOS Output** | | | | | | |
| $V_{OH}$ | High level output voltage | | VDD - 0.5 | | | V |
| $V_{OL}$ | Low level output voltage | | | | GND + 0.4 | V |
| $C_L$ | Capacitive load | | | | 50 | pF |

## 6.1 Electrical System Specification

### 6.1.1 General

*Table 4. General*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VDD | Supply voltage | operational | 2.2 | 3.0 | 3.6 | V |
| VDD | Supply voltage | functional | 2.0 | | | V |

### 6.1.2 Modulation Method

*Table 5. Modulation Method*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Modulation | | | FSK | | |
| | Frequency range | 27.12 MHz ISM Band ±163 kHz | | 26.957 | | MHz |
| | | | | 27.283 | | |
| BR | Bit rate | Values derived from 27.12 MHz | | 26.5 | | kbit/s |
| | | | | 53 | | kbit/s |
| | | | | 106 | | kbit/s |
| | | | | 212 | | kbit/s |
| FDev | Frequency deviation | Values derived from 27.12 MHz | | ±53 | | kHz |
| | | | | ±106 | | |

### 6.1.3 Transmission Frame

*Table 6. Transmission Frame*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| TFS | Transmission Frame Size | Minimum Frame Size | | 9 | | bytes |
| | | Maximum Frame Size | | 32 | | |
| TPre | Preamble | | | 16 | | bits |
| TAddr | Address | | | 24 | | bits |
| TDataL | Data Length Indicator | | | 8 | | bits |
| TSynch | Synchronization | | | 8 | | bits |
| TPayl | Transmission Frame Payload | Minimum Payload | | 0 | | bytes |
| | | Maximum Payload | | 26 | | |
| | CRC16 | CRC-CCITT (CRC-16) | | | 16 | bits |

### 6.1.4 Receiver RX

*Table 7. Receiver RX*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Sensitivity | | PER (Packet Error Rate) = 1%<br>TFS = 32 bytes | | | | |
| | @ 26.5kbps Datarate<br>f_dev = 106kHz | 420Ω seen by LNA input | | 90 | | dBm |
| | | | | 20.5 | | µVrms |
| | @ 53kbps Datarate<br>f_dev = 106kHz | 420Ω seen by LNA input | | 88 | | dBm |
| | | | | 25.8 | | µVrms |
| | @ 106kbps Datarate<br>f_dev = 106kHz | 420Ω seen by LNA input | | 88 | | dBm |
| | | | | 25.8 | | µVrms |
| | @ 212kbps Datarate<br>f_dev = 106kHz | 420Ω seen by LNA input | | 79 | | dBm |
| | | | | 72.7 | | µVrms |
| Blocking | | C = Sensitivity + 3dB | | B[dB] = C[dBm] - I[dBm] | | |
| DR = 53kbps,<br>f_dev = 106kHz | 0 MHz | Unmodulated interferer | | -25 | | dB |
| | 0 MHz | Modulated interferer | | 16 | | dB |
| | ± 1MHz | Unmodulated interferer | | -26 | | dB |
| | ± 1MHz | Modulated interferer | | -21 | | dB |
| DR = 106kbps,<br>f_dev = 106kHz | 0 MHz | Unmodulated interferer | | -25 | | dB |
| | 0 MHz | Modulated interferer | | 16 | | dB |
| | ± 1MHz | Unmodulated interferer | | -24 | | dB |
| | ± 1MHz | Modulated interferer | | -22 | | dB |
| DR = 212kbps,<br>f_dev = 106kHz | 0 MHz | Unmodulated interferer | | -25 | | dB |
| | 0 MHz | Modulated interferer | | 25 | | dB |
| | ± 1MHz | Unmodulated interferer | | -15 | | dB |
| | ± 1MHz | Modulated interferer | | -15 | | dB |
| | Maximum input signal | | | 100 | | mVrms |
| | IP3 | Measured at the balun input with two carriers of -82dBm | | -69 | | dBm |
| RSSI | | 4 Bit linear, read from register | | | | |
| | RSSI start | | | 10 | | µVrms |
| | RSSI stop | | | 150 | | µVrms |
| | RSSI resolution | | | 10 | | µVrms |
| | current consumption | | | 3.8 | | mA |

### 6.1.5 Transmitter TX

*Table 8. Transmitter TX*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | TX linear output power | Power delivered to the matching network including antenna | | 10 | | dBm |
| | | | | 5 | | dBm |
| | | | | 0 | | dBm |
| Current Consumption | | | | | | |
| $I_{TX}$ | Current consumption | No power delivered to antenna | 1.6 | 2.3 | 2.9 | mA |
| $I_{TX10}$ | Operation current consumption | 10 dBm power delivered to matching network @ 420Ω | | 7.6 | | mA |
| | Harmonic Level | With Evaluation Board (including PCB antenna) | Meets: ETSI EN 300 220-1 v1.3.1 Sept. 2001 FCC CFR47 Section 15.227, May 2007 | | | |

### 6.1.6 Wakeup RX

*Table 9. Wakeup RX*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Sensitivity @ 96kbps On Off Keying | 420Ω seen by Wakeup receiver input | | 30 | | µVrms |
| | Maximum Input Signal | | | 10 | | mVrms |
| | Antenna impedance | With external matching network | | 420 | | Ω |
| | Current consumption | | 1.8 | 2.5 | 3.3 | mA |

### 6.1.7 RTC Crystal Oscillator 32.768 kHz

*Table 10. RTC Crystal Oscillator 32.768 kHz*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Crystal accuracy (initial) | Overall accuracy | | | ±120 | p.p.m. |
| | Frequency | | | 32.768 | | kHz |
| | Start-up Time | Crystal dependent | | 200 | | ms |
| | Duty cycle | Depends on XTAL properties | 45 | 50 | 55 | % |
| | Current consumption | | | 600 | | nA |

### 6.1.8 XREF Crystal Oscillator 27 MHz

*Table 11. XREF Crystal Oscillator 27 MHz*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Crystal accuracy (initial + temp + ageing) | | | | ±120 | p.p.m. |
| | Frequency | | | 27.12 | | MHz |
| | Duty cycle | | 45 | 50 | 55 | % |
| | Start-up time | 22 clock cycles of 32kHz XTAL | | 671 | | µs |
| | Current consumption | Crystal and Pulling Capacitor dependent | | 340 | | µA |

### 6.1.9 Battery Level Detector

*Table 12. Battery Level Detector*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VDD | Operation Supply Voltage | | 1.9 | | 3.6 | V |
| $V_{LS}$ | Low Supply Voltage Threshold | Hysteresis = ±40mV<br>4 bit Register selectable | | 1.98<br>2.18<br>2.39<br>2.57 | | V |

### 6.1.10 Power-On-Reset Generator

*Table 13. Power On Reset Generator*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VDD | Operation Supply Voltage | | 0.0 | | 3.6 | V |
| $V_{PHS}$ | Power ON Threshold | Rising slope (0.3V/ms) of Supply Voltage | | 1.35 | | V |

# 7 Typical Operating Characteristics

*Figure 3. Blocking of Interferer vs Frequency (DR=106kbps, f_dev=106kHz)*

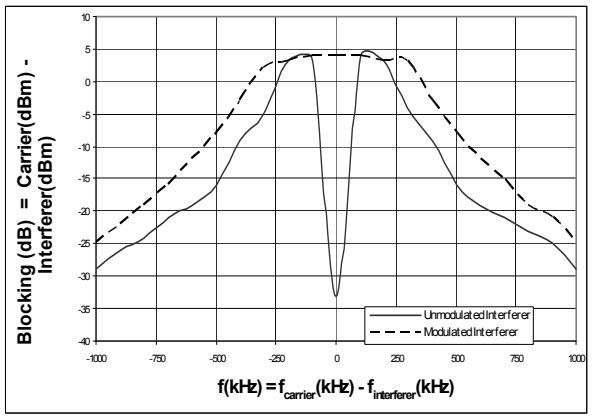



*Figure 4. Blocking of Interferer vs Frequency (DR=53kbps, f_dev=106kHz)*

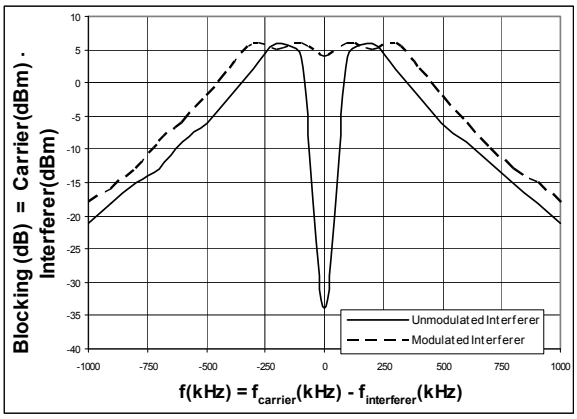



*Figure 5. Supply Current vs. Impedance of Antenna+Matching Network (PA=differential, Rout=12.5Ohm, cont. Tx)*

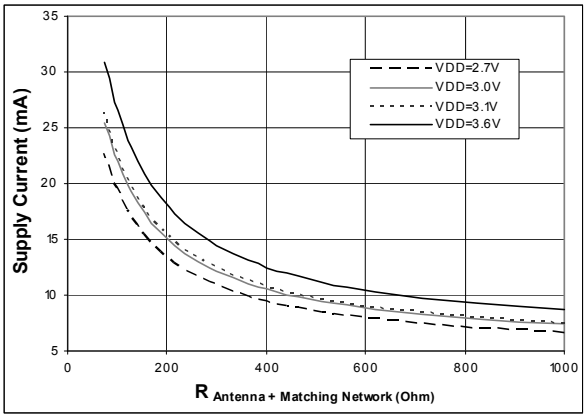



*Figure 6. Output Power vs. Impedance of Antenna+Matching Network (PA=differential, Rout=12.5Ohm, cont. Tx)*

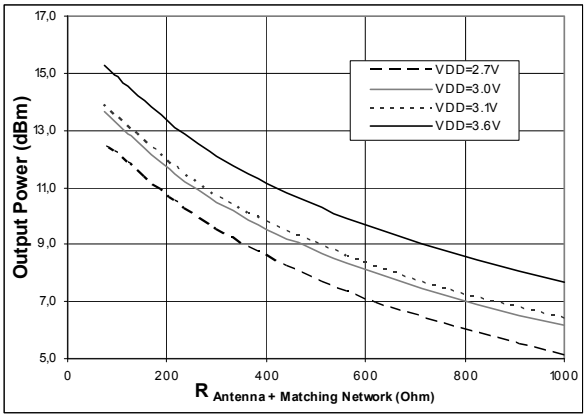



*Figure 7. Output Power vs. Supply Voltage (PA=differential, R Ant+Matching=422Ohm, cont. Tx)*

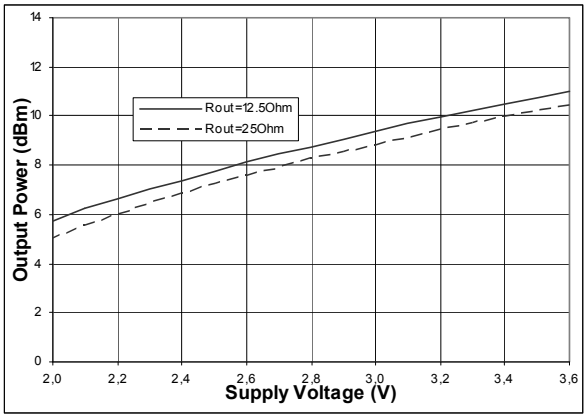
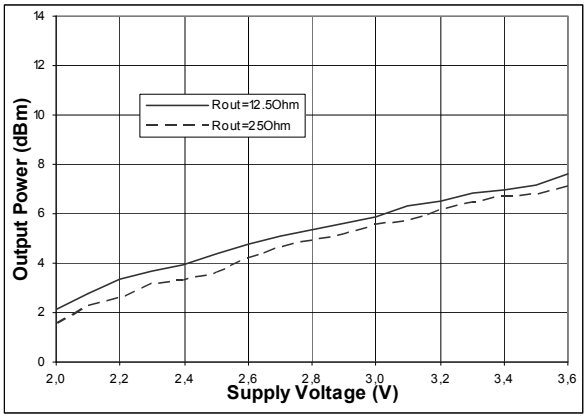



*Figure 8. Output Power vs. Supply Voltage (PA=single ended, R Ant+Matching=422Ohm, cont. Tx)*



# 8 Detailed Description

The AS3900 transceiver is an integrated solution of one receiver and one transmitter capable of supporting a bidirectional communication between one Master and up to eight Clients via the 27MHz ISM band. The AS3900 is designed to operate with a single 2.2V to 3.6V supply and consumes less than 3.8mA in receive mode and 7.6mA in transmit mode (10dBm). The device is even functional down to a supply voltage of 2.0V and has a built in battery level detector, that level can be read via the SDI interface.

The AS3900 provides an adjustable data rate of 26.5 kbps up to 212kbps and transmits an adjustable (via external matching circuitry) output power of maximal 10dBm. The transmission is done through a power amplifier that sends a Miller coded FSK modulated signal. A I/Q up mixer generates the modulated RF-signal based on the carrier of 27.12MHz. The deviation of the frequency shift can be set to ±106kHz or to ±53kHz in order to limit the allocated bandwidth in the ISM band. An integrated low pass filter cuts off additional interference frequencies.

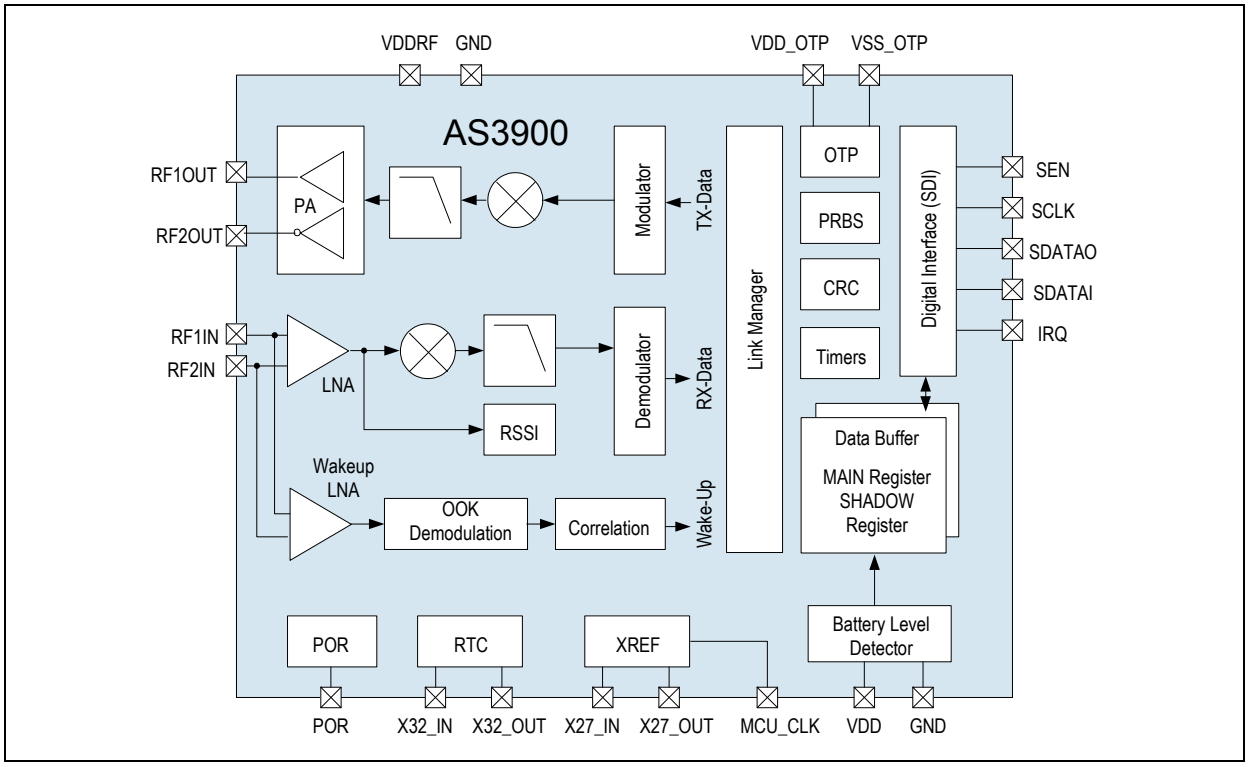
The analog outputs of the PA can be programmed as single ended or fully differentially, which doubles the transmitter output voltage level. In addition the output impedance of the PA can be selected between 25Ω and 12.5Ω. The output power is mainly determined by the applied output impedance of the antenna and the matching network.

The AS3900 features a zero-IF receiver. The receiver consists of a differential low noise amplifier (LNA) that amplifies the incoming RF signal. The actual received signal strength (RSSI) is measured and converted to a digital value that can be read via the serial data interface. Afterwards the incoming signal is down converted (I and Q) to the base band by the mixer. The I/Q signal is filtered and fed to the demodulator.

Furthermore the receiver consists of a Wakeup LNA. The amplified wakeup signal is demodulated and correlated with the OOK-pattern. This functionality guarantees very low power requirements ideal for battery-operated applications. The device is set to STANDBY mode and scans periodically for the ON OFF keying signal (OOK) with the Wakeup receiver, which only consumes an average current of 2.5µA. Once detected the AS3900 enters the normal RX mode.

A key feature of the AS3900 is the integrated Link Manager. The Link Manager controls all issues regarding the low level communication. It manages the link parameters and the timings in order to set-up and to maintain up to 8 communication links simultaneously. The link manager uses the integrated timers and the pseudorandom binary sequence (PRBS), to run the low level actions automatically. For reliable data transmission a 16 bit CRC block is integrated. Furthermore the transmitted data is Miller coded. Two crystal oscillators must be connected in order to generate the carrier of 27.12MHz and the time base for the timers (RTC), which is 32.768 kHz. The clock source for the MCU_CLK can be converted from the 32.768 kHz real-time clock or from the 27.12MHz carrier. The 4-wire SDI (Serial Data Interface) is used for configuration of the AS3900 and to serve the link manager. The SDI interface allows the access to the MAIN register as well as to the SHADOW register. The data for the RF transmission is saved into the data buffer at the Clients and can be collected at the Master that is again saved in the data buffer in the MAIN register. A simplified block diagram of the AS3900 is shown in Figure 9.

*Figure 9. Block Diagram of Low Power Star Network Transceiver AS3900*



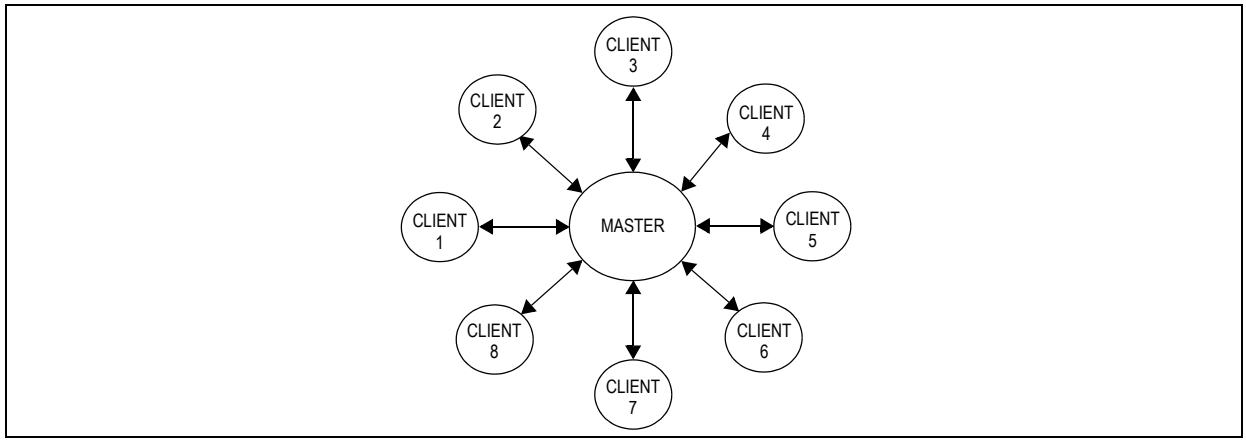
## 8.1 Network Management

The transceiver is optimized for short range, low data rate applications where low power consumption is very critical, and therefore the data is sent in short packages with higher data rate.

### 8.1.1 Network

The transceiver supports a star network consisting of one master and maximum 8 clients as presented in Figure 10. The master acts as a data processor and collector, the clients act as data producers. In one-way communication mode, a client sends a data package to a master and is not aware of lost packages. In two-way communication mode, a client sends a data package to a master, and waits an acknowledgement from the master. The master manages the parameters used for communication.

*Figure 10. Star Network*




### 8.1.2 Link Manager or Network Manager

The link manager has an essential role in receiving and transmitting of data in the star network. It manages the link parameters and the timings in order to set-up and to maintain up to 8 communication links simultaneously.

- Data transmission:
  The microcontroller (MCU) supplies data via SDI to an integrated TX data buffer from where the link manager takes the data, adds the needed network management bits (preamble, device ID, time code, and CRC), and enables the transmitter for transmitting the data package at the dedicated time slot.

- Data Reception:
  The link manager wakes up the receiver at the dedicated time slot. It checks the CRC of the payload data and if that is correct, it removes all network management bits and stores the data to a RX data buffer. The link manager gives an interrupt to the MCU, which can then retrieve data via SDI.

### 8.1.3 Principle of Communication

The data communication between the Master and the Client proceeds in the following way:

The MCU, via the serial data interface, writes the payload data into the data buffer of the AS3900. The link manager takes this data from the registers and adds the header for the network management. Preamble, Client ID, Timing Information, and CRC are added to the data, which takes 51 Bytes. The 192 bits (24 bytes) of data can be transmitted within one frame. The total maximum size is 75 Bytes (51 bytes header + 24 bytes data). The Client sends this packet at a certain time slot that is allocated for this Client. The timing information is part of every frame. Master and Client are re-synchronized automatically by using this timing information.

The Master opens the receive window at the allocated time slot and receives the packet. Therefore the link manager wakes up from sleep mode at this timeslot and turns on the RX mode (LNA is active). Afterwards the packet is checked for transmission errors with the 16 bit CRC check. If no error occurred the link manager removes the header and forwards the payload data to the data buffer. If the transmission is finished the MCU is informed via the interrupt line (IRQ). All settings can be changed in the register maps. Main and Shadow Register availability depends on operation mode.

## 8.2 Operating Modes

The following different operation modes are supported by the AS3900. These operating modes are entered automatically by the link manager and need not to be set manually. The device enters these modes depending on the current status of the communication. All operating modes require different current consumptions.

### 8.2.1 Power-down

Power-down mode is entered after connecting the battery. The POR signal is provided at the POR pin and registers will have their default values. The lowest current consumption is achieved in this mode. No clock is provided at MCU_CLK pin (the MCU must have other CLK source). The ENABLE pin LOW is needed to switch to Power-down (DATAO pin is set to High Impedance). Make sure to apply LOW level on the SDI-Interface to avoid leakage currents via the digital lines.

### 8.2.2 Standby

No active communication (idle mode), no connection (no synchronization) established between master and client, SDI is operational. Wakeup Timer and 32 kHz oscillator are running. Wakeup receiver is switched on periodically. Clock can be provided at MCU_CLK pin (divided 27MHz clock or 32 kHz clock). A Clock Interface Mode selection is required.

### 8.2.3 Sleep

This mode is active between communication time slots without data transmission. The timer (cycle time) indicate next active communication time slots. Timers and 32kHz oscillator are active in this mode.

### 8.2.4 Pairing

Permanent pairing: The device ID of the Clients are permanently stored in the Master (can be overwritten).

Temporary pairing: The device ID of the Clients are not permanently stored. The exchange of communication parameters is done for each temporary session.

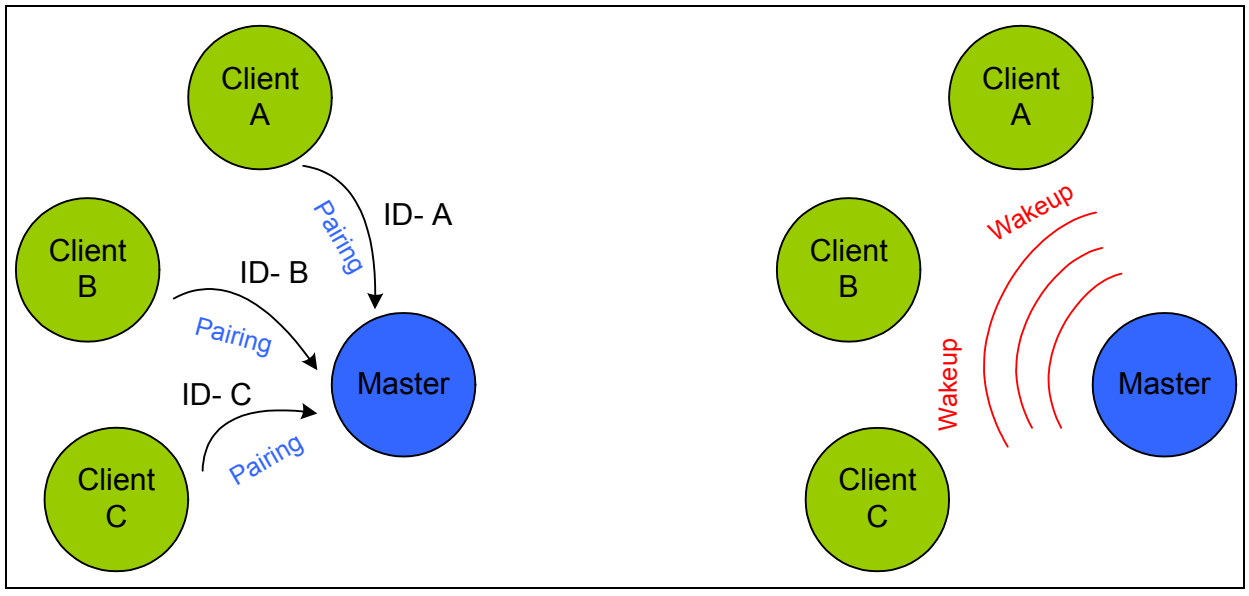
**Note:** It is important to note that the Pairing procedure must be executed in a clean RF environment. All Clients need to be close to the Master.

### 8.2.5 Wakeup

After a Wakeup sequence is received, the exchange of time code is performed and master is synchronized to client time base.

Applying wakeup means, Client (Master) is set to Wakeup receive mode for short time with a long wakeup interval. Master (Client) transmits long enough wakeup sequence to catch the receiving window of the Client (Master) or the Master is set to Wakeup receive mode for long time to catch the transmitted Client Wakeup sequences. Once the Client (Master) is woken up, it turns out of Sleep Mode and the time base is synchronized.

*Figure 11. Pairing and Wakeup Principle*



### 8.2.6 Data Transmit/Receive

The transmission is usually operated timer controlled in data packet mode. Packets can be sent bidirectional from 8 possible Clients to the Master. The Clients send their packets periodically selected by the cycle time. The AS3900 is also able to provide a not timer controlled bidirectional fast package mode, a timer controlled one way package mode and a not timer controlled one way streaming mode. The device features auto-acknowledgement as well as automatic retransmit of lost data.

The following different communication types are possible:

- One-way or bidirectional data transmission
- Timer controlled or not timer controlled transmission

## 8.3 Link Manager

### 8.3.1 Establishing Network

In order to build up a star network the connections between the Master and all available Clients must be established.

#### *8.3.1.1 Permanent Pairing*

The first arrangement of the star-network is associated with the keyword “Pairing”. Basically the ID of the available Clients are transmitted to the Master, because first all Clients are unknown for the Master. This is accomplished by sending a Wakeup signal from the Master to the Clients, so that all Clients exit from standby-mode. All Clients are woken up and answer after a random delay with the first data packet that includes the unique identification number (ID). The Master receives the packets from the different Clients after random time delays (set by MCU). After MCU verification the ID’s are stored in the Master’s ID registers.

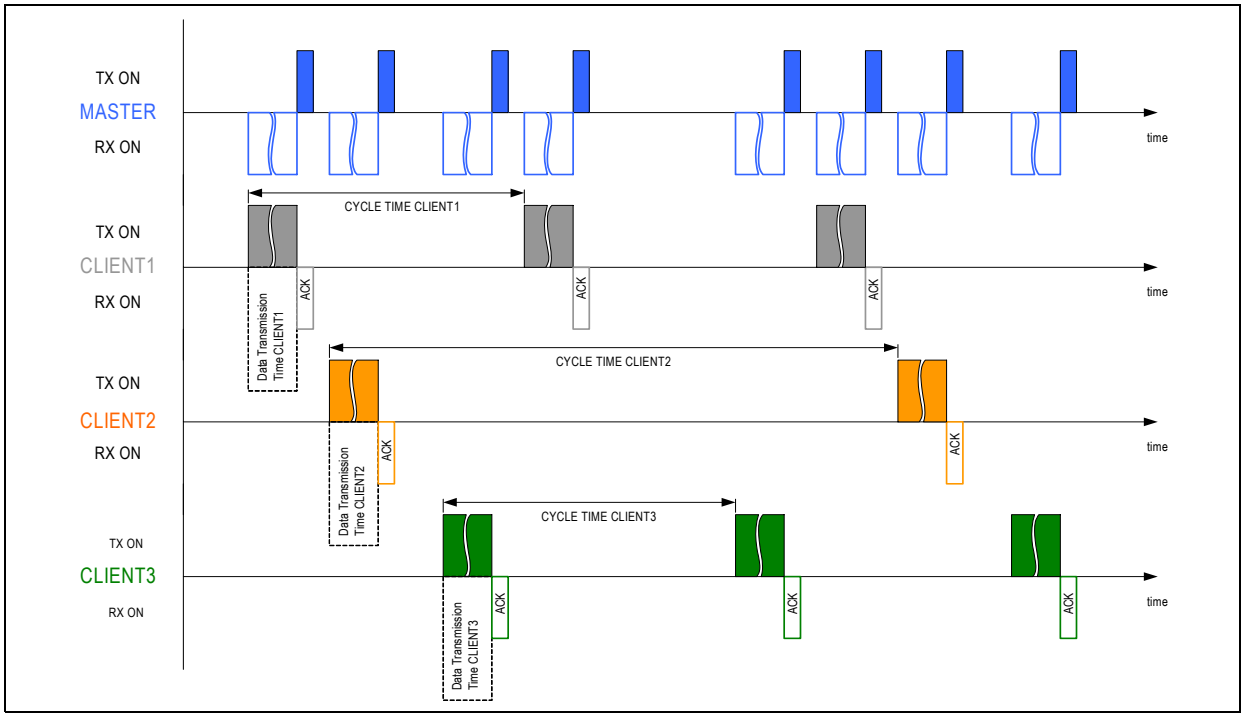
After that the Clients are paired to the Master and switched to Power-down mode. See detailed description in 8.6 Pairing.

#### *8.3.1.2 Wakeup and Data Transmit/Receive*

For transmitting data it is necessary to follow the listed procedure. First all Clients have to be set to Standby mode (periodically listen for Wakeup signal). Then the Master sends a “Wakeup” signal to exit all Clients from Standby mode. With this wakeup signal, all Clients are synchronized and send the timing information to the Master. Once synchronized, the whole communication is controlled by the Link manager in Auto-acknowledge mode. See detailed description in chapter 8.7 Transmission Modes.

The communication between the Master and up to eight Clients is timer controlled. Figure 8 shows the communication between 1 Master and 3 Clients. The cycle time is adjustable via the register map. The data rate and the frequency deviation must be the same for all members of the star network.

*Figure 12. Time Division Multiplexing Principle*



### 8.3.2 Handling the Link Manager

In general there are three different actions to operate the link manager.

- Setting register
- Sending direct commands
- Handling interrupts

#### *8.3.2.1 Setting Registers*

The AS3900 has a MAIN register with 82bytes and a SHADOW register with 22 bytes. All configuration registers are readable and writable and can be directly accessed via their register address. The registers are non volatile as long as the supply voltage is not decreased below the specified minimum level of 2.0V. The two registers contain blocks for configuration, bits for setting direct commands, status bits, an ID table, different data buffers as well as an interrupt table.

The complete register maps are directly addressable via the SDI interface that features:

- Reading of a single register byte
- Reading of register data with auto-incrementing address
- Writing of a single register byte
- Writing of register data with auto-incrementing address

#### *8.3.2.2 Sending Direct Commands*

The AS3900 can be directed via direct Commands that are executed via the SDI interface. With the direct Commands often used features of the device can be activated or deactivated. Some of the commands can also be accessed via the register maps.

#### *8.3.2.3 Handling Interrupt*

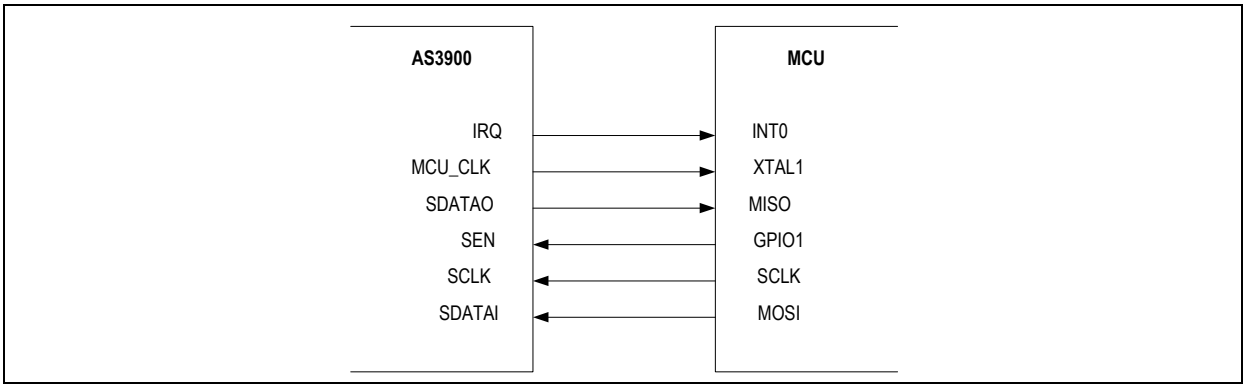
Different interrupts are set by the link manager according to certain events in the interrupt registers (in the MAIN register). 16 possible interrupt sources can be enabled or disabled by the use of the Interrupt Mask Register.

If one of the enabled interrupt conditions is met, the AS3900 apply a HIGH level on the IRQ pin. The IRQ level is set to LOW level after reading the interrupt register. The MCU reads the interrupt register to distinguish between the different interrupt sources. The interrupt registers are reset automatically after reading.

## 8.4 Digital Interface

The interface is used for the serial communication between the Microcontroller and the AS3900.The maximum operation frequency of the Serial Data Interface (SDI) is 2MHz. The Interrupt Interface (IRQ) provides a CMOS compatible HIGH level at the occurrence of an interrupt. This level will be set to LOW if one of the interrupt registers is read. In active modes of the AS3900, a register selectable frequency is provided at the pin MCU_CLK. A typical connection to the MCU is shown in Figure 13

*Figure 13. Microcontroller Interface*



### 8.4.1 SDI Operation Mode Bits

In general there are 3 modes that can be selected by A7 and A6. A5 to A0 contains the register address of the selected register. D7 to D0 contain one byte that can be written or read from the selected address. A Write and Read cycle can be covered with 2 bytes, a Command cycle within 1 byte operation. An Enable LOW pulse indicates the end of all possible modes.

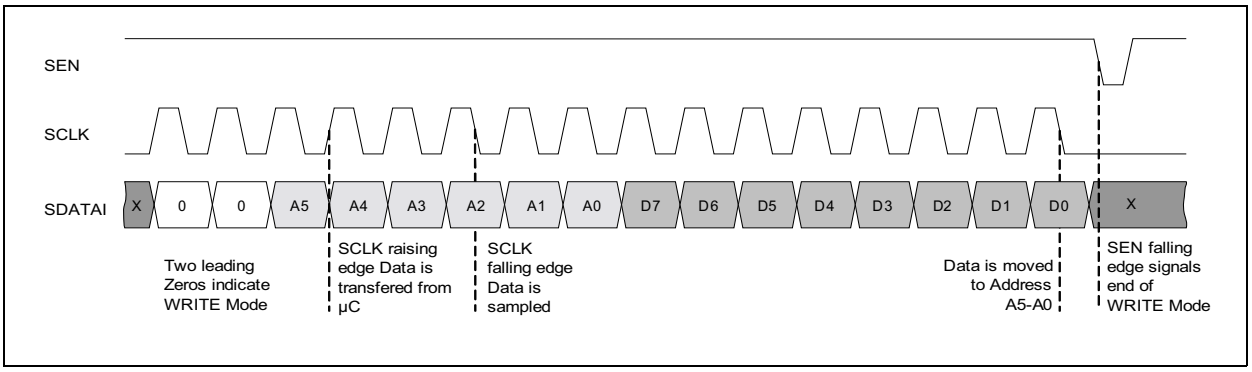
*Table 14. SDI Operation Patterns*

| Mode | Mode Pattern | | | | | | | | Mode related Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Mode | | Register Address | | | | | | Register Data | | | | | | | |
| | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write Mode | 0 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| Read Mode | 0 | 1 | x | x | x | x | x | x | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 |
| Spare Mode | 1 | 0 | | | | | | | | | | | | | | |
| Command Mode | 1 | 1 | C5 | C4 | C3 | C2 | C1 | C0 | | | | | | | | |

### 8.4.2 Writing of Data to Addressable Registers (WRITE Mode)

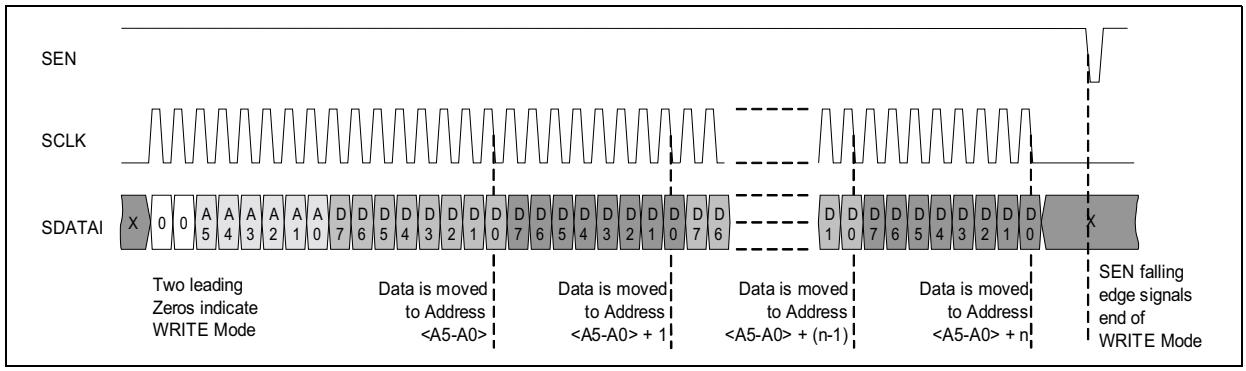
DATAI is sampled at the falling edge of SCLK as shown in the following diagrams. An Enable LOW pulse indicates the end of the WRITE command after register has been written. The following example shows a write command.

*Figure 14. Writing of a Single Byte (falling edge sampling)*




Due to the limited range of the Register Address of 6 bits (A5 to A0), only the register 0x00 to 0x3F are directly addressable. All other registers (0x3F to 0x51 in the MAIN register) can only be accessed via the auto-incrementing Write cycle. The auto-incrementing Write cycle can be applied by remaining SEN to HIGH and providing further clock cycles on SCLK (falling edges).

*Figure 15. Writing of Register Data with Auto-incrementing Address*



### 8.4.3 Reading of Data from Addressable Registers (READ Mode)

DATAI is sampled at the falling edge of SCLK, consequently, data to be read from the microcontroller are driven by the AS3900 (SDI slave) at the transfer edge and sampled by the microcontroller (SDI master) at the sampling edge of SCLK.

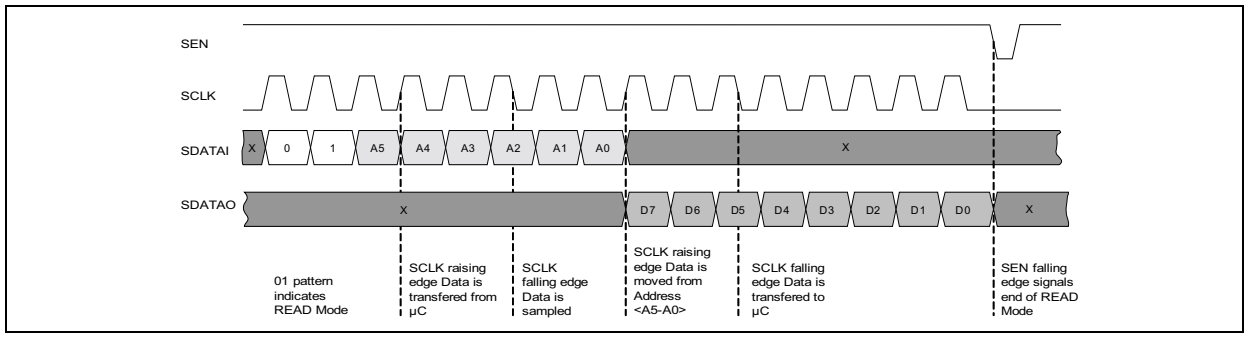
An Enable LOW pulse has to be performed after register data has been transferred in order to indicate the end of the READ command and prepare the Interface to the next command control Byte.

The command control Byte for a read command consists of a command code and an address. After the command code, the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred from the SDI slave to the master, always from the MSB to the LSB. To transfer bytes from consecutive addresses, SDI master has to keep the SDI enable signal high and the SDI clock has to be active as long as data need to be read from the slave.

Each bit of the command and address sections of the frame have to be driven by the SDI master on the SDI clock transfer edge and the SDI slave samples it on the next SDI clock edge. Each bit of the data section of the frame has to be driven by the SDI slave on the SDI clock transfer edge and the SDI master on the next SDI clock edge samples it. If the read access is interrupted (by de-asserting the SDI enable signal), data provided to the master is consistent to given address, but it is only the register content from MSB to LSB. If more SDI clock cycles are provided, the data remains consistent and each data byte belongs to the given or incremented address.

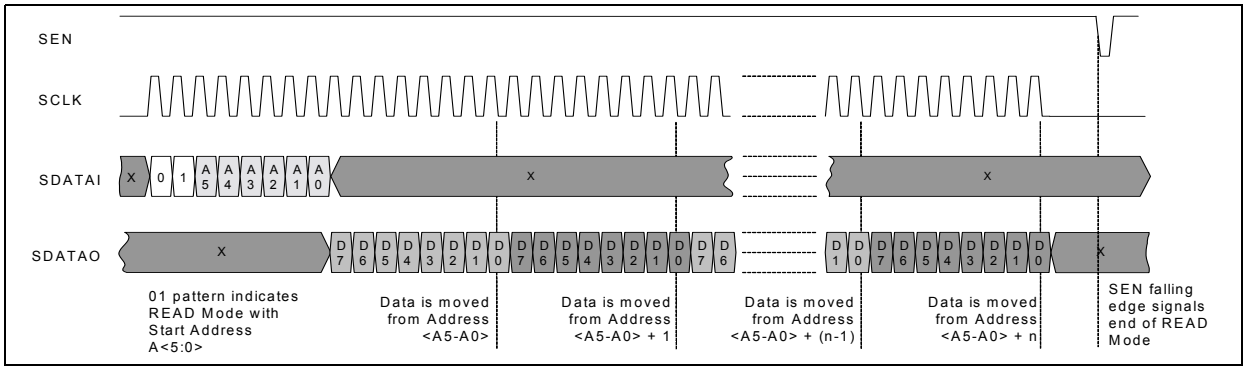
In the following figures two examples for a read command (without and with address self-increment) are given.

*Figure 16. Reading of a Single Register Byte*




Due to the limited range of the Register Address of 6 bits (A5 to A0) for reading a single Byte, only the register 0x00 to 0x3F are directly addressable. All other registers (0x3F to 0x51 in the MAIN register) can only be accessed via the auto-incrementing Read cycle. The auto-incrementing Read cycle can be applied by remaining SEN to HIGH and providing further clock cycles on SCLK (falling edges).

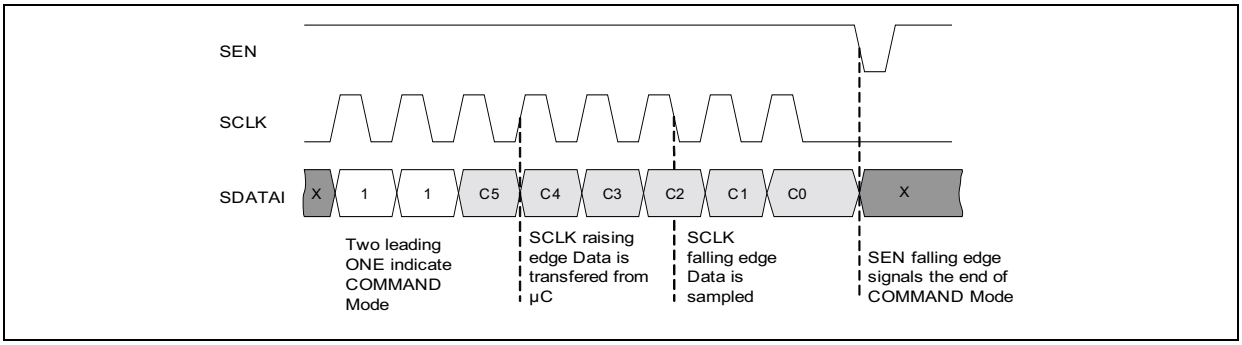
*Figure 17. Reading of Register Data with Auto-incrementing Address*



### 8.4.4 Send Single COMMAND byte

Command mode is entered if the SDI read is started with two leading ONE. After the COMMAND mode code (11), the further mode (e.g. DATA_TRANSMIT) could be provided from the MSB to the LSB or <C5-C0>. If <C5-C0> = 0 no mode change (used for Load Transmitting Data).

*Figure 18. Single COMMAND byte*




A full command to change the Operation Mode of the AS3900 has a length of only 8 bit followed by an SEN LOW pulse. The AS3900 offers the following direct commands.

*Table 15. Direct Commands*

| Command Name | MODE Pattern (com. bits) | | | | | | MODE Description |
|---|---|---|---|---|---|---|---|
| | C5 | C4 | C3 | C2 | C1 | C0 | |
| CHIP_RESET | 0 | 0 | 0 | 0 | 0 | 0 | Software reset, takes 2ms to load PROM |
| IRQ_CLEAR | 0 | 0 | 0 | 0 | 0 | 1 | Clear all interrupt registers |
| WAKE_TX | 0 | 0 | 0 | 1 | 0 | 0 | Starts the wake-up call sequence, composed of OOK |
| TRANSMIT | 0 | 0 | 0 | 1 | 0 | 1 | Initiates Tx sequence (depends on communication mode selected) |
| SCAN | 0 | 0 | 0 | 1 | 1 | 0 | Master enters Rx mode for 1s or longer, if 'longscan' bit is set |
| PROM_COPY | 0 | 0 | 1 | 0 | 0 | 0 | bank=1; copies the data from PPROM dprom registers REG 0x08 … 0x0A to register id0 in REG 0x08 … 0x0A |
| PROM_FUSE | 0 | 0 | 1 | 0 | 0 | 1 | bank=1, fuseen=1; starts the PPROM fuse procedure |
| PROM_LOAD | 0 | 0 | 1 | 0 | 1 | 0 | bank=1; load the fuse bits to PPROM registers |
| PROM_RST | 0 | 0 | 1 | 0 | 1 | 1 | bank=1; resets the PPROM modes |
| MAIN_BANK | 0 | 1 | 0 | 0 | 0 | 0 | Change selected bank to MAIN register |
| SHADOW_BANK | 0 | 1 | 0 | 0 | 0 | 1 | Change selected bank to SHADOW register |
| POWER_OFF | 0 | 1 | 0 | 0 | 1 | 0 | pwr bit off; clears all modes and stops timers; exceptions for bits osc32f, reff, osc27f |
| POWER_ON | 0 | 1 | 0 | 0 | 1 | 1 | pwr bit on |
| WAKE_RX_OFF | 0 | 1 | 0 | 1 | 0 | 0 | Wake_rx bit off |
| WAKE_RX_ON | 0 | 1 | 0 | 1 | 0 | 1 | Wake_rx bit on |
| STREAM_OFF | 0 | 1 | 0 | 1 | 1 | 0 | Stream bit off |
| STREAM_ON | 0 | 1 | 0 | 1 | 1 | 1 | Stream bit on |
| CLEAR_TIMER_0 | 1 | 0 | 0 | 0 | 0 | 0 | Deactivate timing system 0 |
| CLEAR_TIMER_1 | 1 | 0 | 0 | 0 | 0 | 1 | Deactivate timing system 1 |
| CLEAR_TIMER_2 | 1 | 0 | 0 | 0 | 1 | 0 | Deactivate timing system 2 |
| CLEAR_TIMER_3 | 1 | 0 | 0 | 0 | 1 | 1 | Deactivate timing system 3 |
| CLEAR_TIMER_4 | 1 | 0 | 0 | 1 | 0 | 0 | Deactivate timing system 4 |

*Table 15. Direct Commands*

| Command Name | MODE Pattern (com. bits) | | | | | | MODE Description |
|---|---|---|---|---|---|---|---|
| | C5 | C4 | C3 | C2 | C1 | C0 | |
| CLEAR_TIMER_5 | 1 | 0 | 0 | 1 | 0 | 1 | Deactivate timing system 5 |
| CLEAR_TIMER_6 | 1 | 0 | 0 | 1 | 1 | 0 | Deactivate timing system 6 |
| CLEAR_TIMER_7 | 1 | 0 | 0 | 1 | 1 | 1 | Deactivate timing system 7 |
| CLEAR_TIMER_ALL | 1 | 0 | 1 | 0 | 0 | 0 | Deactivate all timing systems |

### 8.4.5 Read Received Data

After successfully receive of the data the interrupt line is set.

- The microcontroller reads the interrupt register (with this read the IRQ line is reset).
- The microcontroller reads the ADDRESS (ID) to which sensor the data belongs.
- The microcontroller reads the DATALEN register.
- With this read the received DATA is transferred to the SDI output register and clocked out by means of the SDI Clock (SCLK).

### 8.4.6 Interrupt Interface Description

If an interrupt condition is met a HIGH level is applied to the IRQ pin. The IRQ level is set to LOW level after reading the Interrupt registers.

The microcontroller than reads the interrupt register to distinguish between different interrupt sources. The interrupt sources could be enabled or disabled by the use of the Interrupt Mask Registers. The Interrupt Mask Register defines which interrupt leads to a LOW to HIGH transition of the IRQ line.

*Figure 19. Interrupt Operation*

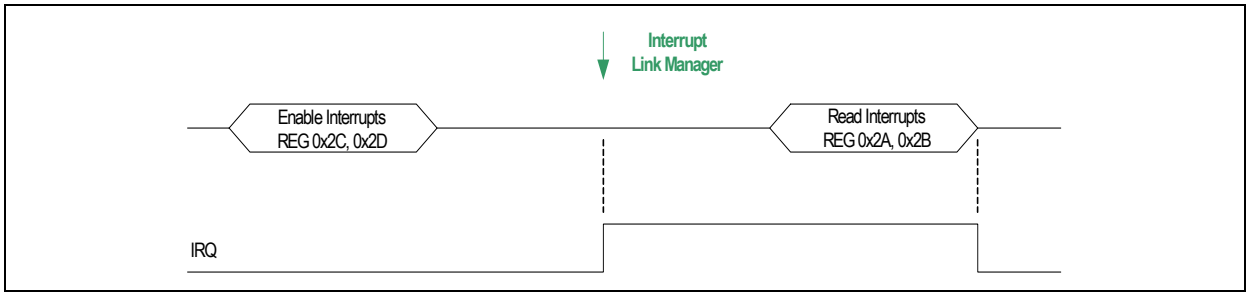



*Table 16. Interrupt Electrical Interface Description*

| Name | Signal | Signal Level | Description |
|---|---|---|---|
| IRQ | Digital Output | CMOS | Interrupt Output pin (max Load = 10pF) |

*Table 17. Table of Interrupts*

| MAIN Reg. Addr# | Interrupt name | Int bits bit | Interrupt Description |
|---|---|---|---|
| 0x2A | scan_end | [7] | One second scanning has been finished (if not enlarged with longscan bit) |
| | dat_rtx | [6] | Indicates that data was received and is ready to be read |
| | wake_call | [5] | For client to send transmit command |
| | stream_end | [4] | In client mode it indicates new data should be written into send register.<br>In master mode it indicates end of transmission |
| | wrong_id | [3] | Activated if ID is not in the ID list |
| | wrong_crc | [2] | Activated if CRC error occurs |
| | timer_irq | [1] | Always activated if one of the irq<7:0>, REG 0x28<7:0> is activated |
| | Reserved | [0] | Reserved |
| 0x2B | txend | [7] | Activated after last bit of CRC is transmitted |
| | txstart | [6] | Activated after last bit of PREAMBLE was transmitted |
| | rxend | [5] | Activated after the whole data was received |
| | rxstart | [4] | Activated after PREAMBLE was received |
| | nar_rtx | [3] | Activated after NAR was received or transmitted |
| | nak_rtx | [2] | Activated after NAK was received or transmitted |
| | acp_rtx | [1] | Activated after ACP was received or transmitted |
| | ack_rtx | [0] | Activated after ACK was received or transmitted |

*Table 18. Table of Interrupt Mask Registers*

| MAIN Reg. Addr# | Interrupt Mask name | Mask bits bit | Interrupt Mask Description |
|---|---|---|---|
| 0x2C | msk_scan_end | [7] | Mask interrupt: scan_end |
| | msk_dat_rtx | [6] | Mask interrupt: dat_rtx |
| | msk_wake_call | [5] | Mask interrupt: wake_call |
| | msk_stream_end | [4] | Mask interrupt: stream_end |
| | msk_wrong_id | [3] | Mask interrupt: wrong_id |
| | msk_wrong_crc | [2] | Mask interrupt: wrong_crc |
| | msk_timer_irq | [1] | Mask interrupt: timer_irq |
| | Reserved | [0] | Reserved |
| 0x2D | msk_txend | [7] | Mask interrupt: txend |
| | msk_txstart | [6] | Mask interrupt: txstart |
| | msk_rxend | [5] | Mask interrupt: rxend |
| | msk_rxstart | [4] | Mask interrupt: rxstart |
| | msk_nar_rtx | [3] | Mask interrupt: nar_rtx |
| | msk_nak_rtx | [2] | Mask interrupt: nak_rtx |
| | msk_acp_rtx | [1] | Mask interrupt: acp_rtx |
| | msk_ack_rtx | [0] | Mask interrupt: ack_rtx |

**Note:** It is important to note that the enabling/disabling of the timers via REG 0x01<7:0> require a double readout of the interrupts REG 0x2A, 0x2B to release the IRQ line again.

### 8.4.7 Microcontroller Clock Interface

The output frequency is derived from the 27MHz crystal oscillator. The division ratio is defined by register settings. To enable or disable the clock output set the Clock Mode register bit. Additional different operation modes for the output could be set by Clock Mode register bits. For more information on the operation modes of the clock output see Table 20. Clock Interface Modes.

*Table 19. Clock Interface Electrical Description*

| Name | Signal | Signal Level | Description |
|---|---|---|---|
| MCU_CLK | Buffered Digital Output | CMOS | Buffered slope controlled clock output Maximum Load = 50pF |

*Table 20. Clock Interface Modes*

| # | Mode | Mode (bit) | | Clock Mode Description |
|---|---|---|---|---|
| | | CM7 | CM6 | |
| 1 | MCUclk_Off | 0 | 0 | No clock is provided to pin MCU_CLK. Output Level is set to LOW. |
| 2 | MCUclk_32K | 0 | 1 | 32kHz is always provided to pin MCU_CLK except in POWER DOWN Mode |
| 3 | MCUclk_27M | 1 | 0 | A division ratio of 27MHz is provided to pin MCU_CLK in all active modes except in SLEEP and POWER DOWN Mode. For division ratio (see Clock Division Ratios) |
| 4 | MCUclk_32K/27M | 1 | 1 | In active modes (RX or TX active) a division ratio of 27MHz is provided to pin MCU_CLK. In SLEEP Mode 32kHz is set. POWER DOWN Mode switches off the MCU_CLK output. |

*Table 21. Clock Division Ratios*

| Division ratio | Pattern (com. bits) | | | | Mode Description |
|---|---|---|---|---|---|
| | mcdr[3] | mcdr[2] | mcdr[1] | mcdr[0] | Derived from 27.12MHz |
| 8 | 0 | 0 | 0 | 0 | 3.39MHz |
| 12 | 0 | 0 | 0 | 1 | 2.26MHz |
| 12 | 0 | 0 | 1 | 0 | 2.26MHz |
| 18 | 0 | 0 | 1 | 1 | 1.50MHz |
| 16 | 0 | 1 | 0 | 0 | 1.69MHz |
| 24 | 0 | 1 | 0 | 1 | 1.13MHz |
| 24 | 0 | 1 | 1 | 0 | 1.13MHz |
| 36 | 0 | 1 | 1 | 1 | 753kHz |
| 32 | 1 | 0 | 0 | 0 | 847kHz |
| 48 | 1 | 0 | 0 | 1 | 565kHz |
| 48 | 1 | 0 | 1 | 0 | 565kHz |
| 72 | 1 | 0 | 1 | 1 | 376kHz |
| 64 | 1 | 1 | 0 | 0 | 423kHz |
| 96 | 1 | 1 | 0 | 1 | 281kHz |
| 96 | 1 | 1 | 1 | 0 | 281kHz |
| 144 | 1 | 1 | 1 | 1 | 188kHz |

## 8.5 Wakeup Procedure

In general the Wakeup is introduced in order to handle two different challenges:

- Wakeup Clients that are in Standby Mode. Clients in standby consume a small amount of power from the battery
- Exchange actual time code (Cycle time, random pointer) and synchronize all Clients with the Master

The Client (Master) is set to Wakeup receive mode for short time with a long wakeup interval. Master (Client) transmits long enough wakeup sequence to catch the receiving window of the Client (Master) or the Client is set to Wakeup receive mode for long time to catch the transmitted Master Wakeup sequences. If the Client (Master) receives a Wakeup sequence the link manager triggers the wake_call interrupt.

The Link Manager needs to be instructed via the direct **COMMANDS** and via **REGISTER** settings. The MCU is informed of the current status via **INTERRUPTS**, which need to be read out as soon as an external interrupt on the IRQ line appears.

### 8.5.1 Wakeup Receive Mode

The Wakeup Receive Window can be set to:

- Sampling: The Wakeup Receive Window is turned on for a fixed time of 250µs and turned off again for the remaining cycle time. The cycle time for the receive window can be set by the wakecyc bits in REG 0x04<2:4>. The ON interval itself is fixed to 250µs. The current consumption is defined by the ON to OFF ratio of the Wakeup receiver.

### 8.5.2 Wakeup Transmit Mode

Transmitting a Wakeup Signal means that the PA applies an OOK Signal (On Off Keying), in order to wakeup the Master (Client). The OOK pattern is a 27MHz signal that is ON OFF modulated with 96kHz. The following parameters for this OOK signal can be configured:

- Wakeup Transmitter On time: The Wakeup call can be applied between 125ms up to 1s in REG 0x04<1:0>.
- Longwake TX: The Wakeup call can be applied as long as the longwake_tx bit is set in REG 0x04<5>.

The Wakeup transmit mode shows a Wakeup procedure initialized by the Master. The Client samples for the Wakeup signal periodically. The figure shows the Wakeup procedure.

*Figure 20. Wakeup Transmit Mode*

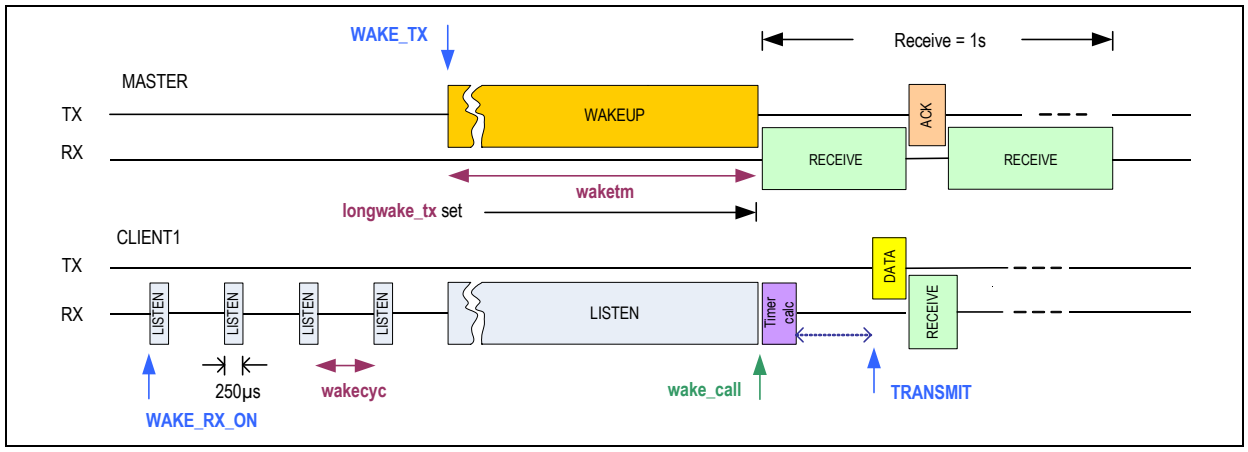



*Table 22. Wakeup Procedure Initialized by the Master*

| Step | Master | Client |
|---|---|---|
| 1 | | Client wakeup receiver listens during periodic time windows. This action is started by MCU with the command WAKE_RX_ON. The duration of wakeup listening is hardwired to 250µs and the wakeup listening cycle-time is defined by the wakecyc bits, REG 0x04<4:2>. |
| 2 | The Master starts the wakeup call with the command WAKE_TX The duration of the call is defined by the waketm bits, REG 0x04<1:0> (for MCU defined wakeup call duration the long wake_tx bit, REG 0x04<5> has to be used). | |