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AS3911

NFC Initiator / HF Reader IC

General Description

The AS3911 is a highly integrated NFC Initiator / HF Reader IC. It includes the analog front end (AFE) and a highly integrated data framing system for ISO 18092 (NFCIP-1) initiator, ISO 18092 (NFCIP-1) active target, ISO 14443 A and B reader (including high bit rates) and FeliCa™ reader. Implementation of other standard and custom protocols is possible through using the AFE and implementing framing in the external microcontroller (Stream and Transparent modes).

Compared with concurrent NFC devices designed with the mobile phone in mind, the AS3911 is positioned perfectly for the infrastructure side of the NFC system, where users need optimal RF performance and flexibility combined with low power.

With **ams** unique Automatic Antenna Tuning technology, the device is optimized for applications with directly driven antennas. The AS3911 is alone in the domain of HF Reader ICs in that it contains two differential low impedance (1Ω) antenna drivers.

The AS3911 includes several features, which make it incomparable for low power applications. It contains a low power capacitive sensor, which can be used to detect the presence of a card without switching on the reader field. Additionally, the presence of a card can also be detected by performing a measurement of amplitude or phase of signal on antenna LC tank and comparing it to stored reference. It also contains a low power RC oscillator and wake-up timer, which can be used to wake the system after a defined time period and check for the presence of a tag using one or more techniques of low power detection of card presence (capacitive, phase or amplitude).

The AS3911 is designed to operate from a wide power supply range from 2.4V to 5.5V; peripheral interface IO pins support power supply range from 1.65V to 5.5V.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3911, NFC Initiator / HF Reader IC are listed below:

Figure 1:
Added Value of Using AS3911

Benefits	Features
NFC Active P2P support	ISO 18092 (NFCIP-1) Active P2P
	ISO14443 A, B and FeliCa (TM)
High data transfer with ASK VHBR and fast SPI	Support of VHBR (3.4 Mbit/s PICC to PCD framing, 6.8 Mbit/s AFE and PCD to PICC framing)
6µA consumption at sensing every 100ms	Capacitive sensing - Wake-up
Antenna tuning on the fly	Automatic Antenna Tuning system providing tuning of antenna LC tank
Stable modulation index at ASK modulation	Automatic modulation index adjustment
No communication holes	AM and PM (I/Q) demodulator channels with automatic selection
High output power for EMVCo readers	Up to 1 W in case of differential output
High Rx sensitivity	User selectable and automatic gain control
Allows implementation of custom framings	Transparent and Stream modes to implement MIFARE™ Classic compliant or other custom protocols
Multi Antenna support	Possibility of driving two antennas in single ended mode
Smaller Oscillator size	Oscillator input capable of operating with 13.56 MHz or 27.12 MHz crystal with fast start-up
Easy FIFO handling	10 M bit SPI with 96 bytes FIFO
	Wide supply voltage range from 2.4 V to 5.5 V
Fits Temperature requirements for various applications	Wide temperature range: -40°C to 125°C
Small outline, good cooling through exposed pad	QFN 5mm x 5mm LD32 package

Applications

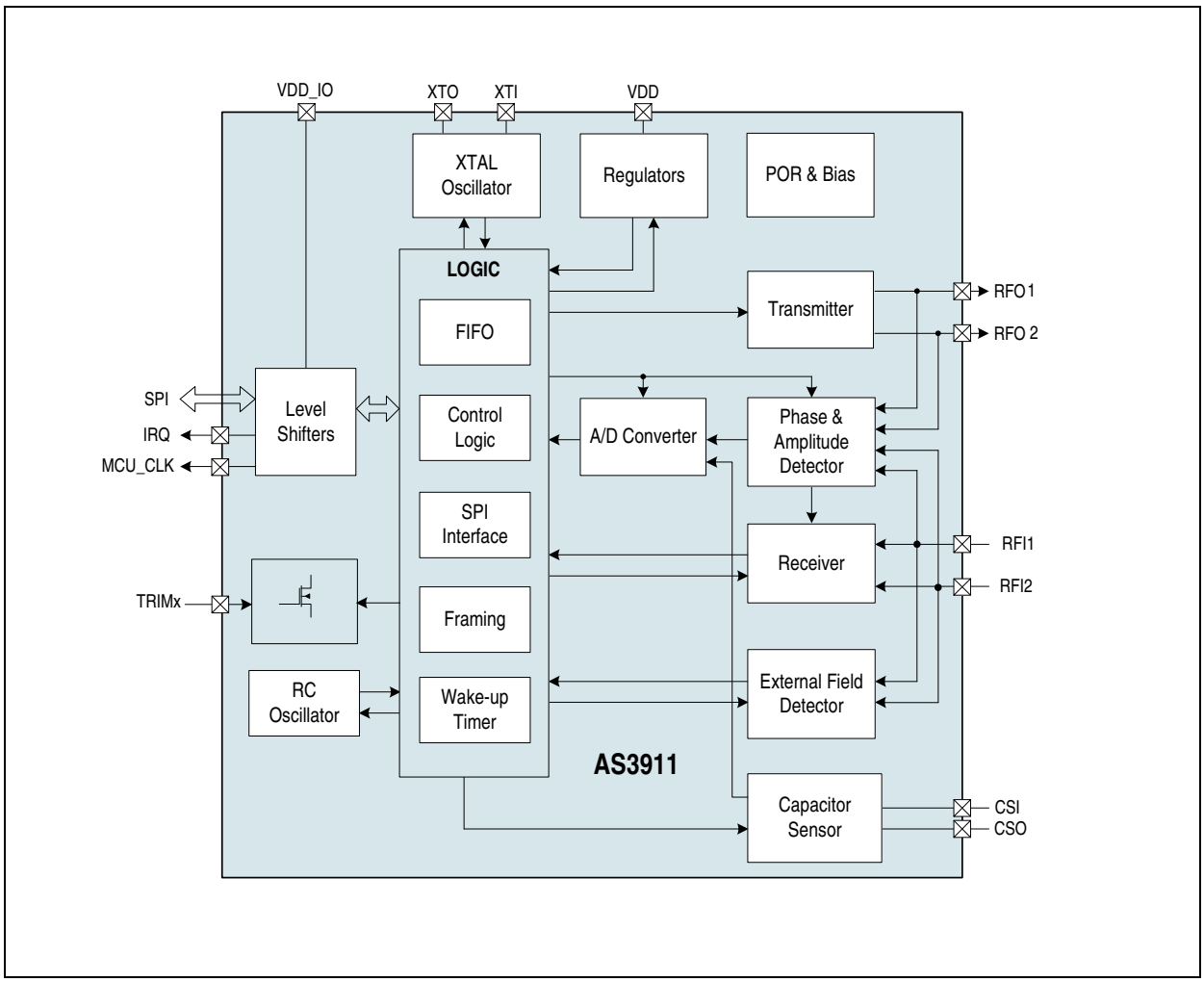
The AS3911 is suitable for a wide range of applications including:

- EMV Payment
- Access Control
- NFC Infrastructure
- Ticketing

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
AS3911 Block Diagram



Pin Assignment

The AS3911 pin assignments are described below.

Figure 3:
Pin Diagram

AS3911 Pin Assignment: This figure shows the pin assignment and location viewed from top.

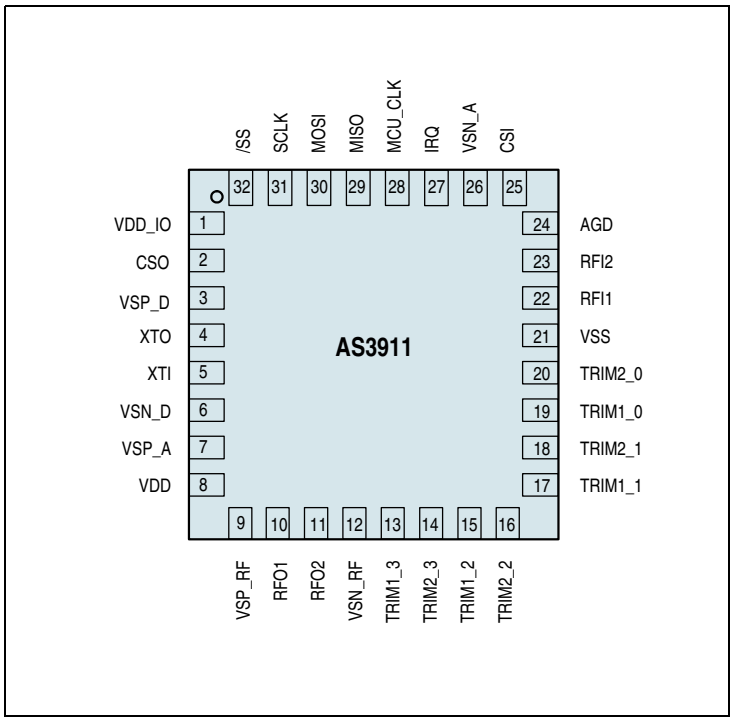


Figure 4:
Pin Description

Pin Number 32-pin QFN	Pin Name	Pin Type	Description
1	**V_{DD_IO}**	Supply pad	Positive supply for peripheral communication
2	**CSO**	Analog output	Capacitor sensor output
3	**VSP_D**		Digital supply regulator output
4	XTO		Xtal oscillator output
5	XTI	Analog input / Digital input	Xtal oscillator input
6	VSN_D	Supply pad	Digital ground
7	VSP_A	Analog output	Analog supply regulator output
8	V_{DD}	Supply pad	External positive supply

Pin Number 32-pin QFN	Pin Name	Pin Type	Description
9	VSP_RF	Analog output	Supply regulator output for antenna drivers
10	RFO1		Antenna driver output
11	RFO2		
12	VSN_RF	Supply pad	Ground of antenna drivers
13	TRIM1_3	Analog I/O	Input to trim antenna resonant circuit
14	TRIM2_3		
15	TRIM1_2		
16	TRIM2_2		
17	TRIM1_1		
18	TRIM2_1		
19	TRIM1_0		
20	TRIM2_0		
21	VSS	Supply pad	Ground, die substrate potential
22	RFI1	Analog input	Receiver input
23	RFI2		
24	AGD	Analog I/O	Analog reference voltage
25	**CSI**	Analog input	Capacitor sensor input
26	VSN_A	Supply pad	Analog ground
27	IRQ	Digital output	Interrupt request output
28	MCU_CLK		Microcontroller clock output
29	MISO	Digital output / tristate	Serial Peripheral Interface data output
30	MOSI	Digital input	Serial Peripheral Interface data input
31	SCLK		Serial Peripheral Interface clock
32	/SS		Serial Peripheral Interface enable (active low)
#	VSS	Exposed Pad	Ground, die substract potential, connect to VSS on PCB

Note(s):

1. Pins in **bold** have different functionality in comparison to the AS3910.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{DD}	DC supply voltage	-0.5	6.0	V	
V_{DD_IO}	DC_IO supply voltage	-0.5	6.0	V	
V_{INTRIM}	Input pin voltage TRIM pins	-0.5	25.0	V	
V_{IN}	Input pin voltage for peripheral communication pins	-0.5	6.5	V	
V_{INA}	Input pin voltage for analog pins	-0.5	6.0	V	
I_{scr}	Input current (latch-up immunity)	-100	100	mA	JEDEC 78
I_{outmax}	Drive capability of output driver	0	600	mA	
Electrostatic Discharge					
ESD	Electrostatic discharge	±2		kV	MIL 883 E method 3015 (Human Body Model)
		±500		V	Valid for Trimx.x pins (pins 13 - 20)

Symbol	Parameter	Min	Max	Unit	Comments
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-55	125	°C	
T_{body}	Package body temperature		260	°C	IPC/JEDEC J-STD-020. *The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices."* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	3			Represents a max. floor life time of 168 hours
Thermal Resistance					
θ_{ja}	Theta ja	36.4		C/W	@ 85°C room temperature, power consumption 1W

Note(s):

1. Please refer to Figure 10 and Figure 11 for typical operating characteristics of thermal resistance and max. power dissipation.

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Operating Conditions

All defined tolerances for external components in this specification need to be assured over the whole operation condition range and also over lifetime.

Figure 6:
Operating Conditions

Symbol	Parameter	Min	Max	Unit	Comments
V_{DD}	Positive supply voltage	2.4	5.5	V	In case power supply is lower than 2.6V, PSSR cannot be improved using internal regulators (minimum regulated voltage is 2.4V)
V_{DD_IO}	Peripheral communication supply voltage	1.65	5.5	V	
VSS	Negative supply voltage	0	0	V	
V_{INTRIM}	Input pin voltage TRIM pins		20	V	
T_{JUN}	Junction temperature	-40	125	°C	
V_{RFI_A}	RFI input amplitude	150 m	3	V_{pp}	Minimum RFI input signal definition is meant for NFC receive mode. In HF reader mode and NFC transmit mode, the recommended signal level is $2.5V_{pp}$
RFO	Driver current	0	500	mA	

DC/AC Characteristics for Digital Inputs and Outputs

CMOS Inputs:

Valid for input pins /SS, MOSI, and SCLK

Figure 7:
CMOS Inputs

Symbol	Parameter	Min	Max	Unit
V_{IH}	High level input voltage	$0.7 * V_{DD\_IO}$		V
V_{IL}	Low level input voltage		$0.3 * V_{DD\_IO}$	V
I_{LEAK}	Input leakage current		1	µA

CMOS Outputs:

Valid for output pins MISO, IRQ and MCU_CLK, *io_18*=0 (See IO Configuration Register 2).

Figure 8:
CMOS Outputs

Symbol	Parameter	Conditions	Min	Type	Max	Unit
V_{OH}	High level input voltage	I_{SOURCE} = 1mA I_{SINK} = 1mA	0.9 * V_{DD_IO}			V
V_{OL}	Low level input voltage				0.1 * V_{DD_IO}	V
C_L	Capacitive load				50	pF
R_O	Output Resistance			250	500	Ω
R_{PD}	Pull-down resistance pin MISO	Pull-down can be enabled while MISO output is in tristate. The activation is controlled by register setting.		10		kΩ

Electrical Specification

V_{DD}= 3.3V, Temperature 25°C unless noted otherwise.

3.3V supply mode, regulated voltages set to 3.4V, 27.12 MHz Xtal connected to XTO and XTI.

Figure 9:
Electrical Specification

Symbol	Parameter	Min	Typ	Max	Unit	Comments
I_{PD}	Supply current in Power-down mode		0.7	2	µA	Register 00_h set to $0F_h$ (no clock on MCU_CLK), register 01_h set to 80_h (3V supply mode), register 02_hset to 00_h register 03_h set to 08_h, other registers in default state.
I_{NFCT}	Supply current in initial NFC Target mode		3.5	7	µA	Register 00_h set to $0F_h$ (no clock on MCU_CLK), register 01_h set to 80_h (3V supply mode), register 02_hset to 00_h register 03_h set to 80_h (enable NFC Target mode), other registers in default state.

Symbol	Parameter	Min	Typ	Max	Unit	Comments
I_{WU}	Supply current in Wake-up mode		3.6	6	µA	Register 00_h set to $0F_h$ (no clock on MCU_CLK), register 01_h set to 80_h (3V supply mode), register 02_h set to 04_h (enable Wake-up mode), register 03_hset to 08_h, register 31_h set to 08_h (100ms timeout, IRQ at every timeout), other registers in default state.
I_{CS}	Capacitive sensor supply current		1.1	2	mA	Register 00_h set to $0F_h$ (no clock on MCU_CLK), register 01_h set to 80_h (3V supply mode), register 02_h set to 00_h, analog test mode 14, other registers in default state.
I_{RD}	Supply current in Ready mode		5.4	7.5	mA	Register 00_h set to $0F_h$ (no clock on MCU_CLK), register 01_h set to $C0_h$ (3V supply mode, disable VSP_D), register 02_h set to 80_h, register 03_h set to 08_h, other registers in default state, short VSP_A and VSP_D.
I_{AL}	Supply current all active		8.7	12.5	mA	Register 00_h set to $0F_h$, register 01_h set to $C0_h$ (3V supply mode, disable VSP_D), register 02_h set to $E8_h$ (one channel Rx, enable Tx), register 03_h set to 08, register $0B_h$set to 00, register 27_h set to FF (all RFO segments disabled), other registers in default state, short VSP_A and VSP_D.
I_{LP}	Supply current all active, low power receiver mode		6.8	10	mA	Register 00_h set to $0F_h$, register 01_h set to $C0_h$ (3V supply mode, disable VSP_D), register 02_h set to $E8_h$ (one channel Rx, enable Tx), register 03_h set to 08, register $0B_h$ set to 80 (low power mode), register 27_h set to FF (all RFO segments disabled), other registers in default state, short VSP_A and VSP_D.

Symbol	Parameter	Min	Typ	Max	Unit	Comments
R_{RFO}	RFO1 and RFO2 driver output resistance		0.6	1.8	Ω	I_{RFO} = 10 mA The following measurement procedure which cancels resistance of measurement setup is used: • All driver segments are switched on, resistance is measured, • All driver segments except the MSB segment are switched on, resistance is measured, • Difference between the two measurements is resistance of MSB segment, • Resistance of MSB segment divided by two is the value of R_{RFO}.
Z_{load}	Load impedance across RFI1 & RFI2	8	10	50	Ω	Using Load impedance lower than minimum value can result in permanent damage of the IC
V_{RFI}	RFI input sensitivity		0.5		mV_{rms}	f_{SUB}=848 kHz, AM channel with peak detector input stage selected.
R_{RFI}	RFI input resistance		10	15	kΩ	
V_{POR}	Power on Reset voltage	1.2	1.65	2.0	V	
V_{AGD}	AGD voltage	1.4	1.5	1.6	V	Register 00_h set to $0F_h$ (no clock on MCU_CLK), register 01_h set to $C0_h$ (3V supply mode, disable VSP_D), register 02_h set to 80_h, register 03_h set to 08_h, other registers in default state, short VSP_A and VSP_D.
V_{REG}	Regulated voltage	2.85	3.0	3.15	V	Manual regulator mode, regulated voltage set to 3.0V, measured on pin VSP_RF: register 00_h set to $0F_h$, register 01_h set to 80_h (3V supply mode), register 02_h set to $E8_h$ (one channel Rx, enable Tx), register $2A_h$ set to $D8_h$.
T_{OSC}	Oscillator start-up time	0.65	0.7	10	ms	13.56MHz or 27.12MHz crystal R_S = 50 Ω max, load capacitance according to crystal specification, IRQ is issued once the oscillator frequency is stable.

Typical Operating Characteristics

Thermal Resistance and Max. Power Dissipation

Figure 10:
TCASE vs. Power with Different Copper Area @ T_{AMB} = 25°C

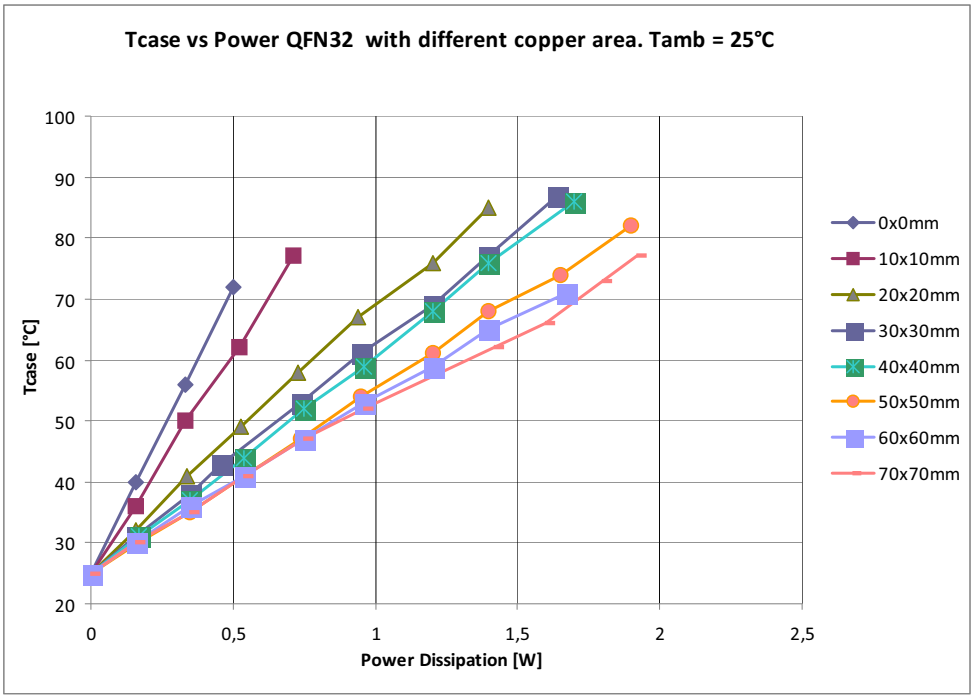
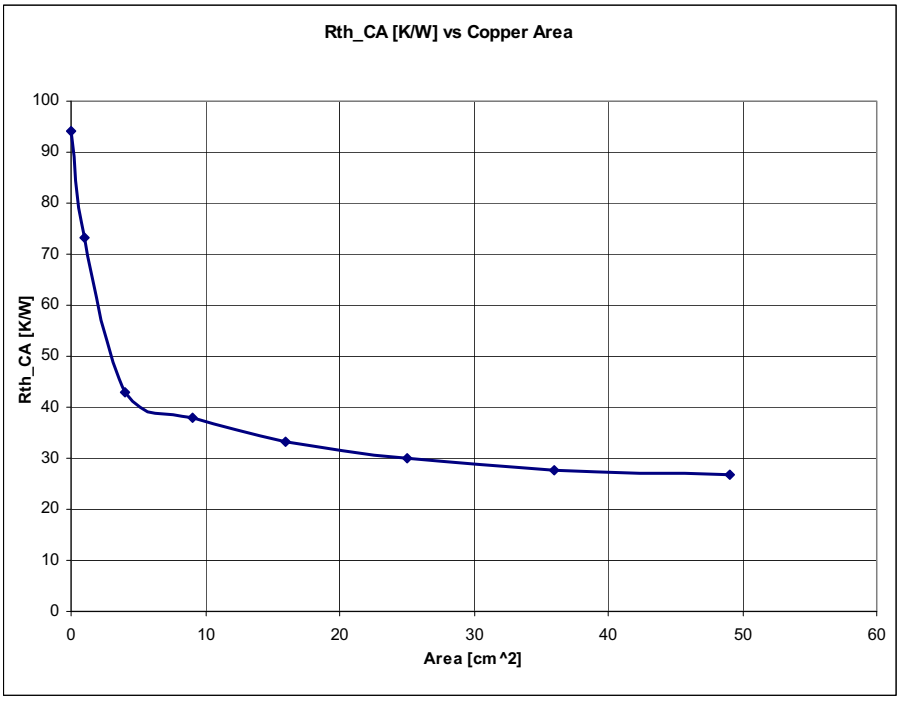


Figure 11:
RthCA vs. Copper Area



Detailed Description

The circuit diagram in Figure 2 shows the AS3911 building blocks.

Figure 12:
Minimum Configuration with Single Sided Antenna Driving Including EMC Filter

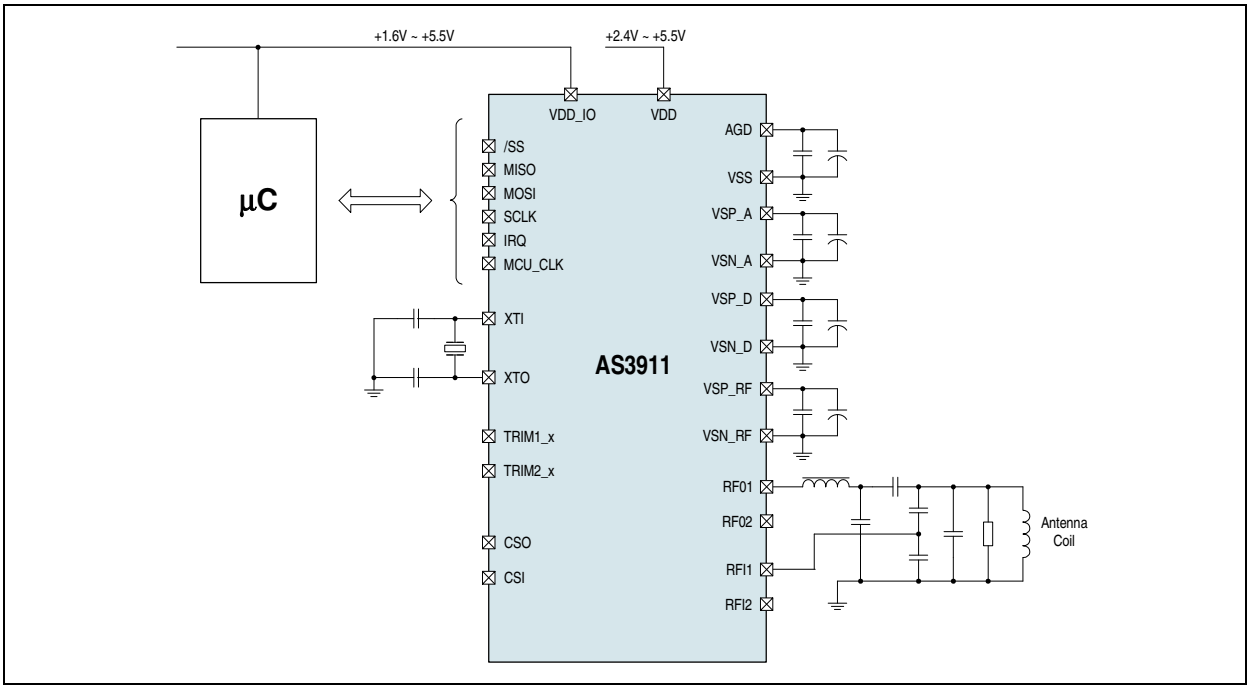
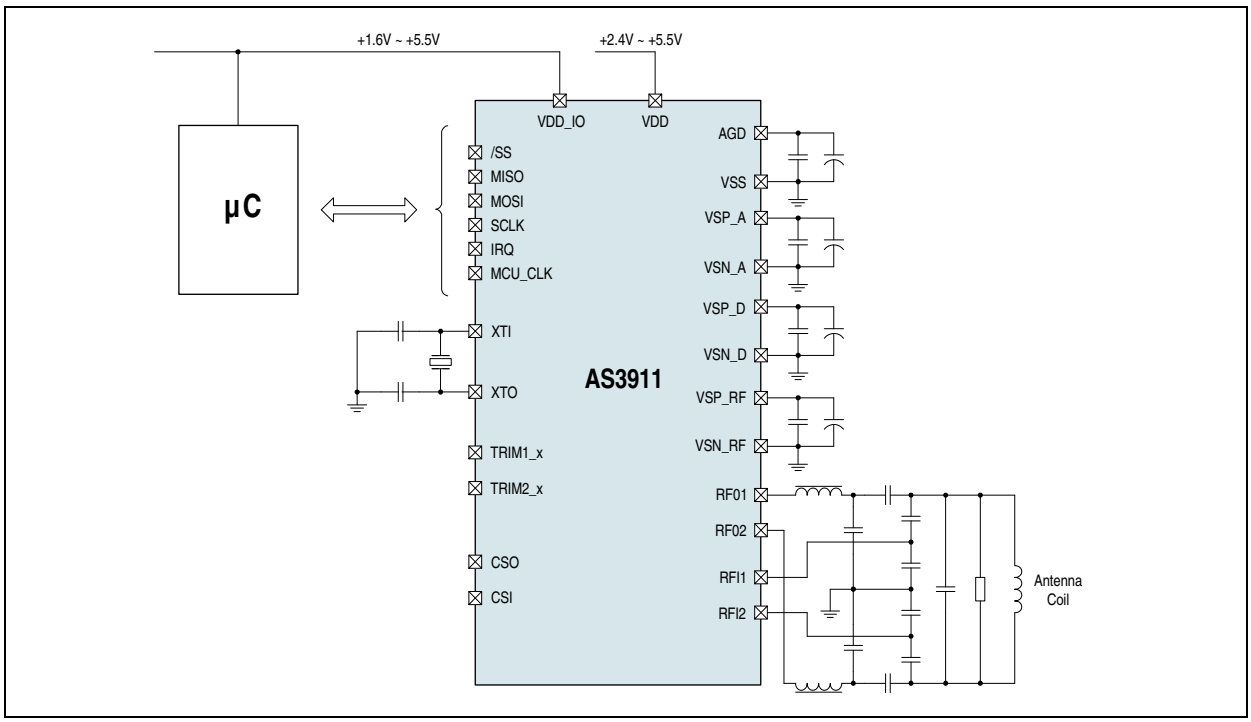


Figure 13:
Minimum Configuration with Differential Antenna Driving Including EMC Filter



Transmitter

The transmitter incorporates drivers which drive external antenna through pins RFO1 and RFO2. Single sided and differential driving is possible. The transmitter block additionally contains a sub-block which modulates transmitted signal (OOK or configurable AM modulation).

The AS3911 transmitter is indented to directly drive antennas (without 50Ω cable, usually antenna is on the same PCB). Operation with 50Ω cable is also possible, but in that case some of the advanced features are not possible.

By applying FFh to the register 27h, the output driver are in tristate.

Receiver

The receiver detects transponder modulation superimposed on the 13.56MHz carrier signal. The receiver contains two receive chains (one for AM and another for PM demodulation) which are composed of a peak detector followed by two gain and filtering stages and a final digitizer stage. The filter characteristics are adjusted to optimize performance over different ISO modes and bit rates (sub-carrier frequencies from 212 kHz to 6.8 MHz are supported). The receiver chain inputs are RFI1 and RFI2 pins; output of digitizer stage is demodulated sub-carrier signal. The receiver chain incorporates several features which enable reliable operation in challenging phase and noise conditions.

Phase and Amplitude Detector

The phase detector is observing the phase difference between the transmitter output signals (RFO1 and RFO2) and the input signals RFI1 and RFI2. Signals RFI1 and RFI2 are proportional to the signal on the antenna LC tank. RFI1 and RFI2 signals are also used to run the self-mixer which generates output proportional to their amplitude. The phase detector and self-mixer blocks are used for several purposes:

- PM demodulation by observing RFI1 and RFI2 phase variation (LF signal is fed to the Receiver)
- Average phase difference between RFOx pins and RFIx pins is used to check antenna tuning
- Output of mixer is used to measure amplitude of signal present on pins RFI1 and RFI2

A/D Converter

The AS3911 contains a built in A/D Converter. Its input can be multiplexed from different sources and is used in several applications (measurement of RF amplitude and phase, calibration of modulation depth…). The result of A/D conversion is stored in a register which can be read through the SPI interface.

Capacitive Sensor

The Capacitive sensor is used to implement low power detection of transponder presence. Capacitive sensor performs measurement of capacitance between its two electrodes. Presence of an object (card, hand) changes the capacitance. During calibration the reference capacitance, which represents parasitic capacitance of environment is stored. In normal operation capacitance is periodically measured and compared to stored reference value. When the measured capacitance is larger than stored reference value (threshold value can be defined in a register) an interrupt is sent to external controller.

External Field Detector

The External Field Detector is a low power block which is used in NFC mode to detect presence of external RF field. It supports two different detection thresholds, Peer Detection Threshold and Collision Avoidance Threshold. Peer Detection Threshold is used in the NFCIP-1 target mode to detect presence of initiator field. It is also used in active communication initiator mode to detect activation of target field. Collision Avoidance Threshold is used to detect a presence of RF field during NFCIP-1 RF Collision Avoidance procedure.

Quartz Crystal Oscillator

The quartz crystal oscillator can operate with 13.56 MHz and 27.12 MHz crystals. At start-up the transconductance of the oscillator is increased to achieve fast start-up. Since the start-up time varies depending on crystal type, temperature and other parameters, the oscillator amplitude is observed and an interrupt is sent when stable operation is reached to inform the controller that the clock signal is stable and reader field can be switched on. The use of 27.12 MHz crystal is mandatory in case VHBR framing is used.

It also provides a clock signal to the external microcontroller (MCU_CLK) according to setting in the control register.

Power Supply Regulators

Integrated power supply regulators ensure high power supply rejection of a complete reader system. In case PSRR of the reader system has to be improved, the command Adjust Regulators is sent. As result of this command, the power supply level of V_{DD} is measured in maximum load conditions and the regulated voltage reference is set 250 mV below this measured level to assure a stable regulated supply. The resulting regulated voltage is stored in a register. It is also possible to define regulated voltage by writing a configuration register. In order to decouple any noise sources from different parts of IC there are three regulators integrated with separated external blocking capacitors (regulated voltage of all is the same in 3.3V supply mode).

One regulator is for the analog blocks, one for digital blocks, there is also a separate one for the antenna drivers. In case of low cost applications some (or all) regulators may not be used to save on external components.

This block additionally generates a reference voltage for the analog processing (AGD - analog ground). This voltage also has an associated external buffer capacitor.

POR and Bias

This block contains the bias current and voltage generator which provides bias currents and reference voltages to all other blocks. It also incorporates a Power on Reset (POR) circuit which provides a reset at power-up and at low supply levels.

RC Oscillator and Wake-up Timer

The AS3911 includes several possibilities of low power detection of a card presence (capacitive sensor, phase measurement, amplitude measurement). RC oscillator and register configurable Wake-up timer are used to schedule periodic detection. When presence of a card is detected an interrupt is sent to controller.

ISO14443 and NFCIP-1 Framing

This block performs framing for receive and transmit according to the selected ISO mode and bit rate settings.

In reception it takes demodulated sub-carrier signal from Receiver. It recognizes the SOF, EOF and data bits, performs parity and CRC check, organizes the received data in bytes and places them in the FIFO.

During transmit, it operates inversely, it takes bytes from FIFO, generates parity and CRC bits, adds SOF and EOF and performs final encoding before passing modulation signal to transmitter.

In Transparent mode, the framing and FIFO are bypassed, the digitized sub-carrier signal, which is Receiver output, is directly sent to MISO pin, signal applied to MOSI pin is directly used to modulate the transmitter.

FIFO

The AS3911 contains a 96 byte FIFO. Depending on the mode, it contains either data which has been received or data which is to be transmitted.

Control Logic

The control logic contains I/O registers which define operation of device.

SPI Interface

A 4-wire Serial Peripheral Interface (SPI) is used for communication between external microcontroller and the AS3911.

Application Information

Operating Modes

The AS3911 operating mode is defined by the contents of the Operation Control Register.

At power-up all bits of the Operation Control Register are set to 0, the AS3911 is in **Power-down** mode. In this mode AFE static power consumption is minimized, only the POR and part of the bias are active, the regulators are transparent and are not operating. The SPI is still functional in this mode so all settings of ISO mode definition and configuration registers can be done.

Control bit *en* (bit 7 of the Operation Control Register) is controlling the quartz crystal oscillator and regulators. When this bit is set, the device enters in **Ready** mode. In this mode the quartz crystal oscillator and regulators are enabled. An interrupt is sent to inform the microcontroller when the oscillator frequency is stable.

Enable of Receiver and Transmitter are separated so it is possible to operate one without switching on the other (control bits *rx_en* and *tx_en*). In some cases this may be useful, in case the reader field has to be maintained and there is no transponder response expected receiver can be switched-off to save current. Another example is NFCIP-1 active communication receive mode in which RF field is generated by the initiator and only Receiver operates.

Asserting the Operation Control Register bit *wu* while the other bits are set to 0 puts the AS3911 into the **Wake-up** mode which is used to perform low power detection of card presence. In this mode the low power RC oscillator and register configurable Wake-up timer are used to schedule periodic measurement(s). When a difference to the predefined reference is detected an interrupt is sent to wake-up the micro. Capacitive sensor, phase measurement and amplitude measurement are available.

Transmitter

The Transmitter contains two identical push-pull driver blocks connected to the pins RFO1 and RFO2. These drivers are differentially driving external antenna LC tank. It is also possible to operate only one of the two drivers by setting the IO Configuration Register 1 bit single. Each driver is composed of 8 segments having binary weighted output resistance. The MSB segment typical ON resistance is 2Ω, when all segments are turned on; the output resistance is typically 1Ω. Usually all segments are turned on to define the normal transmission (non-modulated) level.

It is also possible to switch off certain segments when driving the non-modulated level to reduce the amplitude of signal on the antenna and/or to reduce the antenna Q factor without making any hardware changes. The RFO Normal Level Definition Register defines which segments are turned on to define the normal transmission (non-modulated) level. Default setting is that all segments are turned on.

Using the single driver mode the number and therefore the cost of the antenna LC tank components is halved, but also the output power is reduced. In single mode it possible to connect two antenna LC tanks to the two RFO outputs and multiplex between them by controlling the IO Configuration Register 1 bit *rfo2*.

In order to transmit the data the transmitter output level needs to be modulated. The AM and OOK modulation are supported. The type of modulation is defined by setting the bit *tr_am* in the Auxiliary Definition Register. For the operation modes supported by the AS3911 framing the setting of modulation type is done automatically by sending direct command Analog Preset.

During the OOK modulation (for example ISO14443A) the Transmitter drivers stop driving the carrier frequency; drivers are frozen in state before the modulation. As consequence the amplitude of the antenna LC tank oscillation decays, the time constant of the decay is defined with the LC tank Q factor. The decay time in case of OOK modulation can be shortened by asserting the Auxiliary Definition Register bit *ook_hr*. When this bit is set to logic one the drivers are put in tristate during the OOK modulation.

AM modulation (for example ISO14443B) is done by increasing the output driver impedance during the modulation time. This is done by reducing the number of driver segments which are turned on. The AM modulated level can be automatically adjusted to the target modulation depth by defining the target modulation depth in the AM Modulation Depth Control Register and sending the Calibrate Modulation Depth direct command. Please refer to AM Modulation Depth: Definition and Calibration for further details.

Slow Transmitter Ramping

When transmitter is enabled it starts to drive the antenna LC tank with full power, the ramping of field emitted by antenna is defined by antenna LC tank Q factor.

However there are some reader systems where the reader field has to transition with a longer transition time when it is enabled. The STIF (Syndicat des transports d'Ile de France) specification requires a transition time from 10% to 90% of field longer than or equal to 10 µs.

The AS3911 supports that feature. It is realized by collapsing VSP_RF regulated voltage when transmitter is disabled and ramping it when transmitter is enabled. Typical transition time is 15 µs at 3V supply and 20 µs at 5V supply.

Procedure to implement the slow transition:

- When transmitter is disabled set IO Configuration Register 2 bit *slow_up* to 1. Keep this state at least 2 ms to allow discharge of VSP_RF.
- Enable transmitter, its output will ramp slowly.
- Before sending any command set the bit *slow_up* back to 0.

Receiver

The receiver performs demodulation of the transponder sub-carrier modulation which is superimposed on the 13.56MHz carrier frequency. It performs AM and/or PM demodulation, amplification, band-pass filtering and digitalization of sub-carrier signals. Additionally it performs RSSI measurement, automatic gain control (AGC) and Squelch function.

In typical application the Receiver inputs RFI1 and RFI2 are outputs of capacitor dividers connected directly to the terminals of antenna coil. Such concept assures that the two input signals are in phase to the voltage on antenna coil. Care has to be taken during design of capacitive divider that the RFI1 and RFI2 input signal pp value does not exceed the VSP_A supply voltage.

Receiver comprises two complete receive channels for AM demodulation and PM demodulation. In case both channels are active the selection of channel used for reception framing is done automatically by receive framing logic. The receiver is switched on when Operation Control Register bit *rx_en* is set to one. Additionally the Operation Control Register contains bits *rx_chn* and *rx_man*; *rx_chn* defines whether both, AM and PM, demodulation channels will be active or only one of them, while bit *rx_man* defines the channel selection mode in case both channels are active (automatic or manual). Operation of the Receiver is controlled by four Receiver Configuration registers.

The operation of the receiver is additionally controlled by the signal *rx_on* which is set high when modulated signal is expected on the receiver input. This signal is used to control RSSI and AGC and also enables processing of receiver output by Framing logic. Signal *rx_on* is automatically set high after Mask Receive timer expires. Signal *rx_on* can also be directly controlled by the controller by sending direct commands Mask Receive Data and Unmask Receive Data. Figure 14 illustrates the Receiver block diagram.

Demodulation Stage

First stage performs demodulation of transponder sub-carrier response signal, which is superimposed on HF field carrier. Two different blocks are implemented for AM demodulation: Peak Detector and AM demodulator mixer. The choice of the demodulator, which is used, is made by the Receiver Configuration Register 1 bit *amd_sel*.

Peak detector performs AM demodulation using peak follower. Both, the positive and negative peaks are tracked to suppress common mode signal. It is limited in speed; it can operate for sub-carrier frequencies up to fc/8 (1700 kHz). It has demodulation gain G = 0.7. Its input is taken from one demodulator input only (usually RFI1).

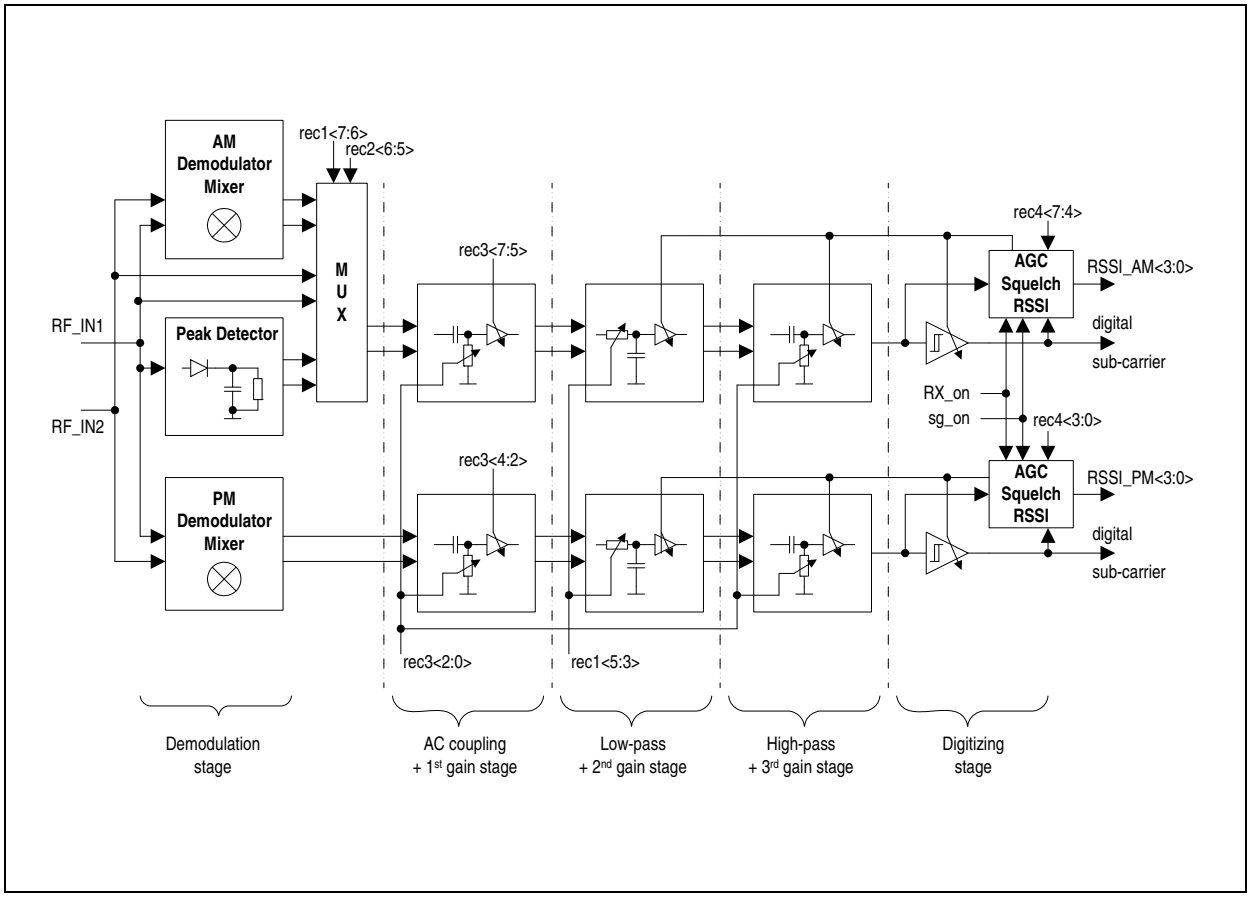
AM demodulator mixer uses synchronous rectification of both receiver inputs (RFI1 and RFI2). Its gain is G = 0.55. Mixer demodulator is optimized for VHBR sub-carrier frequencies. (fc/8 and higher). For sub-carrier frequency fc/8 (1700 kHz) both peak follower and mixer can be used, while for fc/4 and fc/2 are supported only by mixer.

By default the Peak detector is used, for data rates fc/8 and higher use of mixer is automatically preset by sending direct command Analog Preset.

PM demodulation is also done by a mixer. The PM demodulator mixer has differential outputs with 60mV differential signal for 1% phase change (16.67 mV per degree). Its operation is optimized for sub-carrier frequencies up to fc/8 (1700 kHz).

In case the demodulation is done externally of the AS3911 it is possible to multiplex the LF signals applied to pins RFI1 and RFI2 directly to the gain and filtering stage by selecting the Receiver Configuration Register 2 bit *lf_en*.

Figure 14:
Receiver Block Diagram



Filtering and Gain Stages

The receiver chain has band pass filtering characteristics. Filtering is optimized to pass sub-carrier frequencies while rejecting carrier frequency and low frequency noise and DC component. Filtering and gain is implemented in three stages where the first and the last stage have the first order high pass characteristics, while the mid stage has second order low pass characteristic.

Gain and filtering characteristics can be optimized for current application by writing the Receiver Configuration Register 1 (filtering), Receiver Configuration Register 3 (gain in first stage) and Receiver Configuration Register 4 (gain in second and third stage).

Gain of first stage is about 20dB and can be reduced in six 2.5 dB steps. There is also a special boost mode available, which boosts the maximum gain for additional 5.5 dB. In case of VHBR (fc/8 and fc/4) the gain is lower. The first stage gain can only be modified by writing Receiver Configuration Register 3. The default setting of this register is the minimum gain. Default first stage zero is located at 60 kHz, it can also be lowered to 40kHz or 12 kHz by writing option bits in the Receiver Configuration Register 1. The control of the first and third stage zeros is done with common control bits (see Figure 16).

Gain in the second and third stage is 23 dB and can be reduced in six 3 dB steps. Gain of these two stages is included in AGC and Squelch loops or can be manually set in Receiver Configuration Register 4. Sending of direct command Reset Rx Gain is necessary to reset the AGC, Squelch and RSSI block. Sending this command clears the current Squelch setting and loads the gain reduction configuration from Receiver Configuration Register 4 into the internal shadow registers of AGC/Squelch block. Second stage has a second order low pass filtering characteristic, the pass band is adjusted according to sub-carrier frequency using the bits lp2 to lp0 of the Receiver Configuration Register 1. See Figure 15 for -1dB cut-off frequency for different settings.

Figure 15:
Low Pass Control

rec1<5> lp2	rec1<4> lp1	rec1<3> lp0	-1 dB point
0	0	0	1200 kHz
0	0	1	600 kHz
0	1	0	300 kHz
1	0	0	2 MHz
1	0	1	7 MHz
Other			Not used

Figure 16:
First and Third Stage Zero Setting

rec1<2> h200	rec1<1> h80	rec1<0> z12k	First Stage Zero	Third Stage Zero
0	0	0	60 kHz	400 kHz
1	0	0	60 kHz	200 kHz
0	1	0	40 kHz	80 kHz
0	0	1	12 kHz	200 kHz
0	1	1	12 kHz	80 kHz
1	0	1	12 kHz	200 kHz
Other			Not used	

Figure 17 provides information on the recommended filter settings. For all supported operation modes and receive bit rates there is an automatic preset defined, additionally some alternatives are listed. Automatic preset is done by sending direct command Analog Preset. There is no automatic preset for Steam and Transparent modes. Since selection of filter characteristics also modifies gain, the gain range for different filter settings is also listed.

Figure 17:
Receiver Filter Selection and Gain Range

rec1<5:3> lp<2:0>	rec1<2> h200	rec1<1> h80	rec1<0> z12k	Gain [dB]					Comment
				Max All	Min1 Max23	Max1 Min23	Min All	With Boost	
000	0	0	0	43.4	28	26.4	11	49.8	Automatic preset for ISO14443A fc/128 and NFC Forum Type 1 Tag
000	1	0	0	44	29	27.5	12	49.7	Automatic preset for ISO14443B fc/128 ISO14443 fc/64
001	1	0	0	44.3	29	27	11.7	49.8	Recommended for 424/484 kHz sub-carrier
000	0	1	0	41.1	25.8	23.6	8.3	46.8	Alternative choice for ISO14443 fc/32 and fc/16
100	0	1	0	32	17	17.2	2	37.6	Automatic preset for ISO14443 fc/32 and fc/16 Alternative choice for fc/8 (1.7 kbit/s)
100	0	0	0	32	17	17.2	2	37.6	Alternative choice for fc/8 (1.7 kbit/s)

rec1<5:3> lp<2:0>	rec1<2> h200	rec1<1> h80	rec1<0> z12k	Gain [dB]					Comment
				Max All	Min1 Max23	Max1 Min23	Min All	With Boost	
000	0	1	1	41.1	25.8	23.6	8.3	46.8	Automatic preset FeliCa (fc/64, fc/32) Alternative choice for ISO14443 fc/32 and fc/16
101	0	1	0	30	20	12	2	34	Alternative choice for fc/8 and fc/4
101	1	0	0	30	20	12	2	34	Automatic preset for fc/8 and fc/4
000	1	0	1	36.5	21.5	24.9	9.9	41.5	Automatic preset for NFCIP-1 (initiator and target)

Digitizing Stage

Digitizing stage is producing a digital form of sub-carrier signal which is output of Receiver and input to Framing Logic. It is a window comparator with adjustable digitizing window (five possible settings, 3 dB steps, adjustment range from ±33 mV to ±120 mV). Adjustment of the digitizing window is included in AGC and Squelch loops or can be manually set in Receiver Configuration Register 4.

AGC, Squelch and RSSI

As mentioned above second and third gain stage gain and the Digitizing stage digitizing window are included in AGC and Squelch loops. Eleven settings are available, default state features minimum digitizer window and maximum gain, first four steps increase the digitizer window in 3 dB steps, next six steps additionally reduce the gain in 2nd and 3rd gain stage also in 3 dB steps. The initial setting with which Squelch and AGC start is defined in Receiver Configuration Register 4. The Gain Reduction State Register displays the actual state of gain which results from Squelch, AGC and initial settings in Receiver Configuration Register 4.

Squelch

This feature is designed for operation of receiver in noisy environment. The noise can come from tags in which processing of data sent by the reader is going on and an answer is being prepared. Noise can also be generated by noisy environment. This noise may be misinterpreted as start of transponder response which results in decoding error.

During execution of the Squelch procedure the output of Digitizing comparator is observed. In case there are more than two transitions on this output in 50 µs time period, gain is reduced for 3 dB and output is observed during next 50 µs. This procedure is repeated until number of transitions in 50 µs is lower or equal to 2 or until maximum gain reduction is reached.

This setting is cleared by sending direct command Reset Rx Gain.

There are two possibilities of performing squelch: automatic mode and using direct command Squelch.

- Automatic mode is started in case bit *sqm_dyn* in the Receiver Configuration Register 2 is set. It is activated automatically 18.88 µs after end of Tx and is terminated with Mask Receive timer expire. This mode is primarily intended to suppress noise generated by tag processing during the time when the tag response is not expected (covered by Mask Receive timer).
- Command Squelch is accepted in case it is sent when signal *rx_on* is low. It can be used in case the time window in which noise is present is known by the controller.

AGC

AGC (automatic gain control) is used to reduce gain to keep receiver chain out of saturation. In case gain is properly adjusted the demodulation process is also less influenced by system noise.

AGC action starts when signal *rx_on* is asserted high and is reset when it is reset to low. At high to low transitions of the *rx_on* the state of the receiver gain is stored in the Gain Reduction State Register, therefore reading this register later gives the information of the gain setting used during last reception.

When AGC is switched on receiver gain is reduced so that the input to digitizer stage is not saturated. The AGC system comprises a window comparator which has its window 3.5 times larger than window of digitalization window comparator. When the AGC function is enabled gain is reduced until there are no transitions on its output. Such procedure assures that the input to digitalization window comparator is less than 3.5 times larger than its window.

AGC operation is controlled by the control bits *agc_en*, *agc_m* and *agc_fast* in the Receiver Configuration Register 2. Bit *agc_en* enables the AGC operation; bit *agc_m* defines the AGC mode while bit *agc_alg* define the AGC algorithm.

Two AGC modes are available, AGC can operate during complete Rx process (as long as signal *rx_on* is high) or it can be enabled only during first eight sub-carrier pulses.

Two AGC algorithms are available; AGC can either start by presetting of code 4_h (max digitizer window, max gain) or by resetting the code to 0_h (min digitizer window, max gain). Algorithm with preset code is faster, therefore it is recommended for protocols with short SOF (like ISO14443A fc/128).

Default AGC settings are: AGC is enabled, AGC operates during complete Rx process, algorithm with preset is used.

RSSI

The receiver also performs the RSSI (Received Signal Strength Indicator) measurement of both channels. RSSI measurement is started after rising edge of **rx_on**. It stays active while signal **rx_on** is high; while **rx_on** is low it is frozen. It is a peak hold system; the value can only increase from initial zero value. Every time the AGC reduces the gain the RSSI measurement is reset and starts from zero. Result of RSSI measurements is 4-bit value which can be observed by reading the RSSI Display Register. The LSB step is 2.8 dB, the maximum code is D_h (13_d).

Since the RSSI measurement is of peak hold type the RSSI measurement result does not follow any variations in the signal strength (the highest value will be kept). In order to follow RSSI variation it is possible to reset RSSI bits and restart the measurement by sending direct command Clear RSSI.

Receiver in NFCIP-1 Active Communication Mode

There are several features built in receiver to enable reliable reception of active NFCIP-1 communication. All these settings are automatically preset by sending direct command Analog Preset after the NFCIP-1 mode has been configured. In addition to filtering options there are two NFC specific configuration bits stored in the Receiver Configuration Register 3.

Bit *lim* enables clipping circuits which are positioned after first and second gain stages. The intention of clipping circuits is to limit the signal level for the following filtering stage (in case the NFC peer is close the input signal level can be quite high).

Bit *rg_nfc* forces gain reduction of second and third filtering stage to -6dB while keeping the digitizer comparator window at maximum level.

Capacitive Sensor

The Capacitive Sensor block provides a possibility of low power detection of tag presence.

The capacitive measurement system comprises two electrodes. One is excitation electrode emitting electrical field of a fixed frequency in range of few hundred kHz (CSO) and the second one is the sensing electrode (CSI). The amount of charge generated in sensing electrode represents the capacitance between the two electrodes. Capacitive sensor electrodes are tolerant to parasitic capacitance to ground (up to 25 pF) and to input leakage (up to 1 MΩ).

Since the charge on the sensing electrode is generated with the frequency of excitation electrode, synchronous rectifier is used to detect it. This ensures good rejection of interference and high tolerance to parasitic capacitances (to all nodes except the excitation electrode).