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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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AS3932

3D Low Frequency Wakeup Receiver

General Description

The AS3932 is a 3-channel low power ASK receiver that is able to generate a wake-up upon detection of a data signal which uses a LF carrier frequency between 110 - 150 kHz. The integrated correlator can be used for detection of a programmable 16-bit wake-up pattern. The device can operate using one, two, or three active channels.

The AS3932 provides a digital RSSI value for each active channel, it supports a programmable data rate. The AS3932 offers a real-time clock (RTC), which is either derived from a crystal oscillator or the internal RC oscillator.

The programmable features of AS3932 enable to optimize its settings for achieving a longer distance while retaining a reliable wake-up generation. The sensitivity level of AS3932 can be adjusted in presence of a strong field or in noisy environments.

The device is available in 16-pin TSSOP and 16LD QFN (4×4) packages.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3932, 3D Low Frequency Wakeup Receiver are listed below:

Figure 1:
Added Value of Using AS3932

Benefits	Features
Enables low power active tags	3-channel ASK wake-up receiver
Selectable carrier frequency	Carrier frequency range 110 - 150 kHz
One, two, or three channel operation	1-D, 2-D, or 3-D wake-up pattern detection
Highly resistant to false wake-ups	16-bit programmable wake-up pattern
Improved immunity to false wake-ups	Supporting doubling of wake-up pattern
Allows frequency only detection	Wake-up without pattern detection selectable
Improved range with best-in-class sensitivity	Wake-up sensitivity 100µVRMS (typ.)
Adjustable range	Sensitivity level adjustable
Provides tracking of false wake-ups	False wake-up counter
Ensures wake-up in a noise environment	Periodical forced wake-up supported (1s – 2h)
Extended battery life	Current consumption in 3-channel listening mode 1.7µA (typ.)

Benefits	Features
Flexible clock configuration	RTC based 32 kHz XTAL, RC-OSC, or external clock
Operates from a 3V battery	Operating supply range 2.4V – 3.6V (TA = 25°C)
Industrial temperature range	Operation temperature range -40°C to +85°C

Applications

The AS3932 is ideal for:

- Active RFID tags,
- Real-time location systems,
- Operator identification,
- Access control, and
- Wireless sensors.

Figure 2:
AS3932 Typical Application Diagram with Crystal Oscillator

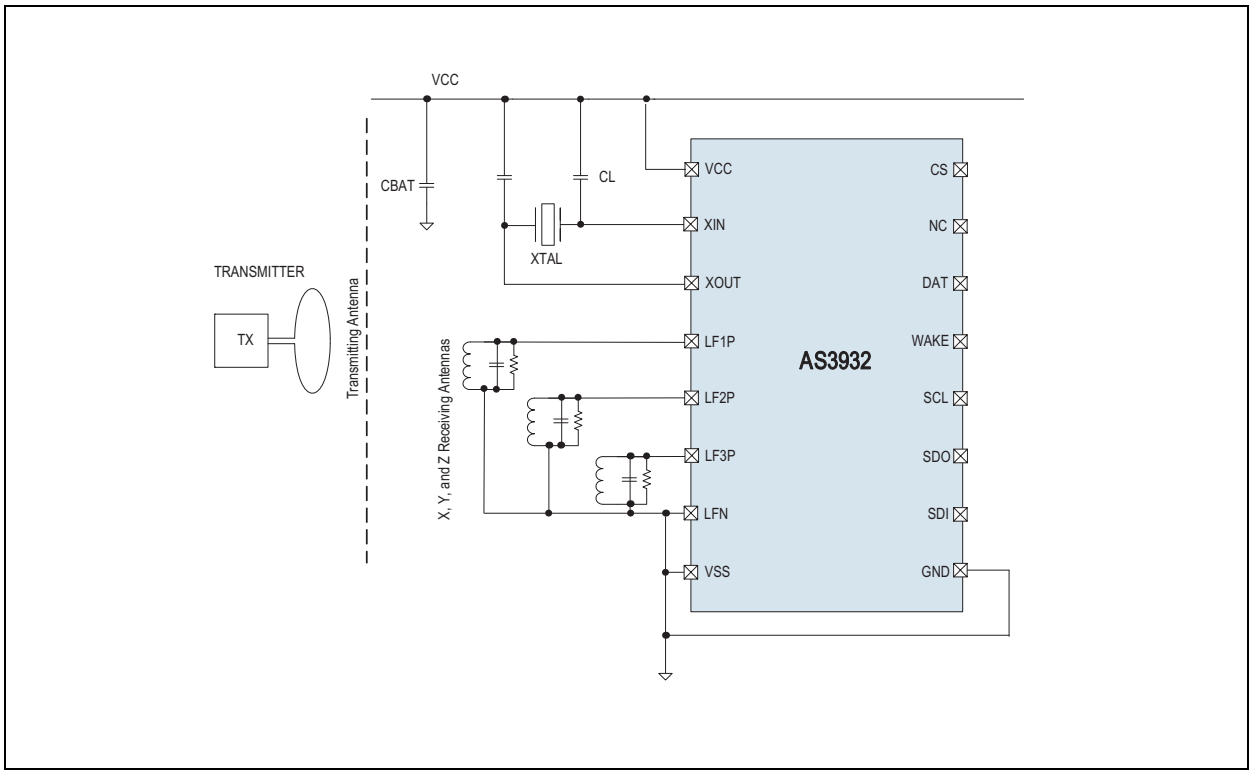


Figure 3:
AS3932 Typical Application Diagram with RC Oscillator

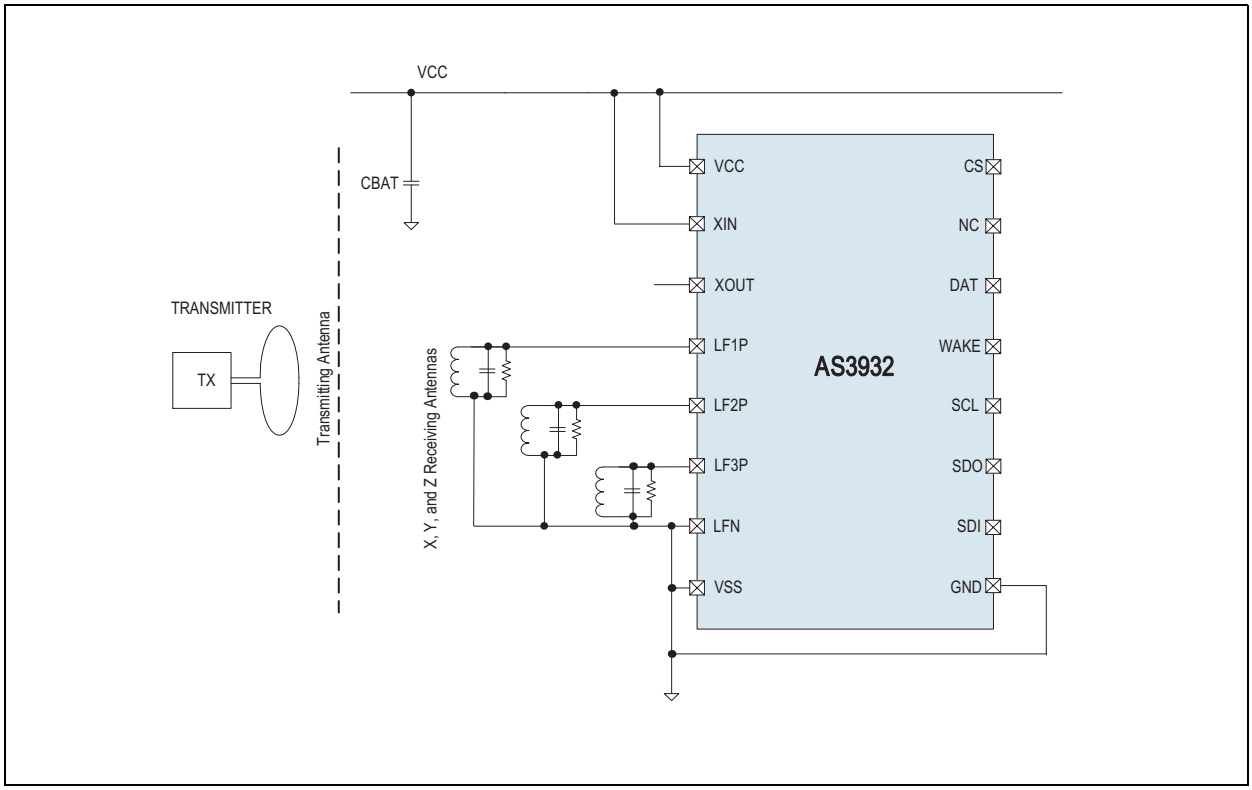
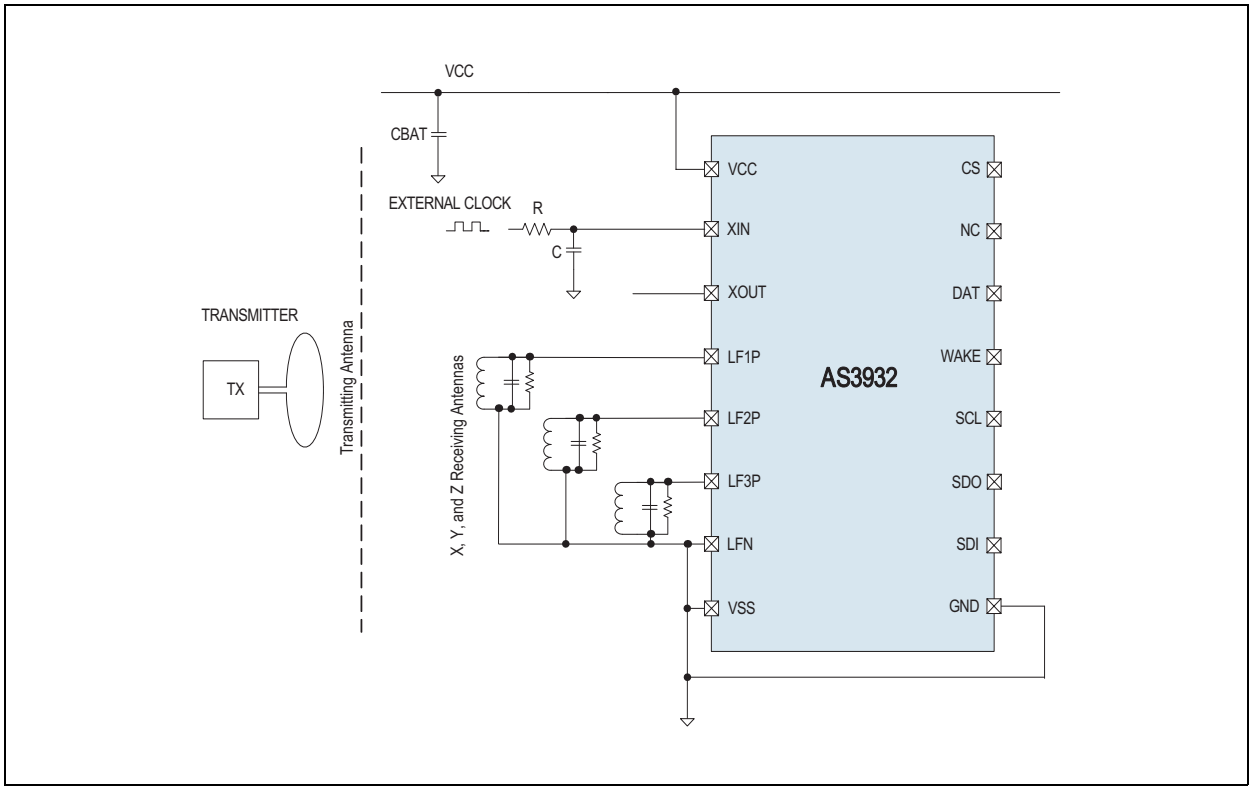


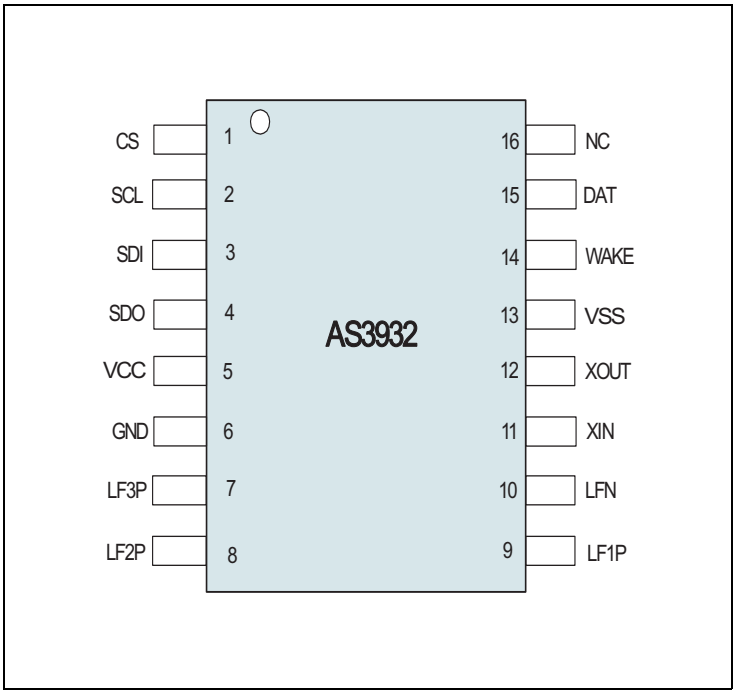
Figure 4:
AS3932 Typical Application Diagram with Clock from External Source



Pin Assignment

TSSOP Package

Figure 5:
Pin Assignments 16-pin TSSOP Package



Pin Description

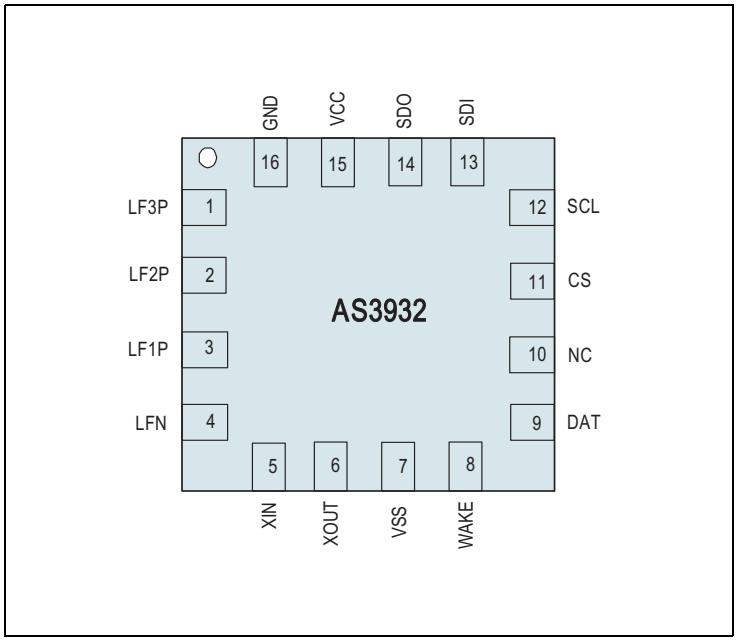
Figure 6:
Pin Descriptions 16-pin TSSOP Package

Pin Name	Pin Number	Pin Type	Description
CS	1	Digital input	Chip select
SCL	2		SDI interface clock
SDI	3		SDI data input
SDO	4	Digital output / tristate	SDI data output (tristate when CS is low)
VCC	5	Supply pad	Positive supply voltage
GND	6	Supply pad	Negative supply voltage

Pin Name	Pin Number	Pin Type	Description
LF3P	7	Analog I/O	Input antenna channel three
LF2P	8		Input antenna channel two
LF1P	9		Input antenna channel one
LFN	10		Common ground for antenna one, two and three
XIN	11		Crystal oscillator input
XOUT	12		Crystal oscillator output
V_{SS}	13	Supply pad	Substrate
WAKE	14	Digital output	Wake-up output IRQ
DAT	15		Data output
NC	16	-	Not connected

QFN Package

Figure 7:
Pin Assignments 16LD QFN (4×4) Package



Pin Description

Figure 8:
Pin Descriptions 16LD QFN (4×4) Package

Pin Name	Pin Number	Pin Type	Description
LF3P	1	Analog I/O	Input antenna channel three
LF2P	2		Input antenna channel two
LF1P	3		Input antenna channel one
LFN	4		Common ground for antenna one, two and three
XIN	5		Crystal oscillator input
XOUT	6		Crystal oscillator output
V_{SS}	7	Supply pad	Substrate
WAKE	8	Digital output	Wake-up output IRQ
DAT	9		Data output
NC	10	-	Not connected
CS	11	Digital input	Chip select
SCL	12		SDI interface clock
SDI	13		SDI data input
SDO	14	Digital output / tristate	SDI data output (tristate when CS is low)
VCC	15	Supply pad	Positive supply voltage
GND	16	Supply pad	Negative supply voltage

Note(s) and/or Footnote(s):

1. The exposed pad has to be connected to ground.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 9:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
Electrical Parameters					
V_{DD}	DC supply voltage	-0.5	5	V	
V_{IN}	Input pin voltage	-0.5	5	V	
I_{SOURCE}	Input current (latch up immunity)	-100	100	mA	Norm: Jedec 78
Electrostatic Discharge					
ESD	Electrostatic discharge	±2		kV	Norm: MIL 883 E method 3015 (HBM)
Continuous Power Dissipation					
P_t	Total power dissipation		0.07	mW	All supplies and outputs
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-65	150	°C	
T_{body}	Package body temperature		260	°C	Norm: IPC/JEDEC J-STD-020 *The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices".*
RH_{NC}	Relative Humidity non-condensing	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h

Electrical Characteristics

Figure 10:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Operating Conditions						
V_{DD}	Positive supply voltage		2.4		3.6	V
V_{SS}	Negative supply voltage		0		0	V
T_{AMB}	Ambient temperature		-40		85	°C
DC/AC Characteristics for Digital Inputs and Outputs						
CMOS Input						
V_{IH}	High level input voltage		0.58* V_{DD}	0.7* V_{DD}	0.83* V_{DD}	V
V_{IL}	Low level input voltage		0.125* V_{DD}	0.2* V_{DD}	0.3* V_{DD}	V
I_{LEAK}	Input leakage current				100	nA
CMOS Output						
V_{OH}	High level output voltage	With a load current of 1mA	V_{DD} - 0.4			V
V_{OL}	Low level output voltage	With a load current of 1mA			V_{SS} + 0.4	V
C_L	Capacitive load	For a clock frequency of 1 MHz			400	pF
Tristate CMOS Output						
V_{OH}	High level output voltage	With a load current of 1mA	V_{DD} - 0.4			V
V_{OL}	Low level output voltage	With a load current of 1mA			V_{SS} + 0.4	V
I_{OZ}	Tristate leakage current	To V_{DD} and V_{SS}			100	nA

Figure 11:
Electrical System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Characteristics						
R_{IN}	Input Impedance	In case no antenna damper is set (R1<4>=0)		2		MΩ
Fmin	Minimum Input Frequency			110		kHz
Fmax	Maximum Input Frequency			150		kHz
Current Consumption						
IPWD	Power Down Mode			400		nA
I1CHRC	Current Consumption in standard listening mode with one active channel and RC-oscillator as RTC			2.7		µA
I2CHRC	Current Consumption in standard listening mode with two active channels and RC-oscillator as RTC			4.2		µA
I3CHRC	Current Consumption in standard listening mode with three active channels and RC-oscillator as RTC			5.7	8.3	µA
I3CHSCRC	Current Consumption in scanning mode with three active channels and RC-oscillator as RTC			2.7		µA
I3CHOORC	Current Consumption in ON/ OFF mode with three active channels and RC-oscillator as RTC	11% Duty Cycle		1.7		µA
		50% Duty Cycle		3.45		
I3CHXT	Current Consumption in standard listening mode with three active channels and crystal oscillator as RTC			6.5	8.9	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IDATA	Current Consumption in Preamble detection / Pattern correlation / Data receiving mode (RC-oscillator)	With 125 kHz carrier frequency and 1kbpsdata-rate. No load on the output pins.		8.3	12	µA
Input Sensitivity						
SENS	Input Sensitivity on all channels	With 125 kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		100		µVrms
Channel Settling Time						
TSAMP	Amplifier settling time			250		µs
Crystal Oscillator						
FXTAL	Frequency	Crystal dependent		32.768		kHz
TXTAL	Start-up Time	Crystal dependent			1	s
IXTAL	Current consumption			1		µA
External Clock Source						
IEXTCL	Current consumption			1		µA
RC Oscillator						
FRCNCAL	Frequency	If no calibration is performed	27	32.768	42	kHz
FRCCAL32	Frequency	If calibration with 32.768 kHz reference signal is performed	31	32.768	34.5	kHz
FRCCALMAX	Frequency	Maximum achievable frequency after calibration		35		kHz
FRCCALMIN	Frequency	Minimum achievable frequency after calibration		30		kHz
TRC	Start-up time	From RC enable (R1<0> = 0)			1	s
TCALRC	Calibration time				65	Periods of reference clock
IRC	Current consumption			200		nA

Typical Operating Characteristics

Figure 12:
Sensitivity over Voltage and Temperature

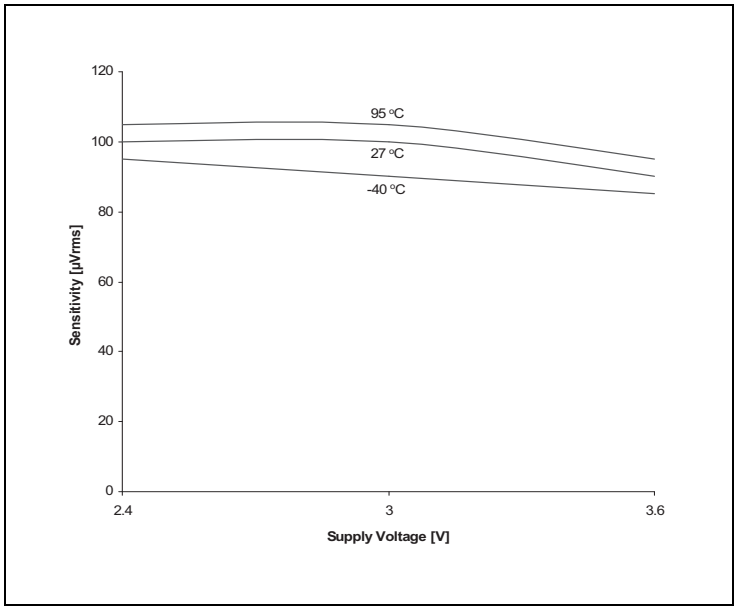


Figure 13:
Sensitivity over RSSI

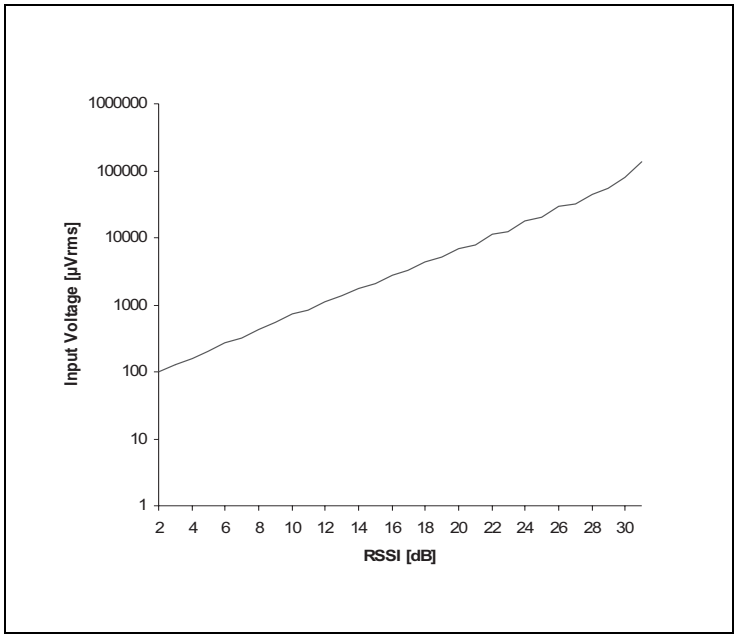


Figure 14:
RC-Osc Frequency over Voltage (calibr.)

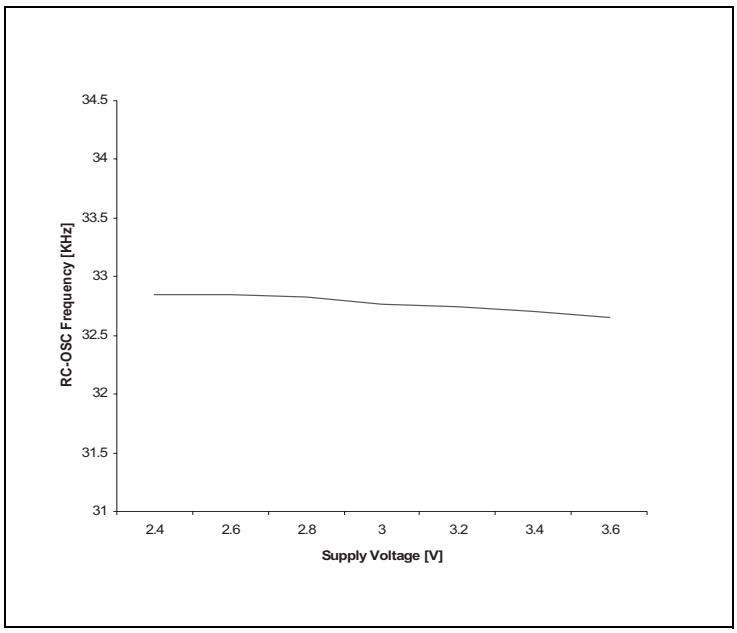
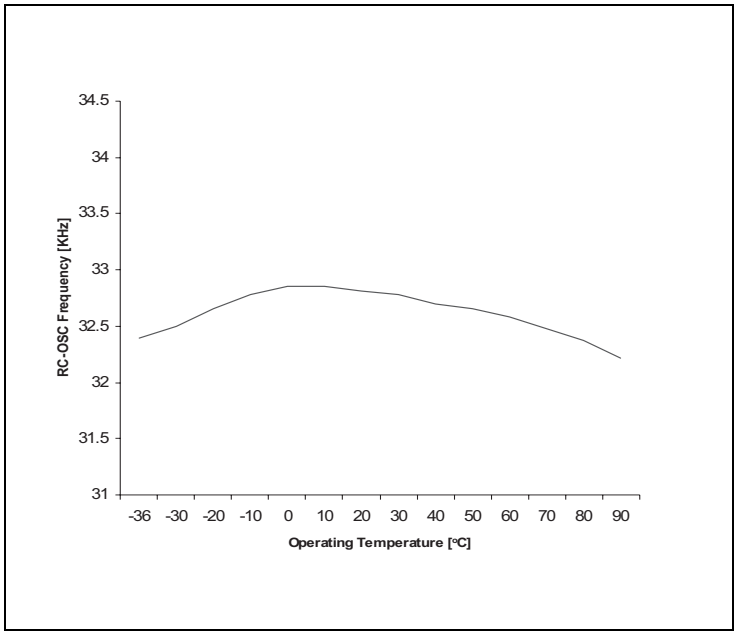


Figure 15:
RC-Osc Frequency over Temperature (calibr.)



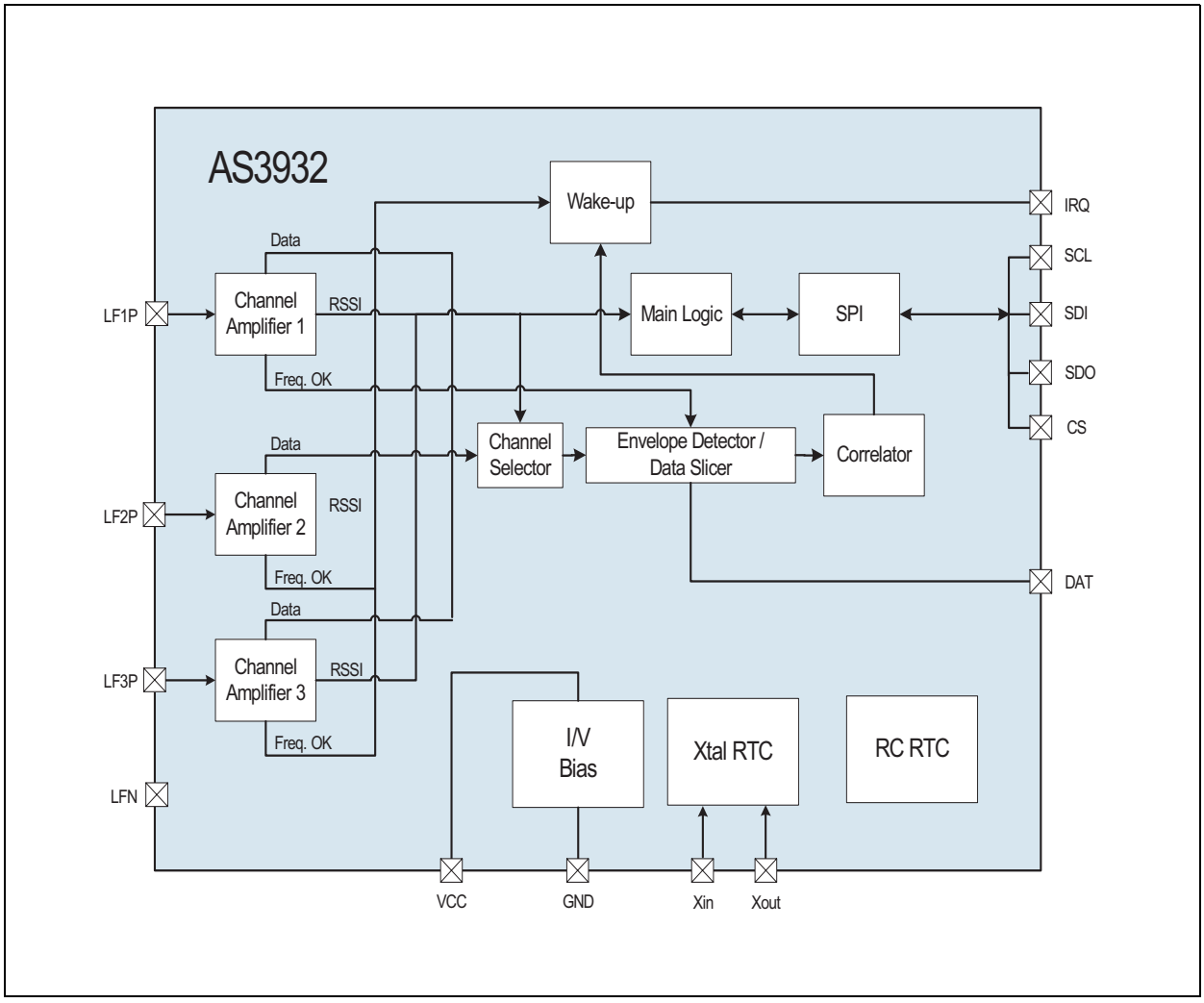
Detailed Description

The AS3932 is a three-dimensional low power low-frequency wake-up receiver. The AS3932 is capable to detect the presence of an inductive coupled carrier and extract the envelope of the ON-OFF-Keying (OOK) modulated carrier. If the detected pattern corresponds to the stored one a wake-up signal (IRQ) is risen up. The pattern correlation can be bypassed in which case the wake-up detection is based only on the frequency detection.

The AS3932 is made up by three independent receiving channels, one envelop detector, one data correlator, 8 programmable registers with the main logic and a real time clock.

The digital logic can be accessed by an SPI. The real time clock can be based on a crystal oscillator or on an internal RC one. If the internal RC oscillator is used, a calibration procedure can be performed to improve its accuracy.

Figure 16:
Block Diagram of LF Wake-up Receiver AS3932



AS3932 needs the following external components:

- Power supply capacitor - CBAT - 100 nF.
- 32.768 kHz crystal with its two pulling capacitors - XTAL and CL - (it is possible to omit these components if the internal RC oscillator is used instead of the crystal oscillator).
- One, two, or three LC resonators according to the number of used channels.

In case the internal RC-oscillator is used (no crystal oscillator is mounted), the pin XIN has to be connected to the supply, while pin XOUT should stay floating. Application diagrams with and without crystal are shown in Figure 2 and Figure 3.

Operating Modes

Power Down Mode

In Power Down Mode AS3932 is completely switched OFF. The typical current consumption is 400 nA.

Listening Mode

In listening mode only the active channel amplifiers and the RTC are running. In this mode the system detects the presence of a carrier. In case the carrier is detected the RSSI can be displayed.

If the three dimensional detection is not required it is possible to deactivate one or more channels. In case only two channels are required the deactivated channel must be the number two, while if only one channel detection is needed the active channel must be the number one.

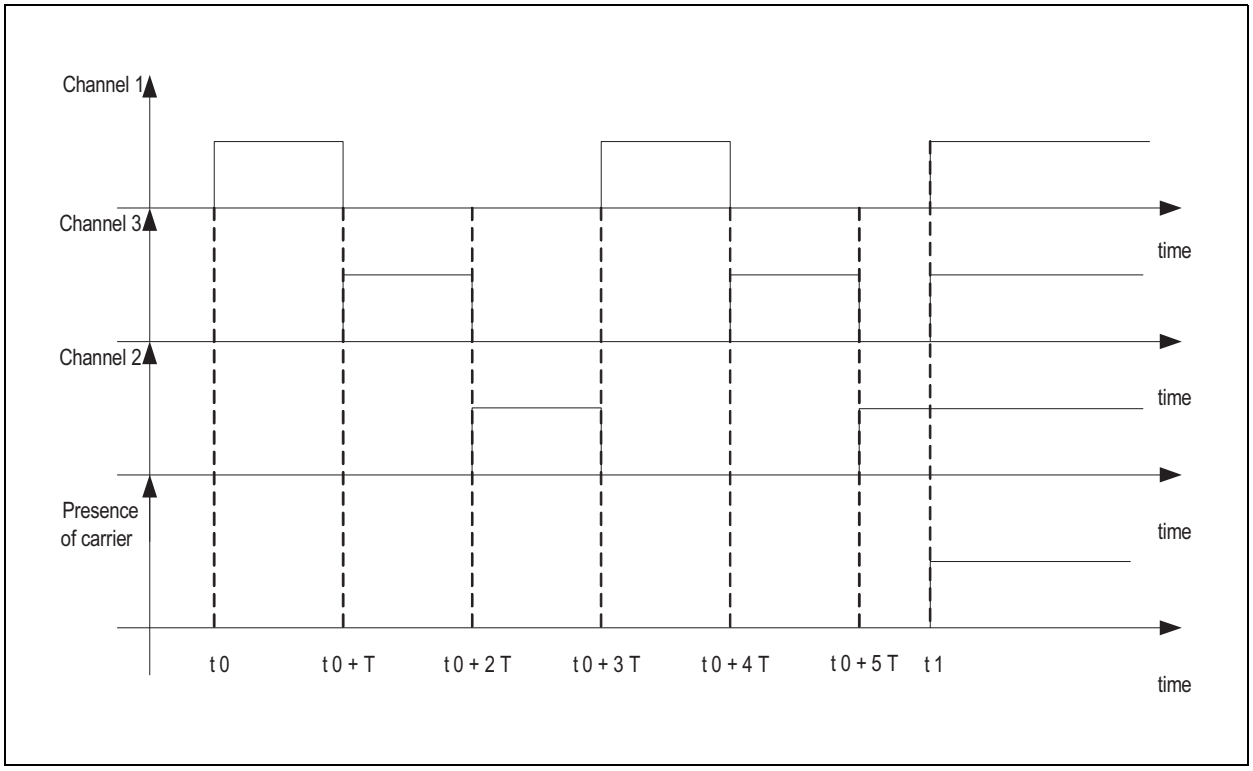
Inside this mode it is possible to distinguish the following three sub modes:

Standard Listening Mode. All channels are active at the same time.

Scanning Mode (Low Power Mode 1). All used channels are active, but only one per time slot, where the time slot T is defined as 1ms. Thus, if all three channels are active the procedure is as follows (see Figure 17): for the first millisecond only channel one is active while channel two and three are powered down; for the next millisecond only channel three is active while channel one and two are powered down; finally, channel two is active while the other two are deactivated. This channel rotation goes on until the presence of the carrier is detected by any of the channels; then immediately all three channels will become active at the same time. Now AS3932 can perform a simultaneous multidirectional evaluation (on all three channels) of the field and evaluate which channel has the strongest RSSI. The channel with the highest RSSI will be put through to the demodulator.

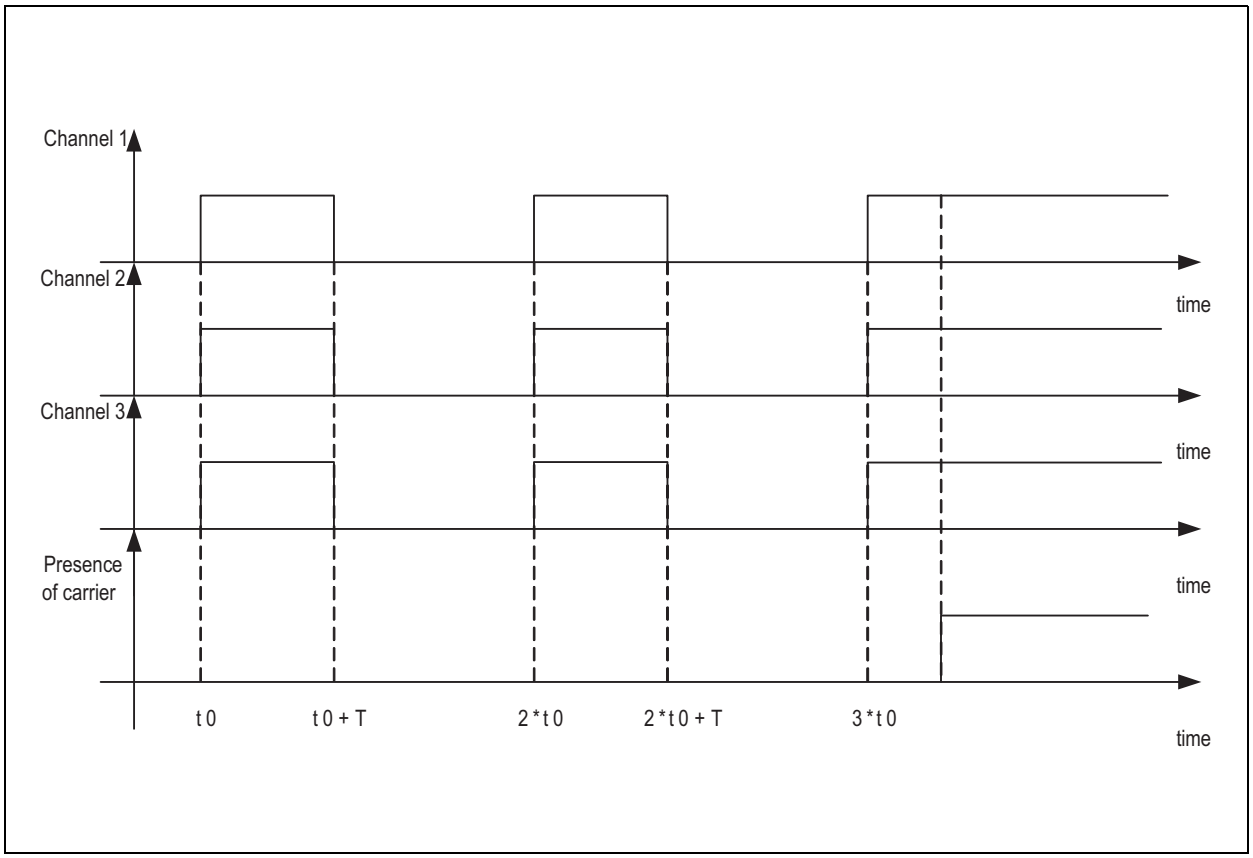
In this way it is possible to perform multidirectional monitoring of the field with a current consumption of a single channel, keeping the sensitivity as good as if all channels are active at the same time.

Figure 17:
Scanning Mode



ON/OFF Mode (Low Power Mode 2). All active channels are ON at the same time but not for the whole time (time slot T is defined as 1ms). An ON-OFF duty-ratio is defined. This duty ratio is programmable see R4<7:6>.

Figure 18:
ON/OFF Mode



For each of these sub modes it is possible to enable a further feature called Artificial Wake-up. The Artificial Wake-up is a counter based on the used RTC. Three bits define a time window see R8<2:0>. If no activity is seen within this time window the chip will produce an interrupt on the WAKE pin that lasts 128µs. With this interrupt the microcontroller (µC) can get feedback on the surrounding environment (e.g. read the false wake-up register R13<7:0>) and/or take actions in order to change the setup.

Preamble Detection / Pattern Correlation

The preamble detection and pattern correlation are only considered for the wake-up when the data correlator function is enabled (see R1<1>). The correlator searches first for preamble frequency (constant frequency of Manchester clock defined according to bit-rate transmission, see Figure 37) and then for data pattern.

If the pattern is matched the wake-up interrupt is displayed on the WAKE output and the chip goes in Data receiving mode. If the pattern fails the internal wake-up (on all active channels) is terminated and no IRQ is produced.

Data Receiving

After a successful wake-up the chip enters the data receiving mode. In this mode the chip can be retained a normal OOK receiver. The received data are streamed out on the pin DAT. It is possible to put the chip back to listening mode either with a direct command (CLEAR_WAKE (see Figure 25)) or by using the timeout feature. This feature automatically sets the chip back to listening mode after a certain time R7<7:5>.

System and Block Specification

Register Table

Figure 19:
Register Table

	7	6	5	4	3	2	1	0
R0	n.a.		ON_OFF	MUX_123	EN_A2	EN_A3	EN_A1	PWD
R1	ABS_HY	AGC_TLIM	AGC_UD	ATT_ON		EN_PAT2	EN_WPAT	EN_RTC
R2	S_ABSH	W_PAT_T<1:0>		Reserved			S_WU1<1:0>	
R3	HY_20m	HY_POS	FS_SLC<2:0>			FS_ENV<2:0>		
R4	T_OFF<1:0>		R_VAL<1:0>		GR<3:0>			
R5	TS2<7:0>							
R6	TS1<7:0>							
R7	T_OUT<2:0>			T_HBIT<4:0>				
R8	n.a					T_AUTO<2:0>		
R9	n.a	Reserved						
R10	n.a			RSSI1<4:0>				
R11	n.a			RSSI3<4:0>				
R12	n.a			RSSI2<4:0>				
R13	F_WAKE							

Register Table Description and Default Values

Figure 20:
Default Values of Registers

Register	Name	Type	Default Value	Description
R0<5>	ON_OFF	R/W	0	ON/OFF operation mode. (Duty-cycle defined in the register R4<7:6>
R0<4>	MUX_123	R/W	0	Scan mode enable
R0<3>	EN_A2	R/W	1	Channel 2 enable
R0<2>	EN_A3	R/W	1	Channel 3 enable
R0<1>	EN_A1	R/W	1	Channel 1 enable
R0<0>	PWD	R/W	0	Power down
R1<7>	ABS_HY	R/W	0	Data slicer absolute reference
R1<6>	AGC_TLIM	R/W	0	AGC acting only on the first carrier burst
R1<5>	AGC_UD	R/W	1	AGC operating in both direction (up-down)
R1<4>	ATT_ON	R/W	0	Antenna damper enable
R1<2>	EN_PAT2	R/W	0	Double wake-up pattern correlation
R1<1>	EN_WPAT	R/W	1	Data correlation enable
R1<0>	EN_RTC	R/W	1	Crystal oscillator enable
R2<7>	S_ABSH	R/W	0	Data slicer threshold reduction
R2<6:5>	W_PAT	R/W	00	Pattern correlation tolerance (see Figure 38)
R2<4:2>	Reserved		000	Reserved
R2<1:0>	S_WU1	R/W	00	Tolerance setting for the stage wake-up (see Figure 32)
R3<7>	HY_20m	R/W	0	Data slicer hysteresis if HY_20m = 0 then comparator hysteresis = 40mV if HY_20m = 1 then comparator hysteresis = 20mV
R3<6>	HY_POS	R/W	0	Data slicer hysteresis on both edges (HY_POS = 0 → hysteresis on both edges; HY_POS = 1 → hysteresis only on positive edges)
R3<5:3>	FS_SCL	R/W	100	Data slicer time constant (see Figure 36)
R3<2:0>	FS_ENV	R/W	000	Envelop detector time constant (see Figure 35)

Register	Name	Type	Default Value	Description	
R4<7:6>	T_OFF	R/W	00	OFF time in ON/OFF operation mode	
				T_OFF=00	1ms
				T_OFF=01	2ms
				T_OFF=10	4ms
				T_OFF=11	8ms
R4<5:4>	D_RES	R/W	01	Antenna damping resistor (see Figure 34)	
R4<3:0>	GR	R/W	0000	Gain reduction (see Figure 33)	
R5<7:0>	TS2	R/W	01101001	2nd Byte of wake-up pattern	
R6<7:0>	TS1	R/W	10010110	1st Byte of wake-up pattern	
R7<7:5>	T_OUT	R/W	000	Automatic time-out (see Figure 39)	
R7<4:0>	T_HBIT	R/W	01011	Bit rate definition (see Figure 37)	
R8<2:0>	T_AUTO	R/W	000	Artificial wake-up	
				T_AUTO=000	No artificial wake-up
				T_AUTO=001	1 sec
				T_AUTO=010	5 sec
				T_AUTO=011	20 sec
				T_AUTO=100	2 min
				T_AUTO=101	15min
				T_AUTO=110	1 hour
				T_AUTO=111	2 hour
R9<6:0>	Reserved		000000	Reserved	
R10<4:0>	RSSI1	R		RSSI channel 1	
R11<4:0>	RSSI2	R		RSSI channel 2	
R12<4:0>	RSSI3	R		RSSI channel 3	
R13<7:0>	F_WAK	R		False wake-up register	

Serial Data Interface (SDI)

This 4-wires interface is used by the Microcontroller (µC) to program the AS3932. The maximum clock frequency of the SDI is 2MHz.

Figure 21:
Serial Data Interface (SDI) Pins

Name	Signal	Signal Level	Description
CS	Digital Input with pull down	CMOS	Chip Select
SDI	Digital Input with pull down	CMOS	Serial Data input for writing registers, data to transmit and/or writing addresses to select readable register
SDO	Digital Output	CMOS	Serial Data output for received data or read value of selected registers
SCLK	Digital Input with pull down	CMOS	Clock for serial data read and write

Note(s): SDO is set to tristate if CS is low. In this way more than one device can communicate on the same SDO bus.

SDI Command Structure. To program the SDI the CS signal has to go high. A SDI command is made up by a two bytes serial command and the data is sampled on the falling edge of SCLK. The Figure 22 shows how the command looks like, from the MSB (B15) to LSB (B0). The command stream has to be sent to the SDI from the MSB (B15) to the LSB (B0).

Figure 22:
SDI Command Structure

Mode		Register Address / Direct Command						Register Data						
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B3	B2	B1	B0

The first two bits (B15 and B14) define the operating mode. There are three modes available (write, read, direct command) plus one spare (not used), as shown in Figure 23.

Figure 23:
SDI Command Structure

B15	B14	Mode
0	0	WRITE
0	1	READ
1	0	NOT ALLOWED
1	1	DIRECT COMMAND

In case a write or read command happens the next 6 bits (B13 to B8) define the register address which has to be written respectively read, as shown in Figure 24.

Figure 24:
SDI Command Structure

B13	B12	B11	B10	B9	B8	Read/Write Register
0	0	0	0	0	0	R0
0	0	0	0	0	1	R1
0	0	0	0	1	0	R2
0	0	0	0	1	1	R3
0	0	0	1	0	0	R4
0	0	0	1	0	1	R5
0	0	0	1	1	0	R6
0	0	0	1	1	1	R7
0	0	1	0	0	0	R8
0	0	1	0	0	1	R9
0	0	1	0	1	0	R10
0	0	1	0	1	1	R11
0	0	1	1	0	0	R12
0	0	1	1	0	1	R13

The last 8 bits are the data that has to be written respectively read. A CS toggle high-low-high terminates the command mode.

If a direct command is sent (B15-B14=11) the bits from B13 to B8 defines the direct command while the last 8 bits are omitted. The Figure 25 shows all possible direct commands:

Figure 25:
List of Direct Commands

COMMAND_MODE	B13	B12	B11	B10	B9	B8
clear_wake	0	0	0	0	0	0
reset_RSSI	0	0	0	0	0	1
trim_osc	0	0	0	0	1	0
clear_false	0	0	0	0	1	1
preset_default	0	0	0	1	0	0

All direct commands are explained below:

- clear_wake: clears the wake state of the chip. In case the chip has woken up (WAKE pin is high) the chip is set back to listening mode.
- reset_RSSI: resets the RSSI measurement.
- trim_osc: starts the trimming procedure of the internal RC oscillator (see Figure 46).
- clear_false: resets the false wake-up register (R13<7:0>=00).
- preset_default: sets all register in the default mode, as shown in Figure 20.

Writing of Data to Addressable Registers (WRITE Mode). The SDI is sampled at the falling edge of SCLK (as shown in the following diagrams).

A CS toggling high-low-high indicates the end of the WRITE command after register has been written. The following example shows a write command.

Figure 26:
Writing of a Single Byte (falling edge sampling)

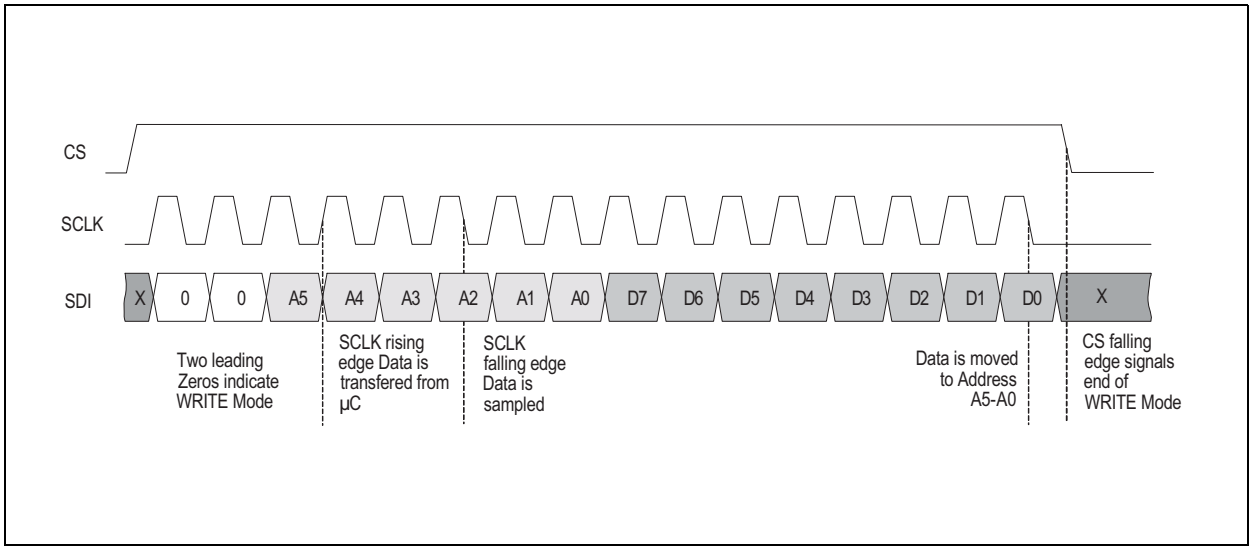
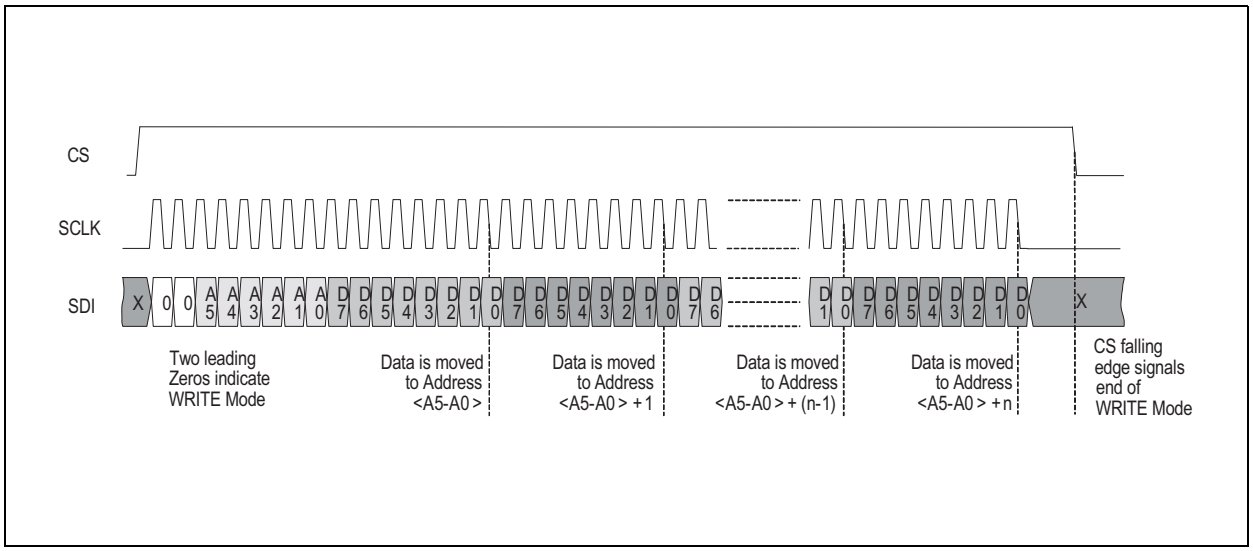


Figure 27:
Writing of Register Data with Auto-incrementing Address



Reading of Data from Addressable Registers (READ Mode)
Once the address has been sent through SDI, the data can be fed through the SDO pin out to the microcontroller.

A CS LOW toggling high-low-high has to be performed after finishing the read mode session, in order to indicate the end of the READ command and prepare the Interface to the next command control Byte.

To transfer bytes from consecutive addresses, SDI master has to keep the CS signal high and the SCLK clock has to be active as long as data need to be read.

Figure 28:
Reading of Single Register Byte

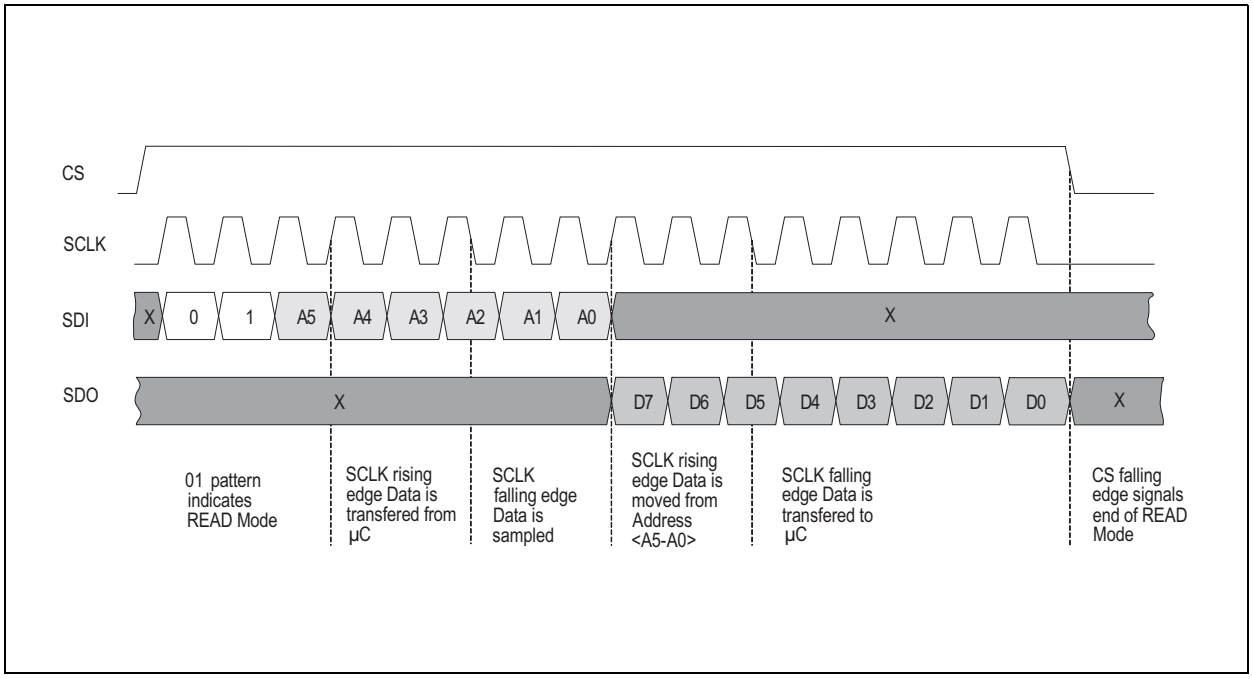
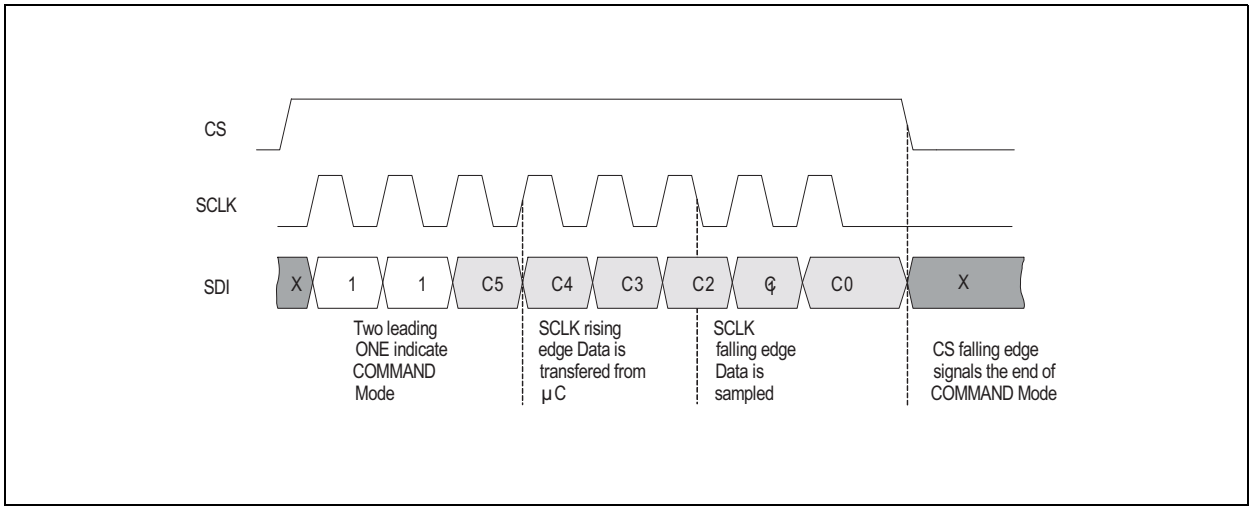


Figure 29:
Send Direct COMMAND Byte



SDI Timing

Figure 30:
SDI Timing Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TCSCLK	Time CS to Sampling Data		500			ns
TDCLK	Time Data to Sampling Data		300			ns
THCL	SCLK High Time		200			ns
TCLK	SCLK period		500			ns
TCLKCS	Time Sampling Data to CS down		500			ns
TCST	CS Toggling time		500			ns

Figure 31:
SDI Timing Diagram