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# AS3953B

## 14443 High Speed Passive Tag Interface

## General Description

The AS3953B NFC interface IC (NFiC) delivers low cost, ultra low power NFC forum functionality to multiple different applications. The AS3953B is a analog front-end with integrated 14443A data framing and SPI interface. It is designed to create a fast data link between an ISO 14443A reader device (PCD) and a microcontroller. The AS3953B is **passively powered** meaning that it can be supplied from the PCD magnetic field, eliminating the need of a continual external supply. This makes the AS3953B perfect for wireless communication to a low-power battery powered device.

The AS3953B is used with an appropriate antenna coil connected to the terminals LC1 and LC2, and behaves as a normal passive ISO 144443A tag (PICC). After the anti-collision protocol is passed, the PCD sends a **Wake-Up** command, which wakes up the microcontroller by sending an interrupt. From this point onwards, the AS3953B serves as a data link between the microcontroller and the PCD. AS3953B can also operate as NFCIP-1 target at 106kbit/s.

The AS3953B includes an onboard EEPROM that can be accessed either from the PCD or from the microcontroller via the SPI interface. This built-in flexibility makes it ideal for two types of applications:

- Where personalization data is programmed by the PCD (even in case the SPI side is not powered) and it is later read by microcontroller through SPI interface.
- Where log data is stored periodically by the microcontroller and can then be read by the PCD even when the microcontroller is not powered.

A regulated power supply voltage extracted from the PCD field is also available on a pin and can be used as power supply for external circuitry. For example, an external microcontroller and a sensor could be powered from the PCD field combined with pass through data rates up to 848kbit/s, which means the AS3953B is ideal for contactless passive programming of MCU systems. The AS3953B can also operate as a stand-alone ISO 14443A tag.

The AS3953B supports ISO 14443A up to Level-4, meaning a contactless smart card or an NFC forum compatible tag (Tag Type 4) can be built. Having a NFC Forum compatible tag interface allows the AS3953B to be used in an application where a standard NFC enabled phone is used as a PCD.

*Ordering Information and Content Guide appear at end of datasheet.*

## Key Benefits & Features

The benefits and features of AS3953B,14443 High Speed Passive Tag Interface are listed below:

**Figure 1:**
**Added Value of Using AS3953B**

| Benefits | Features |
|---|---|
| • NFC Forum compliance for full interoperability | • ISO 14443A compliant to Level-4 |
| • Data rate transmission up to the maximum allowed by ISO 14443A compliance | • Bit rates from 106 kbit/s till 848 kbit/s<br>• 7 byte UID |
| • ECMA-340 / ISO/IEC_18092 compliance | • NFCIP-1 target at 106 kbit/s |
| • Internal user memory for standalone application | • 1k bit EEPROM (108 bytes of user memory) |
| • Allows zero-power standby | • Configurable wake-up interrupt (after tag is selected or using proprietary command) |
| • Enables long battery life time, or battery-less designs | • Powered from external magnetic field with the possibility to draw up to 5mA |
| • Allows supply of external circuitry | • User configurable regulated voltage extracted from external magnetic field |
| • Easy and fast antenna design and impedance matching | • Integrated resonant capacitor |
| • Guarantees no reset during reader (PCD) modulation | • Integrated buffer capacitor |
| • Design flexibility, easy integration.<br>• Fits requirements for various embedded applications and manage of external microcontroller | • 4-wire Serial Peripheral Interface (SPI) with 32 byte FIFO |
| • Fits supply requirements for various applications, including industrial | • Wide SPI power supply range (1.65V to 3.6V) |
| • Flexibility for wide range of applications | • Wide temperature range: -40°C to 85°C |
| • Small outline, compatibility to common inlay and card manufacturing lines, surface-mount assembly | • Available as sorted wafer and Thin Wafer Level Chip Scale Package |

## Applications

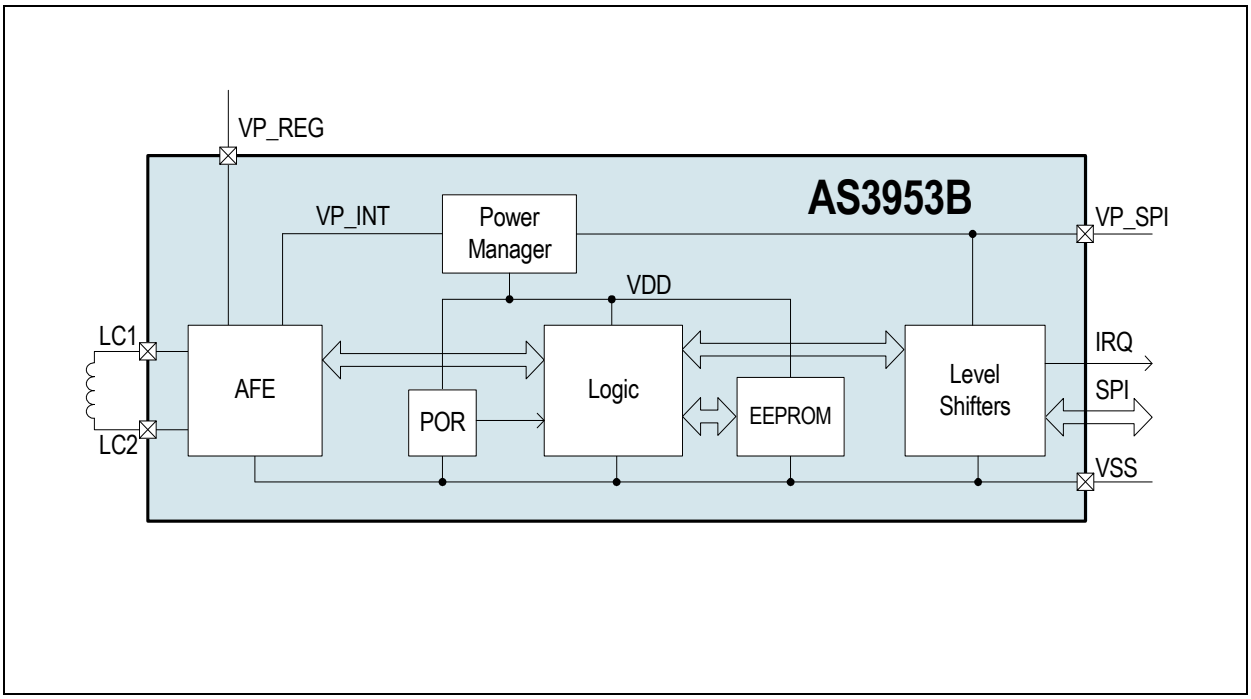
The device is ideal for applications like

- Passive wake-up
- Multipurpose HF interface to a controller
- Low power or passive programming
- Ultra low power data logger
- RFID programmable configuration EEPROM, ISO 14443A smart card, NFC Forum tag type 4
- Bluetooth and Wi-Fi pairing

## Block Diagram

The functional blocks of this device are shown below:

**Figure 2:**
**AS3953B Block Diagram**



## Pin Assignment

**Figure 3:**
**Pin Assignment (Bottom View)**

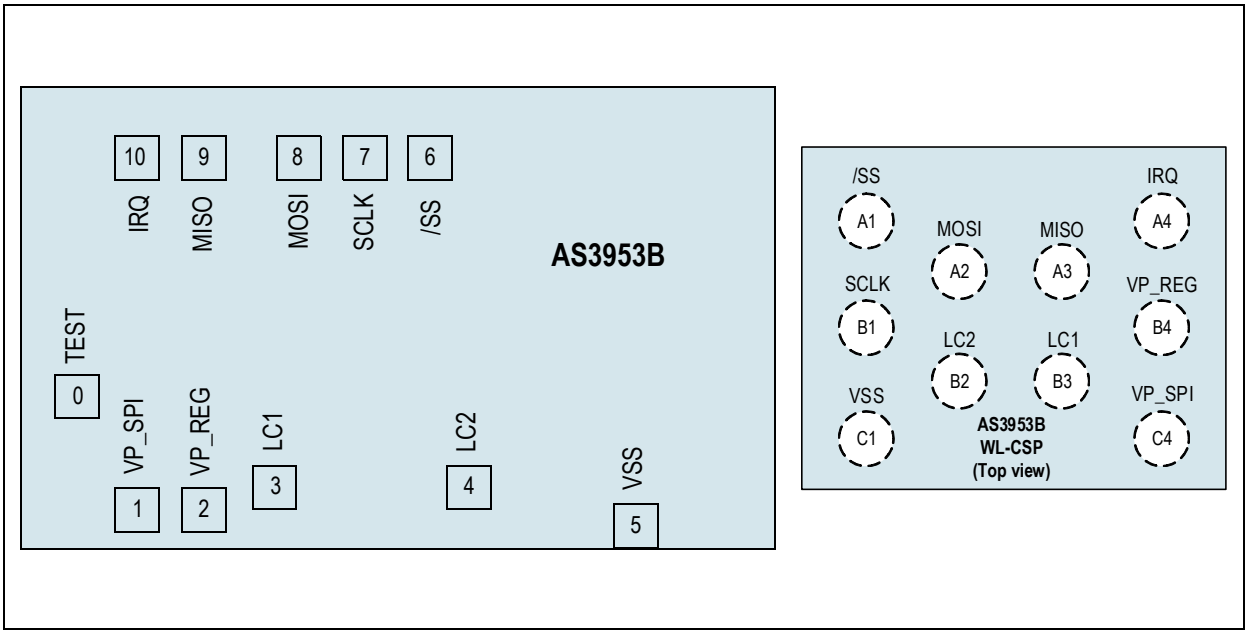



**Figure 4:**
**Pin Description**

| Pin Number Sorted Die | Pin Name | Pin Type | Description |
|---|---|---|---|
| 0 | TEST | Internal use | No connection |
| 1 | VP_SPI | Supply pad | Positive supply of SPI interface |
| 2 | VP_REG | Analog output | Regulator output |
| 3 | LC1 | Analog I/O | Connection to tag coil |
| 4 | LC2 | | |
| 5 | VSS | Supply pad | Ground, die substrate potential |
| 6 | /SS | Digital input | Serial Peripheral Interface enable (active low) |
| 7 | SCLK | | Serial Peripheral Interface clock |
| 8 | MOSI | | Serial Peripheral Interface data input |
| 9 | MISO | Digital output / tristate | Serial Peripheral Interface data output |
| 10 | IRQ | Digital output | Interrupt request output (active high) |
| - | Exposed Pad | Supply | Exposed pad to be connected to ground (optional) |

## Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**
**Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|---|
| **Electrical Parameters** | | | | | |
| $V_{DD}$ | DC supply voltage | -0.5 | 5 | V | |
| $V_{IN}$ | Input pin voltage except LC1 and LC2 | -0.5 | 5 | V | |
| | Input pin voltage pins LC1 and LC2 | -0.5 | 6.5 | V | |
| | Peak current induced on pins LC1 and LC2 | | 100 | mA | |
| $I_{scr}$ | Input current (latchup immunity) | -100 | 100 | mA | Norm: Jedec 78 |
| **Electrostatic Discharge** | | | | | |
| $ESD_{HBM}$ | Electrostatic discharge (human body model) | ±2 | | kV | Norm: MIL 883 E method 3015 |
| **Temperature Ranges and Storage Conditions** | | | | | |
| $T_{strg}$ | Storage temperature | -55 | 125 | °C | |
| $RH_{NC}$ | Relative humidity non-condensing | 5 | 85 | % | |
| MSL | Moisture sensitivity level | 1 | | | Maximum floor life time of unlimited hours |
| $t_{strg\_DOF}$ | Storage time for DOF/dies or wafers on foil | 3 | | months | Refer to indicated date of packing |
| $T_{strg\_DOF}$ | Storage temperature for DOF/dies or wafers on foil | 18 | 24 | °C | |
| $RH_{open\_DOF}$ | Relative humidity for DOF/dies or wafers on foil in open package | | 15 | % | Opened package |
| $RH_{Unopen\_DOF}$ | Relative humidity for DOF/dies or wafers on foil in closed package | 40 | 60 | % | Unopened package |

## Electrical Characteristics

All in this specification defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

**Figure 6:**
**Operating Conditions**

| Symbol | Parameter | Min | Typ | Max | Units | Note |
|---|---|---|---|---|---|---|
| $I_{lim}$ | Limiter current | | | 30 | mA | Till this current limiter clamps VLC1-LC2 to 5.0V |
| $V_{VP\_SPI}$ | SPI power supply | 1.65 | | 3.6 | V | When logic powered from RFID interface |
| | | 1.8 | | 3.6 | V | When logic powered from VP_SPI interface |
| $T_{AMB}$ | Ambient temperature | -40 | | 85 | °C | |

## DC/AC Characteristics for Digital Inputs and Outputs

**Figure 7:**
**CMOS Inputs, Valid for Input Pins /SS, MOSI, SCLK**

| Symbol | Parameter | Min | Typ | Max | Units | Note |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High level input voltage | 0.7 * VP_SPI | | | V | |
| $V_{IL}$ | Low level input voltage | | | 0.3 * VP_SPI | V | |
| $I_{LEAK}$ | Input leakage current | | | 1 | µA | |

**Figure 8:**
**CMOS Outputs, Valid for Output Pins MISO, IRQ**

| Symbol | Parameter | Min | Typ | Max | Units | Note |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High level output voltage | 0.85 * VP_SPI | | | V | $I_{SOURCE}$ = 1mA VP_SPI = 3V |
| $V_{OL}$ | Low level output voltage | | | 0.15* VP_SPI | V | |
| $C_L$ | Capacitive load | | | 50 | pF | |
| $R_O$ | Output resistance | | 200 | 400 | Ω | |
| $R_{PD}$ | Pull-down resistance pad MOSI | | 10 | | kΩ | Pull-down can be enabled while MISO output is in tristate. The activation is controlled by register setting |

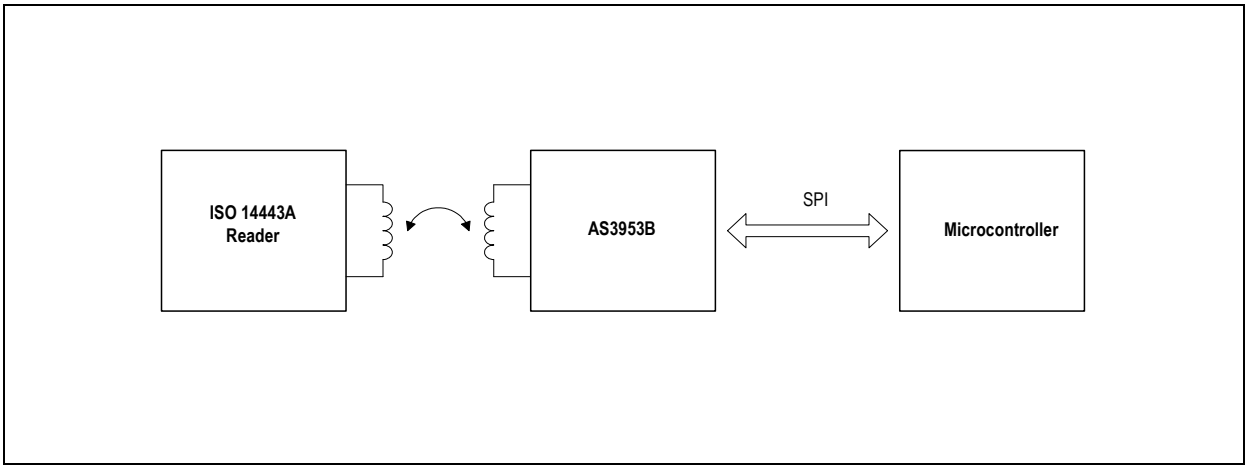
## Electrical Specification

**Figure 9:**
**VP_SPI = 3.0 V, Temperature 25°C (unless noted otherwise)**

| Symbol | Parameter | Min | Typ | Max | Units | Note |
|---|---|---|---|---|---|---|
| $I_{SB\_SPI}$ | Standby consumption on VP_SPI | | 65 | 100 | nA | @ 25°C; RF field not applied |
| | | 1.8 | 2.2 | 2.7 | µA | @ 25°C; RF field applied |
| $V_{LIM}$ | Limiter voltage | | 5.2 | 5.7 | V | $I_{LC}$ = 30mA (DC) |
| $I_S$ | Supply current | | 250 | | µA | Internal supply current measured in test mode on VREC, 13.56 MHz alternative pulses with amplitude 2Vpp, negative peak at VSS, forced to LC1 and LC2 |
| $V_{VP\_REG}$ | Regulated supply voltage | 1.65 | 1.8 | 2.01 | V | Set to 1.8V in EEPROM Configuration word |
| $V_{HF\_PON}$ | HF_PON threshold (rising VREG) | | 2.3 | | V | Guaranteed by design only |
| $V_{POR\_HY}$ | HF_PON hysteresis | | 0.8 | | V | |
| $V_{MOD}$ | Modulator ON voltage drop | | 1.2 | | V | $I_{LC}$ = 1mA |
| | | | 3.3 | | | $I_{LC}$ = 30mA |
| $C_R$ | Resonance capacitor | 25.2 | 28 | 30.8 | pF | Measured at 10MHz, 3.0Vpp (2.5Vpp) |
| $EE_{EN}$ | EEPROM endurance | 100000 | | | cycles | @ 125°C |
| $EE_{RET}$ | EEPROM retention | 10 | | | years | |

# Detailed Description

Figure 10:
System Block Diagram




## Circuit

The AS3953B is composed of ISO 14443A PICC Analog Front-end (PICC AFE), the ISO 14443A PICC Logic (PICC Logic), EEPROM, SPI Interface, Level Shifters and Power Supply Manager Block (Power Manager).

The PICC AFE is connected to an external tag coil, which forms together with integrated resonant capacitor an LC tank with a resonance at the external electromagnetic field frequency of 13.56 MHz. The PICC AFE has a built in rectifier and regulators. Output of internal regulator is called VP_INT. It is used to supply the PICC AFE and usually also the LOGIC and EEPROM (through Power Supply Manager). Output of external regulator VP_REG is available on a pin to supply some external circuitry.

Power Manager is controlling power supply of Logic and EEPROM. The two blocks can be supplied either from VP_INT or from VP_SPI (SPI power supply). In order to save current on VP_SPI, VP_INT is used as power supply whenever it is available. VP_SPI is only used when some activity is started over the SPI and the VP_INT is too low to be used as a power supply.

The PICC Logic is responsible for PICC-to-PCD communication up to the Level-4 (block transmission) of ISO 14443A. This means that anti-collision and other low-level functionality are implemented there.

The SPI Interface logic contains a 32 byte FIFO for block transmission data which is exchanged on Level-4 of ISO 14443A communication. It also contains some control and display registers.

The EEPROM is used to store the UID, the housekeeping data (configuration and control bits) and user data. It can be accessed from both sides (RFID and SPI).

## PICC AFE

Figure 11 depicts main PICC AFE building blocks.

The PICC AFE is connected to external tag coil, which together with the integrated resonant capacitor forms an LC tank with resonance at external electromagnetic field frequency (13.56 MHz). Figure 11 depicts the main PICC AFE building blocks.

**Rectifier**: Extracts DC power supply from AC voltage induced on coil terminals.

**Limiter**: Limits the maximum voltage on coil terminals to protect PICC AFE from destruction. At voltages that exceed limiter voltage it starts to absorb current (acts as some sort of shunt regulator).

**Modulator Switch**: Is used for communication PICC-to-PCD. When switched on, it will draw current from coil terminals. This mechanism is called load modulation. Variation of current in the modulator switch (ON and OFF state) is seen as modulation by the PCD.

**Demodulator**: Is used for communication PICC-to-PCD. It detects AM modulation of the PCD magnetic field. The demodulator is designed to accept modulation according to ISO 14443A; all standard bit rates from 106 kbit/s to 848 kbit/s are supported. The modulation for bit rate 106 kbit/s is 100%, whereas for other bit rates it may be less.

**Clock Extractor**: The clock extractor extracts a digital clock signal from the PCD carrier field frequency which is used as clock signal by logic blocks.

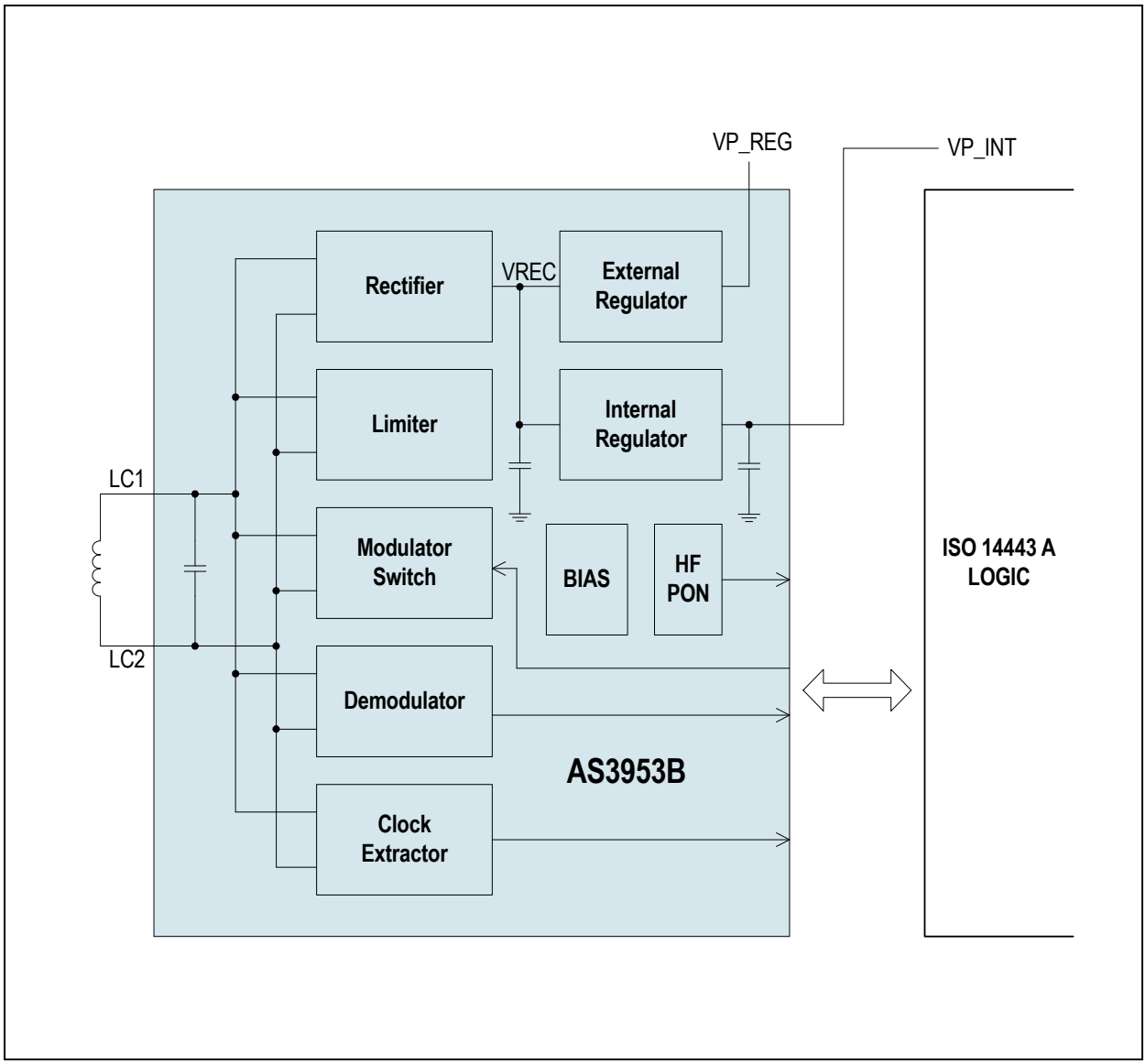
**HF_PON**: Observes rectified regulated voltage VREC. When the supply voltage is sufficiently high it enables operation of the PICC AFE and the digital tag logic. A buffer capacitor and HF_PON hysteresis guarantees that there is no reset during reader (PCD) modulation.

**Internal Regulator**: Provides regulated voltage VP_INT to the PICC AFE and in most cases also to EEPROM and logic blocks. Typical regulated voltage VP_INT is 2.0V. A buffer capacitor is also integrated.

**External Regulator**: Provides regulated voltage on external pin VP_REG where it can be used to supply some external circuitry. The regulated voltage and output resistance can be adjusted using EEPROM settings (see Figure 36). Appropriate external buffer capacitor is needed in case VP_REG is used in the application. The current to be provided depends on reader field strength, antenna size and Q factor, but it is limited to maximum 5mA.

**Bias**: Provides bias currents and reference voltages to PICC AFE analog blocks.

**Figure 11:**
**PICC AFE Block Diagram**



## Power Manager

Power manager is controlling the positive supply voltage of the PICC Logic, EEPROM and SPI Interface (VDD). Its inputs are VP_INT (rectified and regulated supply extracted from PCD field) and the VP_SPI (SPI power supply from external).

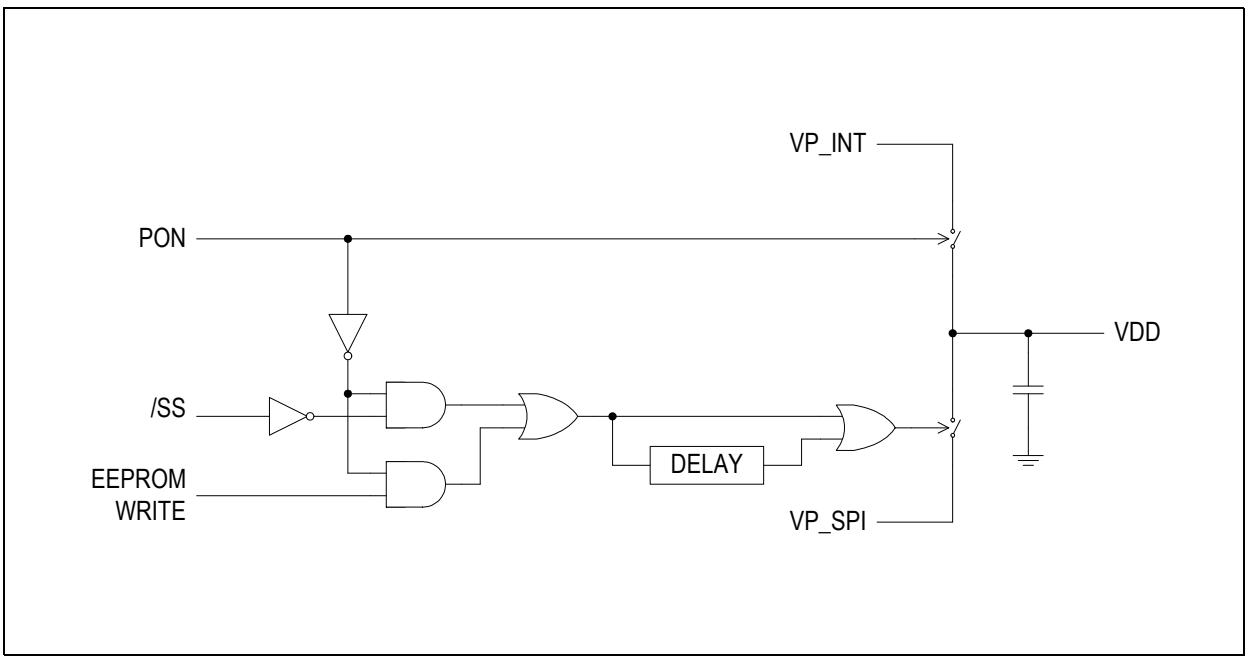
In standby mode, when the AS3953B is not in a PCD field (condition is that rectified supply voltage is below HF_PON threshold) and the SPI is not active (/SS is high) the VDD supply is disconnected not to consume on VP_SPI. The only consumption on VP_SPI is leakage of level shifters and SPI pins.

When the AS3953B is placed in a PCD field the VDD is connected to VP_INT. This happens once the VP_INT level is above the HF_PON threshold.

VP_SPI is connected to VDD only when the AS3953B is not in the PCD field (rectified supply voltage is below HF_PON threshold) and the SPI interface is activated by pulling /SS signal low. The switch to VP_SPI is controlled by /SS signal. The deactivation is delayed by 0.7ms min., thus the switch stays on in case the time between successive SPI activations is short. During EEPROM writing, which is activated over the SPI, the switch is also active.

At activation of the switch the time between the falling edge of /SS signal and rising edge of SCLK has to be at least 50µs to allow charging of internal VDD buffer capacitor and expiration of POR signal. Please note that the only SPI operations, which are allowed in this mode, are reading and writing of the EEPROM and registers.

**Figure 12:**
**Power Manager Concept**



## ISO 14443A Framing Mode

When Framing mode is selected the PICC logic performs receive and transmit framing according to the selected ISO 14443A bit rate.

During reception it recognizes the SOF, EOF and data bits, performs parity and CRC check, organizes the received data in bytes and places them in the FIFO.

During transmit, it operates inversely, it takes bytes from FIFO, generates parity and CRC bits, adds SOF and EOF and performs data encoding.

Default bit rate in the Framing mode is fc/128 (~106 kbit/s). Higher data rates may be configured by controller by writing the Bit Rate Definition Register.

In order to respect the PCD-to-PICC frame delay according to ISO14443-3 at data rate fc/128 bit the PICC logic synchronizes the response to the beginning of the next response window, but not earlier than window with n=9.

In this mode the EEPROM can be accessed via SPI when the RF field is active.

## ISO 14443A Level-4 Protocol Mode

When Level-4 Protocol mode is selected the PICC Logic autonomously execute complete ISO 14443A Level-3 communication and certain commands of Level-4. This also includes the anti-collision sequence during which the AS3953B UID number is read by the PCD (7 bytes UID is supported), the AS3953B is brought in the selected state (ISO14443-4) in which data exchange between the AS3953B and the PCD can start. On this level also a reading and writing of the AS3953B EEPROM is possible.

In case the configuration bit *irq_l4* is set an interrupt is automatically sent to controller once the PICC Logic enters in ACTIVE(*) state (after sending SAK on Cascade Level 2).

**Support of ISO 14443A Level-4**

ISO 14443A-4 commands **RATS**, **PPS** and **DESELECT** are implemented in the PICC Logic. **RATS** and **PPS** define communication parameters, which are going to be used in the following data exchange by using the block transmission protocol. The advantage of implementing *PPS* that defines the bit rate used for communication, is that all bit rate issues are handled by the PICC Logic. The MCU gets the information about the actual receive and transmit bit rate by reading a dedicated display register. It has to be fast enough to serve receive and transmit at the maximum bit rate.

Execution of the block transmission protocol is left to the controller. In case of receiving the block data from the PCD the PICC Logic provides support by detecting and removing start bit, stop bit, parity bits and CRC. Parity bits and CRC are also checked. When the block data is sent to the PCD the PICC Logic calculates and inserts start bit, parity bits, CRC and stop bit.

**DESELECT** puts the PICC Logic in HALT state. An interrupt is sent to controller upon reception of **DESELECT** command to inform it that PCD stopped the Level-4 communication.

Additionally to supporting the ISO14443-4 transmitting protocol the PICC Logic accepts also proprietary commands. Proprietary commands are identified by setting the two MSB bits of first transmitted byte to '01' (This combination is not used by ISO 14443A Level-4 protocol). The following custom commands are implemented:

- **Wake-Up:** Sends a wake-up interrupt to controller
- **Read EEPROM:** Reads data from EEPROM
- **Write EEPROM:** Writes data to EEPROM

**Support of ISO 14443A Optional Features**

- CID is supported
- NAD is not supported
- Historical bytes are not supported
- Power level indication is not supported

### *Coding of UID*

Anti-collision procedure is based on Unique Identification Number (UID). The AS3953B supports double UID size (7 bytes). First three bytes of UID are hard-wired inputs to the PICC Logic (*uid<23:0>*). Last 4 bytes of UID are stored in EEPROM UID word.

***First Byte of UID (uid0)***

First byte of UID is according to [ISO3] ISO/IEC 7816-6 IC Manufacturer ID. It is coded on bits *uid<7:0>*. **ams** IC Manufacturer ID is 3F(hex).

***Second Byte of UID (uid1)***

Second byte of UID – *uid<15:8>* is reserved for **ams** chip type (IC Type). Every **ams** RFID tag IC has its own chip type attributed. Therefore PCD which has read the RFID tag UID knows to which tag IC it is talking.

The AS3953B IC type is 10(hex).

***Third Byte of UID (uid2)***

Third byte of UID – *uid<23:16>* is set to 00(hex). Figure below defines the coding of the first three bytes of UID.

**Figure 13:**
**Coding of First Three Bytes of UID**

| UID Byte | FL Signal Name | Value (hex) |
|---|---|---|
| uid0 | uid<7:0> | 3F |
| uid1 | uid<15:8> | 10 |
| uid2 | uid<23:16> | 00 |

The last 4 bytes of UID are read from EEPROM (UID word).Figure below defines the last four bytes of UID.

**Figure 14:**
**Coding of Last Four Bytes of UID**

| UID Byte | UID Word Bits |
|---|---|
| uid3 | b7-b0 |
| uid4 | b15-b8 |
| uid5 | b23-b16 |
| uid6 | b31-b24 |

### *Coding of ATQA, SAK and ATS*

Several bits of responses ATQA, SAK and ATS are defined as "don't care" in the ISO 14443A standard. Some others are defined by optional choices in standard protocol. This section defines how these bits are set by the AS3953B.

### *ATQA*

ATQA is response to **REQA** and **WUPA** commands. Figure below defines the ATQA coding.

**Figure 15:**
**ATQA Coding**

| b16 | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | | | | | | | UID size | | | Bit frame anti-collision | | | | |

Bits *b16* to *b13* are RFU bits which must be set to '0'.

Bits *b12* to *b9* are proprietary coding and are set to '0'.

Bits *b8* and *b7* indicate double size UID.

Bit *b6* is 'RFU' bit and is set to '0'.

For bit frame anti-collision, the code 00100 is chosen.

**SAK**

SAK is response to **SELECT** command. AS3953B UID has double size, which defines SAK responses for Cascade Level 1 and Cascade Level 2.

**Cascade Level 1:** According to ISO 14443-3, all bits except *b3* are "don't care" for Cascade Level 1. Figure below defines Cascade Level 1 coding.

**Figure 16:**
**Cascade Level1 Coding**

| b8 MSB | b7 | b6 | b5 | b4 | b3 | b2 | b1 LSB | Description |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | As b6 in SAK CL2 | 0 | 0 | 1 | 0 | 0 | Cascade bit set: UID not complete |

Bit *b6* in Cascade Level 1 is always set as bit *b6* in Cascade Level 2. This is done in accordance to EMVCo Level – 1 Contactless Digital Test specifications.

**Cascade Level 2:** According to ISO 14443-3 all bits except *b6* and *b3* are "don't care" for Cascade Level 2.

If configuration *bit16 [nl4]* is set to logic '0' (default state), the SAK on Cascade Level 2 reports that tag is compliant to level4 (see figure below).

**Figure 17:**
**Cascade Level 2 Coding (ISO/IEC14443-4 compliant)**

| b8 MSB | b7 | b6 | b5 | b4 | b3 | b2 | b1 LSB | Description |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | UID complete, tag is compliant to ISO/IEC14443-4 |

If configuration *bit16 [nl4]* is set to logic '1', the SAK on Cascade Level 2 reports that tag is NOT compliant to Level-4 (see figure below).

**Figure 18:**
**Cascade Level 2 Coding (NOT ISO/IEC14443-4 compliant)**

| b8 MSB | b7 | b6 | b5 | b4 | b3 | b2 | b1 LSB | Description |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | UID complete, tag is **NOT** compliant to ISO/IEC14443-4 |

### ATS

ATS is response to ISO 14443-4 command **RATS**. The content of the ATS is used to inform the PCD about PICC capability (like the maximum frame size, support of higher bit rates, etc.)

Several response fields of ATS are stored in EEPROM configuration word. The AS3953B ATS is composed of following 5 bytes according to [ISO4]: TL, T0, TA(1), TB(1) and TC(1).

**TL:** This is the length byte. Since ATS is composed of 5 bytes, its content is 0x05. Figure below defines the coding of the TL byte.

**Figure 19:**
**TL Byte Coding**

| b8 MSB | b7 | b6 | b5 | b4 | b3 | b2 | b1 LSB | Description |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | Coding of ATS byte TL |

**T0:** This is the format byte. Figure below defines the coding of the T0 byte.

**Figure 20:**
**T0 Byte Coding**

| b8 MSB | b7 | b6 | b5 | b4 | b3 | b2 | b1 LSB | Description |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | fsci<3> | fsci<2> | fsci<1> | fsci<0> | Coding of ATS byte T0 |
| | TC(1) | TB(1) | TA(1) | FCSI | | | | |

Bit *b8* is set to '0'.

Bits *b7* to *b5* indicate presence of bytes TA(1), TB(1) and TC(1) and hence are all set to '1'.

Bits *b4* to *b1* are called FCSI and codes FCS. The FCS is maximum size of a frame defined by PICC. It is defined by configuration bits *fsci<3:0>*.

**TA(1):** This codes the bit rate capability of PICC. Supported higher bit rates of AS3953B are 212, 424 and 848 kbit/s. However in specific applications, it is advised to report lower capability to PCD (for example, due to the usage of slow controller or low power application). Due to this reason the TA(1) response is configurable using configuration bits.

**Figure 21:**
**TA(1) Byte Coding**

| b8 MSB | b7 | b6 | b5 | b4 | b3 | b2 | b1 LSB | Description |
|---|---|---|---|---|---|---|---|---|
| dr_sdr | dr_ picc_8 | dr_ picc_4 | dr_ picc_2 | 0 | dr_ pcd_8 | dr_ pcd_4 | dr_ pcd_2 | Coding of ATS byte TA(1) |
| | DS (PICC to PCD) | | | | DR (PCD to PICC) | | | |

Bit *b8* set to '0' codes possibility of having different data rates for each direction.

**TB(1):** The interface byte TB(1) conveys information to define the frame waiting time and the start-up frame guard time. The interface byte TB(1) consists of two parts:

- The most significant half-byte *b8* to *b5* is called FWI and codes frame waiting time (FWT).
- The least significant half byte *b4* to *b1* is called SFGI and codes a multiplier value used to define the SFGT. The SFGT defines a specific guard time needed by the PICC before it is ready to receive the next frame after it has sent the ATS. SFGI is coded in the range from 0 to 14. The value of '0' indicates 'No SFGT needed'.
- The SFGT bits are fixed to default value which is 0x0, while the FWI bits are defined by configuration bits *fwi<3:0>*. Figure below defines the coding of the TB(1) byte.

**Figure 22:**
**TB(1) Byte Coding**

| b8 MSB | b7 | b6 | b5 | b4 | b3 | b2 | b1 LSB | Description |
|---|---|---|---|---|---|---|---|---|
| fwi<3> | fwi<2> | fwi<1> | fwi<0> | 0 | 0 | 0 | 0 | Coding of ATS byte TB(1) |
| FWI | | | | SFGI | | | | |

- **TC(1):** The interface byte TC(1) specifies a parameter of the protocol. The interface byte TC(1) consists of two parts:
- The most significant bits *b8* to *b3* are set to 000000, all other values are 'RFU'.
- The bits *b2* and *b1* define which optional fields in the prologue field are supported by the PICC. The PCD is allowed to skip fields that are supported by the PICC. Bit *b2* indicates support of CID and *b1* indicates support of NAD. The AS3953B value is '10' indicating "CID supported" and "NAD not supported".

Figure below defines the coding of the TC(1) byte.

**Figure 23:**
**TC(1) Byte Coding**

| b8 MSB | b7 | b6 | b5 | b4 | b3 | b2 | b1 LSB | Description |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Coding of ATS byte TC(1) |
| | | | | | | CID | NAD | |

## Proprietary Commands

Proprietary commands have the same format as blocks defined in ISO 14443-4 with the difference that optional NAD field is abandoned since NAD is not supported by the AS3953B. The same format is used for commands sent by PCD and AS3953B responses. Figure below defines the coding of the Proprietary commands.

**Figure 24:**
**Proprietary Commands Coding**

| Prologue Field | | Information Field | Epilogue Field |
|---|---|---|---|
| PCB | [CID] | INF | EDC |
| 1 byte | 1 byte | | 2 bytes |

Prologue field consists of the mandatory Protocol Control Byte and an optional Card Identifier Byte. Card identifier byte is according to ISO 14443-4 definition. Epilogue field contains CRC over transmitted block.

**Prologue Field for Proprietary Commands**

Figure below defines the coding of Prologue field for Proprietary commands.

**Figure 25:**
**Prologue Field (proprietary commands)**

| Bit | Value | Function |
|---|---|---|
| b8 | 0 | 01 indicates proprietary command |
| b7 | 1 | |
| b6 | 0 | Shall be set to this value, other values are 'RFU' |
| b5 | 1 | |
| b4 | | CID following if bit is set to '1' |
| b3 | 1 | Shall be set to this value, other values are 'RFU' |
| b2 | 0 | |
| b1 | 1 | |

The following proprietary commands are implemented:

- **Wake-Up:** Sends a wake-up interrupt to controller
- **Read EEPROM:** Reads data from EEPROM
- **Write EEPROM:** Writes data to EEPROM

**Wake-Up Command**

Information field of **Wake-Up** command consists of one byte only (see figure below). The AS3953B echoes back the same information field.

**Figure 26:**
**Wake-Up Command**

| 01h |
|---|
| 1byte |

Figure below defines the coding of the AS3953B reply INF to **Wake-Up** command.

**Figure 27:**
**Wake-Up Reply**

| 01h |
|---|
| 1byte |

### Word Address Byte

Both proprietary commands related to EEPROM (Read and Write) use Word Address byte to define the address of EEPROM word that is accessed. Seven MSB bits of the Address Byte are used to define the address, while the last bit is "don't care".

**Note(s):** The valid range for the Word Address byte is from 0000 000xb to 0011 111xb (EEPROM words from 00h to 1Fh).

### Read EEPROM

The **Read EEPROM** command is used to read data from the EEPROM. The request information field contains the following three bytes:

- Command code byte (02h)
- Address of the first word to be read
- Number of words to be read

Figure below defines coding of **Read EEPROM** command information field.

**Figure 28:**
**Read EEPROM Command**

| 02h | Address of First Word to Be Read | Number of Words (≤ 8) to Be Read |
|---|---|---|
| 1byte | 1byte | 1byte |

If the request is normally processed, the reply information field contains the status word *90h* followed by the data. In case of error, the information field only contains the error status byte. The following rules apply:

- In case the number of words to be read is higher than 8, first eight words are read.
- In case the read protected word (its read lock bit is set) is accessed, an all '0' data is sent out.
- In case the reading starts at valid address and the number of words to read is such that the reading would be done beyond the EEPROM addressing space, all '0' data is returned for non-existing addresses.
- In case the reading starts at non-existing address, error information field is returned.

Figure below defines the coding of the AS3953B reply information field to **Read EEPROM** command, if command is normally processed.

**Figure 29:**
**Read EEPROM Reply (successful)**

| 90h | Data |
|---|---|
| 1byte | 4 to 32 bytes |

Figure below defines the coding of the AS3953B reply information field to **Read EEPROM** command, in case of an error.

**Figure 30:**
**Read EEPROM Reply (error code)**

| Information Field | Comment |
|---|---|
| 61h | Error (no diagnostic) |

**Write EEPROM**

The **Write EEPROM** command is used to write one EEPROM word (32 bits). The request information field contains 6 bytes:

- Command code byte (04h)
- Address of the word to be written
- Four bytes (32 bits) of data to be written

Figure below defines coding of **Write EEPROM** command information field.

**Figure 31:**
**Write EEPROM Command**

| 04h | Address of Word to Be Written | Data |
|---|---|---|
| 1 byte | 1 byte | 4 bytes |

The AS3953B reply contains one byte informing whether the writing of EEPROM was executed or whether there was an error. Prior to actual programming of data in EEPROM, the control logic checks whether there is enough power available. This is done by performing so called power check during which a dummy EEPROM programming is started. If the power check fails, EEPROM programming is not performed and an error code is sent. The EEPROM programming is a time consuming operation.

Therefore, if the EEPROM programming is executed, the AS3953B reply comes after 8ms typical. Figure below defines the coding of the AS3953B reply to **Write EEPROM** command.

**Figure 32:**
**Write EEPROM Reply**

| Information Field | Comment |
|---|---|
| 90h | Writing is normally processed |
| 61h | Writing is not done due to coding error (error in parity, CRC, nonexistent address…) |
| 62h | Writing is not done since the word is locked |
| 64h | Writing is not done due to power check fail |

### *Passing of Block Data to Controller*

After the PICC Logic has passed the anti-collision procedure and replied with SAK on Cascade Level 2 it passes in ACTIVE(*) state. On this level it expects that blocks received from the PCD have the format according to ISO 14443A-4. The ISO 144443A Logic recognizes the command by observing the first received byte. Based on content of this byte command is either processed by the AS3953B or the complete block data is put in the FIFO for further processing by the controller. The figure below displays the decision criteria.

**Figure 33:**
**First Byte of the ISO 14443-4 PCD Block**

| First Byte | Comment | Action of PICC Logic |
|---|---|---|
| 1110 0000 | RATS | Replies with ATS (1) |
| 1110 not(0000) | | Block is put in FIFO |
| 1101 xxxx | PPS | Replies with PPS response (second character is CID)(1) |
| 1100 x 010 | DESELECT | Replies and go to Halt |
| 1100 x not(010) | See note (2) | Block is put in FIFO |
| 1111 xxxx | WTX, S(PARAMETERS), RFU (1) | Block is put in FIFO since controller needs it to implement chaining |
| 01xx xxxx | Proprietary command | Proprietary command is processed |
| 00xx xxxx | I-block | Block is put in FIFO |
| 10xx xxxx | R-block | |

**Note(s):**

1. RATS and PPS are only processed by the AS3953B logic in case they are sent according to the ISO 14443-4 specification (RATS is first command sent after entry in ACTIVE(*) state, optionally followed by PPS). In case RATS or PPS are sent once the AS3953B logic is in PROTOCOL state the information received is saved into FIFO and not acted upon.
2. Compatible with old and new S(PARAMETERS) definition: Old: 1100 x000 is S(PARAMETERS) block according to the ISO 14443-4/AM2. **New**: 1111 x000 is S(PARAMETERS) block according to the modification SC17/WG8.

As shown in Figure 33, the block data is put in the FIFO whenever the two MSB bits are 00 or 10 and also in the case when the four MSB bits are 1111. Therefore the implemented communication between the PCD and a tag implemented by the AS3953B and a controller does not need to follow the Block transmission protocol defined in the ISO 14443-4.

### *Use of CID*

As mentioned above the AS3953B decides depending on content of the first byte of received message to either execute received message as a command or to put it in the FIFO. The second byte of the message comprises a CID number which is attributed by PCD. PCD will use CID number in case more PICCs are brought to Level-4 of communication at the same time.

CID is only checked for messages (commands) that are executed by the AS3953B. In case CID does not match such a command is rejected (no action is taken).

Messages that are based on first byte are put in FIFO and are not filtered by CID. It is left to controller to check for the CID and decide whether or not to reply (CID number is stored in the RATS Register).

## ISO 14443A Level-3 Protocol Mode

Level-3 Protocol mode is intended for implementation of custom protocols for which coding on Level-4 of ISO 14443A communication according to Figure 33 is not appropriate. In this mode Level-2 and Level-3 behavior of the PICC logic is identical to ISO 14443A Level-4 Protocol mode, while on Level-4 all received data blocks are put in FIFO.

In case the configuration bit *irq_l4* is set an interrupt is automatically sent to controller once the PICC Logic enters in ACTIVE(*) state (after sending SAK on Cascade Level 2).

In this mode the EEPROM can be accessed via SPI when the RF field is active.

## Transparent Mode

In the Transparent Mode the AS3953B logic is bypassed, AFE input and output signals are directly available on SPI interface pins when /SS signal is high.

- Modulator switch is controlled by pin MOSI (high is modulator on)
- Clock extractor output is sent to pin MISO
- Demodulator output is sent to pin IRQ

When /SS signal is low the SPI interface pins resume its normal functionality. In this mode the EEPROM can be accessed via SPI when the RF field is active.