Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AS3955

NFC Forum Compliant Dynamic Tag

General Description

AS3955 NFC Dynamic Tag IC is the ultimate solution to easily add NFC functionality to electronic devices. Thanks to a high sensitivity ISO14443A frontend and high integrated resonance capacitor, AS3955 offers standalone NFC passive tag functionality in a small footprint. Fast system integration and high speed data transfer are guaranteed by the available SPI and I^2C interfaces and by the optimized protocols (Tunneling Mode and Extended Mode), allowing bidirectional communication between the device microcontroller and an external NFC compliant device or ISO14443A reader device (PCD).

AS3955 is able to operate fully powered by the RF field, without any external supply. This, combined with an advanced energy harvesting feature, greatly increases battery life time or even allows battery-less designs.

AS3955 is used with an appropriate antenna coil connected to the terminals LC1 and LC2, and behaves as a standard passive ISO 14443A tag (PICC). After the anti-collision protocol stage, based on configuration, AS3955 can operate as a standalone NFC Forum Type 2 Tag or, when tunneling mode is activated, as a bridge between the PCD and the microcontroller, e.g. to emulate a custom or standard ISO14443A Level 3 or Level 4 PICC or a NFC Forum tag. A configurable wake-up signal notifies the microcontroller on ongoing RF activities, in order to minimize overall power consumption.

AS3955 includes an embedded EEPROM memory that can be accessed from the PCD through the RF link or from the microcontroller through the SPI or I^2C interfaces. Part or all memory can be protected by a 32-bit password, or permanently locked.

AS3955 supports ISO 14443A up to Level 4 and is designed according to EMVCo requirements, to enable the emulation of contactless smart cards or NFC Forum compliant Type 2 or Type 4 Tags.

AS3955 is designed for high reliability, and can operate in a wide power supply range from 1.65V to 5.5V, in a wide temperature range from -40 °C to 125 °C. EEPROM memory reaches automotive grade quality with endurance of 100,000 cycles and data retention of 10 years at 125 °C.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3955, NFC Forum Compliant Dynamic Tag are listed below:

Figure 1:
Added Value of Using AS3955

Benefits	Features
• NFC Forum compliance for full interoperability	• Type 2 Tag standalone functionality • Type 4 Tag emulation with external MCU
• NFC Forum compliance • ISO 14443A compliance up to Level 4	• Operating frequency at 13.56 MHz • Bit rate at 106 kbps • 7-byte UID
• Choice of memory size based on application	• 2 kbit EEPROM (216 bytes of user data) or • 4 kbit EEPROM (472 bytes of user data)
• Allows zero-power standby	• Configurable passive wake-up interrupt
• Enables long battery life time, or battery-less designs	• Energy harvesting to supply up to 5mA @ 4.5V (regulated)
• Allows fast antenna prototyping (ISO antenna classes 1 to 6)	• 45 pF integrated resonant capacitor
• Design flexibility, easy integration. Fits requirements for various embedded applications	• 3/4-wire SPI slave interface up to 5 Mbps • I^2C slave interface up to 1 Mbps
• Design flexibility, easy integration	• Programmable I^2C address
• Fits supply requirements for various applications, including industrial	• Wide interface supply range (1.65V to 5.5V)
• Support for multiple applications, and storage of sensitive data	• 32-bit password memory protection
• High performance and robust data communication, allows custom protocols to be implemented	• Tunneling and Extended modes for MCU communication
• Consistent NFC behavior of battery supplied devices in e.g. pairing applications	• Silent mode (MCU power status detection), configurable between 1.42V and 3.65V
• Possibility to disable RF communication	• Configurable Chip Kill mode
• Small outline, compatibility to common inlay and card manufacturing lines, surface-mount assembly	• Sawn wafer • WL-CSP package • 10-pin MLPD 3x3mm package

Applications

AS3955 is suited to a wide range of applications, including

- NFC connection handover (Bluetooth™, Bluetooth Low Energy, Wi-Fi pairing)
- Equipment setup, service and configuration
- Firmware upgrades
- Activity and status logging
- Wireless authentication (e.g. access control to buildings and equipment)

Typical Markets:

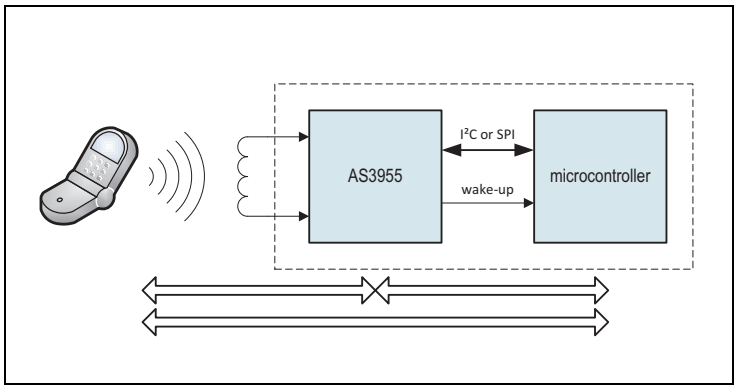
- EMV payment cards
- Consumer electronics, wearables and smart clothing
- Home appliances
- Automotive
- Industrial equipment and building automation
- Remote sensing
- Gaming

A typical system diagram is depicted in Figure 2.

At the presence of a 13.56 MHz field generated by a NFC device, AS3955 powers up, notifies the microcontroller through a wake-up signal and handles the tag activation sequence. Depending on configuration, several operations are then possible:

- AS3955 exchanges with the NFC device NDEF data stored in the internal EEPROM
- The microcontroller exchanges with the NFC device NDEF data stored in external memory
- The microcontroller exchanges data with AS3955. This operation can be performed concurrently with communication over the RF link, or also in absence of RF power, in presence of an external supply.

Figure 2:
Typical System Diagram



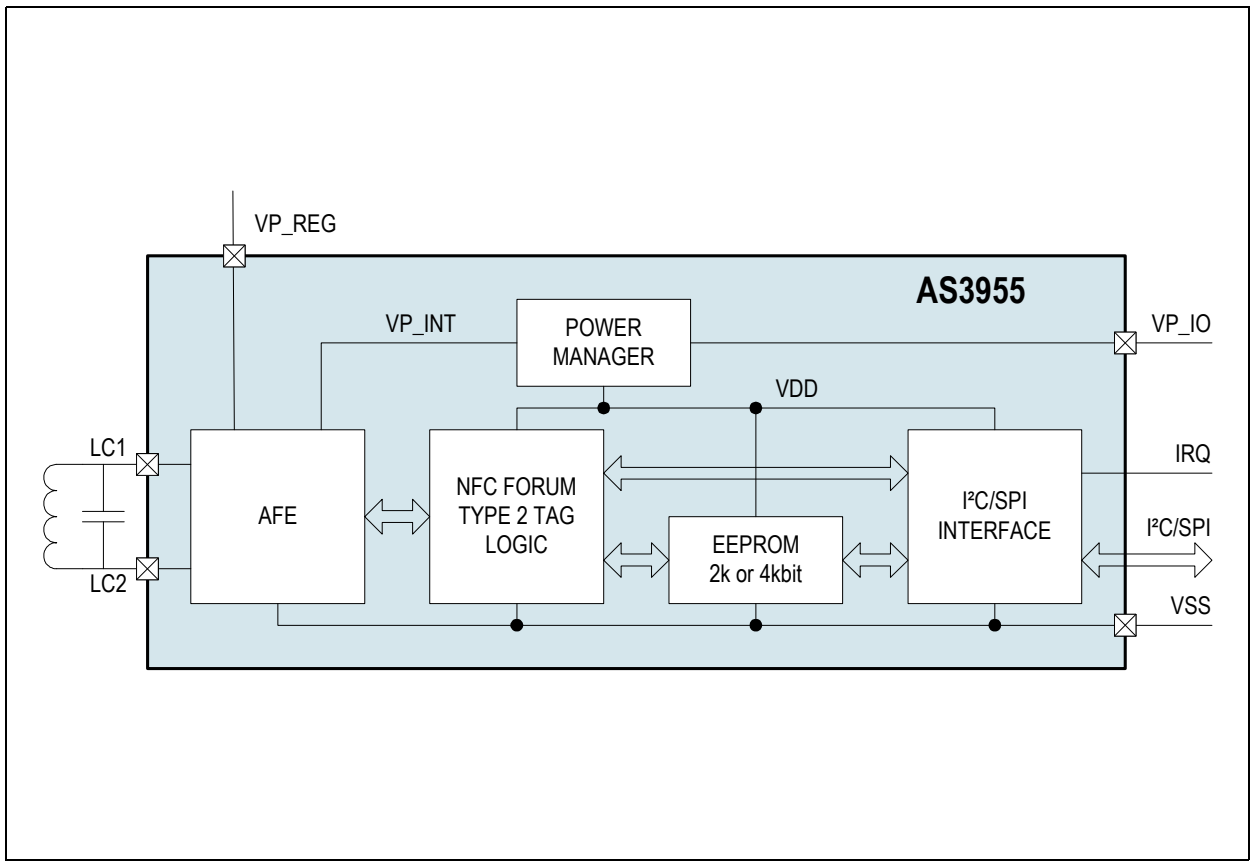
This built-in flexibility makes it ideal for a number of applications requiring non-volatile memory to be accessed when the system is not powered, e.g.:

- personalization data is programmed by the NFC device (even in case SPI / I^2C is not powered) and it is later read by microcontroller through SPI / I^2C interface
- Log data is stored periodically by the microcontroller and can then be read by the NFC device even when the microcontroller is not powered
- A NDEF message is regularly modified by the microcontroller (e.g. Bluetooth pin code, or Wi-Fi key, or dynamic URL) and it is later read by a NFC device.

Block Diagram

The functional blocks of this device are shown below:

Figure 3:
AS3955 Block Diagram



AS3955 is composed of NFC-A Analog Front End (AFE), NFC Type 2 Tag Logic, EEPROM, SPI / I^2C Interface and Power Supply Manager Block (Power Manager).

The AFE is connected to an external tag coil which forms, together with integrated resonant capacitor, a LC tank resonating with the external electromagnetic field frequency of 13.56 MHz. The AFE has built-in rectifier and regulators. The output of the internal regulator (VP_INT) is used to supply the AFE and also the Logic and EEPROM (through Power Supply Manager). A regulator output VP_REG is available on a pin to supply external circuitry by harvesting energy from the RF field.

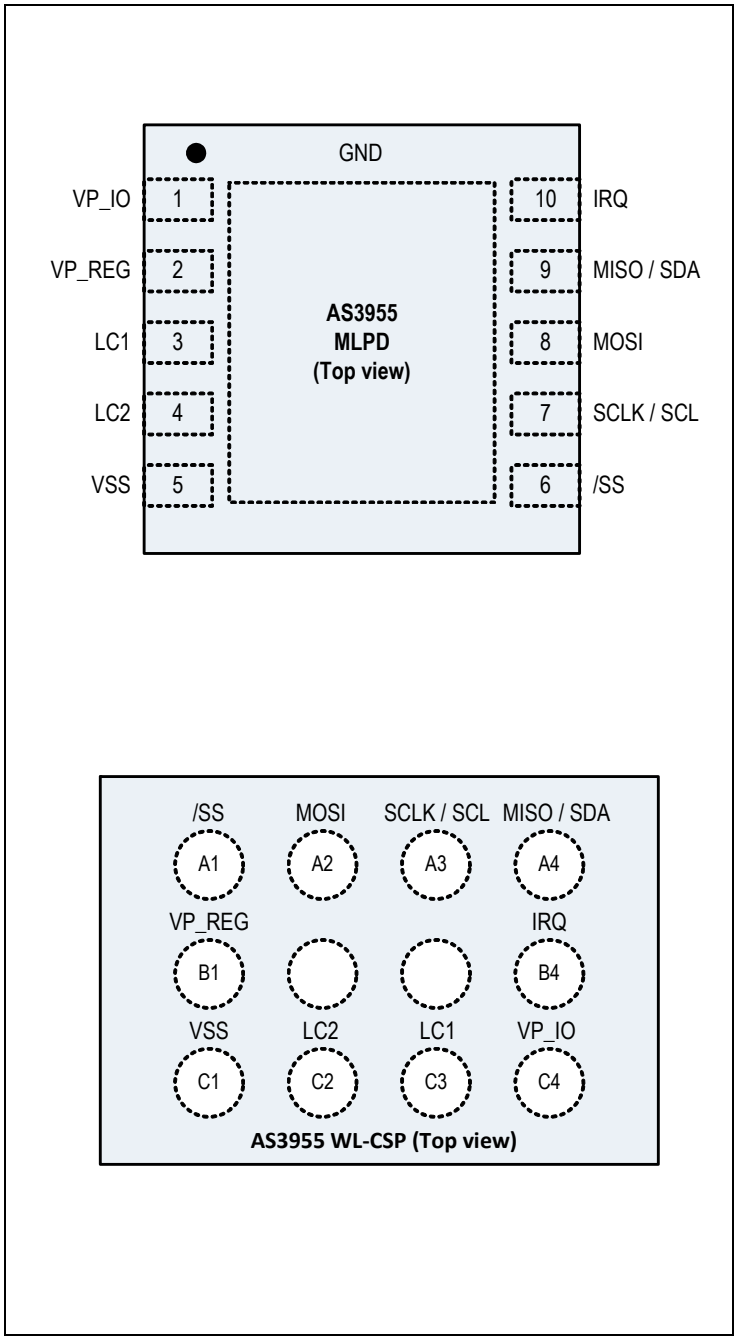
The Power Manager is controlling the power supply of Logic and EEPROM. The two blocks can be supplied either from VP_INT or from VP_IO (SPI / I^2C power supply) depending on the power mode of the chip. AS3955 offers a power mode where VP_IO supply is switched to VP_INT whenever the RF field is present. VP_IO is typically used when some activity is started over the SPI / I^2C and the VP_INT is too low to be used as a power supply.

The Logic is responsible for handling the anti-collision sequence, when acting as NFC Type 2 Tag, and other data transfer. The interface logic contains also a 32-byte buffer for block transmission between NFC device and AS3955.

The EEPROM is used to store the UID, configuration and control bits, and user data which can be accessed also via the SPI / I^2C.

Pin Assignment

Figure 4:
AS3955 Pin Diagram



Pin Description

Figure 5:
Pin Description

10-pin MLPD	10-pin WL-CSP	Die	Pin Name	Pin Type	Description
NA	NA	1	meas	Analog I/O	Analog test pin (1)
1	C4	2	VP_IO	Supply Pad	Positive supply of the interface / IC
2	B1	3	VP_REG	Analog Output	Regulator output
3	C3	4	LC1	Analog I/O	Connection to tag coil
4	C2	5	LC2		Connection to tag coil
5	C1	6	VSS	Supply Pad	Ground, die substrate potential
6	A1	9	/SS	Digital Input	SPI enable (active low) / I^2C interface enable
7	A3	10	SCLK / SCL		SPI / I^2C clock
8	A2	11	MOSI		SPI data input
9	A4	12	MISO / SDA	Digital Output / Tristate	SPI data output / I^2C data line
10	B4	13	IRQ	Digital Output	Interrupt request output (active high)

Note(s):

1. Pin *meas* is not bonded in MLPD package. It is only used during wafer sort test.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
VDD	DC supply voltage	-0.5	6.5	V	
V_{in}	Input pin voltage except LC1 and LC2	-0.5	6.5	V	
	Input pin voltage pins LC1 and LC2	-0.5	6.5	V	
	Peak current induced on pins LC1 and LC2		100	mA	
I_{scr}	Input current (latch-up immunity)	-100	100	mA	Norm: Jedec 78
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge HBM	±2		kV	Norm: MIL 883 E method 3015 (Human Body Model)
ESD_{CDM}	ESD – machine and charged device models	±500		V	
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-55	150	°C	
T_{body}	Package body temperature		260	°C	Norm: IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is matte tin (100% Sn).
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	3			Represents a max. floor life time of 168h

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Operating Conditions

All in this specification defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

Figure 7:
Electrical Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
I_{lim}	Limiter current		30	mA	
V_{VP_IO}	SPI power supply	1.65	5.5	V	When logic powered from RF interface
V_{VP_IO}	SPI power supply	1.65	5.5	V	When logic powered from VP_IO
T_{junc}	Junction temperature	-40	125	°C	

DC/AC Characteristics for Digital Inputs and Outputs

Figure 8:
CMOS Inputs

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{IH}	High level input voltage	0.7 * VDD_IO			V	
V_{IL}	Low level input voltage			0.3 * VDD_IO	V	
I_{LEAK}	Input leakage current			10	µA	@125°C

Note(s):

1. Valid for input pins /SS, MOSI and SCLK

Figure 9:
CMOS Outputs

Symbol	Parameter	Min	Typ	Max	Unit	Note
VOH	High level output voltage	0.85 * VDD_IO			V	Isource=1mA VP_IO = 5V
VOL	Low level output voltage			0.15 * VDD_IO	V	
RO	Output resistance		200	400	Ω	
RPD	Pull-down resistance pad MISO		10		kΩ	See note (1)

Note(s): Valid for output pins MISO and IRQ

1. Pull down can be enabled while MISO output is in tristate. The activation is controlled by register setting.

Electrical Specifications

Figure 10:
Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{SB_SPI}	Stand by consumption on VP_IO		65	100	nA	@ 25°C (RF field not applied)
V_{LIM}	Limiter voltage		5.2	5.5	V	I_{LC}=30mA (DC) (2)
I_S	Supply current		350		µA	See note (3)
V_{HF_PON}	HF_PON threshold (rising VREG)		1.6 2.3		V	See note (4)
V_{POR_HY}	HF_PON hysteresis		0.8		V	
V_{MOD}	Modulator ON voltage drop		1.2 2.6		V	I_{LC}=1mA (2) I_{LC}=30mA (2)
C_{RES}	Resonance capacitor		45		pF	
EE_{EN}	EEPROM endurance	100 000			cycles	@ 125°C (5)
EE_{RET}	EEPROM retention	10			years	@ 125°C (6)

Note(s):

1. VP_IO=1.8V, Temperature 25°C unless noted otherwise.
2. I_{LC} is the current flowing through LC1 and LC2 pins
3. Internal supply current measured over VP_IO pin, by forcing internal digital supply to 2.0V, and applying 13.56 MHz alternative pulses with amplitude 3.0Vpp to LC1 and LC2.
4. 1.6V is set in Power Mode 2 only.
5. See Figure 11.

6. See Figure 12.

Figure 11:
EEPROM Endurance Over Temperature

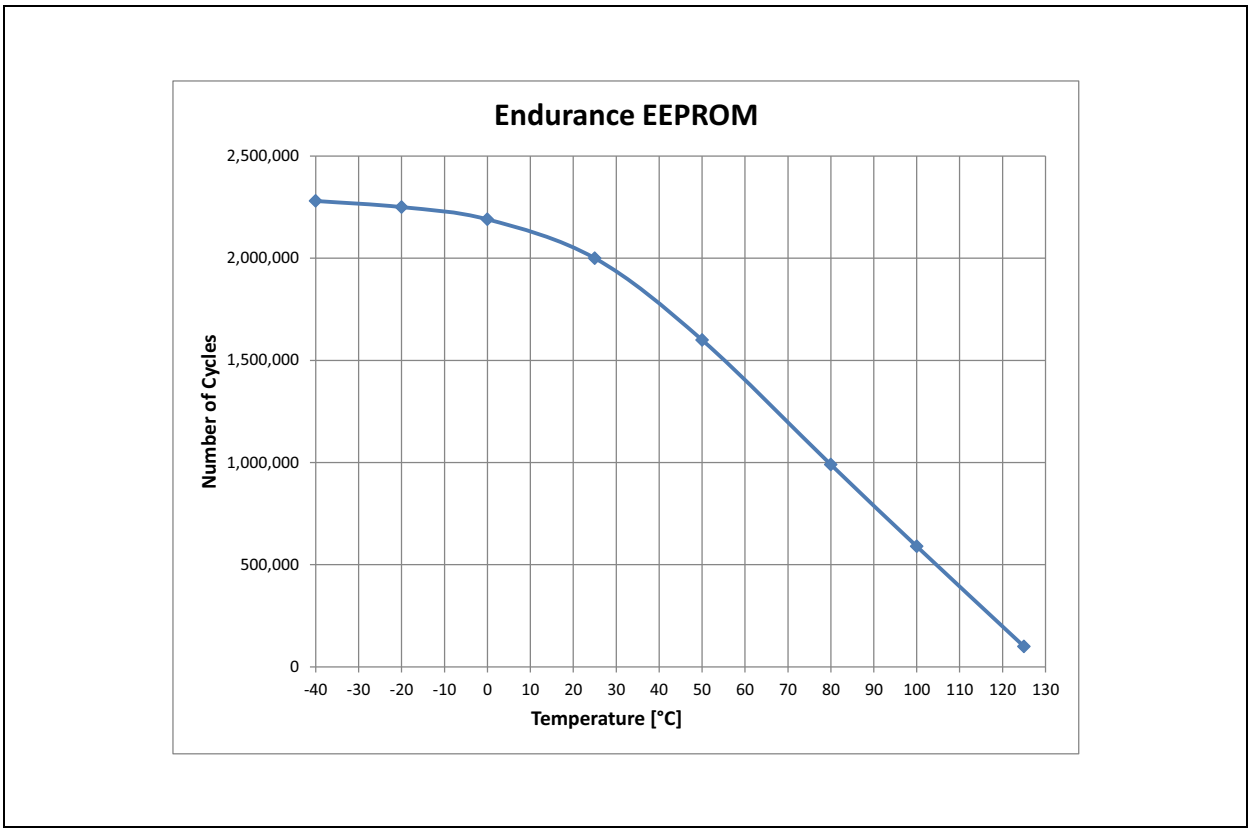
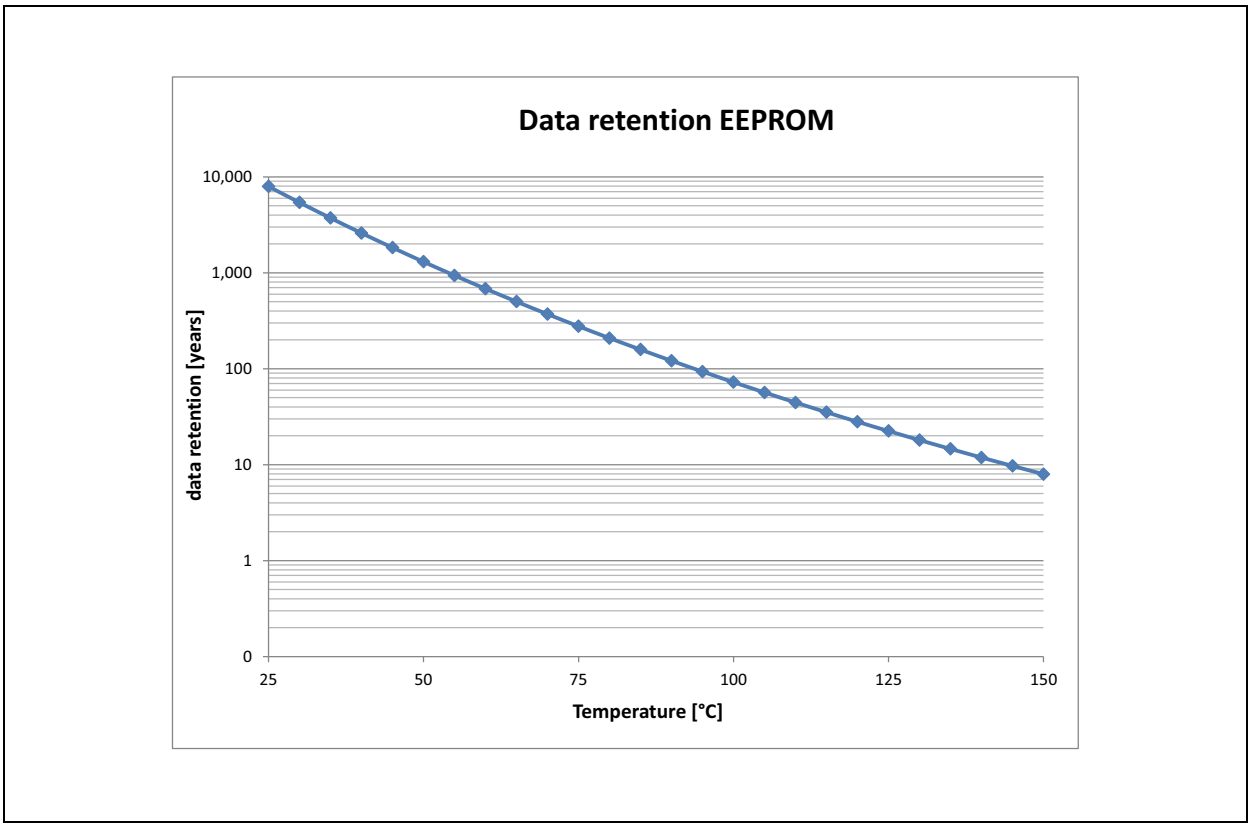


Figure 12:
EEPROM Data Retention Over Temperature

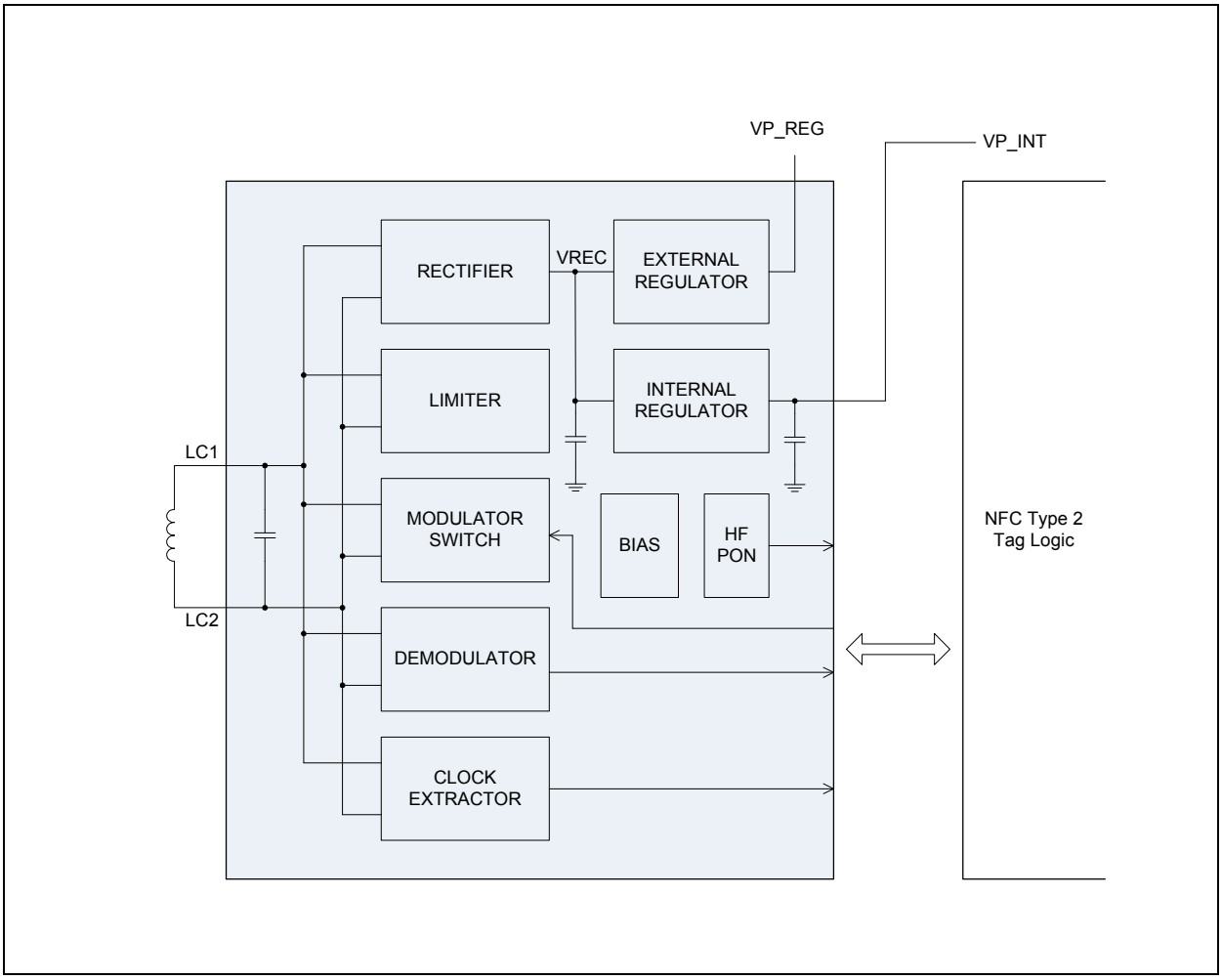


Detailed Description

Analog Frontend (AFE)

The AFE is connected to external tag coil, which together with the integrated resonant capacitor forms an LC tank resonating at the external electromagnetic field frequency (13.56 MHz). Figure 13 depicts the main AFE building blocks.

Figure 13:
PICC AFE Block Diagram



Rectifier extracts DC power supply from the AC voltage induced on coil terminals.

Limiter limits the maximum voltage on coil terminals to protect AFE from destruction. At voltages that exceed limiter voltage it starts to absorb current (acts as some sort of shunt regulator).

Modulator Switch is used for communication the NFC tag to a NFC device. When switched on it will draw current from coil terminals. This mechanism is called load modulation. Variation of current in the modulator switch (ON and OFF state) is seen as modulation by the NFC device.

Demodulator is used for communication NFC device to NFC tag. It detects AM modulation of the NFC device magnetic field. The demodulator is designed to accept modulation according to NFC-A specifications ([NFC Analog] [NFC Digital]).

Clock Extractor extracts a digital clock signal from the PCD carrier field frequency which is used as clock signal by logic blocks.

HF_PON enables operation of the AFE and the logic when the supply voltage is sufficiently high. A buffer capacitor and HF_PON hysteresis guarantee that there is no reset during NFC device modulation.

Internal Regulator provides regulated voltage VP_INT to the AFE and in most cases also to EEPROM and logic blocks. Typical regulated voltage VP_INT is 2.0V. A buffer capacitor is also integrated.

External Regulator provides regulated voltage on external pin VP_REG where it can be used to supply some external circuitry. The regulated voltage and output resistance can be adjusted using EEPROM settings. Appropriate external buffer capacitor is needed in case VP_REG is used in the application. Current which may be provided depends on reader field strength, antenna size and Q factor, but it is limited to maximum 5mA.

Bias provides bias currents and reference voltages to AFE analog blocks.

Power Management

AS3955 power management comprises of four different modes to fit requirements of different applications. AS3955 supports two power sources, whose activation depends on the selected power mode.

Power Mode 0

In this power mode, the Power Manager is controlling the supply of the PICC Logic, EEPROM and SPI / I^2C Interface (VDD). Its inputs are VP_INT (rectified and regulated supply extracted from RF field) and the VP_IO (supplied by external battery).

In standby mode, when AS3955 is not in the RF field (the condition is that rectified supply voltage is below HF_PON threshold) and the SPI / I^2C is not active (/SS is high), the VDD supply is disconnected. The only current consumption in this state is leakage on VP_IO, mainly due to level shifters and SPI / I^2C pins.

When AS3955 is placed in a RF field, VDD is connected to VP_INT. This happens once the VP_INT level is above the HF_PON threshold.

VP_IO is connected to VDD only when AS3955 is not in the RF field (rectified supply voltage is below HF_PON threshold) and the SPI / I^2C interface is activated by pulling /SS signal low. The switch to VP_IO is controlled by /SS signal. The deactivation is delayed by 0.7ms minimum, so that the switch shall stay closed in case of shorter times between successive SPI / I^2C activations. The switch is also closed during EEPROM writes activated over SPI / I^2C.

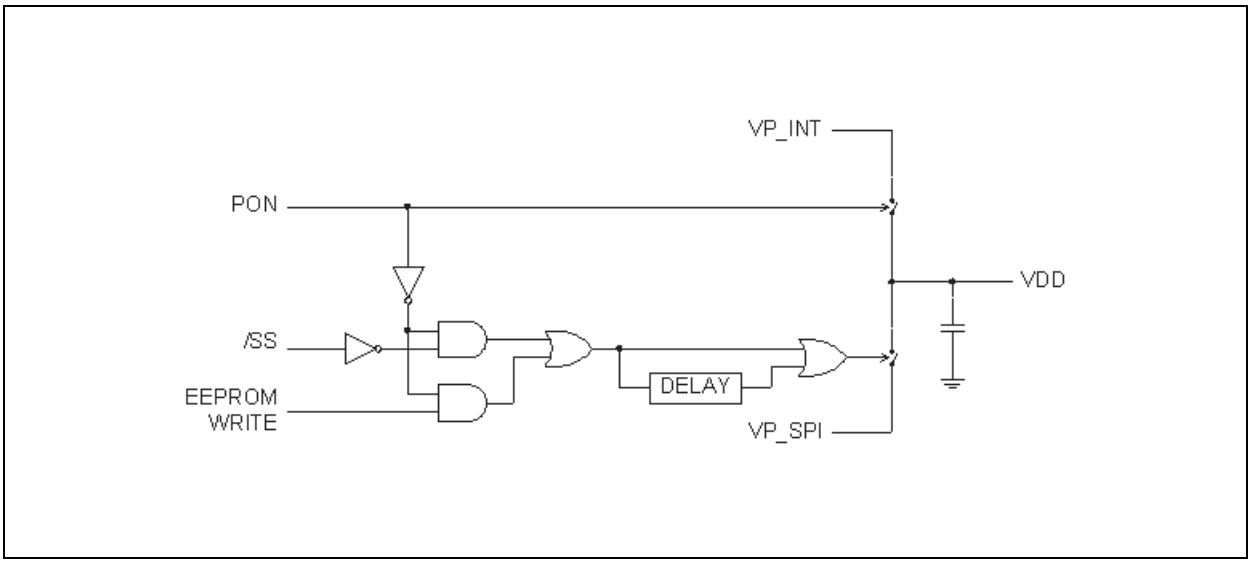
At activation of the switch, the time between the falling edge of the /SS signal and rising edge of SCLK shall be at least 300µs to allow charging of internal VDD buffer capacitor, expiration of POR signal and to perform a complete IC initialization. Please note that the only SPI / I^2C operations, which are allowed in this mode, are read and write of EEPROM and registers.

If the RF filed is lost during operation and the external system (MCU) is supplied over battery and /SS is low then power manager will automatically connect the VDD to VP_IO.

To enable low power mode where tag consumes less than 1uA at room temperature following conditions must be met:

- SPI interface configured
- All SPI interface input lines (including /SS) must be set to high
- All SPI output lines must be open

Figure 14:
Power Manager Concept



Power Mode 1

AS3955 is fully supplied by RF field. AS3955 checks if Extended or Tunneling mode are enabled. In this case, VP_REG supplies the system (SPI / I^2C pads, pull-ups, MCU), otherwise energy harvesting is turned off and VP_REG is set in tristate.

Such power mode can be used in battery-less systems where the system is fully powered by the RF field. In such configuration, the VP_REG output pin for energy harvesting and VP_IO input supply shall be externally connected. Battery, even when present, will not be involved.

If this power mode is enabled and neither tunneling nor extended mode are enabled, *rreg* value from IC Configuration Register 1 will be forced to zero. This will disable energy harvesting.

Power Mode 2

In this case, the external supply is used to provide power to digital blocks, EEPROM, SPI / I^2C pads and MCU. External supply VP_REG is not used. Since this mode can be enabled only after initialization of the chip, the /SS line must be either permanently set to low or pulled low for short time (400µs) to complete the initialization.

This mode is specifically designed to operate with AS392x products (**ams**' Active Boost). In this mode, the HF_PON threshold of the chip will be decreased so that it will operate with external voltage on LC pin in the range of 2.7-3.6Vpp.

If this mode is enabled, AS3955 will not be turned off as long as there is an external supply present.

Power Mode 3

In this case the external supply shall be used to provide power to digital blocks, EEPROM, SPI / I^2C pads and MCU. External supply VP_REG is not used. Since this mode can be enabled only after initialization of the chip, the /SS line must be either permanently set to low or pulled low for short time to complete the initialization.

In this mode, the HF_PON threshold of the chip is set so that it will operate with external voltage on LC pin in the range of 4.1-5Vpp.

If this mode is enabled, AS3955 will not be turned off as long as there is an external power present.

Interface Arbitration

Concurrent access to AS3955 internal EEPROM from RF or SPI / I^2C requires arbitration, to resolve conflicts or undesired behaviour.

AS3955 implements two arbitration modes, which can be set in Configuration Byte IC_CFG0.

Arbitration Mode 0

AS3955 arbitrates EEPROM write accesses according to first-come-first-serve principle.

- In case no write access is currently ongoing, both RF and SPI / I^2C interfaces are allowed to write into EEPROM.
- In case a write request comes over RF, while SPI / I^2C is writing, AS3955 will return a NAK.
- In case a write request comes over SPI / I^2C while RF is writing, AS3955 will trigger a I_err_acc interrupt (see Figure 94).

Arbitration Mode 1

AS3955 gives always priority to RF accesses. In this mode, AS3955 behaves over RF as a pure contactless tag.

- In case SPI / I^2C is performing a EEPROM write while the RF field is turned on, the write operation is interrupted to allow the initialization of the RF communication
- In case the RF field is already on and SPI / I^2C performs a write to EEPROM and a READ or WRITE command is received via RF, the write operation of SPI / I^2C is interrupted so that the RF operation can be performed

In both cases, a *I_err_acc* interrupt (see Figure 94) will be triggered.

Please note that the interruption of an EEPROM write may result in an undefined or "weak" state for the cell being programmed, and a second successful write attempt is suggested.

Energy Harvesting

AS3955 has energy harvesting capability. The regulated voltage output pin for energy harvesting is VP_REG. The energy harvesting is enabled only in Power Mode 0 and 1. Figure 16 shows settings of the regulated voltage output. The output can be set between 1.8V and 4.5V in 100mV step. The output voltage and resistance can be set by Configuration Byte IC_CFG1.The energy harvesting can be disabled by setting the output resistance register to 0 as shown in Figure 15.

Figure 15:
Output Resistance Settings

rreg<1:0>	Output Resistance	Comment
00b	X	Disabled – output pin is in tristate
01b	100Ω	
10b	50Ω	
11b	25Ω	

Figure 15 shows settings of the regulated voltage output. The output can be set between 1.8V and 4.5V in 100mV step.

Figure 16:
Regulated Voltage Output Settings

vreg<4:0>	Output Voltage	Abs. Accuracy
00000b	1.8V	±115mV
00001b : :	Step 100mV ±20mV	Linearly increasing over range
11011b	4.5V	±225mV

Silent Mode

The Silent mode enables detection of the power status of a circuit whose supply (Vdd) is connected to VP_IO pin. If this mode is enabled and the voltage measured on pin VP_IO is below the configured threshold value, the RF part of AS3955 will be disabled, and the IC will not be responsive to incoming commands. Silent mode settings can be performed by using Configuration Byte IC_CFG0.

This feature overcomes a potentially inconsistent behavior in a battery powered system, where a passive NFC tag can always communicate with a NFC device, also in case the battery is not sufficiently charged to supply the rest of the system. A typical example is when the NFC tag is used for Bluetooth pairing: AS3955 would trigger a pairing procedure only in case the system is fully operational by monitoring the supply voltage.

Memory Protection

AS3955 internal memory can be protected from unauthorized access by enabling password authentication. A 32-bit password can be set to protect the full user memory, or part of it, to allow the creation of a public data and a private data area. Password protection can be applied for read and write accesses.

Password authentication is performed through a standard WRITE command to the Authentication Password block. A maximum of 7 negative attempts are permitted before the chip is locked. Once authenticated, the user can modify the password.

Password protection applies to RF communication only.

Further information on how to handle password authentication can be found in Authentication Password, Configuration Byte AUTH_CFG, Configuration Byte AUTH_CNT and Configuration Byte AUTH_LIM.

Passive Wake-Up

AS3955 is able to operate NFC tag operations standalone and fully powered by the RF field. The connected MCU can remain is standby/sleep mode as long as its intervention is not required by the application, in order to save power. AS3955 can be configured to notify the MCU through a wake-up interrupt.

A number of triggering events can be selected, e.g.:

- Power up
- SELECTED state entered
- Reception of SLP_REQ command
- NFC device has updated memory content

For a complete interrupt source list, please refer to the section Interrupt Registers.

Chip Kill

Some applications require that the RF link is active only under certain conditions, e.g. during device configuration only in a controlled environment like a production facility.

AS3955 can be configured by the MCU in order to restrict the NFC device access to the system. By setting the Configuration Byte CHIP_KILL in EEPROM, the MCU can disable access to SPI / I^2C from the RF link (i.e. Tunneling and Extended mode are permanently disabled), or even disable RF communication completely. In the latter case, AS3955 will not respond to incoming RF commands.

This configuration can be modified only by the MCU through SPI / I^2C interfaces.

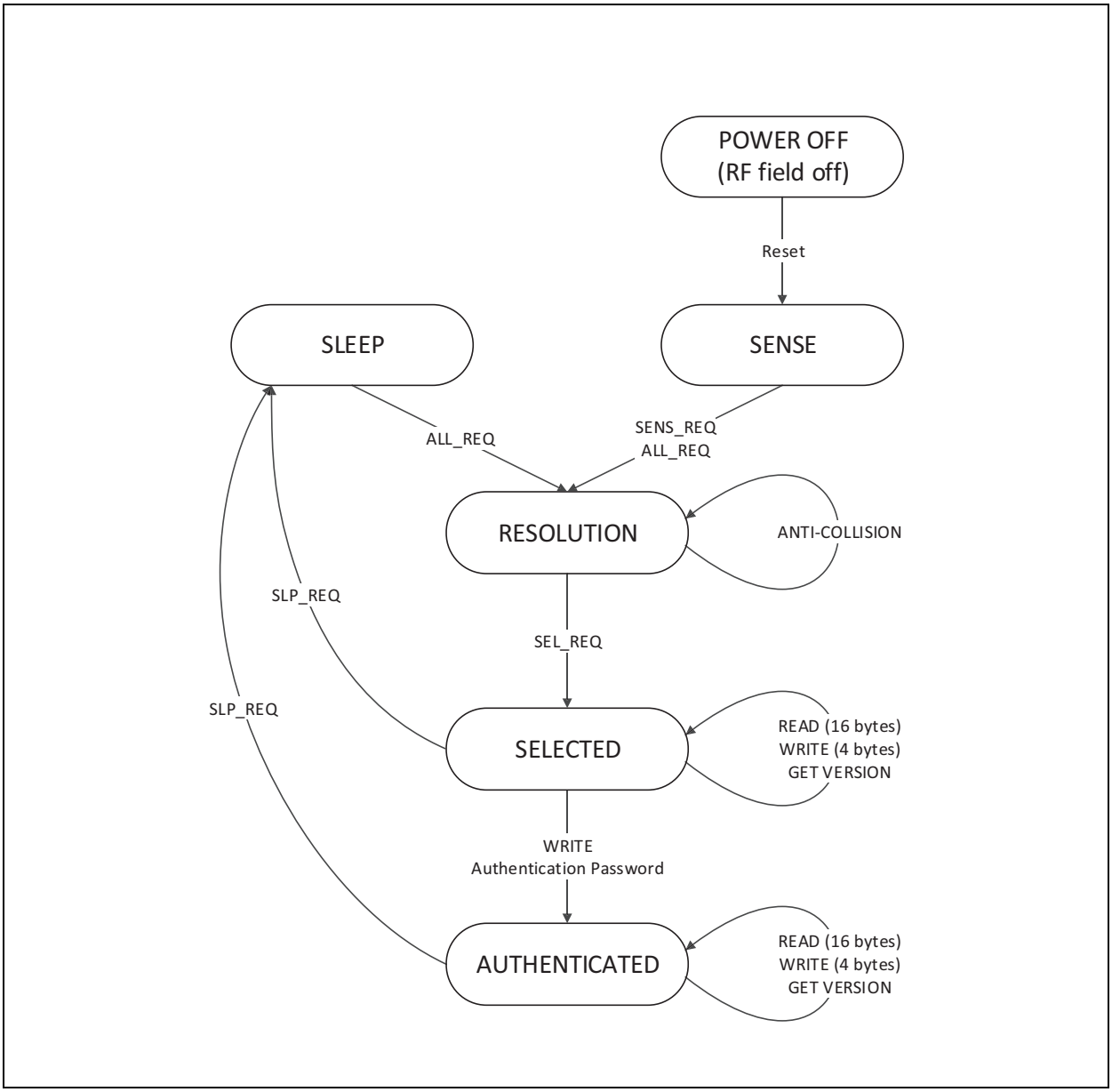
NFC Tag Functionality

Communication Principle

AS3955 autonomously executes complete NFC-A anti-collision communication sequence, during which the 7-byte UID is used ([NFC Analog] [NFC Digital]). After anti-collision, the NFC tag is brought into SELECTED state where read and write commands can be processed. The NFC tag will accept only read and write command issued to the address space actually available in AS3955 EEPROM. Any attempt to access an address outside the internal memory address space will be rejected. This default behavior of the NFC tag can be modified by enabling Tunneling or Extended mode.

A simplified AS3955 state diagram is shown in Figure 17.

Figure 17:
AS3955 State Diagram



SENSE State

After a power-on reset (POR), AS3955 switches to the SENSE state. This state is exited when a SENS_REQ or an ALL_REQ command is received from the NFC device. Any other data received while in this state is interpreted as an error and AS3955 remains in SENSE state.

When in SELECTED or AUTHENTICATED state, a correctly executed SLP_REQ command will modify the default waiting state from SENSE to SLEEP state. SLEEP state can be exited when an ALL_REQ command is received.

SLEEP State

Together with SENSE state, SLEEP state is the other waiting state for AS3955. SLEEP state can be entered upon reception of a SLP_REQ command. The distinction between SENSE and SLEEP state is made necessary to discriminate selected and not yet selected tags.

AS3955 can only exit this state upon reception of an ALL_REQ command. Any other command received in this state is interpreted as an error and AS3955 state remains unchanged.

RESOLUTION State

In RESOLUTION state, the NFC device is resolving the tag UID. Since AS3955 has a double size UID, the RESOLUTION state actually comprises of two sub-states, where the anti-collision procedure is carried out in Cascade Level 1 and 2. Please refer to [ISO18092] for further information.

SELECTED State

All memory operations are operated in SELECTED state.

Upon reception of a SLP_REQ command, SELECTED state is exited and AS3955 transits to SLEEP state. Any other command received when the device is in this state is interpreted as an error. Depending on its previous state, AS3955 returns to either SENSE or SLEEP state.

Upon reception of a SECTOR SELECT command, AS3955 returns a NAK and transits to SENSE or SLEEP state, depending on its previous state.

AS3955 transits to the AUTHENTICATED state after successful password verification, using a standard WRITE command to a dedicated memory address (see Authentication Password). The number of permitted failed authentications is set to 7, after which AS3955 transits to LOCKED sub-state (not shown in the picture). When LOCKED state is entered, only the MCU can bring AS3955 back to SENSE state by resetting the authentication counter (Configuration Byte AUTH_CNT) back to 0 and issue a Set Default, or Go To Sense, or Go To Sleep command.

When in LOCKED sub-state, all memory operations are only allowed in the memory area not password protected, as defined by the configuration byte Configuration Byte AUTH_LIM.

Upon reception of a SLP_REQ command, SELECTED state is exited and AS3955 transits to SLEEP state.

Any other command received when the device is in this state is interpreted as an error and, depending on its previous state, AS3955 returns to either SENSE or SLEEP state.

AUTHENTICATED State

In this state, all operations on memory blocks, which are configured as password verification protected, can be performed.

Upon reception of a SECTOR SELECT command, AS3955 returns a NAK and transits to SENSE or SLEEP state, depending on its previous state.

Upon reception of a SLP_REQ command, AUTHENTICATED state is exited and AS3955 transits to SLEEP state.

Any other command received when the device is in this state is interpreted as an error and, depending on its previous state, AS3955 returns to either SENSE state or SLEEP state.

NFC Forum Type 2 Tag Support

NFC Forum NFC-A commands ALL_REQ, SENS_REQ, SDD_REQ, SEL_REQ, SLP_REQ are required for anti-collision. Commands READ and WRITE are used for internal memory access. If NFC device issues a SECTOR SELECT command, AS3955 shall always reply with NAK.

Figure 18:
NFC-A vs ISO14443 Terminology

NFC-A Term	ISO14443 Term
States	
SENSE	IDLE
SLEEP	HALT
RESOLUTION	READY
SELECTED	ACTIVE
Commands / Responses	
SENS_REQ	REQA
ALL_REQ	WUPA
SENS_RES	ATQA
SSD_REQ	AC
SEL_REQ	SELECT
SLP_REQ	HLTA

UID Coding

Anti-collision procedure is based on the Unique Identification Number (UID). AS3955 supports double size UID (7 bytes). First three bytes of the UID are hardwired inputs to the PICC Logic (uid<23:0>). The last 4 bytes of the UID are stored in EEPROM UID block.

First UID Byte (uid0)

The first byte of UID is Manufacturer ID according to [ISO7816-6]. It is coded on bits *uid<7:0>*. **ams** IC Manufacturer ID is 3Fh.

Second UID Byte (uid1)

The second byte of UID (uid<15:8>) is reserved for **ams**' chip type (IC Type). Every **ams**' RFID tag IC has its own chip type assigned. AS3955 IC type is 14h.

Third UID Byte (uid2)

The third byte of UID (uid<23:16>) is set to 00h.

Figure 19:
Coding of First Three UID Bytes

UID Byte	Value (Hex)
uid0	3F
uid1	14
uid2	00

Last Four UID Bytes (uid3-uid6)

The last 4 bytes of UID are read from EEPROM (UID block) and pre-programmed during IC production. Those 4 bytes are unique, and cannot be modified.

Figure 20:
Last Four UID Bytes

UID Byte	UID Block Bits
uid3	b7-b0
uid4	b15-b8
uid5	b23-b16
uid6	b31-b24

Coding of SENS_RES, SEL_REQ, ACK and NACK

Several bits in certain responses are defined as don't-care in the NFC-A standard [NFC Digital], some others are defined by optional choices in standard protocol. This chapter defines how these bits are actually set in AS3955.

SENS_RES Response

SENS_RES is a response on ALL_REQ and SENS_REQ commands. The SENS_RES is defined by Configuration Bytes SENSR1 and SENSR2 stored in EEPROM.

Figure 21:
Coding of SENS_RES Response

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
SENSR2								SENSR1							

SEL_RES Response, Cascade Level 1 and 2

SEL_RES is the response to SEL_REQ command. Since AS3955 UID is double sized, SEL_RES responses for Cascade Level 1 and Cascade Level 2 are defined. SEL_RES on Cascade Level 1 and 2 is defined with Configuration Byte SELR except for cascade bit 3. The response on Cascade Level 2 is also configured by *selr_b6_inv* bit which, when set, inverts cascade bit 6 in SEL_RES response on Cascade Level 2 (see IC_CFG2).

Figure 22:
SEL_RES CL1 Coding

b8 MSB	b7	b6	b5	b4	b3	b2	b1 LSB	Description
sel_res<7:3>					1	sel_res<1:0>		Cascade bit set: UID not complete

Figure 23:
SEL_RES CL2 Coding

b8 MSB	b7	b6	b5	b4	b3	b2	b1 LSB	Description
sel_res<7:6>		sel_res<5>	sel_res<4:3>		0	sel_res<1:0>		selr_b6_inv set to 0
		NOT sel_res<5>						selr_b6_inv set to 1

Note(s):

1. According to [ISO14443-3], all bits except b3 are "don't care" for Cascade Level 1, and all bits except b6 and b3 are "don't care" for Cascade Level 2. Bit b6 in CL2 indicates whether the tag is compliant to [ISO14443] or not (resp. b6=1 and b6=0). In case of applications requiring EMVCo compliance, bit b6 in Cascade Level 1 shall be set as bit b6 in Cascade Level 2 ([EMVCO-1]).