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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AS3956

NFC Forum Compliant Dynamic Tag

General Description

AS3956 NFC Dynamic Tag IC is the ultimate solution to easily add NFC functionality to electronic devices. Thanks to a high sensitivity ISO14443A frontend and high integrated resonance capacitor, AS3956 offers standalone NFC passive tag functionality in a small footprint. Fast system integration and high speed data transfer are guaranteed by the available SPI and I^2C interfaces and by the optimized protocols (Tunneling Mode and Extended Mode), allowing bidirectional communication between the device microcontroller and an external NFC compliant device or ISO14443A reader device (PCD).

AS3956 is able to operate fully powered by the RF field, without any external supply. This, combined with an advanced energy harvesting feature, greatly increases battery life time or even allows battery-less designs.

AS3956 is used with an appropriate antenna coil connected to the terminals LC1 and LC2, and behaves as a standard passive ISO 14443A tag (PICC). After the anti-collision protocol stage, based on configuration, AS3956 can operate as a standalone NFC Forum Type 2 Tag or, when tunneling mode is activated, as a bridge between the PCD and the microcontroller, e.g. to emulate a custom or standard ISO14443A Level 3 or Level 4 PICC or a NFC Forum tag. A configurable wake-up signal notifies the microcontroller on ongoing RF activities, in order to minimize overall power consumption.

AS3956 includes an embedded EEPROM memory that can be accessed from the PCD through the RF link or from the microcontroller through the SPI or I^2C interfaces. Part or all memory can be protected by a 32-bit password, or permanently locked.

AS3956 supports ISO 14443A up to Level 4 and is designed according to EMVCo requirements, to enable the emulation of contactless smart cards or NFC Forum compliant Type 2 or Type 4 Tags.

AS3956 is designed for high reliability, and can operate in a wide power supply range from 1.65V to 5.5V, in a wide temperature range from -40°C to 125°C. EEPROM memory reaches automotive grade quality with endurance of 100000 cycles and data retention of 10 years at 125°C.

Ordering Information and Content Guide appear at end of datasheet.

Mandatory Documentation

Application Note AN02: Dual Interface Data Integrity

Key Benefits & Features

The benefits and features of AS3956, NFC Forum Compliant Dynamic Tag are listed below:

Figure 1:
Added Value of Using AS3956

Benefits	Features
• NFC Forum compliance for full interoperability	• Type 2 Tag standalone functionality • Type 4 Tag emulation with external MCU
• NFC Forum compliance • ISO 14443A compliance up to Level 3 - stand alone • ISO 14443A compliance up to Level 4 with ext. micro	• Operating frequency at 13.56 MHz • Bit rate at 106 kbps • 7-byte UID
• Choice of memory size based on application	• 4 kbit EEPROM (472 bytes of user data)
• Allows zero-power standby	• Configurable passive wake-up interrupt
• Enables long battery life time, or battery-less designs	• Energy harvesting to supply up to 5mA (regulated)
• Allows fast antenna prototyping (ISO antenna classes 1 to 6)	• 45 pF integrated resonant capacitor
• Design flexibility, easy integration. Fits requirements for various embedded applications	• 3/4-wire SPI slave interface up to 5 Mbps • I^2C slave interface up to 1 Mbps
• Design flexibility, easy integration	• Programmable I^2C address
• Fits supply requirements for various applications, including industrial	• Wide interface supply range (1.65V to 5.5V)
• Support for multiple applications, and storage of sensitive data	• 32-bit password memory protection
• High performance and robust data communication, allows custom protocols to be implemented	• Tunneling and Extended modes for MCU communication
• Consistent NFC behavior of battery supplied devices in e.g. pairing applications	• Silent mode (MCU power status detection), configurable between 1.42V and 3.65V
• Possibility to disable RF communication	• Configurable Chip Kill mode
• Small outline, compatibility to common inlay and card manufacturing lines, surface-mount assembly	• WL-CSP package • 10-pin MLPD 3mm x 3mm package

Applications

AS3956 is suited to a wide range of applications, including

- NFC connection handover (Bluetooth™, Bluetooth Low Energy, Wi-Fi pairing)
- Equipment setup, service and configuration
- Firmware upgrades
- Activity and status logging
- Wireless authentication (e.g. access control to buildings and equipment)

Typical Markets:

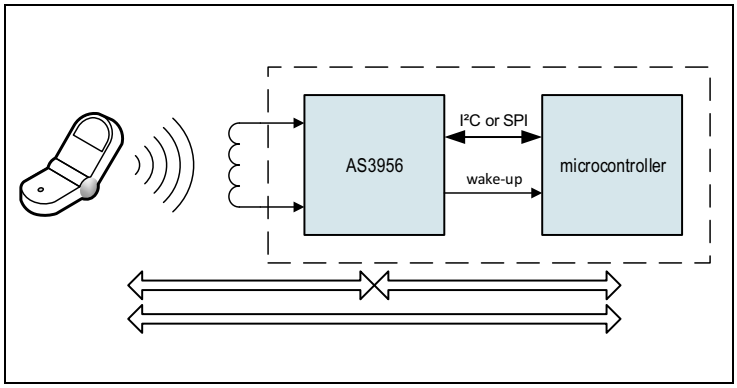
- EMV payment cards
- Consumer electronics, wearables and smart clothing
- Home appliances
- Automotive
- Industrial equipment and building automation
- Remote sensing
- Gaming

A typical system diagram is depicted in Figure 2.

At the presence of a 13.56 MHz field generated by a NFC device, AS3956 powers up, notifies the microcontroller through a wake-up signal and handles the tag activation sequence. Depending on configuration, several operations are then possible:

- AS3956 exchanges with the NFC device NDEF data stored in the internal EEPROM
- The microcontroller exchanges with the NFC device NDEF data stored in external memory
- The microcontroller exchanges data with AS3956. This operation can be performed concurrently with communication over the RF link, or also in absence of RF power, in presence of an external supply.

Figure 2:
Typical System Diagram



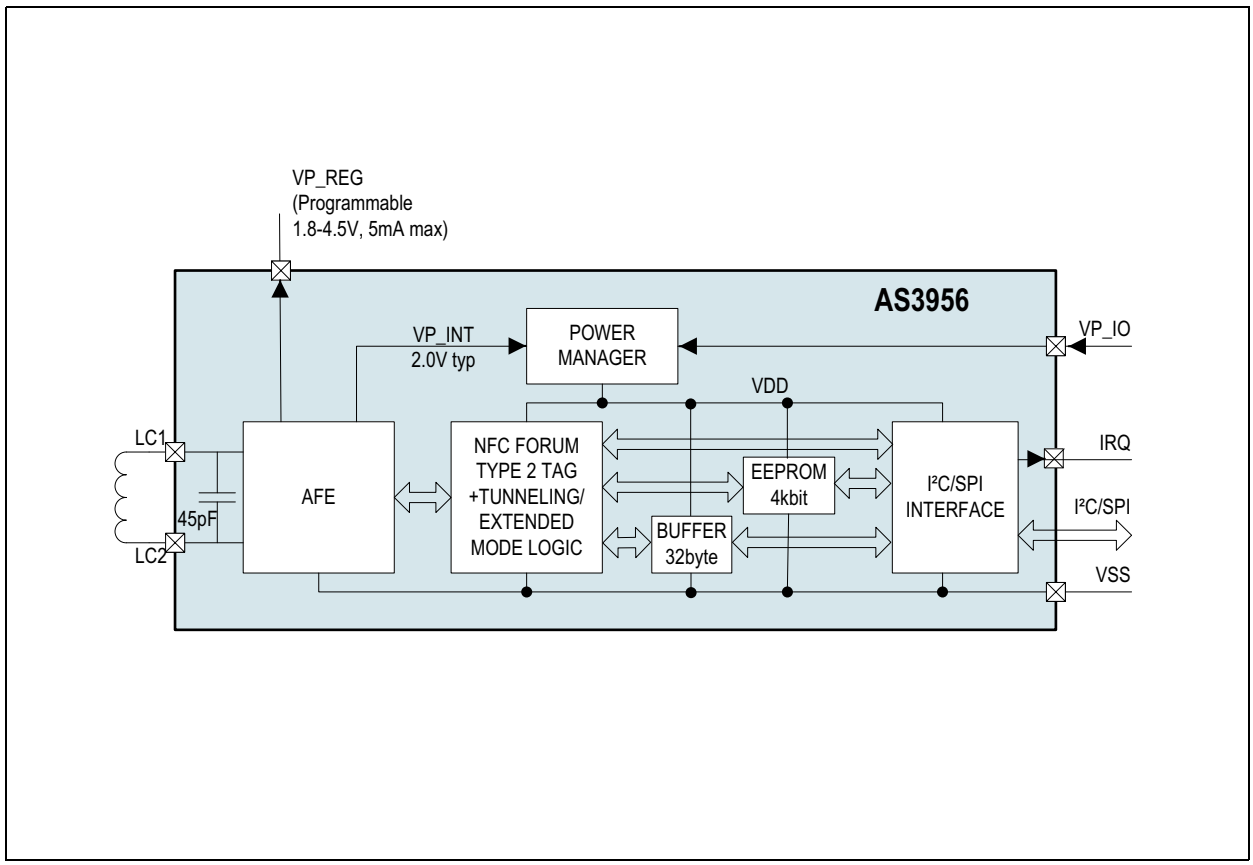
This built-in flexibility makes it ideal for a number of applications requiring non-volatile memory to be accessed when the system is not powered, e.g.:

- personalization data is programmed by the NFC device (even in case SPI / I²C is not powered) and it is later read by microcontroller through SPI / I²C interface
- Log data is stored periodically by the microcontroller and can then be read by the NFC device even when the microcontroller is not powered
- A NDEF message is regularly modified by the microcontroller (e.g. Bluetooth pin code, or Wi-Fi key, or dynamic URL) and it is later read by a NFC device.

Block Diagram

The functional blocks of this device are shown below:

Figure 3:
AS3956 Block Diagram



AS3956 is composed of NFC-A Analog Front End (AFE), NFC Type 2 Tag Logic, EEPROM, SPI / I^2C Interface and Power Supply Manager Block (Power Manager).

The AFE is connected to an external tag coil which forms, together with integrated resonant capacitor, a LC tank resonating with the external electromagnetic field frequency of 13.56 MHz. The AFE has built-in rectifier and regulators. The output of the internal regulator (VP_INT) is used to supply the AFE and also the Logic and EEPROM (through Power Supply Manager). A regulator output VP_REG is available on a pin to supply external circuitry by harvesting energy from the RF field.

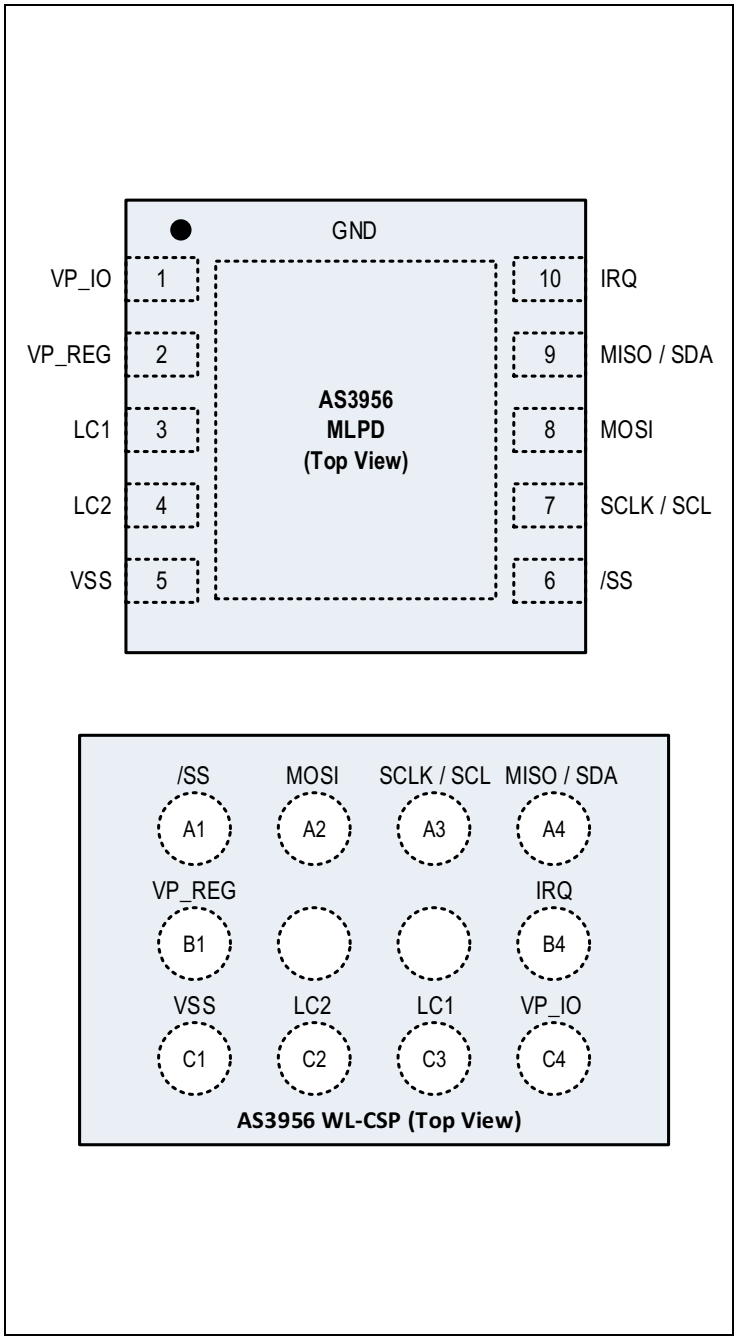
The Power Manager is controlling the power supply of Logic and EEPROM. The two blocks can be supplied either from VP_INT or from VP_IO (SPI / I^2C power supply) depending on the power mode of the chip. AS3956 offers a power mode where VP_IO supply is switched to VP_INT whenever the RF field is present. VP_IO is typically used when some activity is started over the SPI / I^2C and the VP_INT is too low to be used as a power supply.

The Logic is responsible for handling the anti-collision sequence, when acting as NFC Type 2 Tag, and other data transfer. The interface logic contains also a 32-byte buffer for block transmission between NFC device and AS3956.

The EEPROM is used to store the UID, configuration and control bits, and user data which can be accessed also via the SPI / I^2C.

Pin Assignment

Figure 4:
AS3956 Pin Diagram



Pin Description

Figure 5:
Pin Description

10-pin MLPD	10-pin WL-CSP	Die	Pin Name	Pin Type	Description
NA	NA	1	meas	Analog I/O	Analog test pin (1)
1	C4	2	VP_IO	Supply Pad	Positive supply of the interface / IC
2	B1	3	VP_REG	Analog Output	Regulator output
3	C3	4	LC1	Analog I/O	Connection to tag coil
4	C2	5	LC2		Connection to tag coil
5	C1	6	VSS	Supply Pad	Ground, die substrate potential
6	A1	9	/SS	Digital Input	SPI enable (active low) / I^2C interface enable
7	A3	10	SCLK / SCL		SPI / I^2C clock
8	A2	11	MOSI		SPI data input
9	A4	12	MISO / SDA	Digital Output / Tristate	SPI data output / I^2C data line
10	B4	13	IRQ	Digital Output	Interrupt request output (active high)

Note(s):

1. Pin *meas* is not bonded in MLPD package. It is only used during wafer sort test.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
VDD	DC supply voltage	-0.5	6.5	V	
V_{in}	Input pin voltage except LC1 and LC2	-0.5	6.5	V	
	Input pin voltage pins LC1 and LC2	-0.5	6.5	V	
	Peak current induced on pins LC1 and LC2		50	mA	
I_{scrLC}	Input current LC1, LC2 (latch-up immunity)	-50	50	mA	JEDEC JESD78D
I_{scr}	Input current other pins (latch-up immunity)	-100	100	mA	JEDEC JESD78D
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge HBM (all pins except VP_REG)	±2		kV	JEDEC JS-001-2014
ESD_{HBMREG}	Electrostatic discharge HBM (VP_REG pin only)	±1		kV	JEDEC JS-001-2014
ESD_{CDM}	ESD – charged device models	±500		V	JEDEC JESD22-C101F

Symbol	Parameter	Min	Max	Unit	Comments
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-55	150	°C	
T_{body}	Package body temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is matte tin (100% Sn).
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level for MLPD package	3			Represents a max. floor life time of 168h
	Moisture sensitivity level for thin WL-CSP	1			Represents an unlimited floor life time

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Operating Conditions

All in this specification defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

Figure 7:
Electrical Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
I_{lim}	Limiter current		30	mA	
I_{VP_REG}	Output current VP_REG		5.0	mA	
VDD_IO_RF	SPI / I²C power supply on VP_IO pin	0	5.5	V	When logic is powered from RF interface without wired interface operational
VDD_IO	SPI / I²C power supply on VP_IO pin	1.65(1)	5.5	V	When logic is powered from VP_IO or RF powered with wired interface operational
T_{junc}	Junction temperature	-40	125	°C	
VDD_IO_SR	VDD_IO slew rate	15		V/ms	Min. slew rate on VP_IO during power-up for correct operation of wired interface

Note(s):

1. For VDD_IO <1.65V correct operation is not guaranteed.

DC/AC Characteristics for Digital Inputs and Outputs

Figure 8:
CMOS Inputs /SS, MOSI and SCLK

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{IH}	High level input voltage	0.75 * VDD_IO			V	
V_{IL}	Low level input voltage			0.25 * VDD_IO	V	
I_{LEAK}	Input leakage current			10	µA	@125°C

Figure 9:
CMOS Outputs MISO and IRQ

Symbol	Parameter	Min	Typ	Max	Unit	Note
VOH	High level output voltage	0.85 * VDD_IO			V	Isource=1mA VP_IO = 5.5V
VOL	Low level output voltage			0.15 * VDD_IO	V	
RO	Output resistance		200	400	Ω	
RPD	Pull-down resistance pad MISO		10		kΩ	See note (1)

Note(s):

1. Pull down can be enabled while MISO output is in tristate when /SS is high. The activation is controlled by register setting miso_pd1.

Electrical Specifications

Figure 10:
Electrical Specifications (temperature 25°C unless noted otherwise)

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{SB_SPI}	Stand by consumption on VP_IO		<1		µA	@ 25°C (RF field not applied) VP_IO=1.8V
V_{LIM}	Limiter voltage		5.5	6.0	V	I_{LC}=30mA (DC) (1)
I_S	Supply current		450		µA	See note (2)
V_{HF_PON}	HF_PON threshold (rising VP_INT) power modes 0,3		2.7		V	Rectified RF supply voltage
V_{PON_HY}	HF_PON hysteresis		0.5		V	
V_{MOD}	Modulator ON voltage drop across LC1 - LC2		1.3 2.6		V	I_{LC}=1mA (1) I_{LC}=30mA (1) VP_IO=3.3V
C_{RES}	Resonance capacitor		45		pF	

Symbol	Parameter	Min	Typ	Max	Unit	Note
EE_{EN}	EEPROM endurance	100 000			cycles	@ 125°C (3)
EE_{RET}	EEPROM retention	10			years	@ 125°C (4)
$t_{VP\_IO\_DD}$	VP_IO deactivation delay	0.45			ms	

Note(s):

1. I_{LC} is the current flowing through LC1 and LC2 pins. Exposure to very strong RF fields which produce currents as high as I_{LC}=30mA for an extended period of time may damage the device.
2. Internal supply current measured over VP_IO pin, by forcing internal digital supply to 2.0V, and applying 13.56 MHz alternative pulses with amplitude 3.0Vpp to LC1 and LC2.
3. See Figure 11.
4. See Figure 12.

Figure 11:
EEPROM Endurance Over Temperature

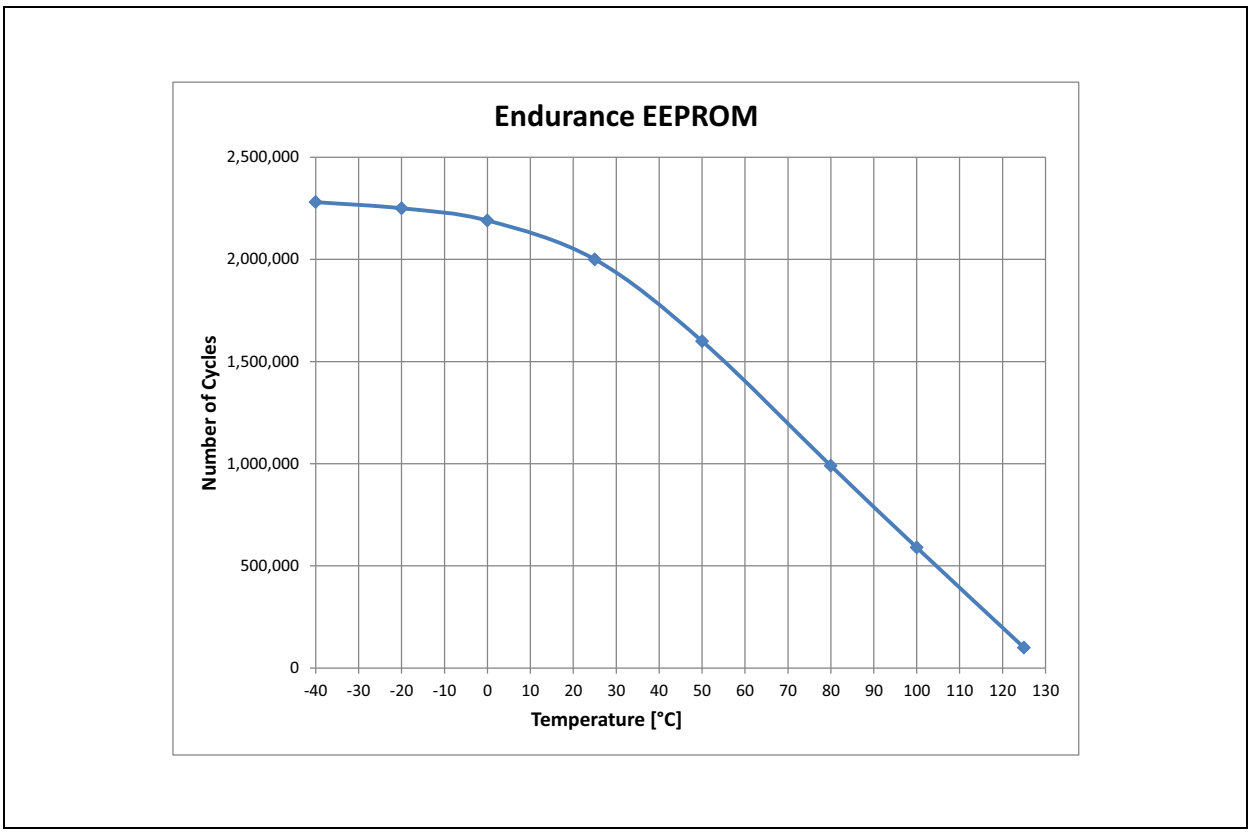
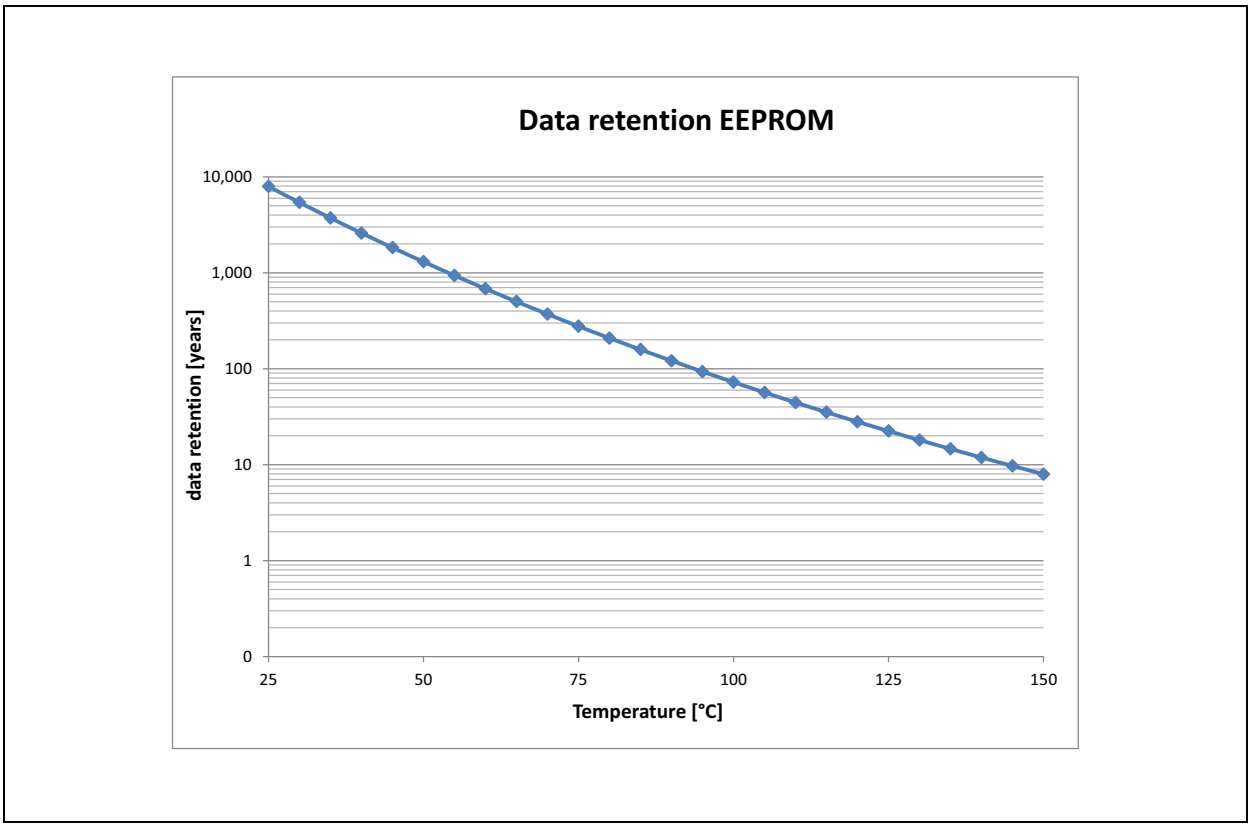


Figure 12:
EEPROM Data Retention Over Temperature

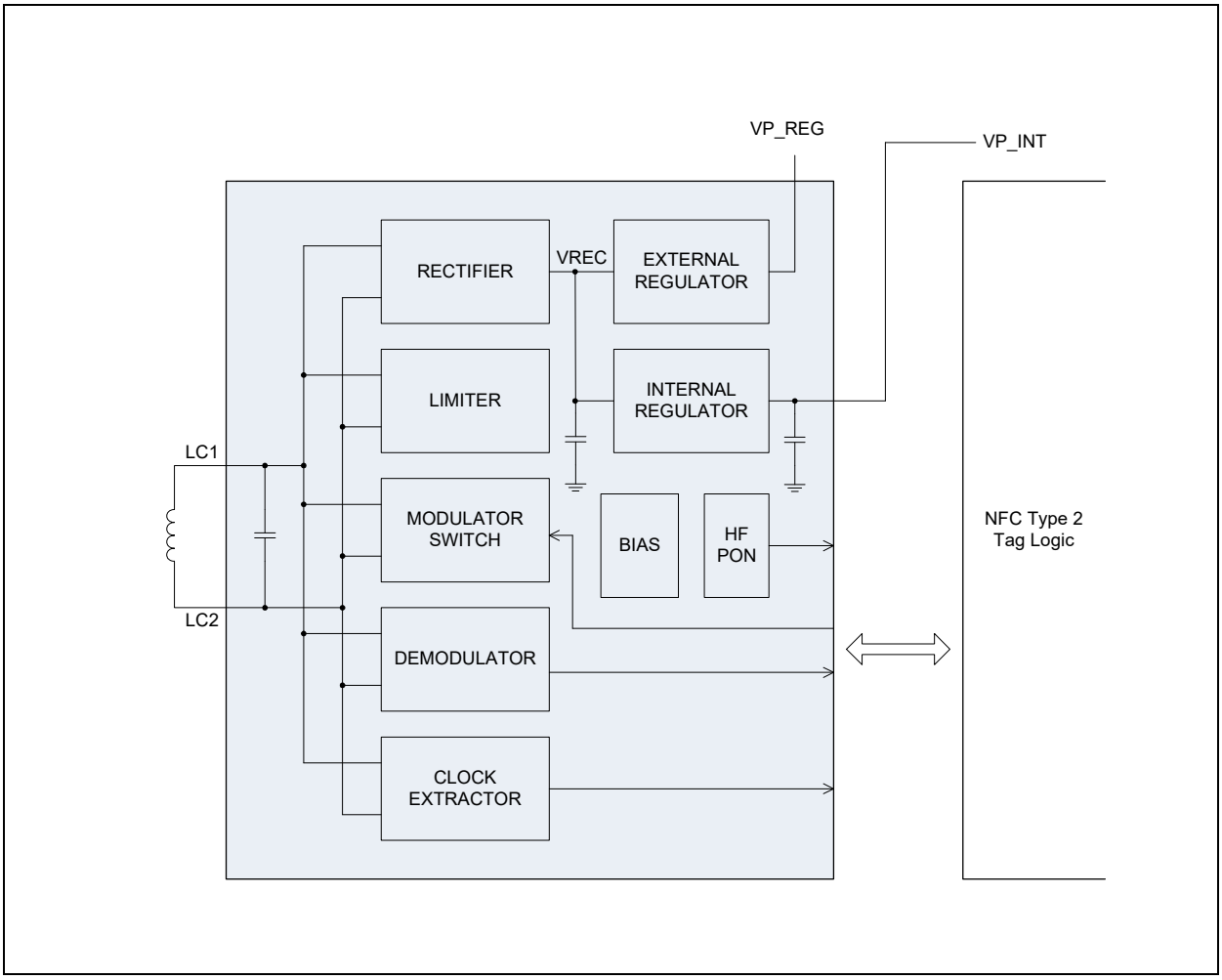


Detailed Description

Analog Frontend (AFE)

The AFE is connected to external tag coil, which together with the integrated resonant capacitor forms an LC tank resonating at the external electromagnetic field frequency (13.56 MHz). Figure 13 depicts the main AFE building blocks.

Figure 13:
PICC AFE Block Diagram



Rectifier extracts DC power supply from the AC voltage induced on coil terminals.

Limiter limits the maximum voltage on coil terminals to protect AFE from destruction. At voltages that exceed limiter voltage it starts to absorb current (acts as some sort of shunt regulator).

Modulator Switch is used for communication the NFC tag to a NFC device. When switched on it will draw current from coil terminals. This mechanism is called load modulation. Variation of current in the modulator switch (ON and OFF state) is seen as modulation by the NFC device.

Demodulator is used for communication NFC device to NFC tag. It detects AM modulation of the NFC device magnetic field. The demodulator is designed to accept modulation according to NFC-A specifications ([NFC Analog] [NFC Digital]).

Clock Extractor extracts a digital clock signal from the PCD carrier field frequency which is used as clock signal by logic blocks.

HF_PON enables operation of the AFE and the logic when the supply voltage is sufficiently high. A buffer capacitor and HF_PON hysteresis guarantee that there is no reset during NFC device modulation.

Internal Regulator provides regulated voltage VP_INT to the AFE and in most cases also to EEPROM and logic blocks. A buffer capacitor is also integrated.

External Regulator provides regulated voltage on external pin VP_REG where it can be used to supply some external circuitry. The regulated voltage and output resistance can be adjusted using EEPROM settings. Appropriate external buffer capacitor is needed in case VP_REG is used in the application. Current which may be provided depends on reader field strength, antenna size and Q factor, but it is limited to I_{VP_REG} maximum.

Bias provides bias currents and reference voltages to AFE analog blocks.

Power Management

AS3956 power management comprises of four different modes to fit requirements of different applications. AS3956 supports two power sources, whose activation depends on the selected power mode. Where an external supply is connected to VP_IO, the slew rate during power-up must be VDD_IO_SR minimum or greater to ensure correct operation.

Power Mode 0 - Default Power Mode

In this power mode, the Power Manager is controlling the supply of the PICC Logic, EEPROM and SPI / I^2C Interface (VDD). Its inputs are VP_INT (rectified and regulated supply extracted from RF field) and the VP_IO (supplied by external battery).

In standby mode, when AS3956 is not in the RF field (the condition is that rectified supply voltage is below HF_PON threshold) and the SPI / I^2C is not active (/SS is high), the VDD supply is disconnected. The only current consumption in this state is leakage on VP_IO, mainly due to level shifters and SPI / I^2C pins.

When AS3956 is placed in a RF field, VDD is connected to VP_INT. This happens once the HF_PON threshold is exceeded.

VP_IO is connected to VDD only when AS3956 is not in the RF field (rectified supply voltage is below HF_PON threshold) and the SPI / I^2C interface is activated by pulling /SS signal low. The switch to VP_IO is controlled by /SS signal. The VP_IO deactivation is delayed by $T_{VP\_IO\_DD}$, so that the switch shall stay closed in case of shorter times between successive SPI / I^2C activations. The switch is also closed during EEPROM writes activated over SPI / I^2C.

At activation of the switch, the time between the falling edge of the /SS signal and rising edge of SCLK shall be at least T_{NCSL} minimum to allow charging of internal VDD buffer capacitor, expiration of POR signal and to perform a complete IC initialization. Please note that the only SPI / I^2C operations, which are allowed in this mode, are read and write of EEPROM and registers.

If the RF field is lost during operation and the external system (MCU) is supplied over battery and /SS is low then power manager will automatically connect the VDD to VP_IO.

To enable low power mode where tag consumes I_{SB_SPI}, the following conditions must be met:

- SPI interface configured
- All SPI interface input lines (including /SS) must be set to high
- All SPI output lines must be open

Power Mode 3- External Supply Used to Power EEPROM and Logic

In this case the external supply shall be used to provide power to digital blocks, EEPROM, SPI / I^2C pads and MCU. External supply VP_REG is not used. Since this mode can be enabled only after initialization of the chip, the /SS line must be either permanently set to low or pulled low for short time to complete the initialization. When reading from or writing to the EEPROM via I^2C/SPI it is recommended that the MCU should first check whether there is enough energy available, then switch to Power mode 3 and execute the SPI/I^2C read or write and finally switch back to the original power mode if required.

In this mode, the HF_PON threshold of the chip is set so that it will operate at V_{HF_PON}.

If this mode is enabled, AS3956 will not be turned off as long as there is an external power present.

Power Mode 3 requires external power to be provided on VP_IO. It is therefore very important to always power up in Power Mode 0 or 1 (power mode set to PM 0 or 1 in EEPROM) and then switch to Power Mode 3 by SPI/ I^2C command only when external power is available by writing to IC Configuration Register 2. Before disconnecting external power i.e. switching off VP_IO, it is recommended to switch the chip back into Power Mode 0 again by writing to IC Configuration Register 2.

Chip Initialization in the Different Power Modes

During chip initialization, values from the EEPROM configuration bytes are loaded into the configuration registers.

Figure 14:
Chip Initialization in the Different Power Modes

Power Mode	Chip Initialization Occurs When
0	RF field or external power VP_IO turns on and /SS is low, whichever first.
3	Power up in PM 0 or 1 first and then switch to PM 3 by command from external microcontroller when external power is available

Resetting the AS3956

To fully reset the AS3956 it is necessary to remove all sources of power:

- Turn off the RF field **and**
- Take /SS pin high **or** remove power from the VP_IO line.

Interface Arbitration

Concurrent access to AS3956 internal EEPROM from RF or SPI / I^2C requires arbitration, to resolve conflicts or undesired behaviour.

Arbitration Mode 0 (first-come-first-serve)

AS3956 arbitrates EEPROM read/write accesses according to first-come-first-serve principle.

- In case no read/write access is currently ongoing, both RF and SPI / I^2C interfaces are allowed to read/write into EEPROM.
- In case a read/write request comes over RF, while SPI / I^2C is reading/writing, AS3956 will return a NAK_5 and will then enter SENSE/SLEEP state. The chip will generate an I_init IRQ and an EEPROM access error IRQ.
- In case a read/write request comes over SPI / I^2C while RF is reading/writing, AS3956 will trigger a I_err_acc interrupt (see Figure 94).
- In case a read request comes over SPI / I^2C while RF is reading/writing to the EEPROM, the AS3956 will reply all zeros over SPI / I^2C.

Energy Harvesting

AS3956 has energy harvesting capability. The regulated voltage output pin for energy harvesting is VP_REG. The energy harvesting is enabled only in Power Mode 0. Figure 16 shows settings of the regulated voltage output. The AS3956 can supply I_{VP_REG} from VP_REG in a strong field. The current which can be supplied by VP_REG and its output resistance will vary with field strength, antenna class and voltage setting. The output voltage and resistance can be set by Configuration Byte IC_CFG1.The energy harvesting can be disabled by setting the output resistance register to 0 as shown in Figure 15.

Figure 15:
Output Resistance Settings

rreg<1:0>	Typ. Output Resistance [Ω]	Comment
00b	X	Disabled – output pin is in tristate
01b	100	
10b	50	
11b	25	

Figure 16:
Regulated Voltage Output Settings

vreg<4:0>	Typ. Output Voltage [V]
00000	1.9
00001	2.0
00010	2.1
00011	2.2
00100	2.3
00101	2.4
00110	2.5
00111	2.6
01000	2.7
01001	2.8
01010	2.9
01011	3.0

vreg<4:0>	Typ. Output Voltage [V]
01100	3.1
01101	3.2
01110	3.3
01111	3.4
10000	3.5
10001	3.6
10010	3.7
10011	3.8
10100	3.9
10101	4.0
10110	4.1
10111	4.2
11000	4.3
11001	4.4
11010	4.5
11011	1.8
11100	1.8
11101	1.8
11110	1.8
11111	1.8

Note(s):

1. The regulated output voltage setting at 1.8V is measured with min. antenna voltage of $V_{LC2-LC1}$= 3.6V DC and the regulated voltage setting at 4.5V is measured with a min. antenna voltage of $V_{LC2-LC1}$= 5.5V DC.
   Abs. accuracy at 25°C is ±150mV at 1.8V linearly increasing to ±225mV at 4.5V, step size is 100mV ±20mV.

Silent Mode

Silent mode enables detection of the power status of a circuit whose supply (Vdd) is connected to VP_IO pin. If this mode is enabled and the voltage measured on pin VP_IO is below the configured threshold value, the RF part of AS3956 will be disabled, and the IC will not be responsive to incoming commands. Silent mode settings can be performed by using Configuration Byte IC_CFG0.

This feature overcomes a potentially inconsistent behavior in a battery powered system, where a passive NFC tag can always communicate with a NFC device, also in case the battery is not sufficiently charged to supply the rest of the system. A typical example is when the NFC tag is used for Bluetooth pairing: AS3956 would trigger a pairing procedure only in case the system is fully operational by monitoring the supply voltage.

Memory Protection

AS3956 internal memory can be protected from unauthorized access by enabling password authentication. A 32-bit password can be set to protect the full user memory, or part of it, to allow the creation of a public data and a private data area. Password protection can be applied for read and write accesses.

Password authentication is performed through a standard WRITE command to the Authentication Password block. A maximum of 7 negative attempts are permitted before the chip is locked. Once authenticated, the user can modify the password.

Password protection applies to RF communication only.

Further information on how to handle password authentication can be found in Authentication Password, Configuration Byte AUTH_CFG, Configuration Byte AUTH_CNT and Configuration Byte AUTH_LIM.

Passive Wake-Up

AS3956 is able to operate NFC tag operations standalone and fully powered by the RF field. The connected MCU can remain in standby/sleep mode as long as its intervention is not required by the application, in order to save power. AS3956 can be configured to notify the MCU through a wake-up interrupt.

A number of triggering events can be selected, e.g.:

- Power up
- SELECTED state entered
- Reception of SLP_REQ command
- NFC device has updated memory content

For a complete interrupt source list, please refer to the section Interrupt Registers.

Chip Kill

Some applications require that the RF link is active only under certain conditions, e.g. during device configuration only in a controlled environment like a production facility.

AS3956 can be configured by the MCU in order to restrict the NFC device access to the system. By setting the Configuration Byte CHIP_KILL in EEPROM, the MCU can disable access to SPI / I^2C from the RF link (i.e. Tunneling and Extended mode are permanently disabled), or even disable RF communication completely. In the latter case, AS3956 will not respond to incoming RF commands.

This configuration can be modified only by the MCU through SPI / I^2C interfaces.

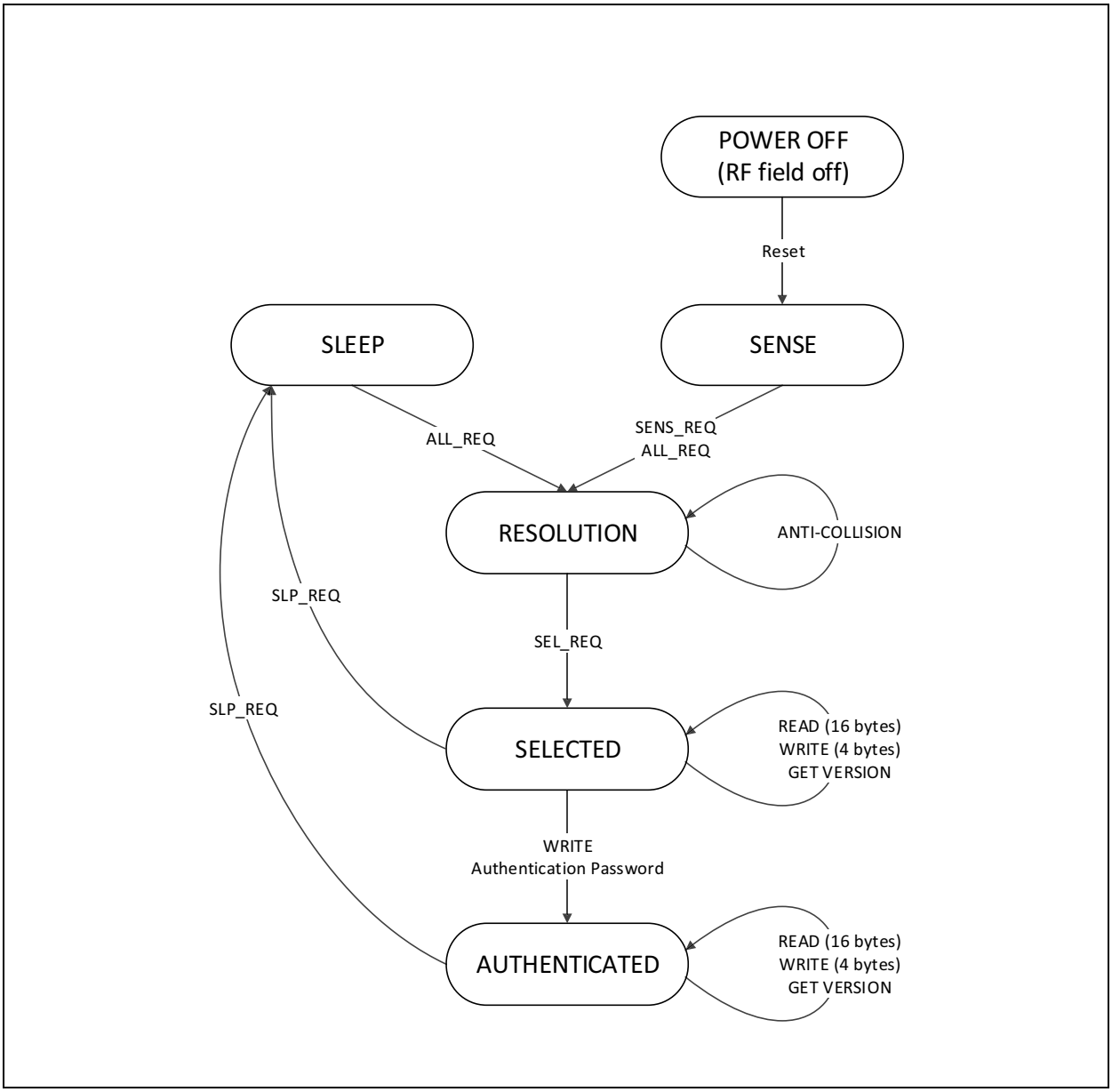
NFC Tag Functionality

Communication Principle

AS3956 autonomously executes complete NFC-A anti-collision communication sequence, during which the 7-byte UID is used ([NFC Analog] [NFC Digital]). After anti-collision, the NFC tag is brought into SELECTED state where read and write commands can be processed. The NFC tag will accept only read and write command issued to the address space actually available in AS3956 EEPROM. Any attempt to access an address outside the internal memory address space will be rejected. This default behavior of the NFC tag can be modified by enabling Tunneling or Extended mode.

A simplified AS3956 state diagram is shown in Figure 17.

Figure 17:
AS3956 State Diagram



SENSE State

After a power-on reset (POR), AS3956 switches to the SENSE state. This state is exited when a SENS_REQ or an ALL_REQ command is received from the NFC device. Any other data received while in this state is interpreted as an error and AS3956 remains in SENSE state.

When in SELECTED or AUTHENTICATED state, a correctly executed SLP_REQ command will modify the default waiting state from SENSE to SLEEP state. SLEEP state can be exited when an ALL_REQ command is received.

SLEEP State

Together with SENSE state, SLEEP state is the other waiting state for AS3956. SLEEP state can be entered upon reception of a SLP_REQ command. The distinction between SENSE and SLEEP state is made necessary to discriminate selected and not yet selected tags.

AS3956 can only exit this state upon reception of an ALL_REQ command. Any other command received in this state is interpreted as an error and AS3956 state remains unchanged.

RESOLUTION State

In RESOLUTION state, the NFC device is resolving the tag UID. Since AS3956 has a double size UID, the RESOLUTION state actually comprises of two sub-states, where the anti-collision procedure is carried out in Cascade Level 1 and 2. Please refer to [ISO18092] for further information.

SELECTED State

All memory operations are operated in SELECTED state.

Upon reception of a SLP_REQ command, SELECTED state is exited and AS3956 transits to SLEEP state. Any other command received when the device is in this state is interpreted as an error. Depending on its previous state, AS3956 returns to either SENSE or SLEEP state.

Upon reception of a SECTOR SELECT command, AS3956 returns a NAK and transits to SENSE or SLEEP state, depending on its previous state.

AS3956 transits to the AUTHENTICATED state after successful password verification, using a standard WRITE command to a dedicated memory address (see Authentication Password). The number of permitted failed authentications is set to 7, after which AS3956 transits to LOCKED sub-state (not shown in the picture). When LOCKED state is entered, only the MCU can bring AS3956 back to SENSE state by resetting the authentication counter (Configuration Byte AUTH_CNT) back to 0 and issue a Set Default, or Go To Sense, or Go To Sleep command.

When in LOCKED sub-state, all memory operations are only allowed in the memory area not password protected, as defined by the configuration byte Configuration Byte AUTH_LIM.

Upon reception of a SLP_REQ command, SELECTED state is exited and AS3956 transits to SLEEP state.

Any other command received when the device is in this state is interpreted as an error and, depending on its previous state, AS3956 returns to either SENSE or SLEEP state.

AUTHENTICATED State

In this state, all operations on memory blocks, which are configured as password verification protected, can be performed.

Upon reception of a SECTOR SELECT command, AS3956 returns a NAK and transits to SENSE or SLEEP state, depending on its previous state.

Upon reception of a SLP_REQ command, AUTHENTICATED state is exited and AS3956 transits to SLEEP state.

Any other command received when the device is in this state is interpreted as an error and, depending on its previous state, AS3956 returns to either SENSE state or SLEEP state.

NFC Forum Type 2 Tag Support

NFC Forum NFC-A commands ALL_REQ, SENS_REQ, SDD_REQ, SEL_REQ, SLP_REQ are required for anti-collision. Commands READ and WRITE are used for internal memory access. If NFC device issues a SECTOR SELECT command, AS3956 shall always reply with NAK.

Figure 18:
NFC-A vs ISO14443 Terminology

NFC-A Term	ISO14443 Term
States	
SENSE	IDLE
SLEEP	HALT
RESOLUTION	READY
SELECTED	ACTIVE
Commands / Responses	
SENS_REQ	REQA
ALL_REQ	WUPA
SENS_RES	ATQA
SSD_REQ	AC
SEL_REQ	SELECT
SLP_REQ	HLTA

UID Coding

Anti-collision procedure is based on the Unique Identification Number (UID). AS3956 supports double size UID (7 bytes). First three bytes of the UID are hardwired inputs to the PICC Logic (uid<23:0>). The last 4 bytes of the UID are stored in EEPROM UID block.

First UID Byte (uid0)

The first byte of UID is Manufacturer ID according to [ISO7816-6]. It is coded on bits *uid<7:0>*. **ams** IC Manufacturer ID is 3Fh.

Second UID Byte (uid1)

The second byte of UID (uid<15:8>) is reserved for **ams**' chip type (IC Type). Every **ams**' RFID tag IC has its own chip type assigned. AS3956 IC type is 14h.

Third UID Byte (uid2)

The third byte of UID (uid<23:16>) is set to 02h.

Figure 19:
Coding of First Three UID Bytes

UID Byte	Value (Hex)
uid0	3F
uid1	14
uid2	02

Last Four UID Bytes (uid3-uid6)

The last 4 bytes of UID are read from EEPROM (UID block) and pre-programmed during IC production. Those 4 bytes are unique, and cannot be modified.

Figure 20:
Last Four UID Bytes

UID Byte	UID Block Bits
uid3	b7-b0
uid4	b15-b8
uid5	b23-b16
uid6	b31-b24