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# AS3977

## Multi-Channel Narrowband FSK Transmitter

## 1 General Description

The AS3977 is a low-power fully integrated ETSI, FCC and ARIB compliant FSK transmitter capable of operating at any ISM frequency in the range of 300 to 928 MHz. It is based on a sigma-delta controlled fractional-N synthesizer phase locked loop (PLL) with fully integrated voltage controlled oscillator (VCO). The power amplifier (PA) output is programmable and can deliver power ranging from –20dBm up to +10dBm. An on-chip low drop-out (LDO) regulator is available in case an accurate output power independent of voltage supply variation is required. The output signal can be shaped using a programmable Gaussian filter to minimize the occupied bandwidth and adjacent channel power. The maximum data rate can be up to 100 kb/s – depending on the required filtering. The FSK frequency deviation is programmable up to a maximum of 64 kHz.

The crystal oscillator can handle a wide range of frequencies. For narrow-band applications, a temperature sensor with digital read-out is included that allows compensation of the crystal frequency drift due to temperature variation.

The AS3977 is connected to an external microcontroller via a bi-directional digital interface. The device operates at very low current consumption with a power supply range from 2.0V to 3.6V and can be powered down when not in use.

The device is fabricated in austriamicroystems advanced 0.35µm SiGe-BiCMOS technology.

## 2 Key Features

- Fully integrated UHF transmitter
- Compliant to ETSI EN 300-220, FCC CFR47 part 15 and ARIB STD-T67
- Multi-channel with narrow bandwidth
- 300 – 928 MHz operating frequency range (ISM)
- Filtered FSK
- Data rate up to 100 kb/s
- FSK deviation programmable up to 64kHz
- Extremely low power consumption

### Main Characteristics

- 2.0 – 3.6V power supply
- Power down current consumption 100 nA (3V, 25ºC)
- Output power up to +10dBm
- Occupied bandwidth 6 kHz (4.8 kb/s, FFSK, ARIB)
- -40 to 85ºC temperature range

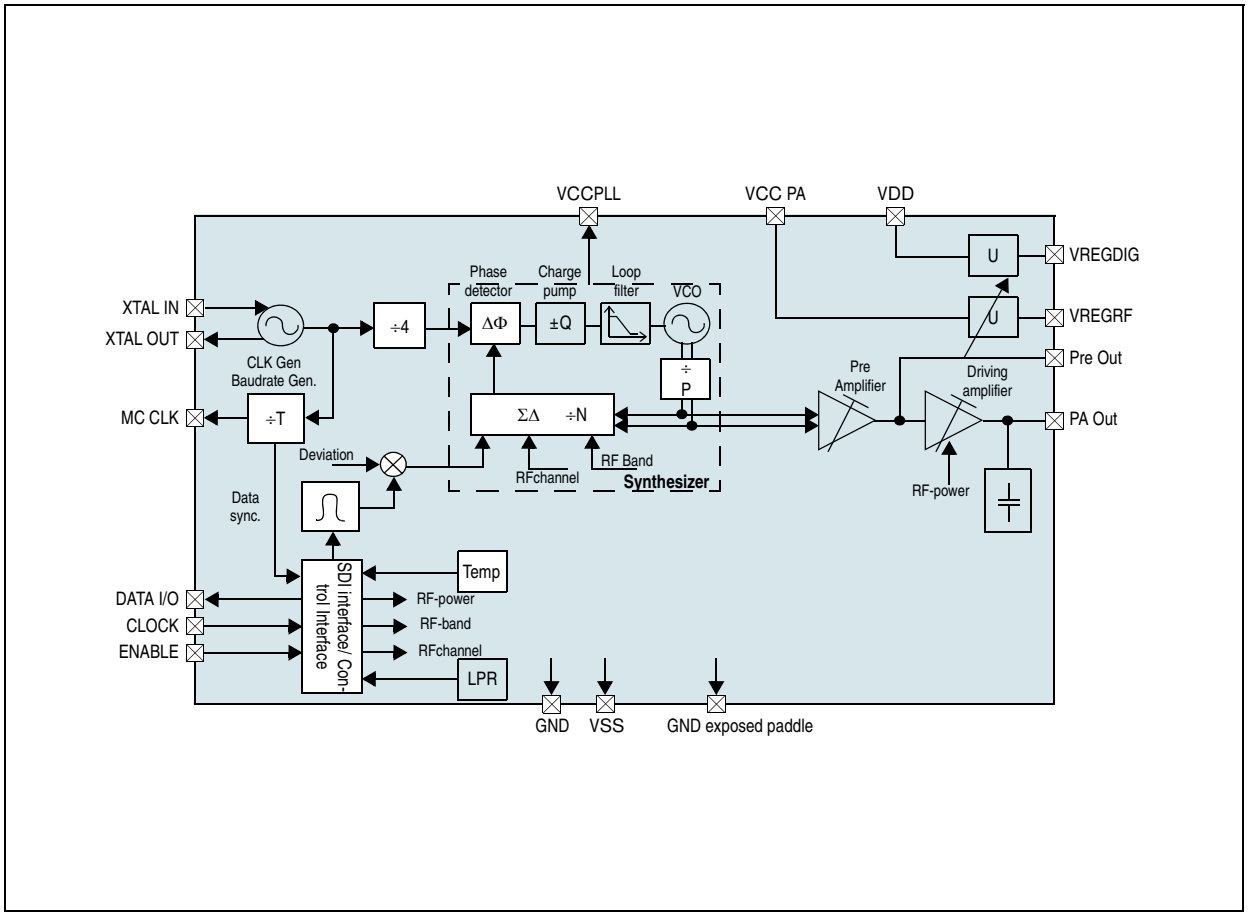
### Additional Features

- Sigma-Delta controlled fractional-N synthesizer
- Resolution of synthesizer < 100Hz
- Fully integrated PLL
- Fully integrated voltage controlled oscillator (VCO)
- 4kV ESD protection (1.5kV for the Analog pins)
- 12 – 20 MHz crystal oscillator
- On-chip temperature sensor with digital readout for AFC purposes
- Fast frequency hopping with predefined channel selection
- Microcontroller clock output to save addition crystal
- Constant output power over battery life time
- Integrated Manchester coder
- Digital lock detector
- Low drop-out regulator
- Bi-directional serial interface
- Low Power Down Mode current consumption

## 3 Applications

The AS3977 is suitable for Remote keyless entry systems, Short range radio data transmission, Domestic and consumer remote control units, Cordless alarm systems, Remote metering, and Low power telemetry.

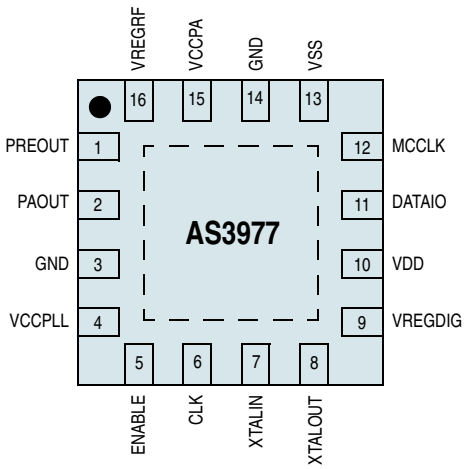
*Figure 1. AS3977 Block Diagram*



## Contents

# 4 Pin Assignments

*Figure 2. Pin Assignments (Top View)*




## 4.1 Pin Descriptions

*Table 1. Pin Descriptions*

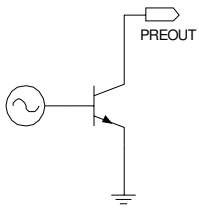
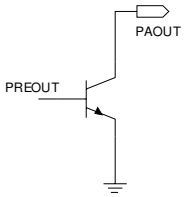
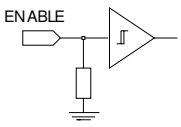
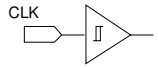
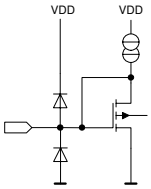
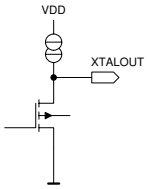
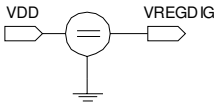
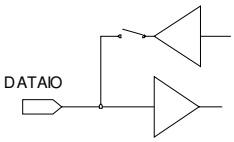
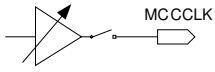
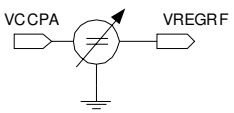
| Pin Name | Pin Number | Type | Description |
|---|---|---|---|
| PREOUT | 1 |  | Open Collector preamplifier output, need a feeding coil connected to VREGRF or VDD and is the input for the Power amplifier |
| PAOUT | 2 |  | Open Collector power amplifier output, need a feeding coil connected to VREGRF or VDD |
| RESERVED | 3 | | Must be connected to GND |
| VCCPLL | 4 | Positive Power Pin | Positive supplies of VCO, for optimum performance, add decoupling capacitors on this Pin. |
| ENABLE | 5 |  | Digital CMOS level input, internal Pull down resistor > 60k |

*Table 1. Pin Descriptions*

| Pin Name | Pin Number | Type | Description |
|---|---|---|---|
| CLK | 6 |  | SDI clock |
| XTALIN | 7 |  | XTAL oscillator input, DC Level approximately 1 Volt, needs an DC Blocker in case of external clock |
| XTALOUT | 8 |  | XTAL oscillator output, DC Level approximately 1 Volt |
| VREGDIG | 9 |  | Voltage regulator2 (VRegDig) output, requires a capacitor with nominal 100 nF. |
| VDD | 10 | Positive Power Pin | Positive supply of digital part and voltage regulator2 (VRegDig) |
| DATAIO | 11 |  | Digital CMOS level input Pin, SDI data input / output |
| MCCLK | 12 |  | Micro controller clock output Digital output with variable driver strength |
| VSS | 13 | GND Pin | Negative supply of digital part |
| Reserved | 14 | | Must be connected to GND |
| VCCPA | 15 | Positive Power Pin | Positive supply of PA and voltage regulator |
| VREGRF | 16 |  | Voltage regulator output to feed the RF Amplifier. For optimum performance a capacitor with nominal 1µF and 100 nF is recommended. |
| GND | 17 | GND Power Pin | Negative supply of analogue part (exposed paddle) |

# 5 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” (see Table 3) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Table 2. Absolute Maximum Ratings*

| Parameter | | Min | Max | Units | Comments |
|---|---|---|---|---|---|
| Positive supply voltage ($V_{SUP}$) | | -0.5 | 5.0 | V | Voltage on all supply Pins VCCPA,VCCPLL,$V_{DD}$ |
| Negative supply voltage (GND, $V_{SS}$) | | 0 | 0 | V | |
| Input current (latch-up immunity) ($I_{SCR}$) | | -40 | 40 | mA | Norm: Jedec 17 |
| ESD for Digital Pins | $ESD_{DHBM}$ | ±4 | | kV | Norm MIL 883 E method 3015 (Human Body Model) |
| | $ESD_{DMM}$ | ±200 | | V | Norm: EIJA IC-121 (Machine Model) |
| ESD for Analog Pins | $ESD_{AHBM}$ | ±1.5 | | kV | Norm MIL 883 E method 3015 (Human Body Model) |
| | $ESD_{AMM}$ | ±100 | | V | Norm: EIJA IC-121 (Machine Model) |
| ESD for RF Pins | $ESD_{RFHBM}$ | ±1.5 | | kV | Norm MIL 883 E method 3015 (Human Body Model) |
| | $ESD_{RFMM}$ | ±100 | | V | Norm: EIJA IC-121 (Machine Model) |
| Total power dissipation (all supplies and outputs) | | | 200 | mW | |
| Storage temperature, ($T_{STRG}$) | | -55 | 125 | ºC | |
| Package body temperature ($T_{BODY}$) | | | 260 | ºC | Norm: IPC/JEDEC J-STD-020C. The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/ JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”. |
| Humidity non-condensing | | 5 | 85 | % | |

# 6 Electrical Characteristics

*Table 3. Operating Conditions*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{SUP}$ | Positive supply voltage analog | Voltage on all supply VCCPA,VCCPLL,VDD | 2.0 | | 3.6 | V |
| GND | Negative supply voltage analog | | 0 | | 0 | V |
| VSS | Negative supply voltage digital | | 0 | | 0 | V |
| A-D | Difference of supplies | VCC-VDD, GND-VSS | -0.1 | | 0.1 | V |
| TAMB | Ambient Temperature | | -40 | | 85 | ºC |

*Table 4. Block Specification*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{OUT315}$ | Output Frequency Range | | 300 | | 320 | MHz |
| $f_{OUT434}$ | | | 425 | | 450 | |
| $f_{OUT868}$ | | | 865 | | 870 | |
| $f_{OUT915}$ | | | 902 | | 928 | |
| $P_{OUT}$ | Output Power | Depends on Power Setting | | | | |
| $f_{FSKdata}$ | FSK Data Rate | Internal Manchester Coding | 1 | | 100 | kbit/s |
| | | | 0.5 | | 50 | |
| **315MHz Frequency Band Section**, FCC part 15 is applicable | | | | | | |
| $\Delta FSK_1$ | FSK Deviation | programmable (8bit) Resolution of FSK Deviation (see Table 5) | 0 | | ±64 | kHz |
| $P_{SPE1}$ | Spurious Emissions (max. –19.6dBm radiated fundamental power)[1] | 216-960MHz at frequencies > 960Mhz at harmonics | | | -49 | dBm |
| | | | | | -41 | |
| | | | | | -40 | |
| | Phase noise @ 50 kHz | Charge pump setting: $I_{CHP}$=50µA; $V_{SUP}$=2.0..3.6V, TAMB=-40..85ºC | | -86 | | dBc/Hz |
| | Phase noise @ 250 kHz | | | -92 | | |
| | Phase noise @ 1 MHz | | | -102 | | |
| **434MHz Frequency Band Section**, EN 300 220 and/or ARIB STD-T67 are applicable | | | | | | |
| $\Delta FSK_2$ | FSK Deviation | Small deviation (ARIB), programmable (8bit) Resolution of FSK Deviation (see Table 5) | ±1.25 | | ±4 | kHz |
| | | | 0 | | ±64 | |
| | Phase noise @ 50 kHz | Charge pump setting: $I_{CHP}$=50µA; $V_{SUP}$=2.0…3.6V, TAMB=-40…85ºC | | -86 | -83 | dBc/Hz |
| | Phase noise @ 250 kHz | | | -94 | | |
| | Phase noise @ 1 MHz | | | -102 | | |
| $P_{ACP2}$ | Adjacent Channel Power | ARIB, $f_{REF}$=4MHz, $I_{CHP}$=50µA | | | -40 | dBc |
| $OBW_2$ | Occupied Bandwidth | Channel spacing 12.5 kHz, FSK data rate 4.8 kbit/s (ARIB) FSK Deviation ±1.8 KHz | | | 8.5 | |
| | | GF Setting (see Gaussian Filter Clock Setting on page 38) Channel spacing 25 kHz, FSK data rate 9.6 kbit/s (ARIB) FSK Deviation ±3.0 KHz | 8.5 | | 16 | kHz |

*Table 4. Block Specification (Continued)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $P_{SPE2}$ | Spurious Emissions excluding Harmonics[1] | 47-74MHz<br>87.5-118MHz<br>174-230MHz<br>470-862MHz (EN 300 220) | | | -54 | dBm |
| | Spurious Emissions and Harmonics[1] | at other frequencies < 1GHz at ≥ 1GHz (EN 300 220) | | | -36<br>-30 | dBm |
| | | ARIB | | | -29 | |
| $f_{ERROR}$ | Output Frequency Error | With ideal crystal, $V_{SUP}$=2.0…3.6V, $T_{AMB}$=-40…85ºC | | | ±1 | ppm |
| **868MHz Frequency Band Section**, EN 300 220 is applicable | | | | | | |
| $\Delta FSK_3$ | FSK Deviation | programmable (8bit)<br>Resolution of FSK Deviation (see Table 5) | 0 | | ±64 | kHz |
| $P_{SPE3}$ | Spurious Emissions excluding Harmonics[1] | 47-74MHz<br>87.5-118MHz<br>174-230MHz<br>470-862MHz (@-10dBm radiated power) | | | -54 | dBm |
| | Spurious Emissions and Harmonics[1] | at other frequencies < 1GHz at frequencies ≥ 1GHz | | | -36<br>-30 | dBm |
| | Phase noise @ 50 kHz | Charge pump setting: $I_{CHP}$=50µA; $V_{SUP}$=2.0…3.6V, $T_{AMB}$=-40…85ºC | | | -78 | dBc/Hz |
| | Phase noise @ 250 kHz | | | | -85 | |
| | Phase noise @ 1 MHz | | | | -89 | |
| **915MHz Frequency Band Section**, FCC part 15 is applicable | | | | | | |
| $\Delta FSK_4$ | FSK Deviation | programmable (8bit)<br>Resolution of FSK Deviation (see Table 5) | 0 | | ±64 | kHz |
| $P_{SPE4}$ | Spurious Emissions (max. –1dBm radiated fundamental power)[1] | 216-960MHz<br>at frequencies > 960MHz and harmonics | | | -49<br>-41 | dBm |

1. These parameters will not be tested.

*Table 5. Resolution of FSK Deviation*

| Symbol | Parameter | Conditions | Equation for Min. Resolution | Units |
|---|---|---|---|---|
| **315MHz and 434MHz Frequency Band Section** | | | | |
| $\Delta FSK_{res1}$ | Resolution of FSK Deviation[1] | For detailed information, See FSK Deviation Setting and Frequency Trimming on page 37 | $\Delta F = (INT <8> +1). \frac{f_{REF}}{2^{16}}$ | Hz |
| **868MHz and 915MHz Frequency Band Section** | | | | |
| $\Delta FSK_{res2}$ | Resolution of FSK Deviation[1] | For detailed information, See FSK Deviation Setting and Frequency Trimming on page 37 | $\Delta F = (INT <8> +1). \frac{f_{REF}}{2^{15}}$ | Hz |

1. INT<8> refer to Register Settings

*Table 6. Reference Frequency Generator and Micro Controller Clock Driver*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Crystal Oscillator** | | | | | | |

*Table 6. (Continued)Reference Frequency Generator and Micro Controller Clock Driver*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{XOSC}$ | Crystal Oscillator Frequency | | 12 | 16 | 20 | MHz |
| $t_{XOSC}$ | Crystal Oscillator Start up time | $V_{SUP}$=2.0…3.6V, TAMB=-40…85ºC crystal series resistance ≤ 100Ω | | | 1.5 | ms |
| $R_{XOSC}$ | Crystal Oscillator Oscillation Margin Level | $f_{XOSC}$=13.56MHz, $C_L$=12pF | 1500 | | | Ω |
| $\Delta f/f_0$ | Frequency Stability vs. Temperature[1] | AS3977 Only | | | ±1 | ppm |
| **Micro Controller Clock Driver** | | | | | | |
| $f_{MCCLK}$ | Clock output frequency | depending on configuration register settings and crystal | | | 4 | MHz |
| $V_{MCL}$ | Low level output voltage | $V_{SUP}$=3V, at nominal high level output current | | | 0.1*$V_{SUP}$ | V |
| $V_{MCH}$ | High level output voltage | $V_{SUP}$=3V, at nominal high level output current | 0.9*$V_{SUP}$ | | | V |
| $C_{LMCC}$ | Capacitive load | | | | 20 | pF |
| $t_{RMCC}$ | Rise time | | | | 62.5 | ns |
| $t_{FMCC}$ | Fall time | | | | 62.5 | ns |
| $I_{MCH}$ | High level output current | | | | 1 | mA |
| $I_{MCL}$ | Low level output current | | | | 1 | mA |

1. These parameters will not be tested.

*Table 7. Phase Locked Loop*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{REF}$ | Comparison Frequency | depending on $f_{XOSC}$ (reference divider division ratio = 4) | 3.0 | 4.0 | 5.0 | MHz |
| $\Delta f_O$ | Output Frequency Resolution | $f_{OUT315}$ / $f_{OUT434}$ | 46 | 61 | 77 | Hz |
| | | $f_{OUT868}$ / $f_{OUT915}$ | 92 | 122 | 153 | |
| $t_{SYNTH}$ | Synthesizer Start up Time | | | 500 | | µs |
| $t_{LOCK}$ | Synthesizer Lock Time | Δf=600kHz, $f_{ERROR}$ @ $t_{LOCK}$=10kHz | | 50 | 200 | µs |

*Table 8. Loop Filter Bandwidth*

| Symbol | Parameter | | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Filter Bandwidth at 315 MHz** | | | | | | | |
| $f_{BW}$ | Charge pump setting: $I_{CHP}$ | @ 12.5 µA | Reference Frequency = 4MHz VSUP = 3.0 V; TAMB = 25ºC | | 55 | | kHz |
| | | @ 25 µA | | | 85 | | |
| | | @ 37.5µA | | | 115 | | |
| | | @ 50 µA | | | 170 | | |
| **Filter Bandwidth at 433 MHz** | | | | | | | |

*Table 8. (Continued)Loop Filter Bandwidth*

| Symbol | Parameter | | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $f_{BW}$ | Charge pump setting: $I_{CHP}$ | @ 12.5 µA | Reference Frequency = 4MHz<br>VSUP = 3.0 V;<br>TAMB = 25ºC | | 50 | | kHz |
| | | @ 25 µA | | | 70 | | |
| | | @ 37.5µA | | | 90 | | |
| | | @ 50 µA | | | 120 | | |
| **Filter Bandwidth at 868 MHz** | | | | | | | |
| $f_{BW}$ | Charge pump setting: $I_{CHP}$ | @ 12.5 µA | Reference Frequency = 4MHz<br>VSUP = 3.0 V;<br>TAMB = 25ºC | | 50 | | kHz |
| | | @ 25 µA | | | 70 | | |
| | | @ 37.5µA | | | 90 | | |
| | | @ 50 µA | | | 120 | | |

*Table 9. Power Amplifier (300 - 320 MHz and 425 - 450 MHz Bands)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| POUT | Min. Output Power @ 50Ω | VSUP=3V, @ 25ºC,<br>Power depending on power setting with or without the use of the internal voltage regulator, external matching network included | | -20 | | dBm |
| POUT | Max. Output Power @ 50Ω | VSUP=3V, @ 25ºC,<br>Power depending on power setting with or without the use of the internal voltage regulator, external matching network included | | 8 | | dBm |
| POUT | Output Power Variation@ 50Ω[1] (300 – 320MHz) | VSUP=3V, @ 25ºC,<br>Power depending on register setting with or without the use of the internal voltage regulator,<br>external matching network included, strong AB operation mode | -2.5 | | +2.5 | dBm |
| POUT | Output Power Variation@ 50Ω[1] (425 – 450MHz) | VSUP=3V, @ 25ºC,<br>Power depending on register setting with or without the use of the internal voltage regulator,<br>external matching network included, strong AB operation mode | -2.0 | | +2.0 | dBm |
| POUT | Output Power Variation vs. VDD and Temperature @ 50Ω | VSUP=2.2…3.6V, TAMB=-40…85ºC, With the use of the internal voltage regulator, external matching network included, strong AB operation mode | -2.8 | +0.6 / -1.5 | 1.0 | dB |
| POUT | Output Power Variation vs. Temperature @ 50Ω | VSUP=3V, TAMB=-40..85ºC,<br>Without the use of the internal voltage regulator,<br>external matching network included, strong AB operation mode | | +1.5 / -2.0 | | dB |
| POUT | Max Output Power @ 50Ω | VSUP=3.6V, @ 25ºC,<br>Power depending on power setting without the use of the internal voltage regulator,<br>external matching network included | | 10 | | dBm |

1. Limits by production test measurement uncertainties

*Table 10. Power Amplifier (865 - 870 MHz and 902 - 928 MHz Bands)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| POUT | Min Output Power @ 50Ω | VSUP=3V, @ 25ºC, Power depending on power setting with or without the use of the internal voltage regulator, external matching network included | | -20 | | dBm |
| POUT | Max Output Power @ 50Ω | VSUP=3V, @ 25ºC, Power depending on power setting with or without the use of the internal voltage regulator, external matching network included | | 4 | | dBm |
| POUT | Output Power Variation @ 50Ω[1] | VSUP=3V, @ 25ºC, Power depending on register setting with or without the use of the internal voltage regulator, external matching network included, strong AB operation mode[2] | -3.5 | | +3.5 | dBm |
| POUT | Output Power Variation vs. VDD and Temperature @ 50Ω | VSUP=2.2…3.6V, TAMB= -40…85ºC, With the use of the internal voltage regulator, external matching network included, strong AB operation mode[2] | | +2.0 / -3.0 | | dB |
| POUT | Output Power Variation vs. Temperature @ 50Ω | VSUP=3V, TAMB=-40…85ºC, Without the use of the internal voltage regulator, external matching network included, strong AB operation mode[2] | | +2.0 / -3.0 | | dB |

1. Limits by production test measurement uncertainties
2. Power line matching needs to be adjusted to VDD to ensure strong AB operation mode

*Table 11. Antenna Tuning Circuit*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $C_{Atmin}$ | Minimum Antenna tuning Capacitor | ATCPH <3:0> = 0000 | | 0.11 | | pF |
| $C_{Atmax}$ | Maximum Antenna tuning Capacitor | ATCPH <3:0> = 1111 | | 1.51 | | pF |

*Table 12. Low Power Reset (Bit LT)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{LPR}$ | Low Power Detection Threshold Voltage | Decreasing Supply Voltage | 1.85 | 1.95 | 2.05 | V |
| $V_{LPR}$ | Low Power Release Threshold Voltage | Rising Supply Voltage | | 2.05 | | V |

*Table 13. Low Supply Voltage Detector (Bit LS)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{LS}$ | Low Supply Detection Threshold Voltage | Decreasing Supply Voltage | 2.0 | 2.1 | 2.2 | V |
| $V_{LS}$ | Low Supply Release Threshold Voltage | Rising Supply Voltage | | 2.17 | | |

*Table 14. Temperature Sensor*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $ERR_{TS}$ | Absolute Error | $T_{AMB}$ = -40…85ºC | -5 | | +5 | ºC |
| $ERR_{TSL}$ | Absolute Error (limited temperature range) | $T_{AMB}$ = -20…65ºC | | ±2 | | ºC |
| | Conversion Factor | $T_{AMB}$ = -40…85ºC | | 0.19 | | ºC/bit |
| $OR_{TS}$ | Output Resolution | | | 10 | | bit |
| $CR_{TS}$ | Conversion Rate | $f_{TS} = f_{CRYSTAL}/12$ after startup time of 256 / $f_{TS}$ | | | $f_{TS}/1354$ | samples/s |

*Table 15. Voltage Regulator for Power Amplifier*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VREGRF | Output Voltage for supply Power Amplifier | Adjustable, nominal value | 1.7 | | 2.0 | V |
| D_VREGRF | Regulator Tolerance | | -0.15 | | 0.1 | V |

*Table 16. Current Consumption*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_{PDWN}$ | Power Down Mode | $V_{SUP}$=3V @ 25ºC | | | 100 | 250 | nA |
| | | $V_{SUP}$=2.0…3.6V, $T_{AMB}$=-40…85ºC | | | 1000 | 5000 | |
| $I_{CLKEN}$ | Clock Enable Mode | $V_{SUP}$=3V @ 25ºC, $C_{load}$≤20pF, $f_{CLK}$=20MHz | | | 1 | 1.25 | mA |
| | | $V_{SUP}$=2.0…3.6V, $T_{AMB}$=-40..85ºC, Cload≤20pF, $f_{CLK}$=20MHz | | | 1.25 | 1.6 | |
| $I_{Temp\_sens}$ | Temperature sensor Current | $V_{SUP}$=2.0..3.6V, $T_{AMB}$=-40..85ºC | | | 0.25 | | mA |
| $I_{PLLEN}$ | PLL Enable Mode | $V_{SUP}$=2.0…3.6V, $T_{AMB}$=-40…85ºC | | | 5.6 | | mA |
| $ITX8dBm_{315}$ | Transmit Mode @ 8dBm output power, 315 MHz band @ 50Ω including matching network, strong AB operation | $V_{SUP}$=3V @ 25ºC | without the use of the internal regulator[1] | | 13.5 | 16.5 | mA |
| | | $V_{SUP}$=2.0…3.6V, $T_{AMB}$=-40…85ºC | | | 15.5 | 19 | mA |
| | | $V_{SUP}$=3V @ 25ºC | with the use of the internal regulator | | 14.0 | 17.0 | mA |
| | | $V_{SUP}$=2.2…3.6V, $T_{AMB}$=-40…85ºC | | | 16.0 | 19.5 | mA |
| $ITX8dBm_{433}$ | Transmit Mode @ 8dBm output power, 433 MHz band @ 50Ω including matching network, strong AB operation | $V_{SUP}$=3V @ 25ºC | without the use of the internal regulator | | 12.5 | 15.5 | mA |
| | | $V_{SUP}$=2.0…3.6V, $T_{AMB}$=-40…85ºC | | | 14.5 | 18 | mA |
| | | $V_{SUP}$=3V @ 25ºC | with the use of the internal regulator | | 13.0 | 16.0 | mA |
| | | $V_{SUP}$=2.2…3.6V, $T_{AMB}$=-40…85ºC | | | 15 | 18.5 | mA |

*Table 16. Current Consumption*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_{TX4dBm_{868}}$ | Transmit Mode @ 4dBm output power, 868 MHz and 906MHz band @ 50Ω including matching network, strong AB operation | $V_{SUP}$=3V @ 25ºC | without the use of the internal regulator | | 14.5 | 17.5 | mA |
| | | $V_{SUP}$=2.0…3.6V, $T_{AMB}$=-40…85ºC | | | 16.5 | 19.0 | mA |
| | | $V_{SUP}$=3V @ 25ºC | with the use of the internal regulator | | 15.0 | 18.0 | mA |
| | | $V_{SUP}$=2.2…3.6V, $T_{AMB}$=-40…85ºC | | | 17.0 | 19.5 | mA |

1. Power line matching needs to be adjusted to VDD to ensure strong AB operation mode

*Table 17. DC/AC Characteristics for Digital Interface*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CMOS Input** | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | 0.7 * $V_{SUP}$ | | $V_{SUP}$ + 0.1 | V |
| $V_{IL}$ | Low Level Input Voltage | | $V_{GND}$ -0.1 | | 0.3 * $V_{SUP}$ | V |
| $I_{IL}$ | Low Level Input Leakage Current | no internal pull up/down | | | ±1 | µA |
| $I_{IH}$ | High Level Input Leakage Current | no internal pull up/down | | | ±1 | µA |
| $I_{IHPD}$ | High Level Input Leakage Current with internal pull down | $V_{SUP}$=3.6V, $V_{IN}$=3.6V | 15 | | 60 | µA |
| **CMOS Output**<br>**Note:** The following specification is valid for the DATAIO standard CMOS output. The MCCLK output can be programmed to different driver strengths according MCCDS register. | | | | | | |
| $V_{OH}$ | High level output voltage | $V_{SUP}$=3V, at nominal high level output current | $V_{SUP}$-0.5 | | | V |
| $V_{OL}$ | Low level output voltage | $V_{SUP}$=3V, at nominal low level output current | | | $V_{SS}$+0.4 | V |
| $C_L$ | Capacitive load | | | | 20 | pF |
| $t_R$ | Rise time | | | | 50 | ns |
| $t_F$ | Fall time | | | | 50 | ns |
| $I_{OH}$ | High level output current | | | | 1 | mA |
| $I_{OL}$ | Low level output current | | | | 1 | mA |

# 7 Timing Characteristics

Be aware that the Power Down Mode can be entered by setting ENABLE low for more than $2^{16}$ XTAL cycles (Power Down Timer).

*Figure 3. Write Data*

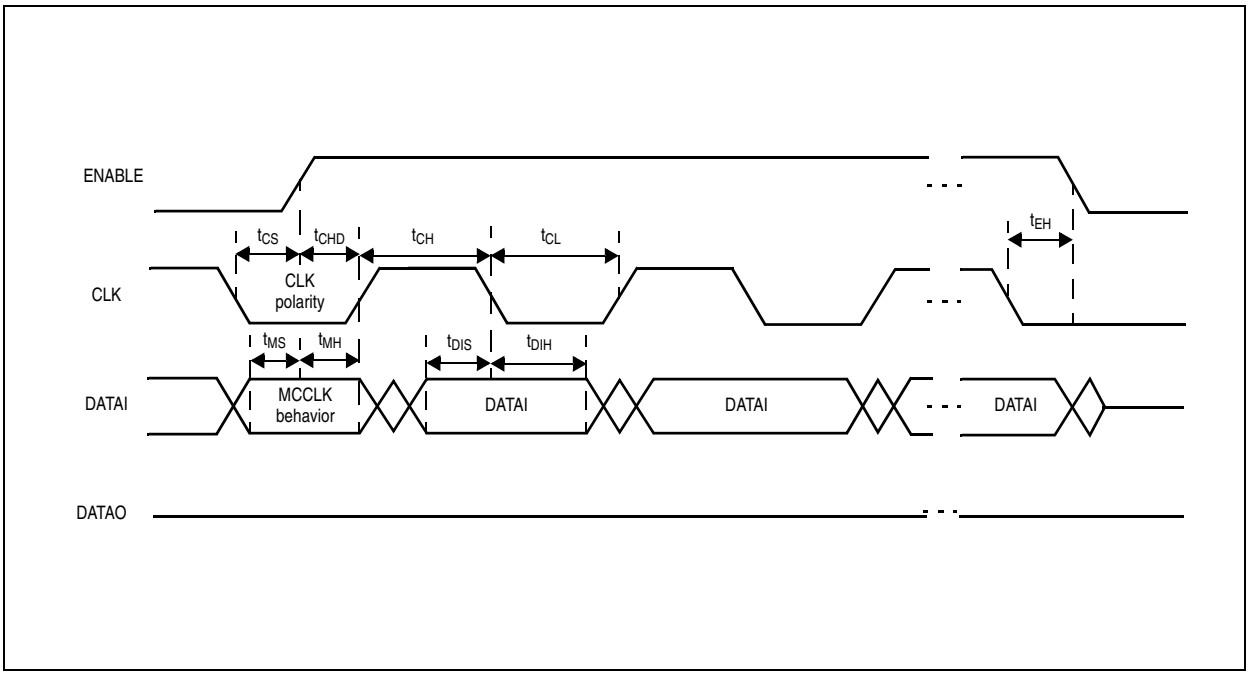
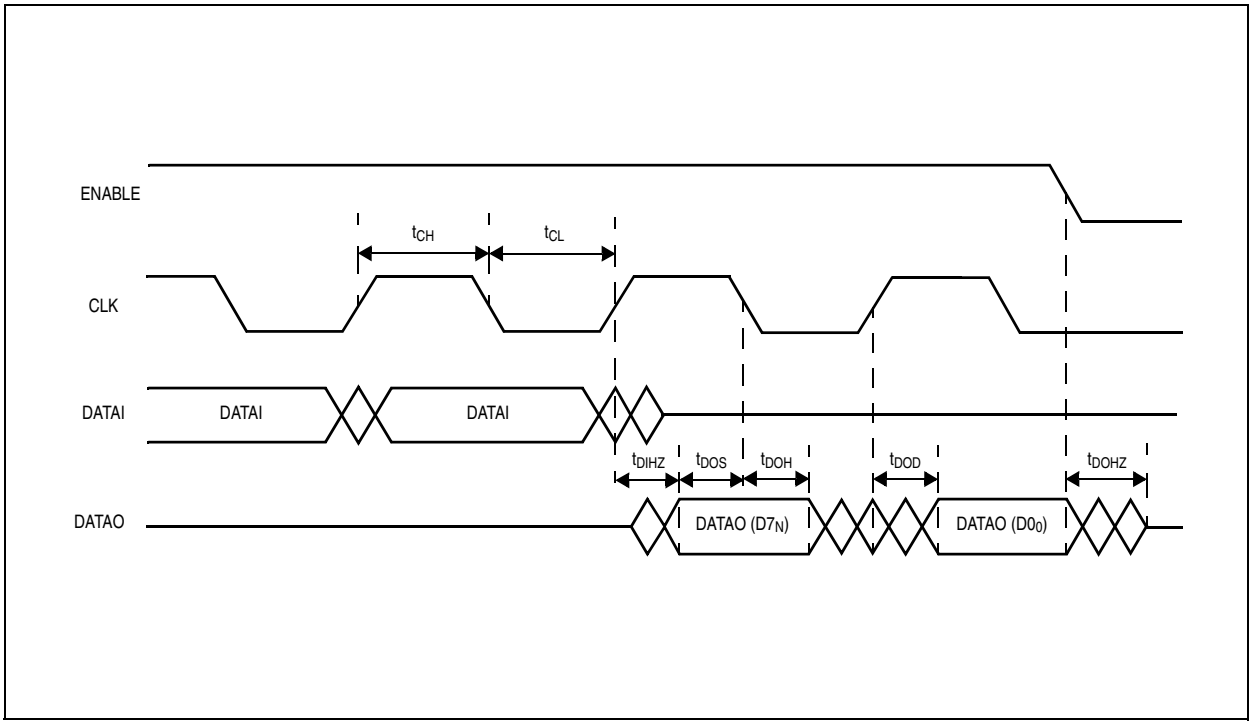



*Figure 4. Read Data*



## 7.1 Timing Parameters

*Table 18. Timing Parameters*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| General | | | | | | |
| $BR_{SDI}$ | Bit rate | | | | 2 | Mbps |
| $t_{CH}$ | Clock high time | | 250 | | | ns |
| $t_{CL}$ | Clock low time | | 250 | | | ns |
| Write timing | | | | | | |
| $t_{DIS}$ | Data in setup time | | 20 | | | ns |
| $t_{DIH}$ | Data in hold time | | 10 | | | ns |
| $t_{EH}$ | Enable hold time | | 20 | | | ns |
| Read timing | | | | | | |
| $t_{DIHZ}$ | Data in to high impedance delay | time for the µC to release the DATAIO bus | | | 45 | ns |
| $t_{DOS}$ | Data out setup time | | 130 | | | ns |
| $t_{DOH}$ | Data out hold time | | 135 | | | ns |
| $t_{DOD}$ | Data out delay | | | | 80 | ns |
| $t_{DOHZ}$ | Data out to high impedance delay | time for the SDI to release the DATAIO bus | | | 80 | ns |
| Timing parameters when leaving the Power Down Mode (for determination of CLK polarity and MCCLK behavior) | | | | | | |
| $t_{CS}$ | Clock setup time (CLK polarity) | Setup time of CLK with respect to ENABLE rising edge | 20 | | | ns |
| $t_{CHD}$ | Clock hold time (CLK polarity) | Hold time of CLK with respect to ENABLE rising edge | 20 | | | ns |
| $t_{MS}$ | Data in setup time (MCCLK behavior) | DATAIO setup time with respect to ENABLE rising edge | 20 | | | ns |
| $t_{MH}$ | Data in hold time (MCCLK behavior) | DATAIO hold time with respect to ENABLE rising edge | 20 | | | ns |

# 8 Detailed System Description

The AS3977 is based on a fully integrated sigma-delta controlled fractional-N synthesizer phase locked loop (PLL) and a power amplifier (PA). A reference frequency generator including a crystal oscillator provides the comparison frequency of the PLL and a high-precision clock output. A programmable Gaussian filter enables to minimize the occupied bandwidth and adjacent channel power. A temperature sensor with digital read-out is included that allows compensation of the crystal frequency drift due to temperature variation. An on-chip low drop out regulator (LDO) is available in case an accurate output power independent of supply voltage variation is required. A second LDO for the digital supply voltage helps to minimize interference between the analog and digital part and decreases the current consumption of the digital part. A PROM enables the compensation of process variation. The AS3977 is controlled by an external microcontroller via a bi-directional serial digital interface (SDI).

## 8.1 Reference Frequency Generator

The reference frequency generator consists of a crystal oscillator and frequency divider. The crystal oscillator can be driven externally in case an external clock frequency is supplied.

## 8.2 Phase Locked Loop

The PLL is of standard charge pump type. The phase frequency detector is designed such that dead zone problems are avoided. The charge pump current is programmable. All loop filter components are on-chip, the bandwidth is programmable through the charge pump current. The differential based voltage controlled oscillator (VCO) has integrated inductors and varactors. The VCO operates at a center frequency around 1.8GHz. To cover the specified frequency range over process variation, the sufficiently wide overall tuning range is split into 16 overlapping frequency bands. At start up of the PLL, an automatic range select circuit (ARS) selects the proper frequency band. The VCO output frequency is divided by 2, 4, and 6, which enables to cover output frequencies in the range of 850 – 928 MHZ, 425 – 450 MHz and 300 – 320 MHz, respectively. A lock detector enables to monitor the PLL lock status.

## 8.3 Gaussian Filter and Digital Modulator

The programmable sigma-delta modulator controls the output frequency of the PLL. The order of the modulator is programmable (MASH2 or MASH3). In combination with the programmable Gaussian filter for the data signal, the modulator performs the FSK modulation with programmable deviation, whereby the Gaussian Filter enables to minimize the occupied bandwidth and the adjacent channel power.

## 8.4 Power Amplifier

The power amplifier is single ended and consists of a preamplifier and an output stage, both with open collector. The necessary external chokes can be connected to a LDO in case an accurate output power independent of supply voltage variation is required. The output power is programmable up to 10dBm.

## 8.5 Temperature Sensor

The AS3977 includes a temperature sensor to measure the absolute temperature inside the chip. The analog value is converted to a digital value and can then be read out by the microcontroller in order to control the output frequency and/or the transmission power. The value of the chip temperature in degree can be obtained using following formula:

$$Temperature = TS < 9...0 > * 0.19 - 50 \quad (EQ\ 1)$$

The temperature sensor can be used to compensate the crystal drift over temperature.

**Note:** AS3977 has the same temperature than the crystal only at start up and the temperature will increase immediately thereafter due to self heating.

Temperature sensor must be used only in the Clock Enable Mode as a stand alone block. It is mandatory to be used with the PLL and Power Amplifier switched off.

## 8.6 Low Power Reset

The low power reset (LPR) disables the power amplifier, if the supply voltage falls below the low power threshold.

## 8.7 Low Drop Out Regulators

In order to avoid stability issues, external capacitors are required. (see Table 1)

## 8.8 SDI / Control Interface

This interface enables a serial and synchronous communication between external microcontroller and AS3977. Data can be written to and read out from AS3977. Additionally, it facilitates the transmission of TX-data. The rising edge on the SDI enable signal (transition to the active state), while the device is in Power Down Mode has various effects on the circuit:

- It wakes up the crystal oscillator (this takes maximum 1.5 ms with the specified Crystal parameters)
- It sets the transfer and sampling edge of the AS3977 SDI data signal.
- It activates the Micro Controller clock output depending on the register setting and the value of the data signal.

Thus, the wakeup event through the SDI interface determines the basic communication between AS3977 and the microcontroller. In addition it takes some time to have a stable crystal oscillator clock available. Therefore all functions that require a stable crystal oscillator clock are not immediately available after the wakeup.

## 8.9 Baud Rate Generator

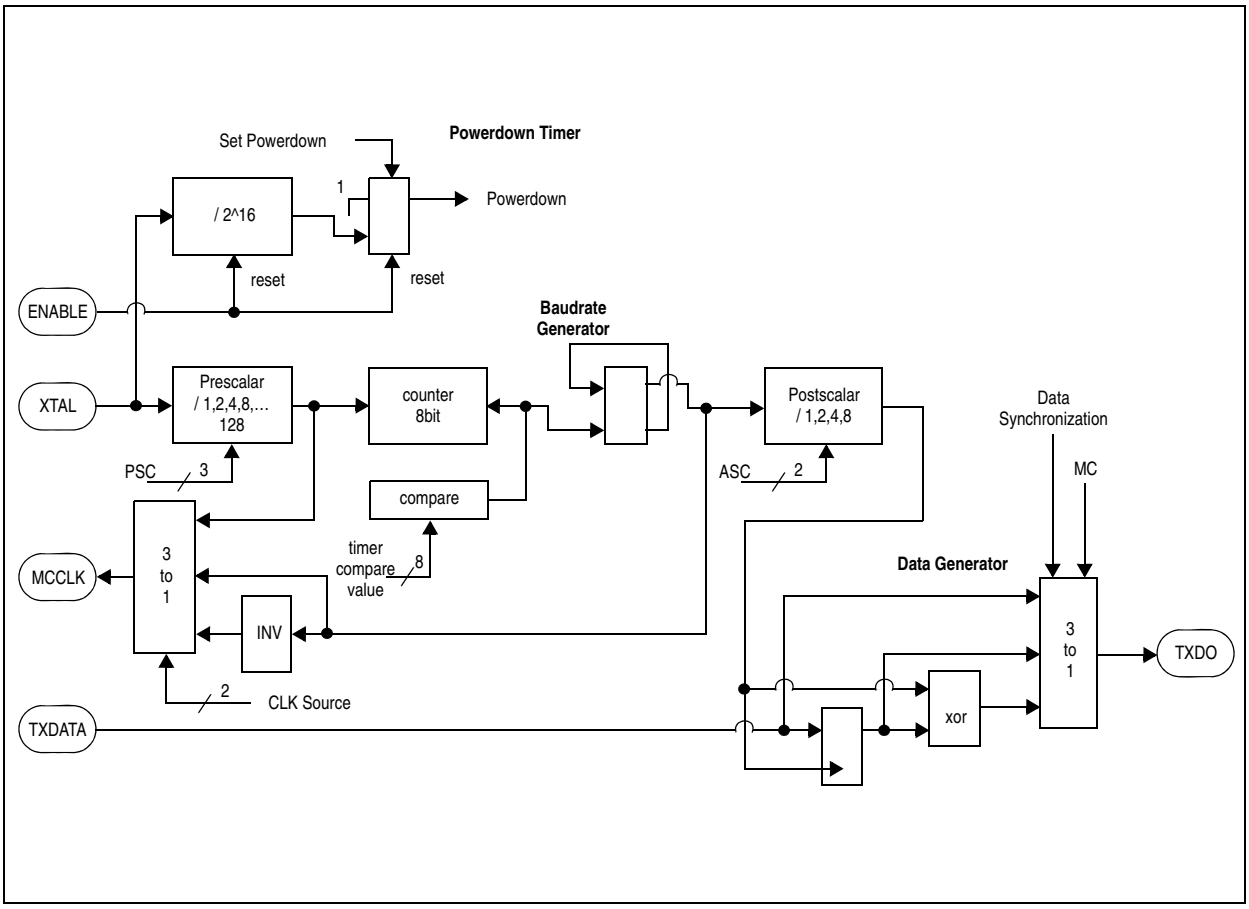
This module generates two clocks; one used for the microcontroller (MCCLK) and one as baud rate clock with 50% duty cycle. The baud rate clock is used by the microcontroller to properly synchronize the provided data during transmission with the internal Manchester coder.

The baud rate generator maintains the behavior of MCCLK and keeps it properly synchronized to the TX data clock. For example, a missing synchronization can occur when clock settings are changed by an asynchronous event like SDI programming or when a new transmission starts.

The Baud rate generator offers different types of data outputs: one fully asynchronous, one synchronous and one synchronous but Manchester coded. By means of AS3977 command control Byte, any of the three different output data types can be selected.

# 9 Application Information

*Figure 5. Functional Description Diagram of Timers and Data Synchronization*




The Prescaler divides the XTAL frequency by $f_{OUT}=2^{-PSC<2:0>}*f_{IN}$

The Compare timer divides by $f_{OUT}=f_{IN}/(TCV+1)$ and the Postscaler divides the input frequency by $f_{OUT}=2^{-ASC<1:0>}*f_{IN}$ which leads into a data frequency of:

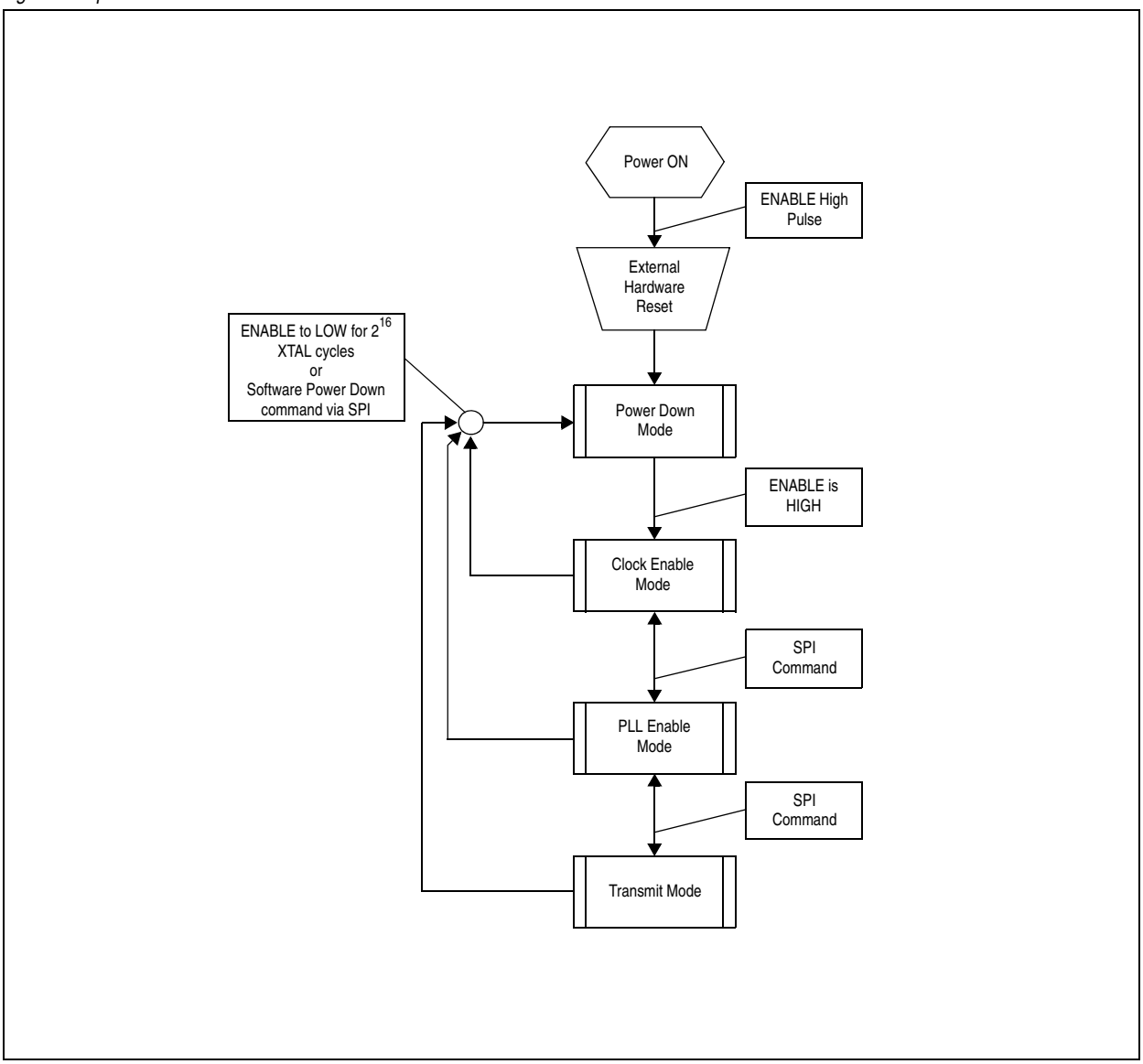
$$f_{OUT}=2^{-(PSC<2:0>+ASC<1:0>+1)} * f_{IN} / (TCV+1) \quad \text{(EQ 2)}$$

## 9.1 Operation Modes

All modes are controlled by the SDI interface.

- **Power Down Mode**
  The AS3977 is connected to the power supply and can be switched to power down mode. The current consumption is limited by the leakage current.
- **Clock Enable Mode**
  In this mode, only the reference frequency generator is switched on and a clock signal is supplied via the clock output.
- **PLL Enable Mode**
  The PLL is switched on and locked at the selected output frequency. The power amplifier is in power down mode. This mode enables OOK-ASK modulation by switching the PA on and off.
- **Transmit Mode**
  The PLL is switched on and locked at the selected output frequency. The power amplifier is in power on mode. This is the FSK mode for transmitting data.

*Figure 6. Operation Mode Relations*




## 9.2 Transmitter Control Interface

The AS3977 is controlled by an external micro controller (µC) via. a bi-directional communication interface (serial digital interface, SDI). The SDI enables data to be read from and written to internal control registers without the necessity of an internal clock signal. Analog de-bouncing of clock and data input is implemented in order to improve the overall system reliability.

The SDI-control interface includes a state machine, which expects a command control word as first byte and in reference to this byte, the interface is configured as write, read, or transmit operation. This method enables an effective and easy control of basic transmitter functions. Four preset independent output frequencies and two preset independent output power levels and modulation types can be selected using the control-command byte, thus enabling fast channel hopping and/or fast changes to the output power level and modulation type. The selection of the active output frequency and/or power level and modulation type is done using the so-called command byte.

As an additional feature, the AS3977 provides a configurable clock signal derived from the crystal frequency. The purpose of this clock signal is to provide a µC clock and to enable data synchronization.

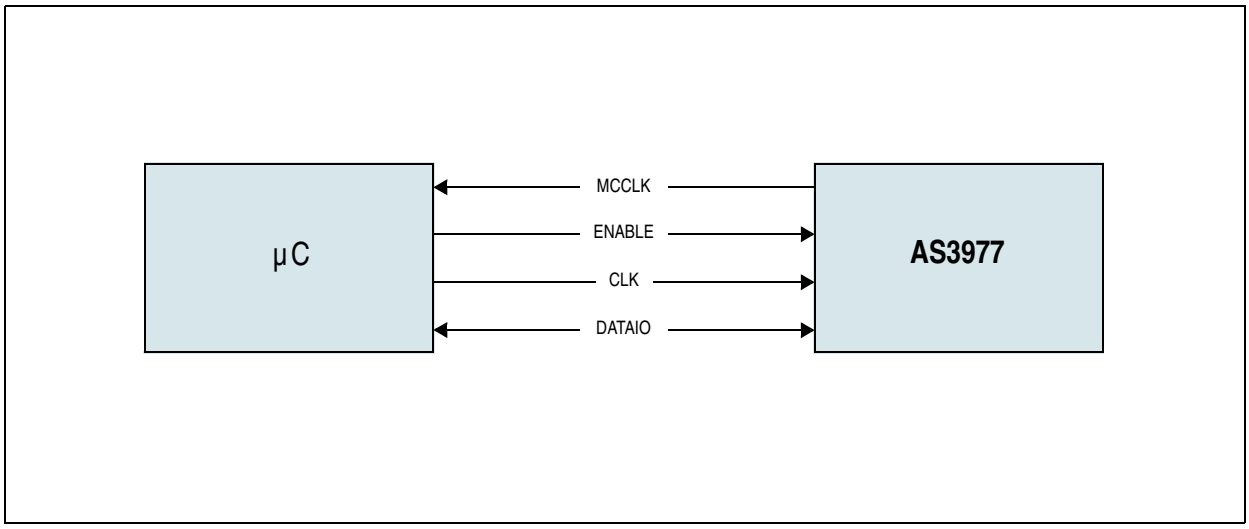
A timer is included to power down (Power Down Mode) the transmitter after a certain time, which is defined as $2^{16}$ multiplied with the crystal oscillator- Period.

### 9.2.1 Configuration Diagram

The interface has one clock signal for the external µC and the SDI input clock. As the MCCLK line can be used to clock the SDI Interface as well as must have a high impedance pin during the clocking phase of the microcontroller, the Pin must be bi-directional. The pad behavior is selected by configuration bits and by setting the SDI DATA-IO Line of the SDI interface when leaving PD. Possible configurations between the interface and the µC are done using 4 wires as shown in Figure 7.

MCCLK is simply connected to the micro controller and can be used to clock a timer or interrupt logic.

*Figure 7. Configuration Diagram*




A connection using a set of three wires is required to implement the SDI protocol.

- ENABLE signal is used to activate the interface and to wake up the whole IC. In addition, the rising edge of the ENABLE after power down mode is used to set the starting point of the communication protocol.
- CLK represents the SDI clock and both edges can be used for data transfer, dependable on the configuration after wake-up.
- DATAIO is a bi-directional signal that goes from microcontroller to the Interface during write and transmit-commands, while it is in the other direction when the interface is sending data read from the micro controller.

The interface supports the following functionality for the micro controller clock output (MCCLK).

- MCCLK can be inactive (MCCLK level not defined), always active after start-up (MCCLK is clocking) or clocking only during transmit.
- It is possible to configure and to maintain MCCLK settings (even when leaving PD).
- Maximum frequency is specified to $f_{XOSC}$ (by using the prescaler output with a division ratio of 1, PSC=0).
- Minimum frequency is $f_{XOSC}$ / 65280 (by using the baud rate generator output with prescaler division ratio of 128 and timer counter value of 255).

The rising edge of ENABLE after a Power Down Mode selects the transfer edge of the SDI-CLK by sampling the SDI clock value itself. This configuration will be valid until the next PD. Each bit must be transferred and sampled according to the configured edges. For example, if at the first rising edge of SDI enable SDI clock is LOW, then each bit is transferred from the microcontroller on the rising edge of SDI clock and it is sampled from AS3977 on falling edge of the SDI clock. This is valid for read as well as for write commands.

During the first byte of the WRITE command communication (command and address), the SDI master drives each new data bit on the transfer active edge and the SDI slave samples it on the next opposite edge. This protocol will be valid until the last data bit has been written to the external registers. Data' are transferred to the registers byte by byte after sampling of the last bit.

It is not necessary to enter the PD mode for reset the Interface. The rising edge of SDI-ENABLE signal starts the communication.

When the command is READ, a direction change on the SDI data wire will be done. This change has to be performed synchronously on SDI master and slave side, however, the master always provide the SDI clock. After sampling the last addressed bit, the SDI slave pin becomes active on the following SDI clock edge and the first readable bit read is transferred from SDI slave to the master.

In any case, the SDI master has to reset the SDI interface on the last bit of the data in order to stop the communication by applying an Enable LOW pulse (duration: min > 1 SDI CLK cycle, max: < $1/f_{crystal} * 2^{16}$).

### 9.2.2 Power On Reset

For stable start up of the AS3977 and to avoid unwanted crystal oscillation, it is strongly recommended to perform a power on reset (Hardware Reset Method). This can be performed as described in Table 19 and must be carried out every time when the supply voltage is less than the minimum allowed value (see Operating Conditions on page 8).

*Table 19. Power On Reset*

| Step | Hardware Reset Method |
|---|---|
| 1 | Apply Power to the AS3977 |
| 2 | Apply Enable high pulse (Low-High-Low transition) |
| 3 | Power on reset complete after xtal start up + $2^{16}$ xtal cycles |

### 9.2.3 Writing of Data to Addressable Registers

When the Power Down Mode is left, the level of CLK at the rising edge of ENABLE determines the sampling edge of CLK. If CLK is low, when ENABLE rises, DATAI is sampled at the falling edge of CLK (see Figure 8 and Figure 9), if CLK is high when ENABLE rises, DATAI is sampled at the rising edge of CLK.

An Enable LOW pulse indicates the end of the WRITE command after register has been written.

Figure 8 illustrates a write command in which the initialization of DATAIO take over condition is done at the falling edge of CLK signal.

*Figure 8. Writing of a Single Byte (falling edge sampling)*

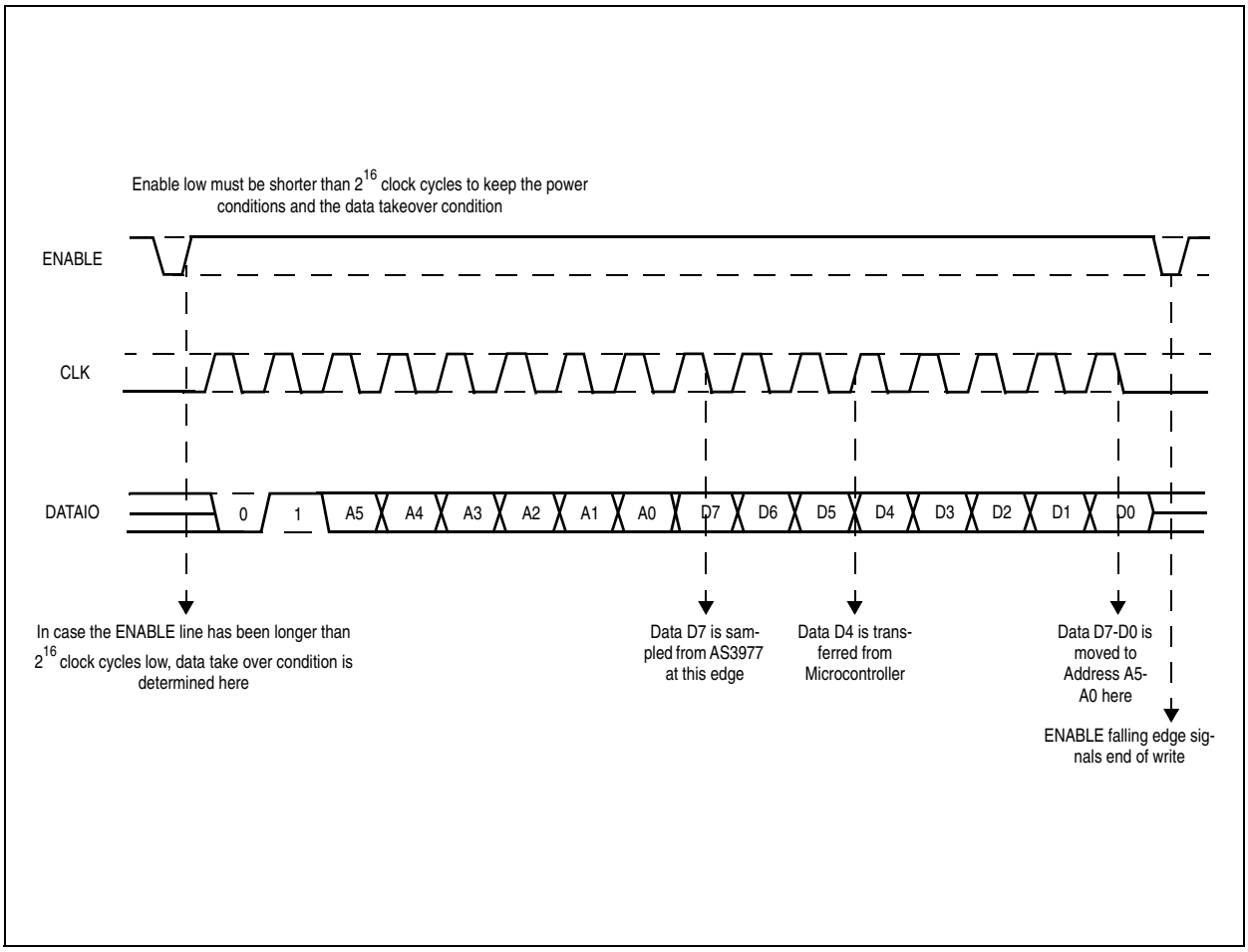
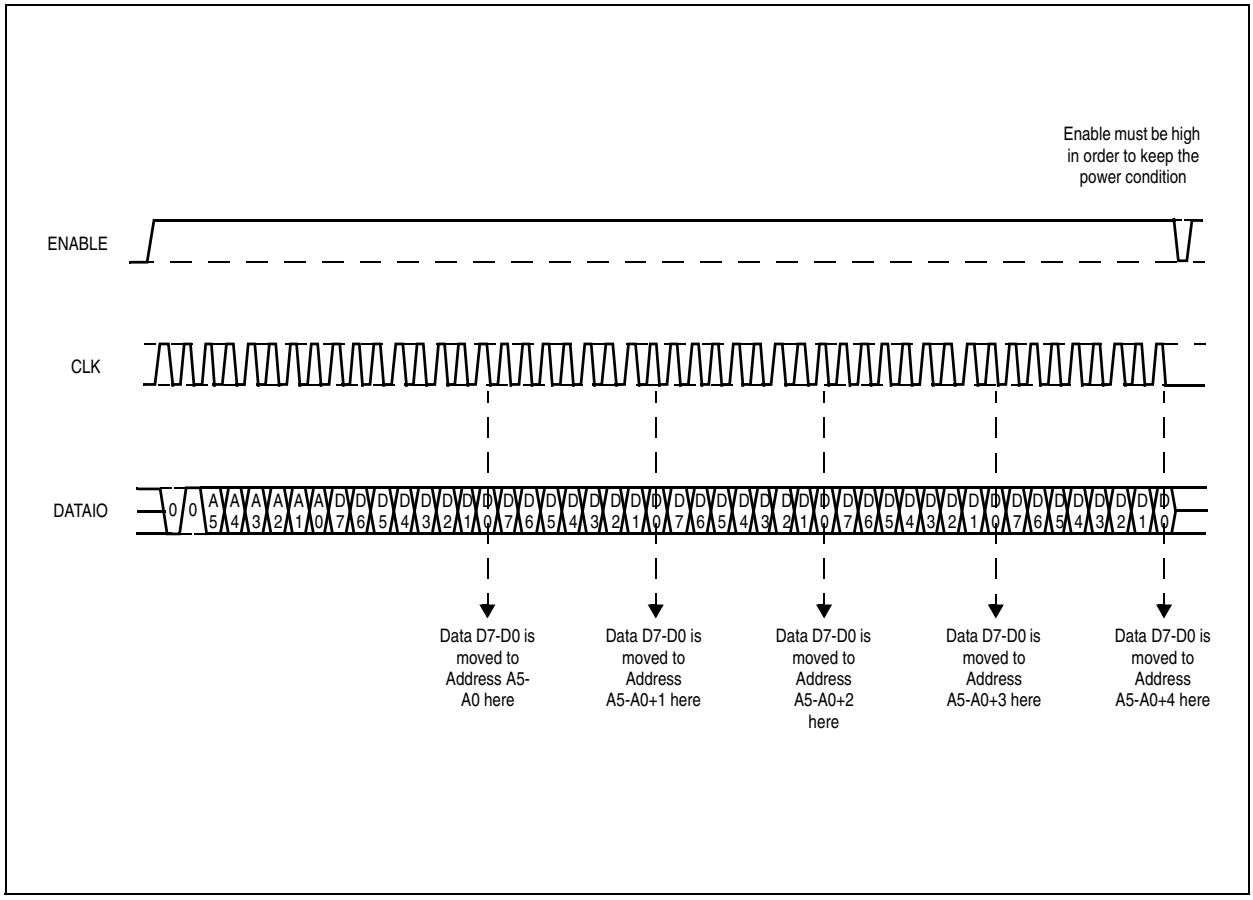


*Figure 9. Writing of Data with Auto-Incrementing Address*




### 9.2.4 Reading of Data from Addressable Registers

By leaving the Power Down Mode through a rising edge of ENABLE, the level of CLK determines the sampling edge of CLK. If CLK is low, DATAI is sampled at the falling edge of CLK (see Figure 10 and Figure 11), if CLK is high when ENABLE rises, DATAI is sampled at the rising edge of CLK. Consequently, data to be read from the microcontroller are driven by the slave (AS3977) at the transfer edge and sampled by the master (µC) at the sampling edge of CLK. An Enable LOW pulse has to be performed after register data has been transferred in order to indicate the end of the READ command and prepare the Interface to the next command control Byte.

The command control Byte for a read command consists of a command code and an address. The Command code has to be provided from least significant bit (LSB) to most significant bit (MSB), e.g. for a read it is <C0, C1> = “01”. After the command code, the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred from the SDI slave to the master, always from the MSB to the LSB. To transfer bytes from consecutive addresses, SDI master has to keep the SDI enable signal high and the SDI clock has to be active as long as data need to be read from the slave.

Each bit of the command and address sections of the frame have to be driven by the SDI master on the SDI clock transfer edge and the SDI slave samples it on the next SDI clock edge. Each bit of the data section of the frame has to be driven by the SDI slave on the SDI clock transfer edge and the SDI master on the next SDI clock edge samples it. These edges are selected on the first access after PD and they cannot be changed until next PD.

If the read access is interrupted (by de-asserting the SDI enable signal), data provided to the master is consistent to given address, but it is only the register content from MSB to LSB. If more SDI clock cycles are provided, data remains consistent and each data byte belongs to given or incremented address.

In the following figures (Figure 10 and Figure 11), two examples for a read command (without and with address self-increment) are given. The initialization base for this timing diagram is a “LOW” on the CLK line during Initialization.

*Figure 10. Reading of a Single Byte (falling edge sampling)*

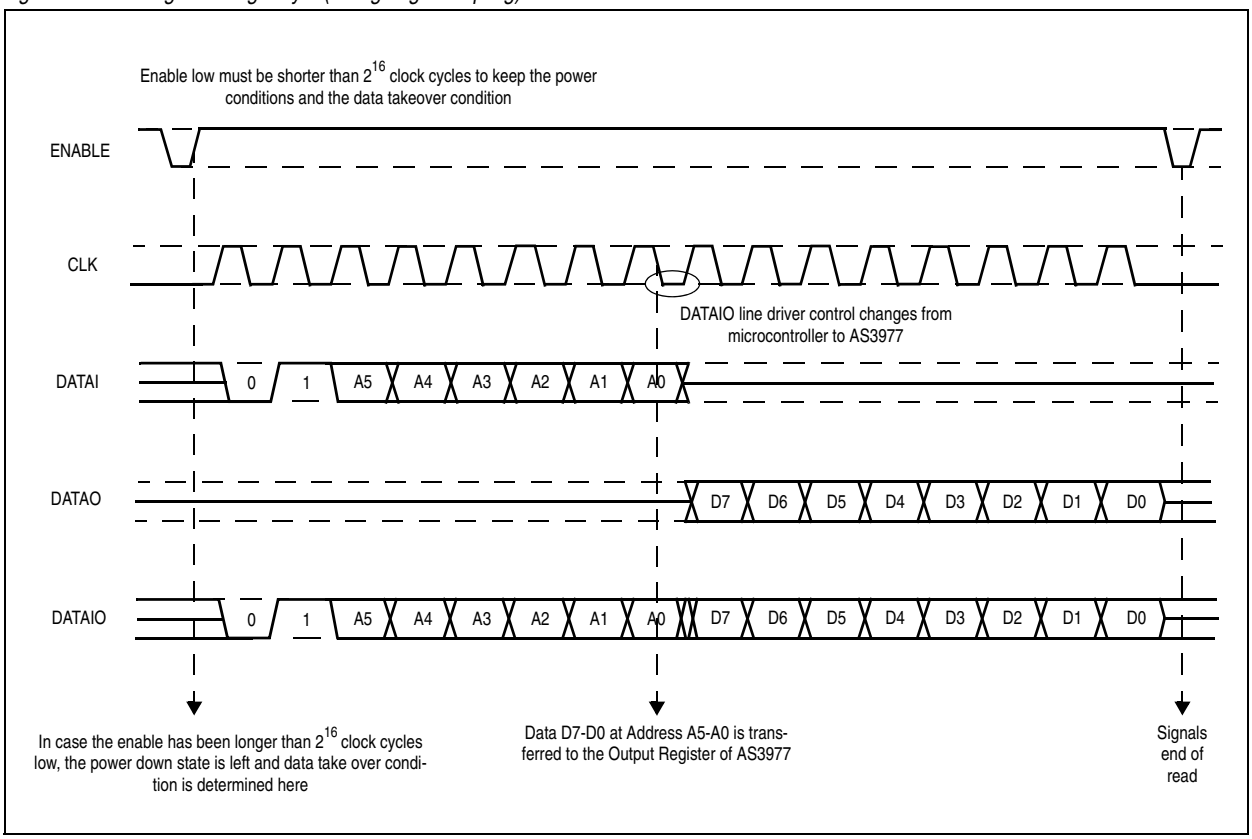
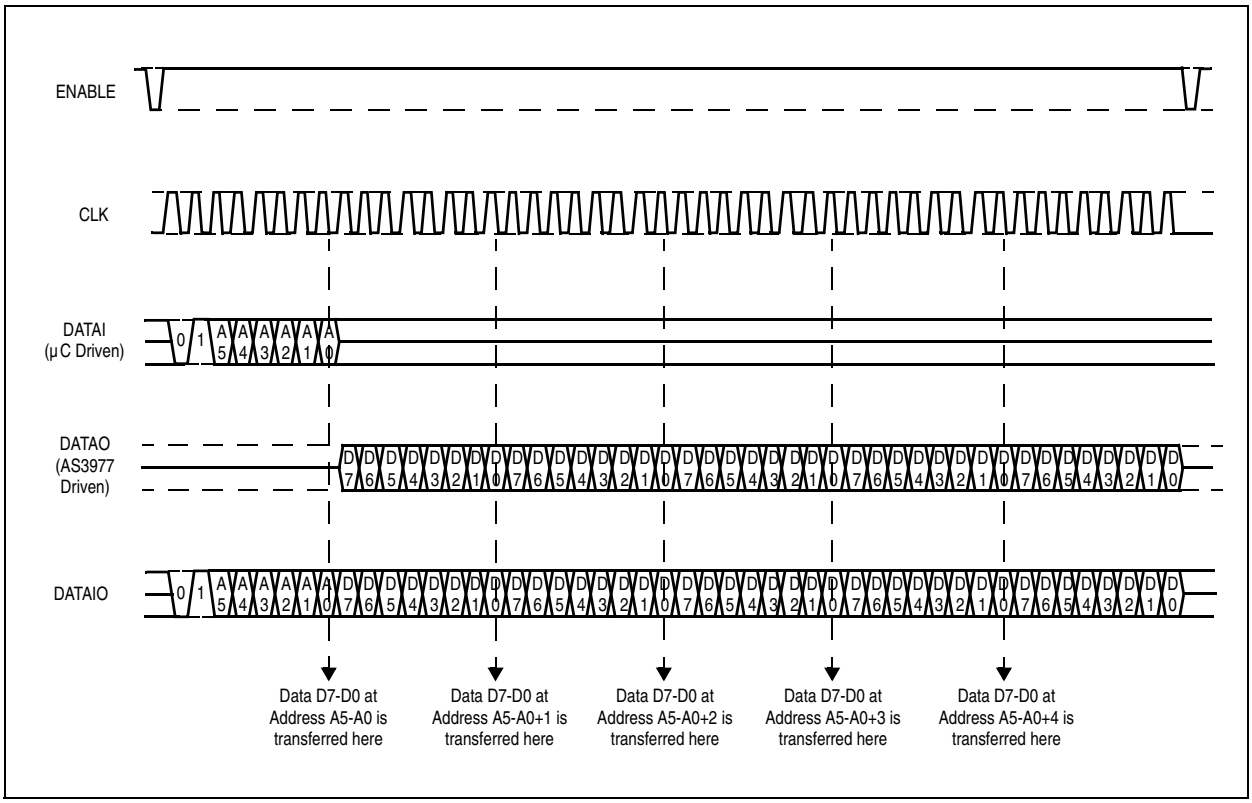



*Figure 11. Reading of Data with Auto-Incrementing Address*



### 9.2.5 Transmitting Data

Command code has to be provided from LSB to MSB and for transmit it is <C0, C1> = “11”. After the command code, further configuration has to be provided from the MSB to the LSB. Then a bit-stream, the data to be sent, can be transferred from the SDI master by keeping SDI enable signal to high. No SDI clock is required for data synchronization or the input bit stream.

Each bit of the command and address sections of the frame have to be driven by the SDI master on the SDI clock transfer edge and the SDI slave on the next SDI clock edge samples it.

The transmission starts as follows:

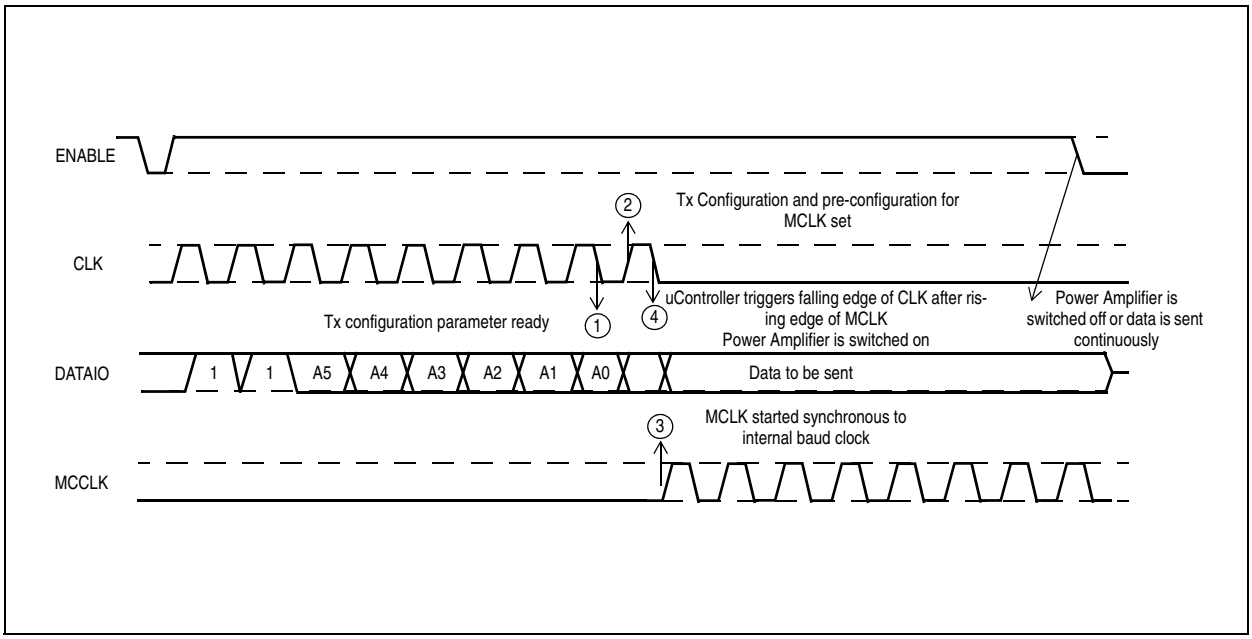
After the last configuration bit has been sampled, the micro controller has to provide an additional SDI clock edge to activate the output amplifier. This allows the SDI state machine to switch to the TX status and to activate MCCLK. Then, together with the first TX data bit, the next SDI clock sampling edge provided by the master starts the transmission itself and powers on the analog output driver.

In case, the MCCLK output is properly configured, the transmission will be stopped by the microcontroller by setting the clock to a high impedance state and the MCCLK output of the Transceiver became active and takes over the communication of the Interface.

The power amplifier is switched on (if not already on) at the subsequent sampling edge of CLK after receiving the transmit command byte. This allows to delay the PAON signal, e.g. to enable locking of the PLL in case a channel hop has to be performed.

The following figure (Figure 12) shows an example (sampling falling edge) of the transmit command with MCCLK active during TX. It is important to note in this mode the sequence of events labelled 1-4 in the diagram, which lead to transmission. This mode allows the baud clock to be synchronized to the external data. In such a case, the synchronization (A5=1) bit should be set within the transmitter configuration.

*Figure 12. Transmit Command with MCCLK Active During Tx (falling edge sampling)*




## 9.3 Transmitter Control States

### 9.3.1 Power Down State

When the Power Down Mode is entered, the crystal oscillator ends running and two very important bits of the registers are set to their inactive values:

1. **Lock transmit:** which is set (1) during PD to forbid any transmission.

2. **Setpd:** it is reset (0) to avoid a locked Power Down Mode.

When the circuit is in Power Down Mode, the crystal oscillator and all the other analog/digital circuits are OFF. The transmitter interface is the only supplied circuit and it is sensitive to SDI signals. The current consumption is limited by the leakage current. The configuration registers do not alter as long as the minimum supply requirements are met. The state can only be left by the rising edge of ENABLE. The state can be entered either by setting the *set power down* bit (SETPD) via. SDI communication or by setting ENABLE low for more than $2^{16}$ XTAL cycles (Power Down Timer). When the Power Down Mode is left (by the rising edge of ENABLE), the crystal oscillator is activated.