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Revision History

4Gb(128M x 32) Low Power **DDR2 SDRAM**

AS4C128M32MD2A 134ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Dec. 2017

DDR2 Sync DRAM Features

- **Functionality**
  - VDD2 = 1.14–1.30V
  - VDDCA/VDDQ = 1.14–1.30V
  - VDD1 = 1.70–1.95V
  - Interface : HSUL_12
  - Data width : x32
  - Clock frequency range : max 533MHz
  - Four-bit pre-fetch DDR architecture
  - Eight internal banks for concurrent operation
  - Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
  - Bidirectional/differential data strobe per byte of data(DQS/DQS#).
  - DM masks write date at the both rising and falling edge of the data strobe
  - Programmable READ and WRITE latencies (RL/WL)
  - Programmable burst lengths: 4, 8, or 16
  - Auto refresh and self refresh supported
  - All bank auto refresh and per bank auto refresh supported
  - Clock stop capability
- **Configuration**
  - 128 Meg X 32 (16 Meg X 32 X 8 Banks).
- **Low Power Features**
  - Low voltage power supply.
  - Auto TCSR (Temperature Compensated Self Refresh).
  - PASR (Partial Array Self Refresh) power-saving mode.
  - DPD (Deep Power Down) Mode.
  - DS (Driver Strength) Control.
- **Timing – Cycle time**
  - 1.875ns @ RL = 8
  - 2.5ns @ RL = 6
  - 3.0ns @ RL = 5
- **Operating Temperature Ranges**
  - Industrial -40℃ to +85℃.
- **Package**
  - 134-Ball FBGA(10.0mm x 11.5mm x 1.0mm)

Table I. Ordering Information

Product part No.	Org	Temperature	Max Clock (MHz)	Package
AS4C128M32MD2A-18BIN	128M x 32	Industrial -40°C to 85°C	533	134-ball FBGA
AS4C128M32MD2A-25BIN	128M x 32	Industrial -40°C to 85°C	400	134-ball FBGA

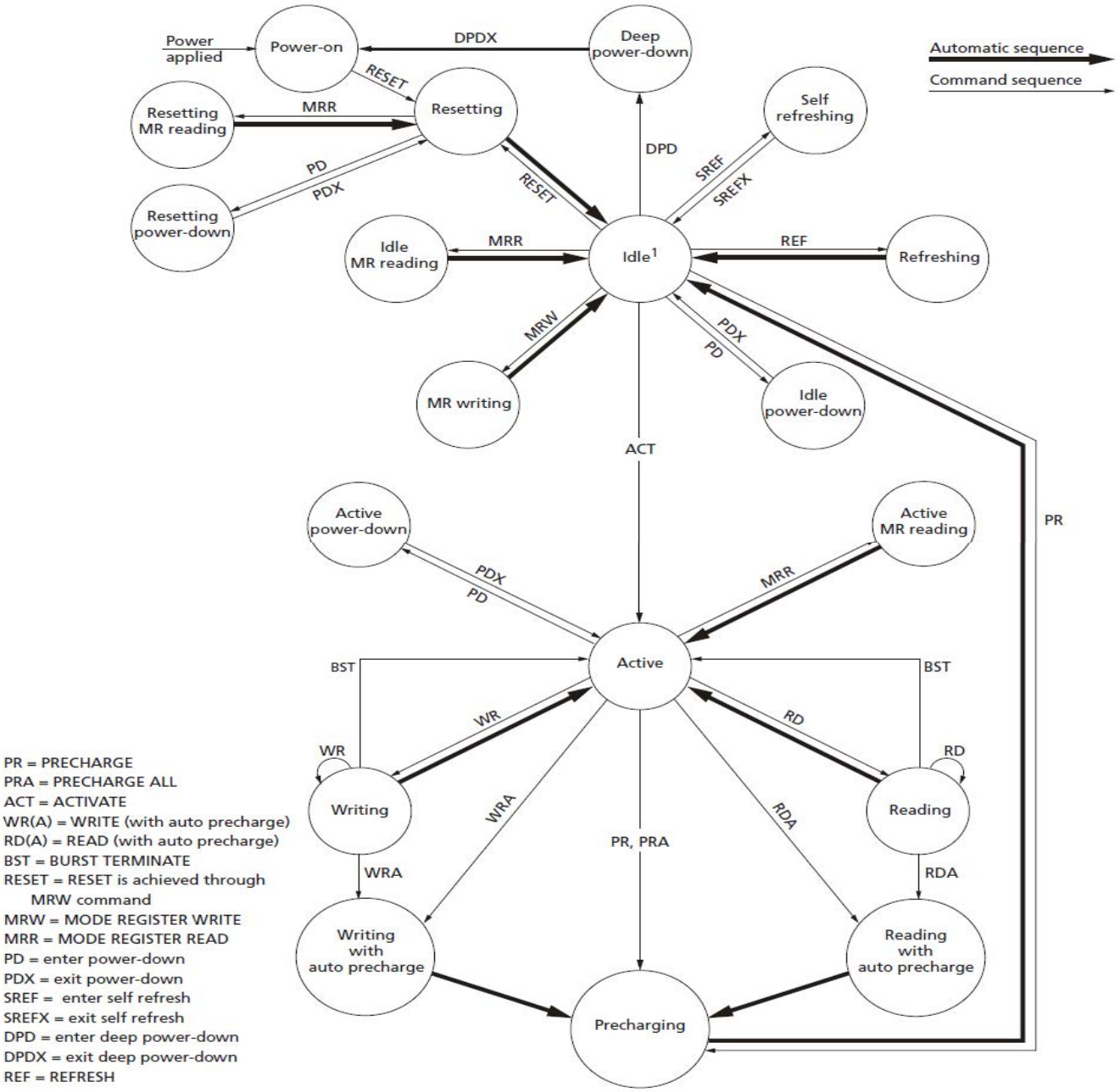
Table II. Speed Grade Information

Speed Grade	Clock Frequency	RL	WL	tRCD (ns)	tRP (ns)
DDR2L-800	400MHz	6	3	18	18
DDR2L-1066	533MHz	8	4	18	18

General Description

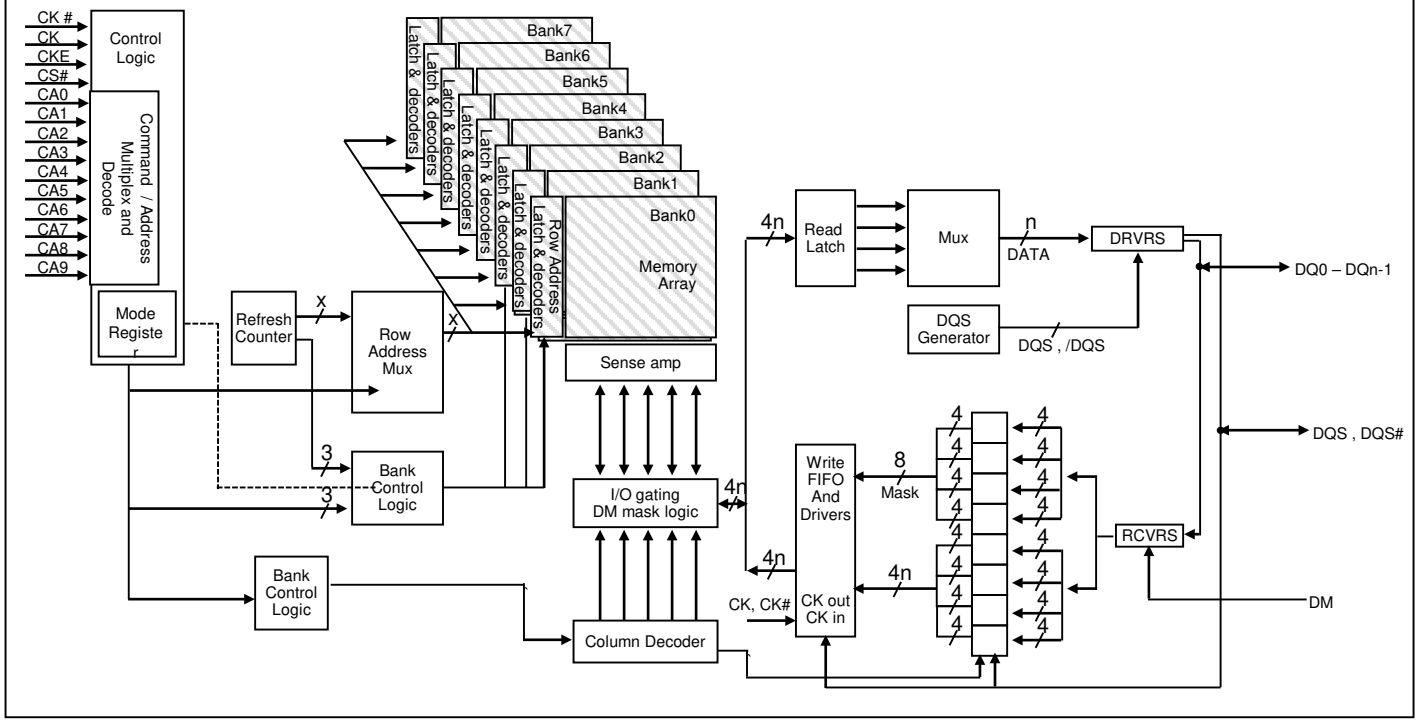
The 4Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 4,294,967,296 bits. The LPDDR2 device is internally configured as an eight-bank DRAM. Each of the x32's 4,294,967,296 bit banks is organized as 16,384 rows by 1024 columns by 32 bits.

Simplified Bus Interface State Diagram



Note: 1. All banks are precharged in the idle state.

Logic Block Diagram



Address Table

Parameter	128Mb X 32
Configuration	16Mb x 8banks x 32
Bank Address	BA0 ~ BA2
Row Address	R0 ~ R13
Column Address	C0 ~ C9

Note : 1. The least-significant column address CA0 is not transmitted on the CA bus, and is implied to be zero.

Pin Description

Symbol	Type	Description
CK, CK#	Input	**Clock :** CK and CK# are differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE	Input	**Clock enable :** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK.
CS#	Input	**Chip select :** CS# is considered part of the command code and is sampled at the rising edge of CK.
DM0–DM3	Input	**Input data mask :** DM is an input mask signal for WRITE data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ0 – DQ31	Input	**Data input/output :** Bidirectional data bus.
DQS0 – DQS3 DQS0# – DQS3#	I/O	**Data strobe :** The data strobe is bidirectional (used for read and write data) and complementary (DQS and DQS#). It is edge-aligned output with read data and centered input with write data. DQS[3:0]/DQS[3:0]# is DQS for each of the four data bytes, respectively.
CA0 – CA9	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
VDDQ	Supply	**DQ Power** : Provide isolated power to DQs for improved noise immunity.
VSSQ	Supply	**DQ Ground** : Provide isolated ground to DQs for improved noise immunity.
VDDCA	Supply	**Command/address power supply :** Command/address power supply.
VSSCA	Supply	**Command/address ground :** Isolated on the die for improved noise immunity**.**
VDD1	Supply	**Core power :** Supply 1.
VDD2	Supply	**Core power :** Supply 2.
VSS	Supply	**Common ground**
VREFCA, VREFDQ	Supply	**Reference voltage :** VREFCA is reference for command/address input buffers, VREFDQ is reference for DQ input buffers.
ZQ0-ZQ1	Reference	**External impedance (240 ohm) :** This signal is used to calibrate the device output impedance for S4 devices.
DNU	–	**Do not use :** Must be grounded or left floating.
NC	–	**No connect :** Not internally connected.
(NC)	–	**No connect :** Balls indicated as (NC) are no connects, however, they could be connected together internally.

Functional Description

Mobile LPDDR2 is a high-speed SDRAM internally configured as a 8-bank memory device. LPDDR2 devices use a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system.

The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

LPDDR2 devices use a double data rate architecture on the DQ pins to achieve high-speed operation. The double data rate architecture is essentially a 4*n* pre-fetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or WRITE access for the LPDDR2 effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command followed by a READ or WRITE command. The address and BA bits registered coincident with the ACTIVATE command are used to select the row and bank to be accessed.

The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Power-Up

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory (see Figure1). Power-up and initialization by means other than those specified will result in undefined operation.

1. Voltage Ramp

While applying power (after Ta), CKE must be held LOW (≤0.2 ×V_{DDCA}), and all other inputs must be between V_{ILMIN} and V_{IHMAX}. The device outputs remain at High-Z while CKE is held LOW. On or before the completion of the voltage ramp (Tb), CKE must be held LOW. DQ, DM, DQS, and DQS# voltage levels must be Between VSSQ and VDDQ during voltage ramp to avoid latch-up. CK, CK#, CS#, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch up.

The following conditions apply for voltage ramp :

- Ta is the point when any power supply first reaches 300mV.
- Noted conditions apply betweenTa and power-down (controlled or uncontrolled).
- Tb is the point at which all supply and reference voltages are within their defined operating ranges.
- Power ramp duration tINIT0 (Tb -Ta) must not exceed 20ms.
- For supply and reference voltage operating conditions, see the Recommended DC Operating Conditions table.
- The voltage difference between any ofVSS,VSSQ, andVSSCA pins must not exceed 100mV.

Voltage Ramp Completion.

After Ta is reached :

- VDD1 must be greater than VDD2 - 200mV
- VDD1 and VDD2 must be greater than VDDCA—200mV
- VDD1 and VDD2 must be greater than VDDQ—200mV
- V_{REF} must always be less than all other supply voltages

Beginning at Tb, CKE must remain LOW for at least tINIT1=100ns, after which CKE can be asserted HIGH. The clock must be stable at least tINIT2 = 5 × tCK prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS#, and CA inputs must observe setup and hold requirements (tIS, tIH) with respect to the first rising clock edge (and to subsequent falling and rising edges). If any MRRs are issued, the clock period must be within the range defined for tCKb(18ns to 100ns). MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least tINIT3=200µs (Td).

2. RESET Command

After tINIT3 is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least tINIT4 while keeping CKE asserted and issuing NOP commands.

3.MRRs and Device Auto Initialization (DAI) Polling

After tINIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications (see Power-Down (page 53)).

The MRR command can be used to poll the DAI bit, which indicates when device auto initialization is complete; otherwise, the controller must wait a minimum of tINIT5, or until the DAI bit is set, before proceeding. Because the memory output buffers are not properly configured by Te, some AC parameters must use relaxed timing specifications before the system is appropriately configured. After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than tINIT5 after the RESET command. The controller must wait at least tINIT5 or until the DAI bit is set before proceeding.

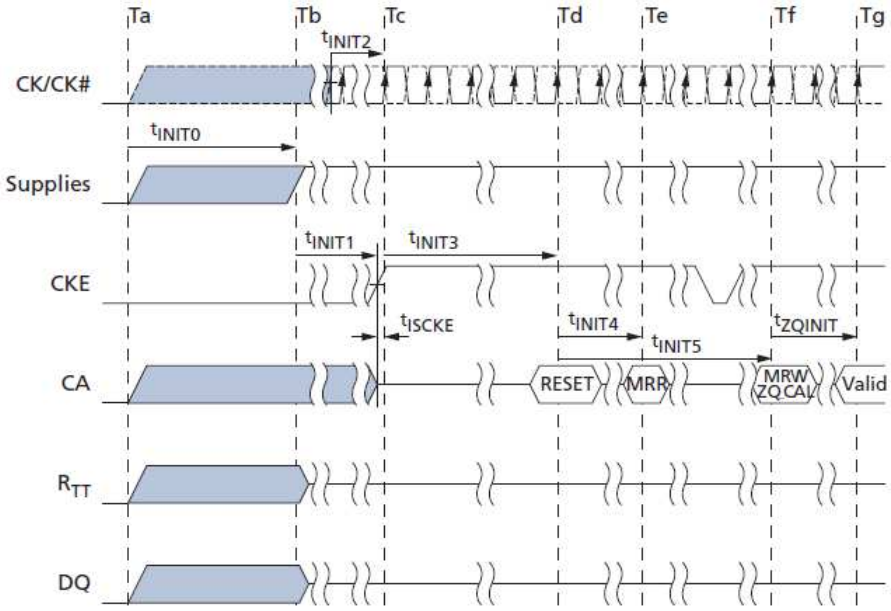
4.ZQ Calibration

After tINIT5 (Tf), the MRW initialization calibration (ZQ calibration) command can be issued to the memory (MR10).
This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one Mobile LPDDR2 device exists on the same bus, the controller must not overlap MRW ZQ calibration commands.
The device is ready for normal operation after tZQINIT.

5.Normal Operation

After (Tg), MRW commands must be used to properly configure the memory (output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration. After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in Input Clock Frequency Changes and Clock Stop with CKE HIGH (page 62).

Figure 1 : Voltage Ramp and Initialization Sequence



Note : 1. High-Z on the CA bus indicates valid NOP.

Table1 : Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	-	20	ms	Maximum voltage ramp time
tINIT1	100	-	ns	Minimum CKE LOW time after completion of voltage ramp
tINIT2	5	-	tCK	Minimum stable clock before first CKE HIGH
tINIT3	200	-	µs	Minimum idle time after first CKE assertion
tINIT4	1	-	µs	Minimum idle time after RESET command
tINIT5	-	10	µs	Maximum duration of device auto initialization
tZQINIT	1	-	µs	ZQ initial calibration (S4 devices only)
tCKb	18	-	ns	Clock cycle time during boot

Initialization After RESET (Without Voltage Ramp)

If the RESET command is issued before or after the power-up initialization sequence, the reinitialization procedure must begin at Td.

Power-Off

While powering off, CKE must be held LOW (≤0.2 ×VDDCA); all other inputs must be between V_{ILMIN} and V_{IHMAX}.
The device outputs remain at High-Z while CKE is held LOW. DQ, DM, DQS, and DQS# voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latch-up. CK, CK#, CS#, and CA input levels must be between VSSCA and VDDCA during the power-off sequence to avoid latch-up.
Tx is the point where any power supply drops below the minimum value specified in the Recommended DC Operating Conditions table. Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Required Power Supply Conditions Between Tx and Tz:

- VDD1 must be greater than VDD2 - 200mV.
- VDD1 must be greater than VDDCA - 200mV.
- VDD1 must be greater than VDDQ - 200mV.
- VREF must always be less than all other supply voltages.

The voltage difference between VSS,VSSQ, and VSSCA must not exceed 100mV.
For supply and reference voltage operating conditions, see Recommended DC Operating Conditions table.

Uncontrolled Power-Off

When an uncontrolled power-off occurs, the following conditions must be met:

- At Tx, when the power supply drops below the minimum values specified in the Recommended DC Operating Conditions table, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.
- After Tz (the point at which all power supplies first reach 300mV), the device must power off.
  The time between Tx and Tz must not exceed tPOFF. During this period, the relative voltage between power supplies is uncontrolled.
  VDD1 andVDD2 must decrease with a slope lower than 0.5V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table2 : Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Maximum power-off ramp time	tPOFF	-	2	Sec

Mode Register Definition

LPDDR2 devices contain a set of mode registers used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignments and Definitions

The MRR command is used to read from a register.The MRW command is used to write to a register. An “R” in the access column of the mode register assignment table indicates read-only; a “W” indicates write-only; “R/W” indicates read or WRITE capable or enabled.

Table3 : Mode Register Assignments

MR #	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00h	Device info	R	RFU			RZQI		DNVI	DI	DAI	go to MR0
1	01h	Device feature 1	W	*nWR (for AP)*			WC	BT	BL			go to MR1
2	02h	Device feature 2	W	RFU					RL and WL			go to MR2
3	03h	I/O config-1	W	RFU					DS			go to MR3
4	04h	SDRAM refresh rate	R	TUF	RFU				Refresh rate			go to MR4
5	05h	Basic config-1	R	LPDDR2 Manufacturer ID								go to MR5
6	06h	Basic config-2	R	Revision ID1								go to MR6
7	07h	Basic config-3	R	Revision ID2								go to MR7
8	08h	Basic config-4	R	I/O width		Density				Type		go to MR8
9	09h	Test mode	W	Vendor-specific test mode								go to MR9
10	0Ah	I/O calibration	W	Calibration code								go to MR10
11-15	0Bh≈0Fh	Reserved	-	RFU								go to MR11
16	10h	PASR_Bank	W	Bank mask								go to MR16
17	11h	PASR_Seg	W	Segment mask								go to MR17
18-19	12h–13h	Reserved	-	RFU								go to MR18
20-31	14h–1Fh	Reserved for NVM										go to MR30
32	20h	DQ calibration pattern A	R	See Table 28								go to MR32
33-39	21h–27h	Do not use										go to MR33
40	28h	DQ calibration pattern B	R	See Table 28								go to MR40
41-47	29h–2Fh	Do not use										go to MR41
48-62	30h–3Eh	Reserved	-	RFU								go to MR48
63	3Fh	RESET	W	X								go to MR63
64-126	40h–7Eh	Reserved	-	RFU								go to MR64
127	7Fh	Do not use										go to MR127
128-190	80h–BEh	Reserved for vendor use		RVU								go to MR128
191	BFh	Do not use										go to MR191
192-254	C0h–FEh	Reserved for vendor use		RVU								go to MR192
255	FFh	Do not use										go to MR255

Notes : 1. RFU bits must be set to 0 during MRW.

2. RFU bits must be read as 0 during MRR.

3. For READs to a write-only or RFU register, DQS will be toggled and undefined data is returned.

4. RFU mode registers must not be written.

5. WRITEs to read-only registers must have no impact on the functionality of the device.

Table4 : MR0 Device information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			RZQI		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read–only	OP0	0b : DAI complete 1b : DAI still in progress
DI (Device Information)	Read–only	OP1	0b : SDRAM 1b : NVM
DNVI (Data Not Valid Information)	Read–only	OP2	LPDDR2 SDRAM will not implement DNV functionality
RZQI(Built in Self Test for RZQ Information)	Read–only	OP[4:3]	00b : RZQ self test not executed 01b : ZQ-pin may connect to VDDCA or float 10b : ZQ-pin may short to GND 11b : ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)

Notes : 1. If RZQI is supported, it will be set upon completion of the MRW ZQ initialization calibration.

2. If ZQ is connected to VDDCA to set default calibration, OP[4:3] must be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 could indicate a ZQ-pin assembly error. It is recommended that the assembly error be corrected.
3. In the case of a possible assembly error(either OP[4:3]=01 or OP[4:3]=10, as defined above), the device will default to factory trim settings for RON and will ignore ZQ calibration commands. In either case, the system might not function as Intended.
4. If a ZQ self test returns a value of 11b, this indicates that the device has detected a resistor connection to the ZQ pin. Note that this result cannot be used to validate the ZQ resistor value, nor does it indicate that the ZQ resistor tolerance meets the specified limits (240 ohms ±1%).

Table5 : MR1 Device Feature 1 (MA[7:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write - only	OP[2:0]	010b : BL4 (default) 011b : BL8 100b : BL16 All others : reserved
BT	Write - only	OP3	0b : Sequential (default) 1b : Interleaved
WC	Write – only	OP4	0b : Wrap (default) 1b : No wrap (allowed for SDRAM BL4 only)
nWR	Write – only	OP[7:5]	001b : nWR = 3 (default) 010b : nWR = 4 011b : nWR = 5 100b : nWR = 6 101b : nWR = 7 110b : nWR = 8 All others : reserved

Note : 1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR / tCK).

Table6 : Burst Sequence by Burst Length(BL), Burst Type(BT), and Wrap Control(WC)

BL	BT	C3	C2	C1	C0	WC	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	46
4	Any	X	X	0b	0b	Wrap	0	1	2	3												
		X	X	1b	0b		2	3	0	1												
	Any	X	X	X	0b	No Wrap	*y*	*y*+1	*y*+2	*y*+3												
8	Seq	X	0b	0b	0b	Wrap	0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	4	5	6	7	0	1								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	0	1	2	3	4	5								
	Int	X	0b	0b	0b		0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	0	1	6	7	4	5								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	4	5	2	3	0	1								
	Any	X	X	X	0b	No Wrap	illegal (not supported)															
16	Seq	0b	0b	0b	0b	Wrap	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0b	0b	1b	0b		2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
		0b	1b	0b	0b		4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		0b	1b	1b	0b		6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
		1b	0b	0b	0b		8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1b	0b	1b	0b		A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
		1b	1b	0b	0b		C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
		1b	1b	1b	0b		E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
	Int	X	X	X	0b		illegal (not supported)															
	Any	X	X	X	0b	No Wrap	illegal (not supported)															

Notes : 1. C0 input is not present on CA bus. It is implied zero.

2. For BL = 4, the burst address represents C[1:0].

3. For BL = 8, the burst address represents C[2:0].

4. For BL = 16, the burst address represents C[3:0].

5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary.

The variable *y* can start at any address with C0 equal to 0, but must not start at any address shown in the following table.

Table7 : No – Wrap Restrictions

Bus Width	4Gb
Not across full page boundary	
X 16	3FE, 3FF, 000, 001*2
Not across sub page boundary	
X 16	1FE, 1FF, 200, 201*2

Notes : 1. No-wrap BL = 4 data orders shown are prohibited.
2. 2Gb x16, 2Chips

Table8 : MR2 Device Feature 2 (MA[7:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				RL and WL			

RL and WL	Write - only	OP [3:0]	0001b : RL=3 / WL=1 (default)
			0010b : RL=4 / WL=2
			0011b : RL=5 / WL=2
			0100b : RL=6 / WL=3
			0101b : RL=7 / WL=4
			0110b : RL=8 / WL=4
			All others : reserved

Table9 : MR3 I/O Configuration 1 (MA [7:0] =03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DS			

DS	Write - only	OP [3:0]	0000b : reserved
			0001b : 34.3 ohm typical
			0010b : 40 ohm typical
			0011b : 48 ohm typical
			0100b : 60 ohm typical
			0101b : reserved for 68.6 ohm typical
			0110b : 80 ohm typical
			0111b : 120 ohm typical
			All others : reserved

Table10 : MR4 Device Temperature (MA [7:0] =04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	RFU				SDRAM Refresh Rate		

SDRAM Refresh rate	Read - only	OP [2:0]	000b : SDRAM Low temperature operating limit exceeded.
			001b : 4x tREF, 4x tREFIpb, 4x tREFW.
			010b : 2x tREF, 2x tREFIpb, 2x tREFW.
			011b : 1x tREF, 1x tREFIpb, 1x tREFW (<= 85℃).
			100b : Reserved.

SDRAM Refresh rate	Read - only	OP [2:0]	101b : 0.25x tREF, 0.25x tREFIpb, 0.25x tREFW, do not de-rate SDRAM AC timing .
			110b : 0.25x tREF, 0.25x tREFIpb, 0.25x tREFW, de-rate SDRAM AC timing .
			111b : SDRAM High temperature operating limit exceeded.
Temperature Update Flag (TUF)	Read - only	OP7	0b : OP [2:0] value has not changed since last read of MR4.
			1b : OP [2:0] value has changed since last read of MR4.

RL and WL	Write – only	OP [3:0]	0001b : RL=3 / WL=1 (default)
			0010b : RL=4 / WL=2
			0011b : RL=5 / WL=2
			0100b : RL=6 / WL=3
			0101b : RL=7 / WL=4
			0110b : RL=8 / WL=4
			All others : reserved

Notes:

1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up
3. If OP2 equals '1', the device temperature is greater than 85℃
4. OP7 is set to'1' if OP2-OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP[2:0] = 000b or 111b.
6. LPDDR2 devices must be de-rated by adding 1.875ns to the following core timing parameters ; tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating value in AC timing table.
   Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
7. The recommended frequency for reading MR4 is provided in Temperature Sensor.

Table11 : MR5 Basic Configuration 1 (MA [7:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

LPDDR2 Manufacturer ID	Read-only	OP[7:0]	1111 1000b : (F8h)
			All others : Reserved

Table12 : MR6 Basic Configuration 2 (MA [7:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP[7:0]	0000 0000b : A-version

Table13 : MR7 Basic Configuration 3 (MA [7:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP[7:0]	0000 0000b : A-version

Table14 : MR8 Basic Configuration 4 (MA [7:0] = 08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read – only	OP [1:0]	00b : S4 SDRAM
Density	Read – only	OP [5:2]	0101b : 2Gb*1
I/O width	Read – only	OP [7:6]	01b : x16*1

Notes : 1. 2Gb x16, 2Chips .

Table15 : MR9 Test Mode (MA [7:0] = 09H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor – specific Test Mode							

Table16 : MR10 Calibration (MA [7:0] = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write - only	OP [7:0]	0xFF : Calibration command after initialization.
			0xAB : Long calibration
			0x56 : Short calibration
			0xC3 : ZQ Reset
			All others : Reserved

Notes : 1. Host processor must not write MR10 with reserved values.

2. The device ignores calibration commands when a reserved value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see MRW ZQ Calibration Commands (page 51)) or default calibration (through the ZQRESET command) is supported.
   If ZQ is connected to V_{DDCA}, the device operates with default calibration and ZQ calibration commands are ignored.
   In both cases, the ZQ connection must not change after power is supplied to the device.

Table17 : MR[11-15] Reserved (MA [7:0] = 0BH – 0FH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved							

Table18 : MR16 PASR Bank Mask (MA [7:0] = 10H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask (4-bank or 8-bank)							

Bank [7:0] Mask	Write - only	OP [7:0]	0b : Refresh enable to the bank = unmasked (default)
			1b : Refresh blocked = masked

Table19 : MR17 PASR Segment Mask (MA [7:0] = 11H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment	Write – only	OP [7:0]	0b : Refresh enable to the Segment = unmasked (default)
			1b : Refresh blocked = masked

Segment [7:0] Mask	OP	Segment Mask	R [13:11]
0	0	XXXXXXX1	000b
1	1	XXXXXX1X	001b
2	2	XXXXX1XX	010b
3	3	XXXX1XXX	011b
4	4	XXX1XXXX	100b
5	5	XX1XXXXX	101b
6	6	X1XXXXXX	110b
7	7	1XXXXXXX	111b

Table20 : Reserved Mode Register

Mode Register	MA	0	Restriction	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR[18:19]	MA[7:0]	12h-13h	RFU	Reserved							
MR[20:31]		14h-1Fh	NVM[1]								
MR[33:39]		21h-27h	DNU[1]								
MR[41:47]		29h-2Fh									
MR[48:62]		30h-3Eh	RFU								
MR[64:126]		40h-7Eh	RFU								
MR[127]		7Fh	DNU								
MR[128:190]		80h-BEh	RVU[1]								
MR[191]		BFh	DNU								
MR[192:254]		C0h-FEh	RVU								
MR[255]		FFh	DNU								

Note : 1. NVM = nonvolatile memory use only; DNU = Do not use; RVU = Reserved for vendor use.

Table21 : MR63 Reset (MA [7:0] = 3FH) – MRW Only

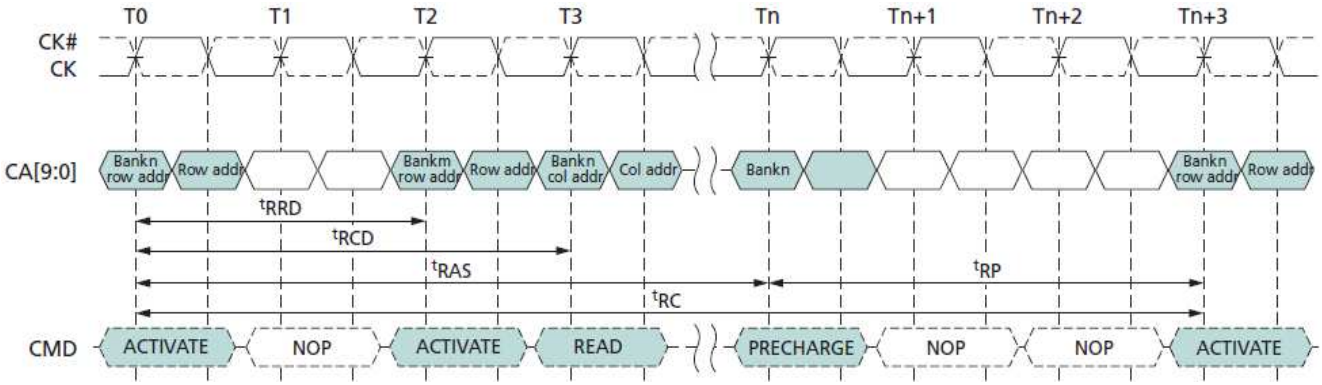
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

Note : For additional information on MRW RESET see MODE REGISTER WRITE Command (page 50).

ACTIVATE Command

The ACTIVATE command is issued by holding CS# LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock.
The bank addresses BA[2:0] are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at tRCD after the ACTIVATE command is issued. After a bank has been activated, it must be precharged before another ACTIVATE command can be applied to the same bank.The bank active and precharge times are defined as tRAS and tRP, respectively.
The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between ACTIVATE commands to different banks is tRRD.

Figure 2: ACTIVATE Command



Notes : 1. tRCD = 3, tRP = 3, tRRD = 2.
2. A PRECHARGE ALL command uses tRPab timing, and a single-bank PRECHARGE command uses tRPpb timing. In this figure, tRP is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE.

8-Bank Device Operation

Two rules regarding 8-bank device operation must be observed.
One rule restricts the number of sequential ACTIVATE commands that can be issued; the second provides additional RAS precharge time for a PRECHARGE ALL command.

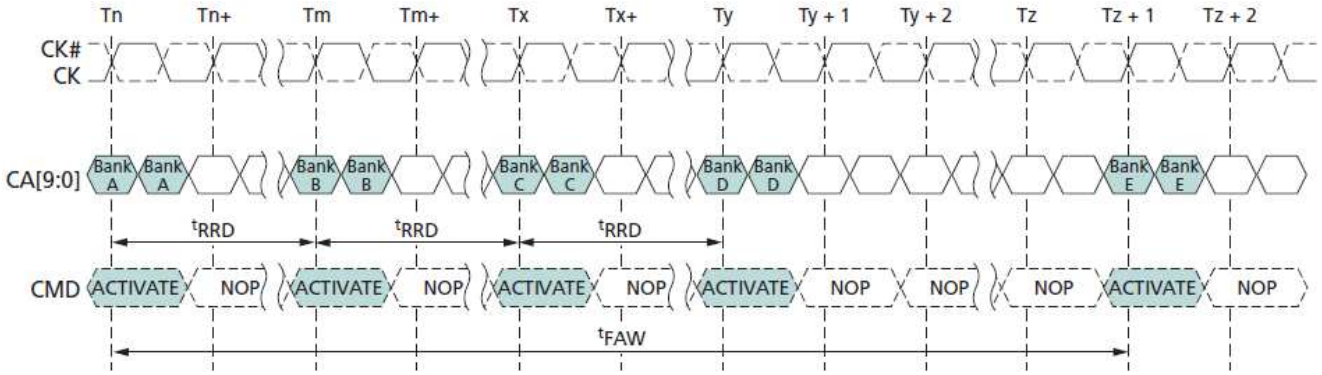
The 8-Bank Device Sequential Bank Activation Restriction :

No more than four banks can be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. To convert to clocks, divide tFAW[ns] by tCK[ns], and round up to the next integer value.
For example, if RU(tFAW/tCK) is 10 clocks, and an ACTIVATE command is issued in clock *n*, no more than three further ACTIVATE commands can be issued at or between clock *n* + 1 and *n* + 9. REFpb also counts as bank activation for purposes of tFAW.

The 8-Bank Device PRECHARGE ALL Provision:

tRP for a PRECHARGE ALL command must equal tRPab, which is greater than tRPpb.

Figure 3 : tFAW Timing (8-Bank Devices)



Note : 1. Exclusively for 8-bank devices.

Read and Write Access Modes

After a bank is activated, a READ or WRITE command can be issued with CS# LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW). A single READ or WRITE command initiates a burst READ or burst WRITE operation on successive clock cycles. A new burst access must not interrupt the previous 4-bit burst operation when BL = 4. When BL = 8 or BL = 16, READs can be interrupted by READs andWRITEs can be interrupted byWRITEs, provided that the interrupt occurs on a 4-bit boundary and that tCCD is met.

Burst READ Command

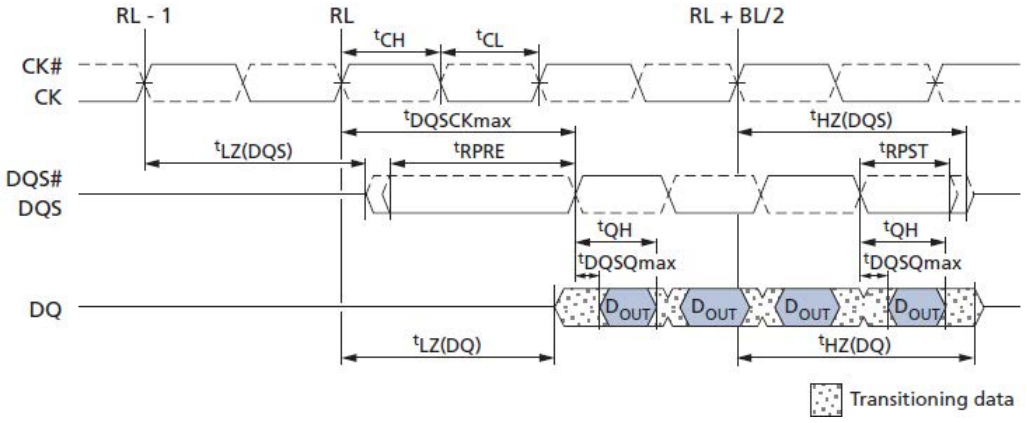
The burst READ command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the tDQSCK delay is measured.The first valid data is available RL × tCK + tDQSCK + tDQSQ after the rising edge of the clock when the READ command is issued.

The data strobe output is driven LOW tRPRE before the first valid rising strobe edge.

The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers.

Pin input timings for the data strobe are measured relative to the crosspoint of DQS and its complement, DQS#.

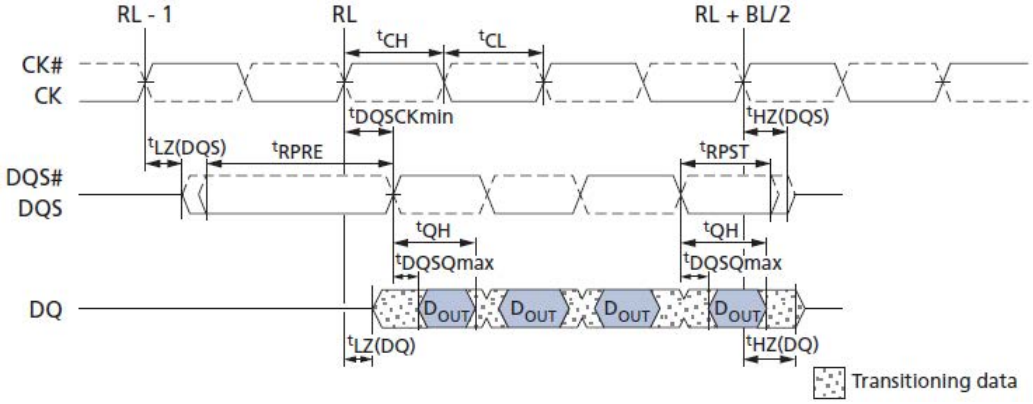
Figure 4 : READ Output Timing – tDQSCK (MAX)



Notes : 1. tDQSCK can span multiple clock periods.

2 An effective burst length of 4 is shown.

Figure 5 : READ Output Timing – tDQSCK (MIN)



Note : 1. An effective burst length of 4 is shown.

Figure 6 : Burst READ – RL = 5, BL = 4, tDQSCK > tCK

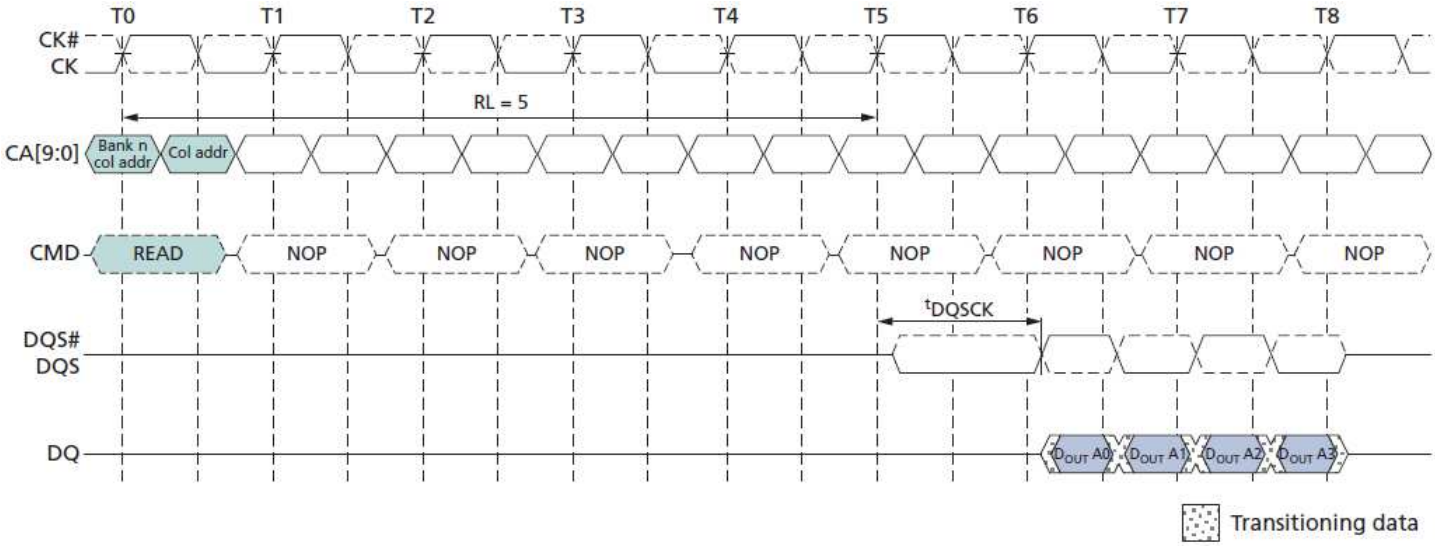


Figure 7 : Burst READ – RL = 3, BL = 8, tDQSCK < tCK

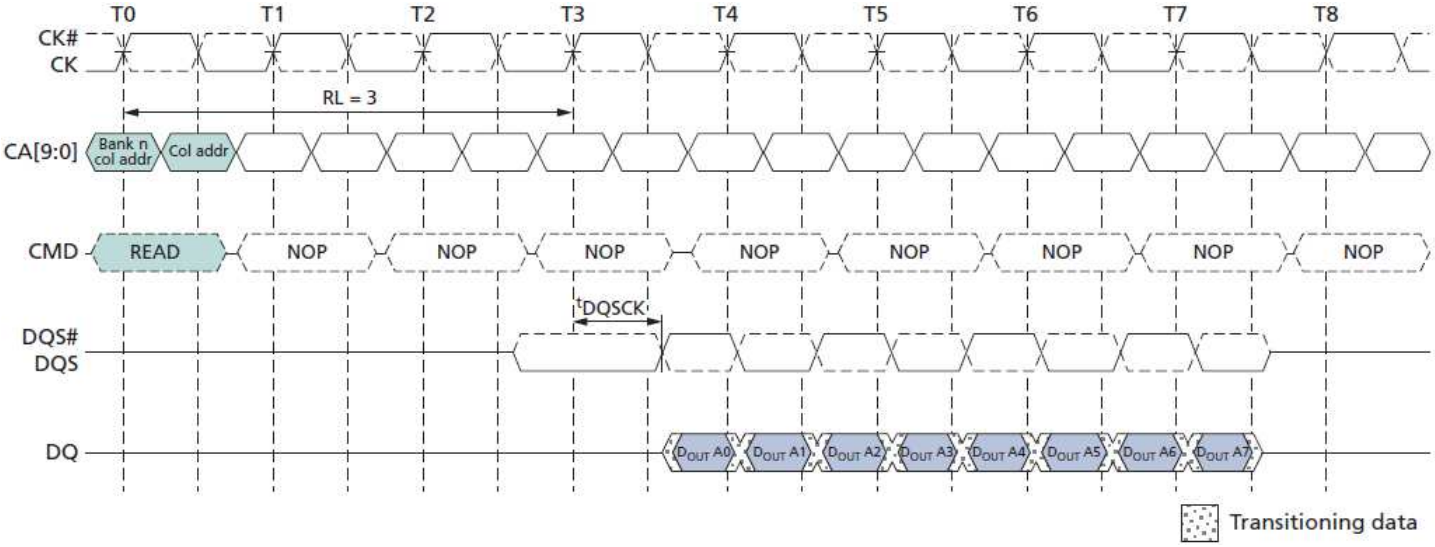
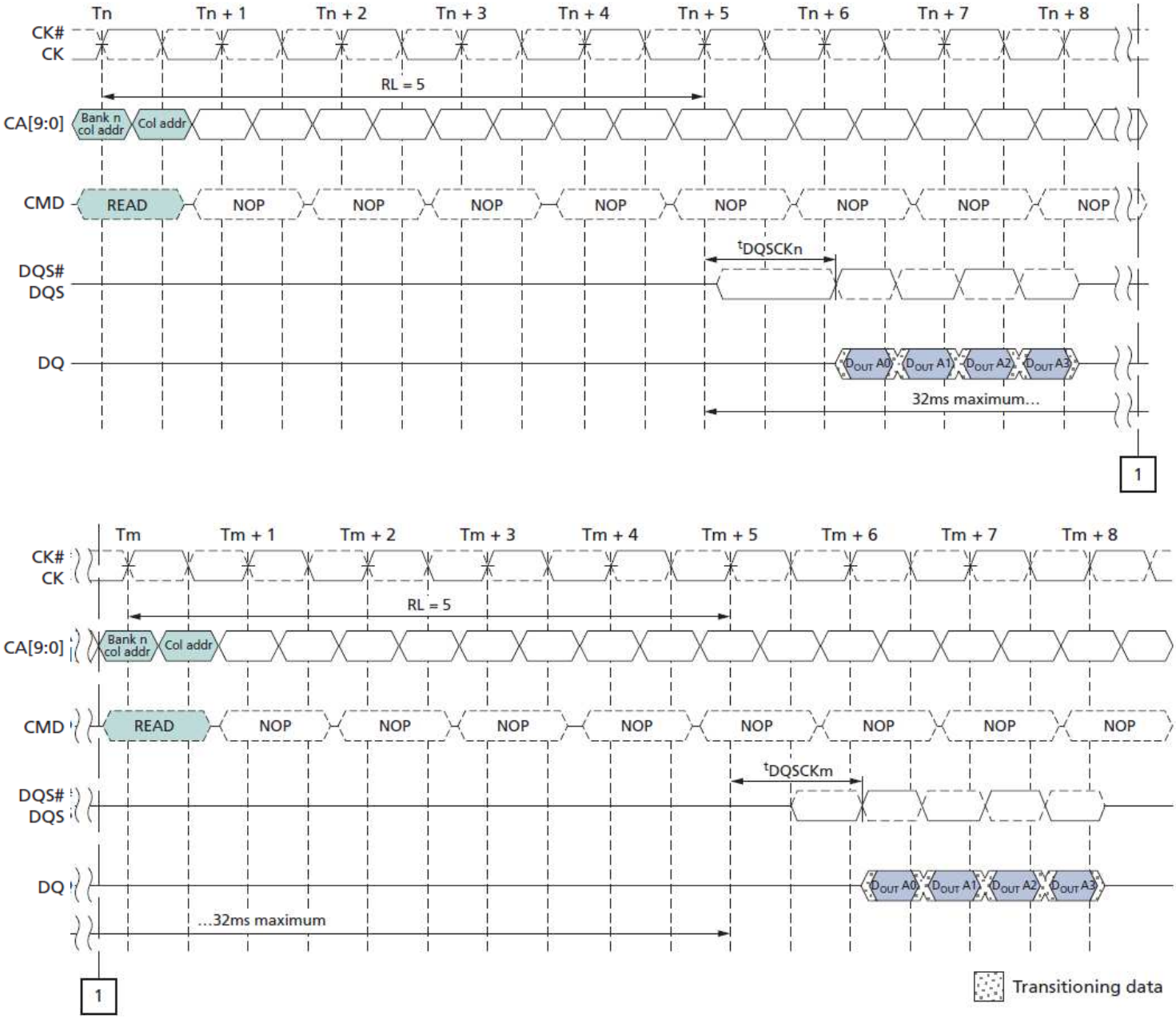


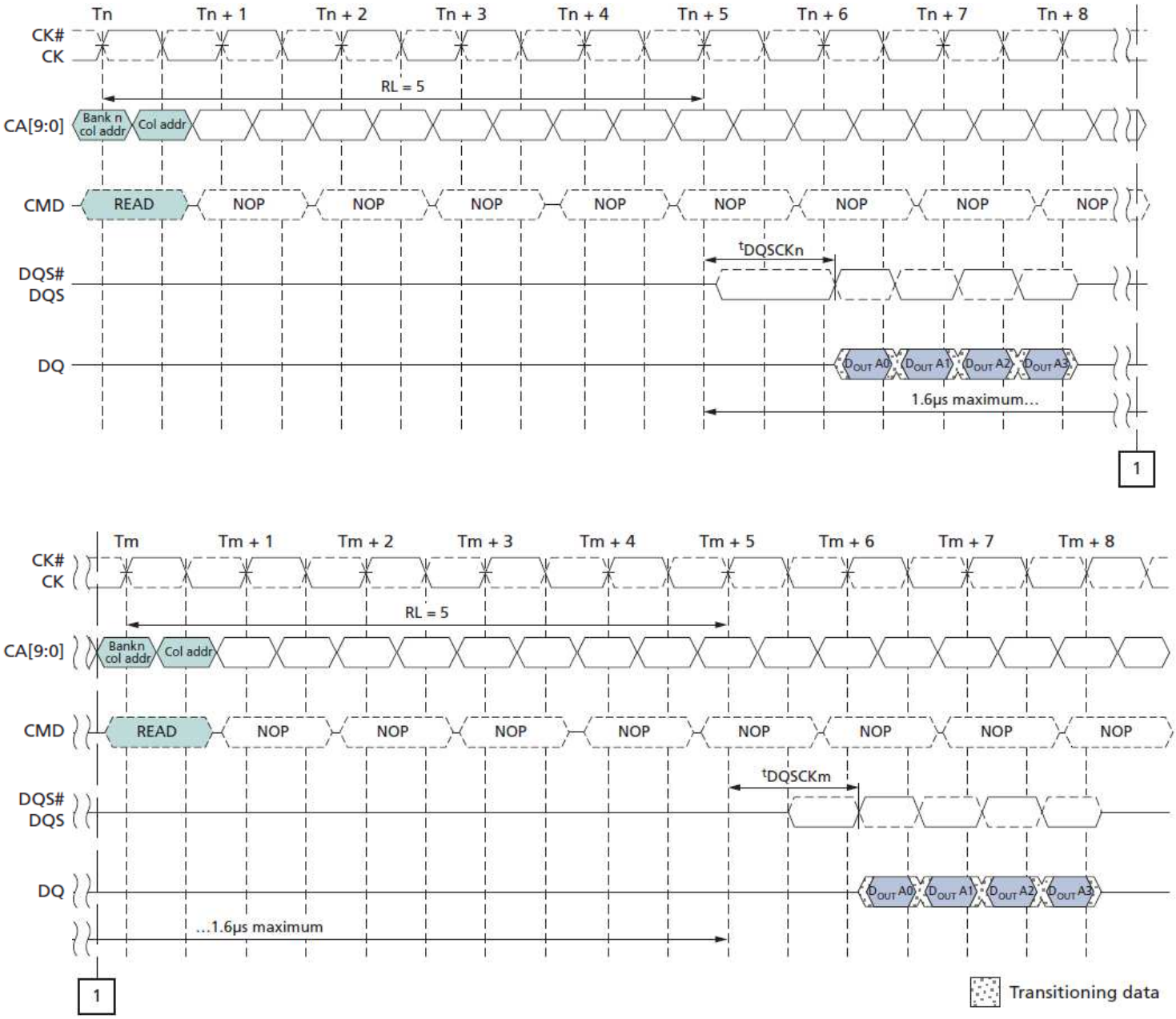
Figure 8 : tDQSCKDL Timing



Notes : 1. tDQSCKDL = (tDQSCK*n* - tDQSCK*m*).

2. tDQSCKDL (MAX) is defined as the maximum of ABS (tDQSCK*n* - tDQSCK*m*) for any (tDQSCK*n*, tDQSCK*m*) pair within any 32ms rolling window.

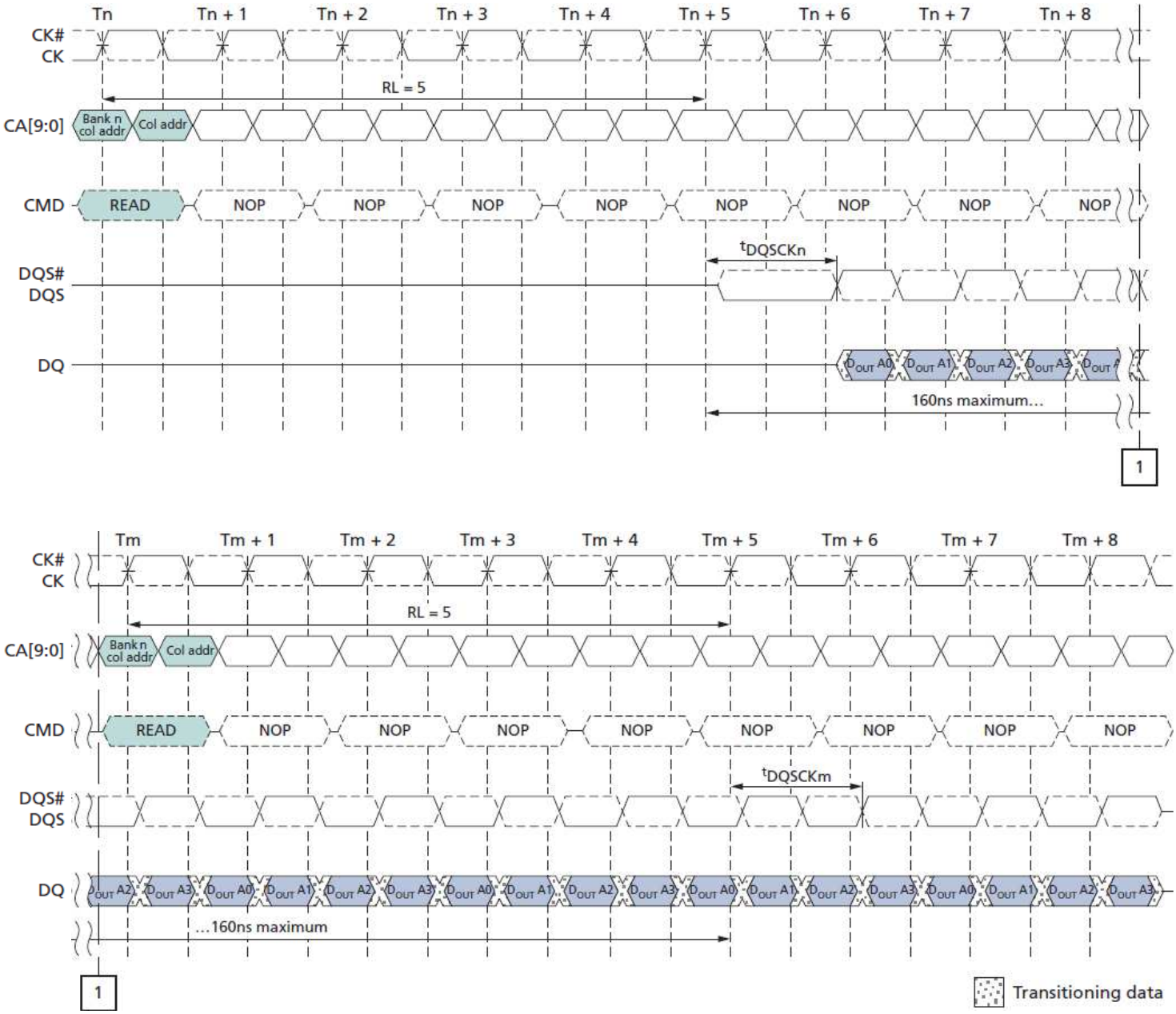
Figure 9 : tDQSCKDM Timing



Notes : 1. tDQSCKDM = (tDQSCK*n* - tDQSCK*m*).

2. tDQSCKDM (MAX) is defined as the maximum of ABS (tDQSCK*n* - tDQSCK*m*) for any (tDQSCK*n*, tDQSCK*m*) pair within any 1.6µs rolling window.

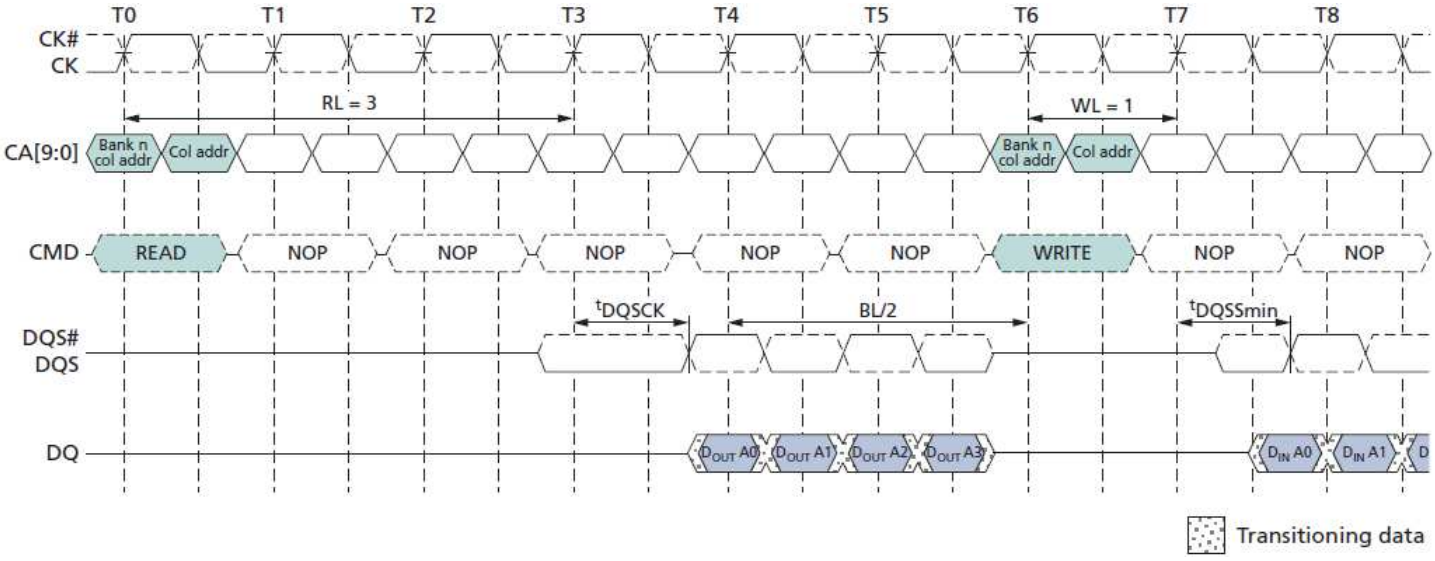
Figure 10 : tDQSCKDS Timing



Notes : 1. tDQSCKDS = (tDQSCK*n* - tDQSCK*m*).

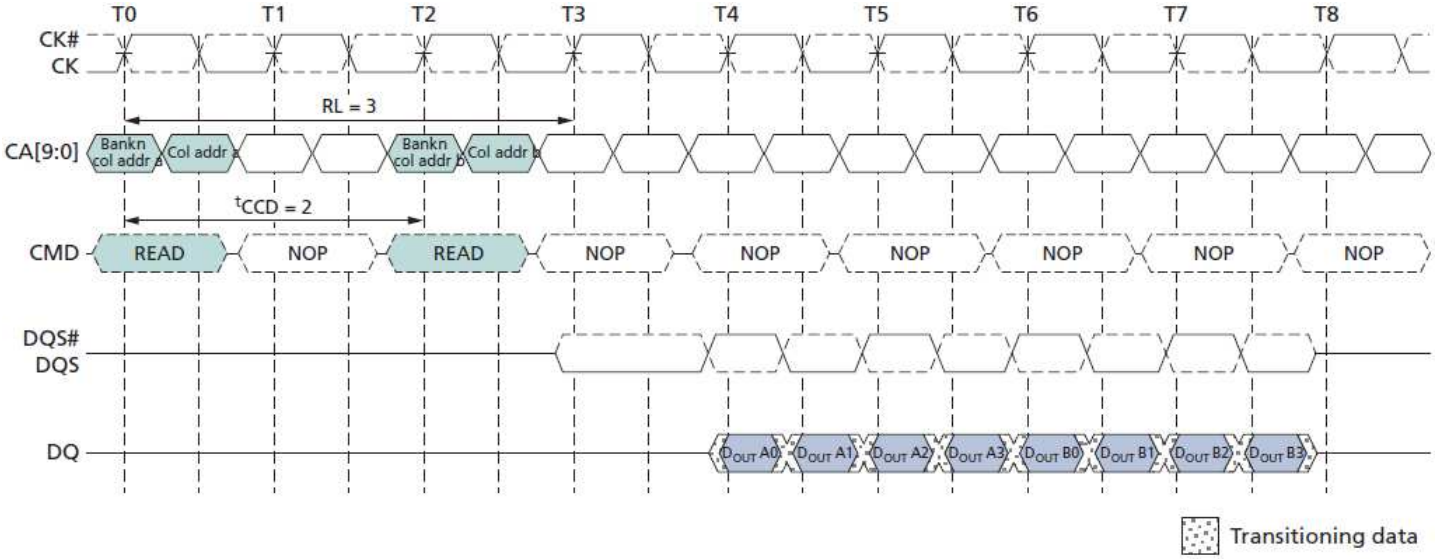
2. tDQSCKDS (MAX) is defined as the maximum of ABS (tDQSCK*n* - tDQSCK*m*) for any (tDQSCK*n*, tDQSCK*m*) pair for READs within a consecutive burst, within any 160ns rolling window.

Figure 11: Burst READ Followed by Burst WRITE – RL = 3, WL = 1, BL = 4



The minimum time from the burst READ command to the burstWRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 -WL clock cycles. Note that if a READ burst is truncated with a burstTERMINATE (BST) command, the effective burst length of the truncated READ burst should be used for BL when calculating the minimum READ-to-WRITE delay.

Figure 12: Seamless Burst READ – RL = 3, BL = 4, CCD = 2



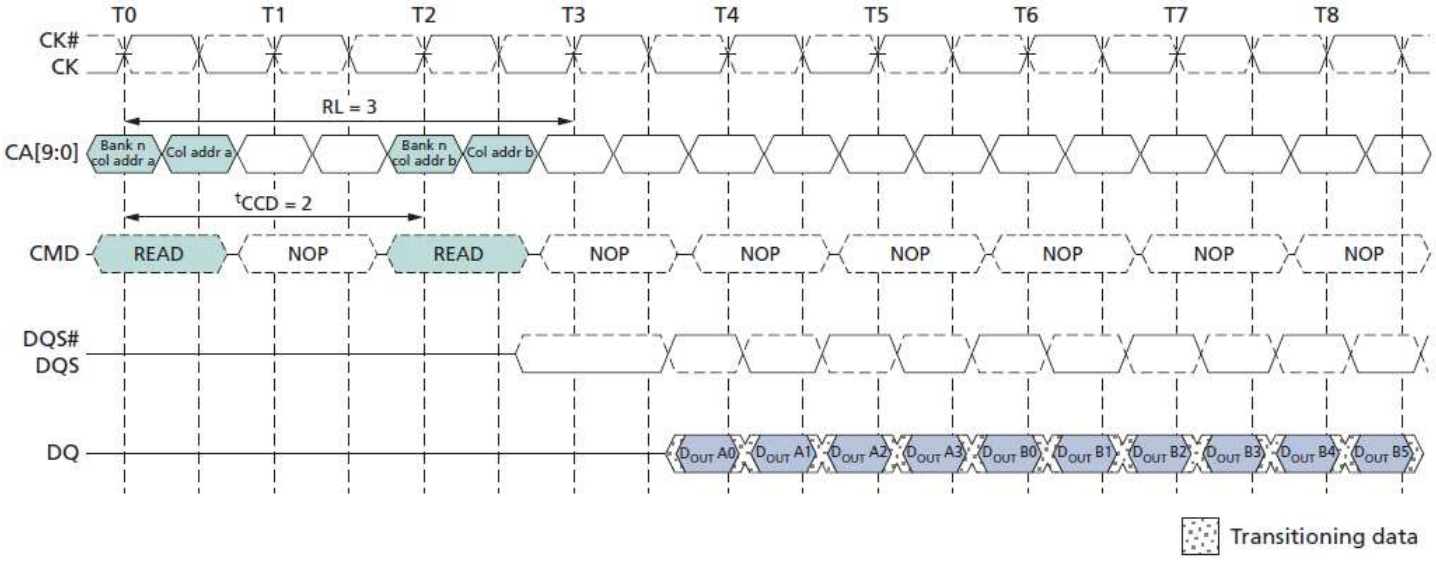
A seamless burst READ operation is supported by enabling a READ command at every other clock cycle for BL = 4 operation, every fourth clock cycle for BL = 8 operation, and every eighth clock cycle for BL = 16 operation.
This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

READs Interrupted by a READ

A burst READ can be interrupted by another READ with a 4-bit burst boundary, provided that tCCD is met.

A burst READ can be interrupted by other READs on any subsequent clock, provided that tCCD is met.

Figure 13: READ Burst Interrupt Example – RL = 3, BL = 8, tCCD = 2



Note : 1. READs can only be interrupted by other READs or the BST command.

Burst WRITE Command

The burstWRITE command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock.

The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst.

Write latency (WL) is defined from the rising edge of the clock on which theWRITE command is issued to the rising edge of the clock from which the tDQSS delay is measured.The first valid data must be drivenWL × tCK + tDQSS from the rising edge of the clock from which the WRITE command is issued.The data strobe signal (DQS) must be driven LOW tWPRE prior to data input.

The burst cycle data bits must be applied to the DQ pins tDS prior to the associated edge of the DQS and held valid until tDH after that edge. Burst data is sampled on successive edges of the DQS until the 4-, 8-, or 16-bit burst length is completed.

After a burstWRITE operation, tWR must be satisfied before a PRECHARGE command to the same bank can be issued.

Pin input timings are measured relative to the crosspoint of DQS and its complement, DQS#.