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1. GENERAL DESCRIPTION

This AS4C16M16D1 is 268,435,456 bits synchronous double data rate Dynamic RAM. Each 67,108,864 bits bank is organized as 8,192 rows by 512 columns by 16 bits, fabricated with Alliance Memory's high performance CMOS technology. This device uses a double data rate architecture to achieve high- speed operation. The double data rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

2. FEATURES

•AS4C16M16MD1
VDD/VDDQ = 1.7~1.95V
• Data width: x16
• Clock rate: 200MHz,166MHz , 133MHz
• Partial Array Self-Refresh(PASR)
• Auto Temperature Compensated Self-Refresh(ATCSR)
• Power Down Mode
• Deep Power Down Mode (DPD Mode)
• Programmable output buffer driver strength
• Four internal banks for concurrent operation
• Data mask (DM) for write data
• Clock Stop capability during idle periods
• Auto Pre-charge option for each burst access
• Double data rate for data output
• Differential clock inputs (CK and $\overline{CK}$)
• Bidirectional, data strobe (DQS)
• $\overline{CAS}$ Latency: 2 and 3
• Burst Length: 2, 4, 8 and 16
• Burst Type: Sequential or Interleave
• 64 ms Refresh period
• Interface: LVCMOS
• Operating Temperature Range
Extended (-25℃ to + 85 ℃)
Industrial (-40℃ to + 85 ℃)

Table 1. Ordering Information

Part Number	Clock rate	Package	Temperature	Temp Range
AS4C16M16MD1-6BCN	166MHz	60-ball FPBGA (8.0X9.0 mm)	Extended	-25°C to +85°C

B: indicates BGA package
C: indicates Extended temp
I: indicates Industrial temp (to follow at a later date)
N: Indicates lead free and ROHS compliant

3. PIN DESCRIPTION

60-Ball FPBGA Assignment

TOP VIEW

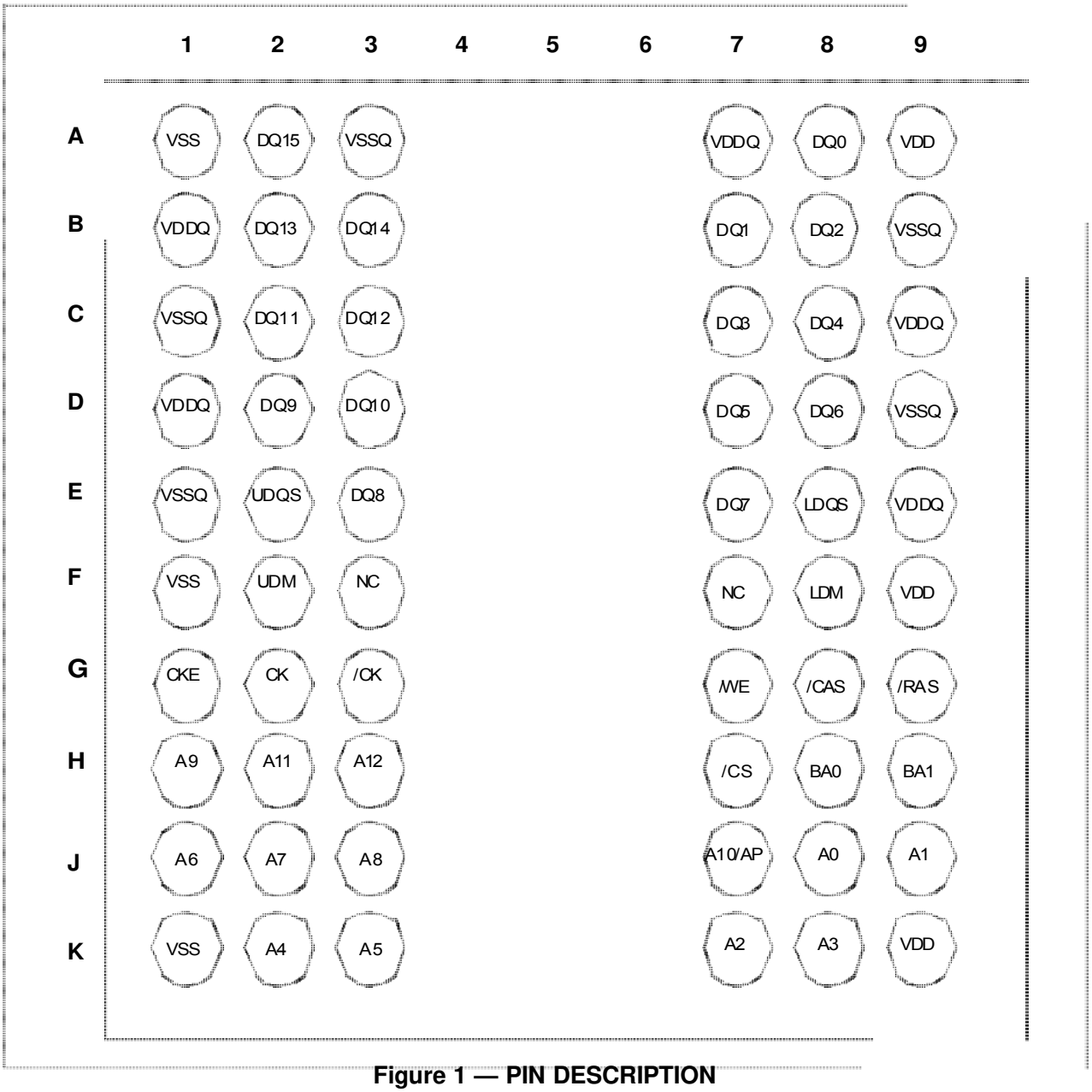


Figure 1 — PIN DESCRIPTION

3.1 Signal Descriptions

SIGNAL NAME	TYPE	DESCRIPTION
CK,/CK	Input	Clock: CK and CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Input and output data is referenced to the crossing of CK and CK (both directions of crossing). Internal clock signals are derived from CK/CK.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWERDOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, CK and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
/CS	Input	Chip Select: CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS is registered HIGH. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
/RAS,/CAS,/WE	Input	Command Inputs: RAS, CAS and WE (along with CS) define the command being entered.
LDM,UDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. For x16 devices, LDM corresponds to the data on DQ0-DQ7, UDM corresponds to the data on DQ8-DQ15.
BA0,BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [n : 0]	Input	Address Inputs: provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command.
DQ0-DQ15	I/O	Data Bus: Input / Output
LDQS,UDQS	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. LDQS corresponds to the data on DQ0-DQ7, UDQS corresponds to the data on DQ8-DQ15.
NC	-	No Connect: No internal electrical connection is presen
VDDQ	Supply	I/O Power Supply
VSSQ	Supply	I/O Ground
VDD	Supply	Power Supply
VSS	Supply	Ground

Table 1 — Signal Descriptions

3.2 Mobile DDR SDRAM Addressing Table

ITEM		256 Mb
Number of banks		4
Bank address pins		BA0,BA1
Auto precharge pin		A10/AP
X16	Row addresses	A0-A12
	Column addresses	A0-A8
	tREFI(μs)	7.8

Table 2 — Addressing Table

4. BLOCK DIAGRAM

4.1 Block Diagram

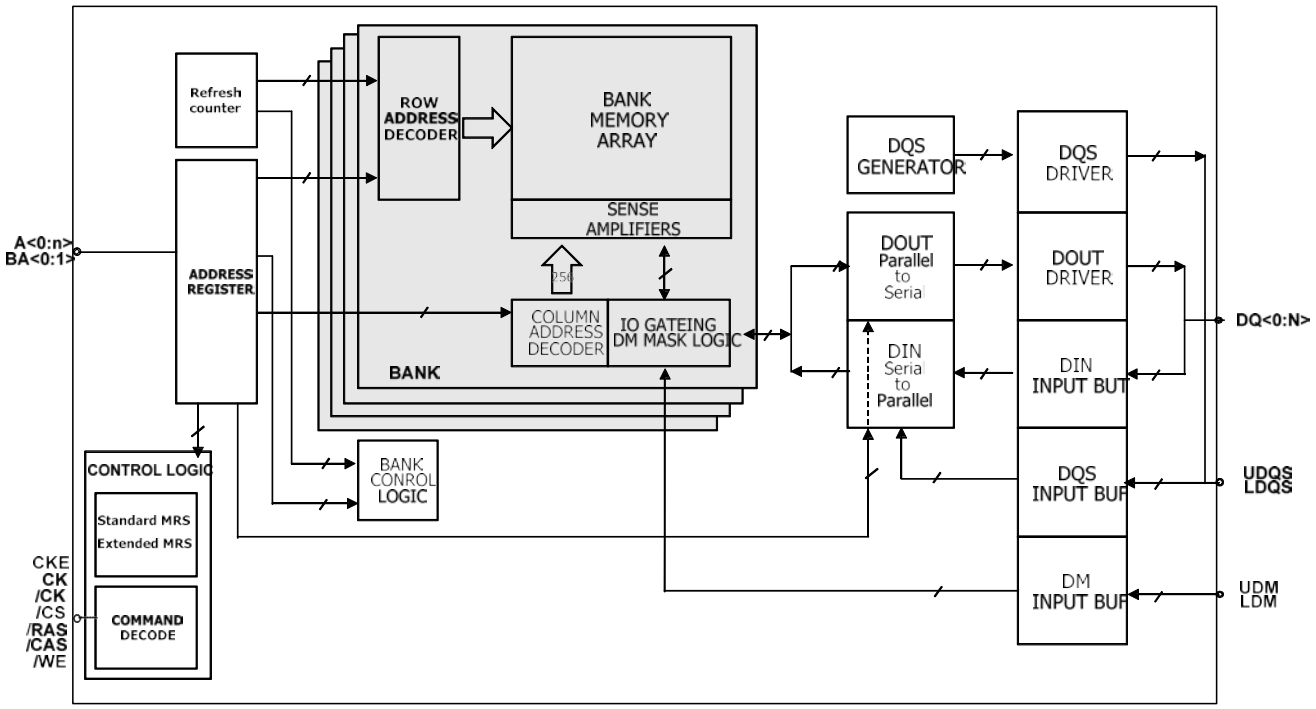
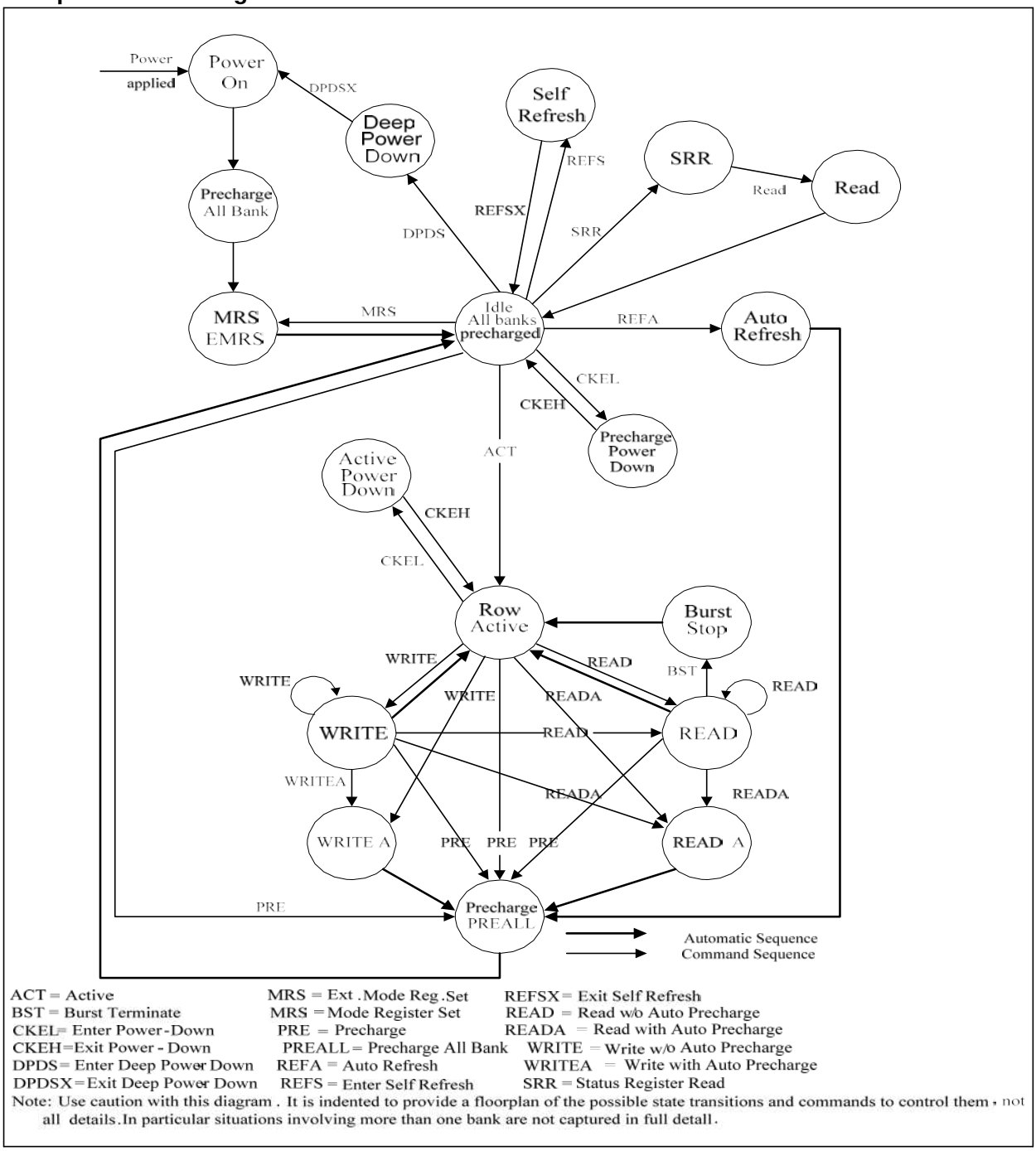


Figure.2 — Block Diagram

4.2 Simplified State Diagram



ACT = Active
BST = Burst Terminate
CKEL= Enter Power-Down
CKEH=Exit Power - Down
DPDS= Enter Deep Power Down
DPDSX=Exit Deep Power Down
MRS = Ext .Mode Reg.Set
MRS =Mode Register Set
PRE = Precharge
PREALL= Precharge All Bank
REFA = Auto Refresh
REFS = Enter Self Refresh
REFSX= Exit Self Refresh
READ = Read w/o Auto Precharge
READA = Read with Auto Precharge
WRITE = Write w/o Auto Precharge
WRITEA = Write with Auto Precharge
SRR = Status Register Read

Note: Use caution with this diagram . It is indented to provide a floorplan of the possible state transitions and commands to control them , not all details.In particular situations involving more than one bank are not captured in full detail.

Figure.3 — State Diagram

5. FUNCTION DESCRIPTION

The LPDDR SDRAM is a high speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. These devices contain the following number of bits: 256 Mb has 268,435,456 bits The LPDDR SDRAM uses a double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the LPDDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clockcycle data transfers at the I/O pins.

Read and write accesses to the LPDDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

5.1 Initialization

LPDDR SDRAMs must be powered up and initialized in a predefined manner. Operations procedures other than those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below. The Initialization Flow diagram is shown in Figure 4, and the Initialization Flow sequence in Figure 5. The Mode Register and Extended Mode Register do not have default values. If they are not programmed during the initialization sequence, it may lead to unspecified operation. The clock stop feature is not available until the device has been properly initialized from Steps 1 through 11.

1. Provide power, the device core power (VDD) and the device I/O power (VDDQ) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that VDD and VDDQ are from the same power source. Also assert and hold Clock Enable (CKE) to a LV-CMOS logic high level
2. Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock
3. There must be at least 200 µs of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Provide NOPs or DESELECT commands for at least tRP time.
6. Issue an AUTO REFRESH command followed by NOPs or DESELECT command for at least tRFC time. Issue the second AUTO REFRESH command followed by NOPs or DESELECT command for at least tRFC time. Note as part of the initialization sequence there must be two auto refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.
7. Using the MRS command, load the base mode register. Set the desired operating modes.
8. Provide NOPs or DESELECT commands for at least tMRD time.
9. Using the MRS command, program the extended mode register for the desired operating modes. Note the order of the base and extended mode register programming is not important.
10. Provide NOP or DESELCT commands for at least tMRD time.
11. The DRAM has been properly initialized and is ready for any valid command.

5.1.1 Initialization Flow Diagram

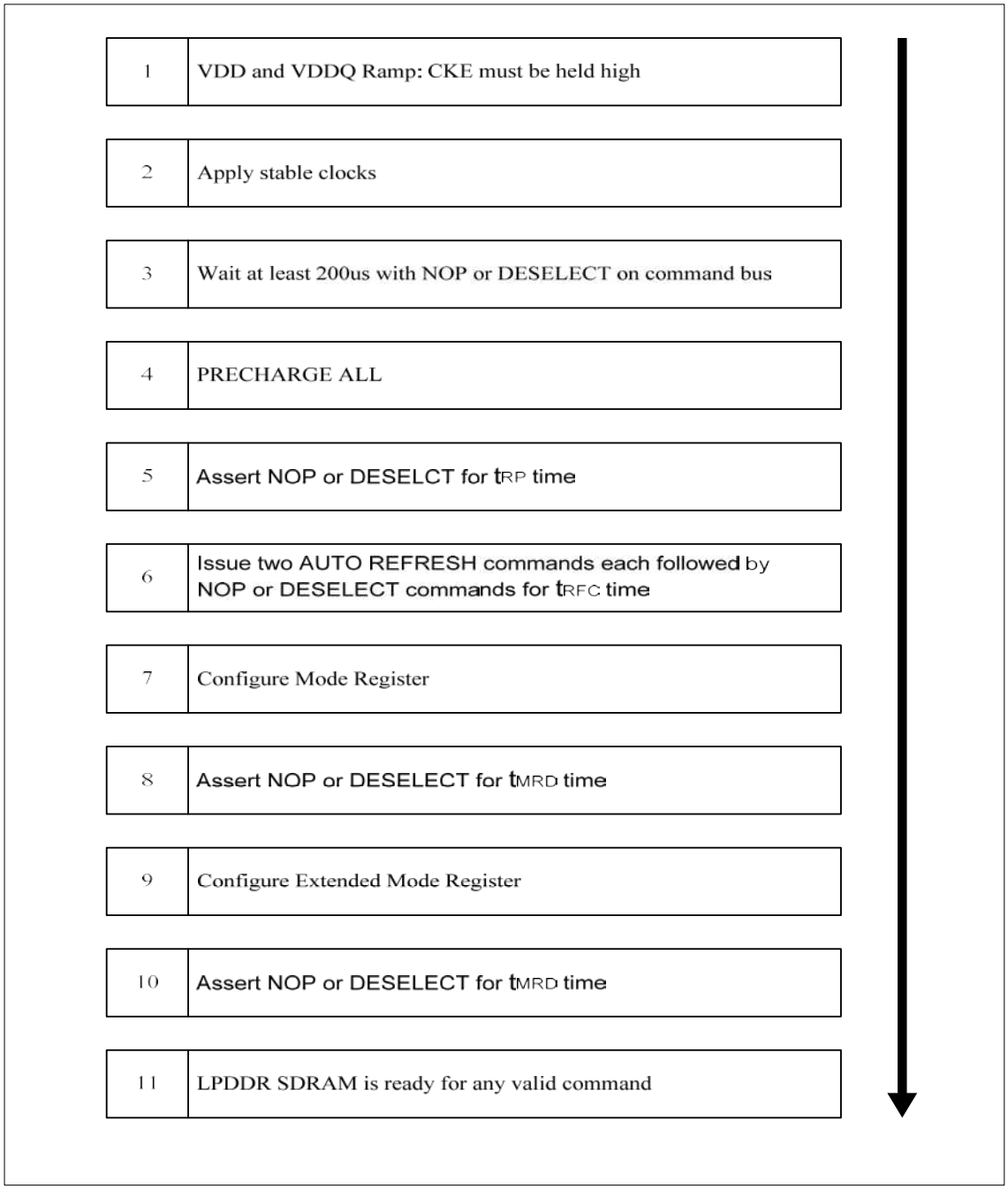


Figure.4 — Flow Diagram

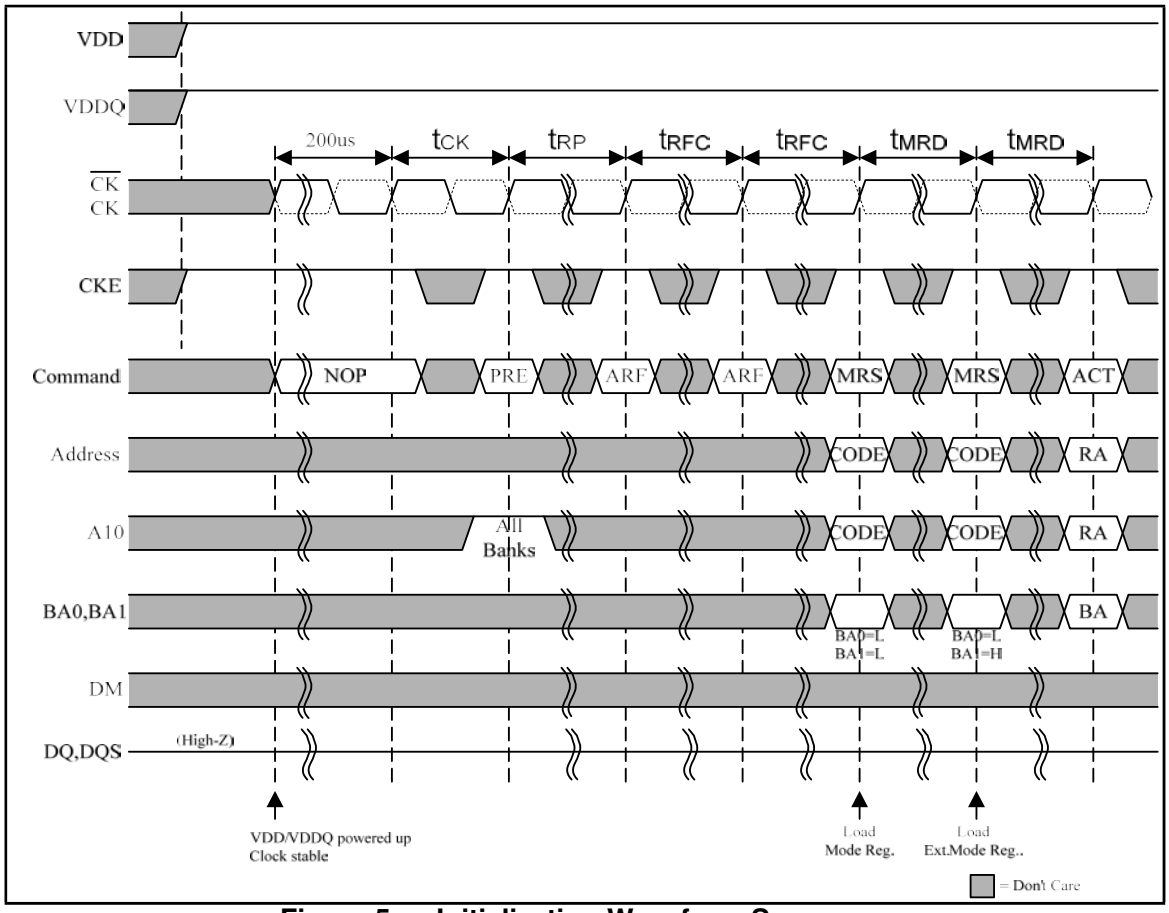


Figure 5 — Initialization Waveform Sequence

5.2 Register Definition

5.2.1 Mode Register

The Mode Register is used to define the specific mode of operation of the LPDDR SDRAM. This definition includes the definition of a burst length, a burst type, a CAS latency as shown below table.
The Mode Register is programmed via the MODE REGISTER SET command (with BA0=0 and BA1=0) and will retain the stored information until it is reprogrammed, the device goes into Deep Power-Down mode, or the device loses power.
Mode Register bits A0-A2 specify the burst length, A3 the type of burst (sequential or interleave), A4-A6 the CAS latency. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility.
The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Mode	BA1	BA0	A[n]~A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Standard MRS	0	0	Reserved			**CAS Latency** 010b: 2 011b: 3			**Burst Type** 0:Sequential 1:Interleave	**Burst Length** 001b : 2 010b : 4 011b : 8 100b : 16		
Reserved	0	1	Reserved									
Extended MRS	1	0	Reserved		**Drive Strength** 000b: Full Strength Driver 001b: Half Strength Driver 010b:Quarter Strength Driver 011b:Octant Strength Driver 100b:ThreeQuarters Strength Driver			Reserved		**PASR** 000b : All banks 001b : 1/2 array(BA1=0) 010b : ¼ array(BA1=BA0=0) 101b : 1/8 array (BA1 = BA0 = Row Addr MSB = 0) 110b : 1/16 array (BA1=BA0 = Row Addr 2 MSB = 0)		

Table 3 – Mode Register Table

5.2.1.1 Burst Length

Read and write accesses to the LPDDR SDRAM are burst oriented, with the burst length being set as in Table 6, and the burst order as in Table 4.
The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types. A burst length of 16 is optional and some vendors may choose to implement it.

5.3 Burst Definition

BURST LENGTH	STARTING COLUMN ADDRESS				ORDER OF ACCESSES WITHIN A BURST (HEXADECIMAL NOTATION)	
	A3	A2	A1	A0	SEQUENTIAL	INTERLEAVED
2				0	0 – 1	0 – 1
				1	1 – 0	1 – 0
4			0	0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
			0	1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
			1	0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
			1	1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8		0	0	0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
		0	0	1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
		0	1	0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
		0	1	1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
		1	0	0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
		1	0	1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
		1	1	0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
		1	1	1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0
16	0	0	0	0	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F
	0	0	0	1	1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0	1-0-3-2-5-4-7-6-9-8-B-A-D-C-F-E
	0	0	1	0	2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1	2-3-0-1-6-7-4-5-A-B-8-9-E-F-C-D
	0	0	1	1	3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2	3-2-1-0-7-6-5-4-B-A-9-8-F-E-D-C
	0	1	0	0	4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3	4-5-6-7-0-1-2-3-C-D-E-F-8-9-A-B
	0	1	0	1	5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4	5-4-7-6-1-0-3-2-D-C-F-E-9-8-B-A
	0	1	1	0	6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5	6-7-4-5-2-3-0-1-E-F-C-D-A-B-8-9
	0	1	1	1	7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-F-E-D-C-B-A-9-8
	1	0	0	0	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7
	1	0	0	1	9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8	9-8-B-A-D-C-F-E-1-0-3-2-5-4-7-6
	1	0	1	0	A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9	A-B-8-9-E-F-C-D-2-3-0-1-6-7-4-5
	1	0	1	1	B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A	B-A-9-8-F-E-D-C-3-2-1-0-7-6-5-4
	1	1	0	0	C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B	C-D-E-F-8-9-A-B-4-5-6-7-0-1-2-3
	1	1	0	1	D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C	D-C-F-E-9-8-B-A-5-4-7-6-1-0-3-2
	1	1	1	0	E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D	E-F-C-D-A-B-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E	F-E-D-C-B-A-9-8-7-6-5-4-3-2-1-0

Table 4 – Burst Definition

Notes:
1. 16-word burst length is optional.
2. For a burst length of two, A1-An selects the two data element block; A0 selects the first access within the block.
3. For a burst length of four, A2-An selects the four data element block; A0-A1 selects the first access within the block.
4. For a burst length of eight, A3-An selects the eight data element block; A0-A2 selects the first access within the block.
5. For the optional burst length of sixteen, A4-An selects the sixteen data element block; A0-A3 selects the first access within the block.
6. Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.
The block is uniquely selected by A1-An when the burst length is set to two, by A2-An when the burst length is set to 4, by A3-An when the burst length is set to 8 and A4-An when the burst length is set to 16 (where An is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

5.2.1.2 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.
The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 4.

5.2.1.3 Read Latency

The READ latency, or CAS latency, is the delay between the registration of a READ command and the availability of the first piece of output data. The latency should be set to 3 clocks. Some vendors may offer additional options of 2 clocks and/or 4 clocks.
If a READ command is registered at a clock edge n and the latency is 3 clocks, the first data element will be valid at n + 2t_{CK} + t_{AC}. If a READ command is registered at a clock edge n and the latency is 2 clocks, the first data element will be valid at n + t_{CK} + t_{AC}. Lastly, if a READ command is registered at a clock edge n and the latency is 4 clocks, the first data element will be valid at n + 3t_{CK} + t_{AC}.

5.2.2 Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include output drive strength selection, Temperature Compensated Self Refresh (TCSR) and Partial Array Self Refresh (PASR), as shown in Figure 7. The TCSR and PASR functions are optional and some vendors may choose not to implement them. Both TCSR and PASR are effective is in Self Refresh mode only.
The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=1 and BA0=0) and will retain the stored information until it is reprogrammed, the device is put in Deep Power-Down mode, or the device loses power.
The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.
Address bits A0-A2 specify PASR, A3-A4 the TCSR, A5-A6 the Drive Strength. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.
Address bits A0-A2 specify PASR, A3-A4 the TCSR, A5-A7 the Drive Strength.
A logic 0 should be programmed to all the undefined address bits to ensure future compatibility.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

BA1	BA0	A[n]~A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	Reserved	**Drive Strength** 000b: Full Strength Driver 001b: Half Strength Driver 010b:Quarter Strength Driver 011b:Octant Strength Driver 100b:ThreeQuarters Strength Driver			Reserved		**PASR** 000b : All banks 001b : 1/2 array(BA1=0) 010b : ¼ array(BA1=BA0=0) 101b : 1/8 array (BA1 = BA0 = Row Addr MSB = 0) 110b : 1/16 array (BA1=BA0 = Row Addr 2 MSB = 0)		

5.2.2.1 Partial Array Self Refresh

Partial Array Self Refresh (PASR) is an optional feature. With PASR, the self refresh may be restricted to a variable portion of the total array. The whole array (default), 1/2 array, or 1/4 array could be selected. Some vendors may have additional options of 1/8 and 1/16 array refreshed as well. Data outside the defined area will be lost. Address bits A0 to A2 are used to set PASR.

5.2.2.2 Temperature Compensated Self Refresh

This function can be used in the LPDDR SDRAM to set refresh rates based on case temperature.This allows the system to control power as a function of temperature. Address bits A3 and A4 are used to set TCSR.
Some vendors may choose to have Internal Temperature Compensated Self Refresh feature, which should automatically adjust the refresh rate based on the device temperature without any register update needed. To maintain backward compatibility, devices having internal TCSR, ignore (don't care) the inputs to address bits A3 and A4 during EMRS programming.

5.2.2.3 Output Drive Strength

The drive strength could be set to full or half or three-quarters strength via address bits A5 and A6 and A7. The I-V curves for the full drive strength and half drive strength and three-quarters drive strength are included in this document (cf. Table 17 and Table 18, Figure 45 and Figure 46 and Figure 47).

6. COMMANDS

All commands (address and control signals) are registered on the positive edge of clock (crossing of CK going high and CK going low). Figure 6 shows basic timing parameters for all commands.
Table 5, Table 6 and Table 7 provide a quick reference of available commands.
Table 8 and Table 9 provide the current state / next state information. This is followed by a verbal description of each command.

NAME (FUNCTION)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10/AP	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (Select Bank and activate row)	L	L	H	H	Valid	Row	Row	
READ (Select bank and column and start read burst)	L	H	L	H	Valid	L	Col	
READ with AP (Read Burst with Auto Precharge)	L	H	L	H	Valid	H	Col	3
WRITE (Select bank and column and start write burst)	L	H	L	L	Valid	L	Col	
WRITE with AP (Write Burst with Auto Precharge)	L	H	L	L	Valid	H	Col	3
BURST TERMINATE or enter DEEP POWER DOWN	L	H	H	L	X	X	X	4, 5,12
PRECHARGE (Deactivate Row in selected bank)	L	L	H	L	Valid	L	X	6
PRECHARGE ALL (Deactivate rows in all banks)	L	L	H	L	X	H	X	6
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	7, 8, 9
MODE REGISTER SET	L	L	L	L	Valid	Op-code		10

Table 5 – Truth Table -Commands

Notes:
1. All states and sequences not shown are illegal or reserved.
2. DESELECT and NOP are functionally interchangeable.
3. Auto precharge is non-persistent. A10 High enables Auto precharge, while A10 Low disables Auto precharge.
4. Burst Terminate applies to only Read bursts with Autoprecharge disabled. This command is undefined and should not be used for Read with Auto precharge enabled, and for Write bursts.
5. This command is BURST TERMINATE if CKE is High and DEEP POWER DOWN entry if CKE is Low.
6. If A10 is low, bank address determines which bank is to be precharged. If A10 is high, all banks are precharged and BA0~BA1 are don't care.
7. This command is AUTO REFRESH if CKE is High and SELF REFRESH if CKE is low.
8. All address inputs and I/O are 'don't care' except for CKE. Internal refresh counters control bank and row addressing.
9. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
10. BA0 and BA1 value select between MRS and EMRS.
11. CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN.

FUNCTION	DM	DQ	NOTES
Write Enable	L	Valid	1
Write Inhibit	H	X	1

Table 6 –Truth Table – DM operations

Notes:
1. Used to mask write data, provided coincident with the corresponding data.

CKEn-1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	L	Deep Power Down	X	Maintain Deep Power Down	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5, 6, 9
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5, 7, 10
L	H	Deep Power Down	NOP or DESELECT	Exit Deep Power Down	5, 8
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	L	All Banks Idle	BURST TERMINATE	Enter Deep Power Down	
H	H	See the other Truth Tables			

Table 7 – Truth Table - CKE [Notes 1 - 10]

Notes:
1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of Mobile DDR SDRAM immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is the result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time (tXP) should elapse before a command other than NOP or DESELECT is issued.
7. SELF REFRESH exit time (tXSR) should elapse before a command other than NOP or DESELECT is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9. The clock must toggle at least once during the tXP period.
10. The clock must toggle at least once during the tXSR time.

Basic Timing Parameters for Commands

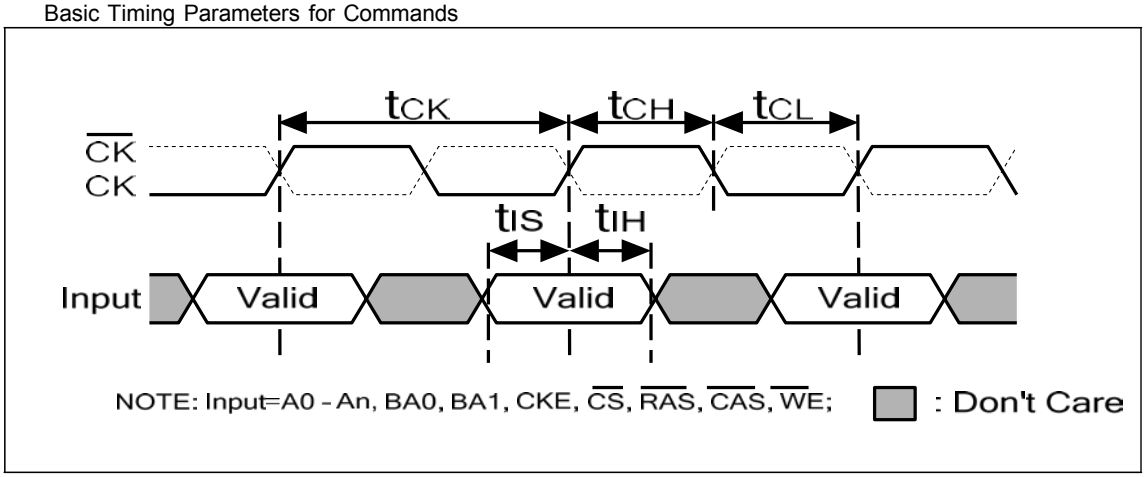


Figure.6 — Basic Timing Parameters

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND	ACTION	NOTES
Any	H	X	X	X	DESELECT	NOP or Continue previous operation	
	L	H	H	H	No Operation	NOP or Continue previous operation	
Idle	L	L	H	H	ACTIVE	Select and activate row	
	L	L	L	H	AUTO REFRESH	Auto refresh	10
	L	L	L	L	MRS	Mode register set	10
Row Active	L	H	L	H	READ	Select column & start read burst	
	L	H	L	L	WRITE	Select column & start write burst	
	L	L	H	L	PRECHARGE	Deactivate row in bank (or banks)	4
Read (Auto precharge Disabled)	L	H	L	H	READ	Select column & start new read burst	5, 6
	L	H	L	L	WRITE	Select column & start write burst	5, 6, 13
	L	L	H	L	PRECHARGE	Truncate read burst, start precharge	
	L	H	H	L	BURST TERMINATE	Burst terminate	11
Write (Auto precharge Disabled)	L	H	L	H	READ	Select column & start read burst	5, 6, 12
	L	H	L	L	WRITE	Select column & start new write burst	5, 6
	L	L	H	L	PRECHARGE	Truncate write burst & start precharge	12

Table 8 – Current State BANK n- Command to BANK n

Notes:
1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. A command other than NOP should not be issued to the same bank while a READ or WRITE burst with Auto Precharge is enabled.
6. The new Read or Write command could be Auto Prechrge enabled or Auto Precharge disabled.
7. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
8. The following states must not be interrupted by a command issued to the same bank. DESEDECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and this table, and according to next table.
   Precharging: Starts with the registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'row active' state.
   Read with AP Enabled: Starts with the registration of the READ command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   Write with AP Enabled: Starts with registration of a WRITE command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
9. The following states must not be interrupted by any executable command; DESEDECT or NOP commands must be applied to each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRFC is met. Once tRFC is met, the Mobile DDR SDRAM will be in an 'all banks idle' state.

Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met. Once tMRD is met, the Mobile DDR SDRAM will be in an 'all banks idle' state.
Precharging All: Starts with the registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

10. Not bank-specific; requires that all banks are idle and no bursts are in progress.
11. Not bank-specific. BURST TERMINATE affects the most recent READ burst, regardless of bank.
12. Requires appropriate DM masking.
13. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ prior to asserting a WRITE command.

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND	ACTION	NOTES
Any	H	X	X	X	DESELECT	NOP or Continue previous Operation	
	L	H	H	H	NOP	NOP or Continue previous Operation	
Idle	X	X	X	X	ANY	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	8
	L	H	L	L	WRITE	Select column & start write burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge disabled	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start new read burst	8
	L	H	L	L	WRITE	Select column & start write burst	8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto Precharge disabled	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	8, 9
	L	H	L	L	WRITE	Select column & start new write burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start new read burst	5, 8
	L	H	L	L	WRITE	Select column & start write burst	5, 8, 10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto Precharge	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	5, 8
	L	H	L	L	WRITE	Select column & start new write burst	5, 8
	L	L	H	L	PRECHARGE	Precharge	

Table 9 – Current State BANK n- Command to BANK m

Notes:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
5. Read with AP enabled and Write with AP enabled: The read with Auto Precharge enabled or Write with Auto Precharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For Write with Auto precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period, of the Read with Auto Precharge enabled or Write with Auto Precharge enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).
6. AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
7. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
8. READs or WRITEs listed in the Command column include READs and WRITEs with Auto Precharge enabled and READs and WRITEs with Auto Precharge disabled.
9. Requires appropriate DM masking.
10. A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.

7.OPERATION

7.1. Deselect

The DESELECT function (/CS HIGH) prevents new commands from being executed by the Mobile DDR SDRAM. The Mobile DDR SDRAM is effectively deselected. Operations already in progress are not affected.

7.2. No Operation

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (/CS = LOW, / RAS = /CAS = /WE = HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

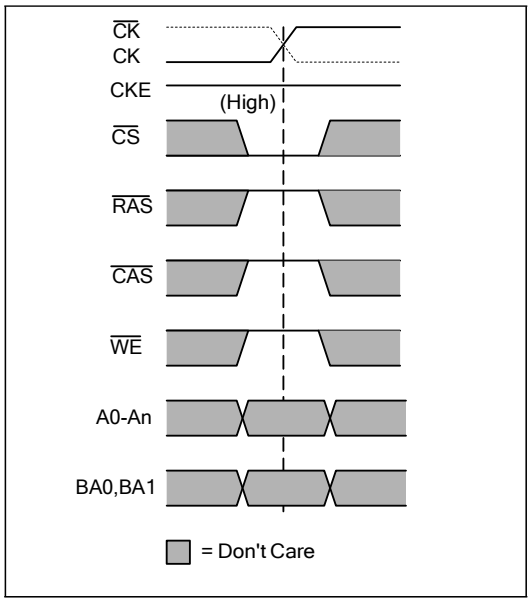


Figure 7 — NOP Command

7.3 MODE REGISTER

The Mode Register and the Extended Mode Register are loaded via the address inputs. See Mode Register and the Extended Mode Register descriptions for further details.

The MODE REGISTER SET command (see Figure 8) can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD (see Figure 9) is met.The values of the mode register and extended mode register will be retained even when exiting deep power-down.

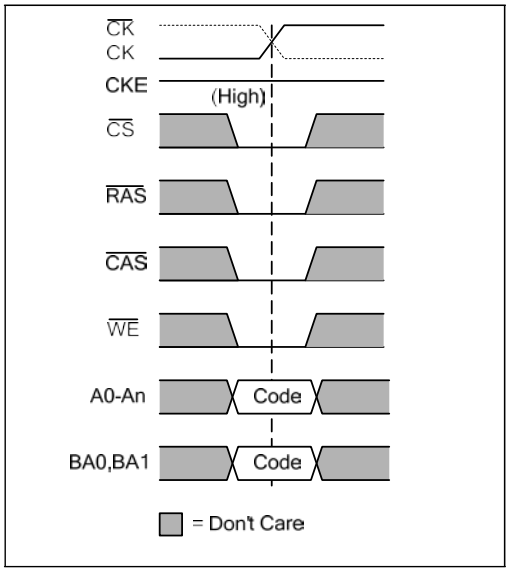


Figure 8 — Mode Register Set Command

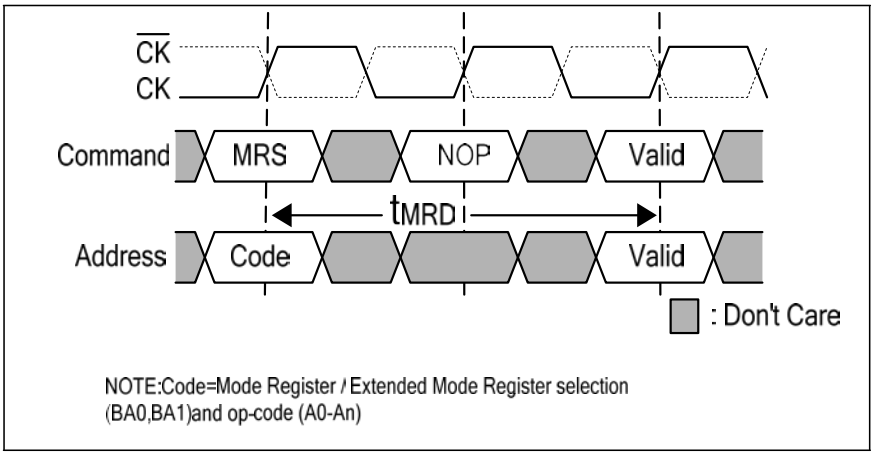


Figure 9 — Mode Register Set Command Timing

7.4. Active

Before any READ or WRITE commands can be issued to a bank in the LPDDR SDRAM, a row in that bank must be opened. This is accomplished by the ACTIVE command (see Figure 10): BA0 and BA1 select the bank, and the address inputs select the row to be activated. More than one bank can be active at any time.

Once a row is open, a READ or WRITE command could be issued to that row, subject to the t_{RCD} specification.

A subsequent ACTIVE command to another row in the same bank can only be issued after the previous row has been closed. The minimum time interval between two successive ACTIVE commands on the same bank is defined by t_{RC}.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between two successive ACTIVE commands on different banks is defined by t_{RRD}. Figure 11 shows the t_{RCD} and t_{RRD} definition.

The row remains active until a PRECHARGE command (or READ or WRITE command with Auto Precharge) is issued to the bank.

A PRECHARGE command (or READ or WRITE command with Auto Precharge) must be issued before opening a different row in the same

bank

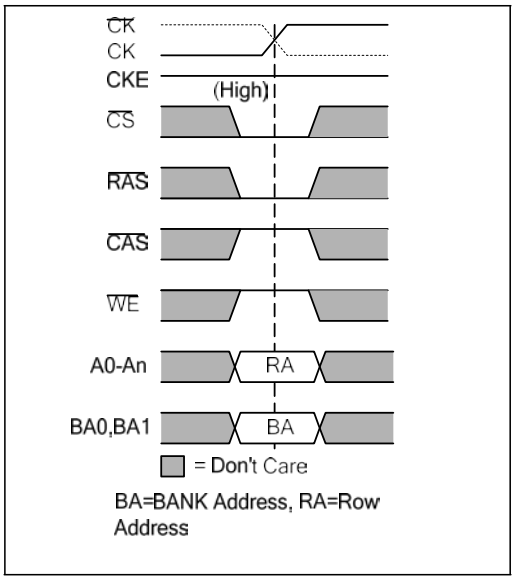


Figure 10 — Active Command

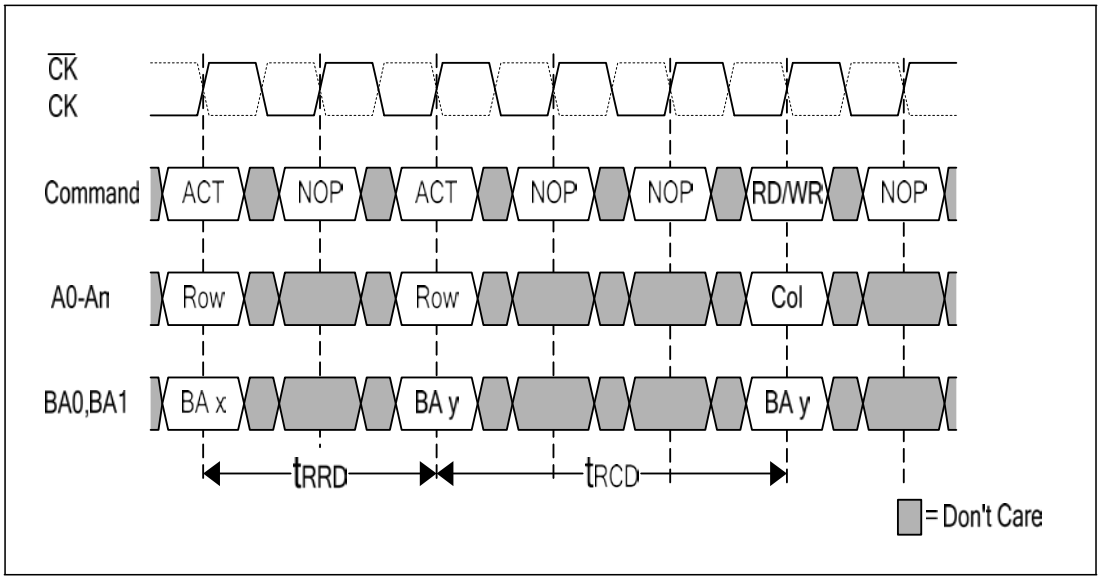


Figure 11 — Bank Activation Command Cycle

7.5. Read

The READ command (see Figure 12) is used to initiate a burst read access to an active row, with a burst length as set in the Mode Register. BA0 and BA1 select the bank, and the address inputs select the starting column location. The value of A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed will be precharged at the end of the read burst; if Auto Precharge is not selected, the row will remain open for subsequent accesses.

The basic Read timing parameters for DQs are shown in Figure 13; they apply to all Read operations.

During Read bursts, DQS is driven by the LPDDR SDRAM along with the output data. The initial Low state of the DQS is known as the read preamble; the Low state coincident with last data-out element is known as the read postamble. The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS. This is shown in Figure 14 with a CAS latency of 2 and 3.

Upon completion of a read burst, assuming no other READ command has been initiated, the DQs will go to High-Z.

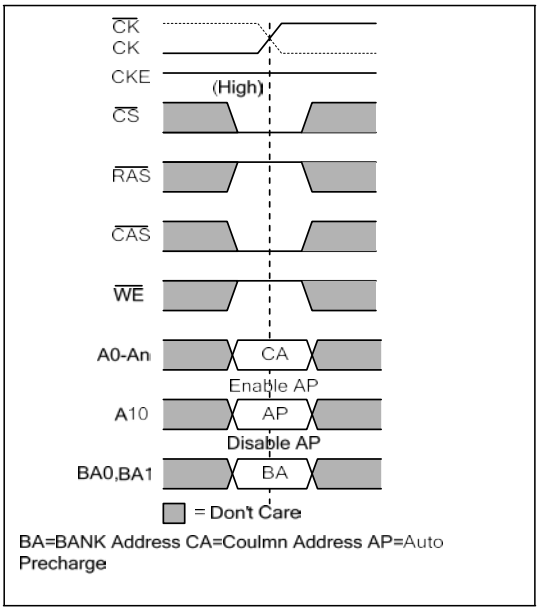


Figure 12 — Read Command

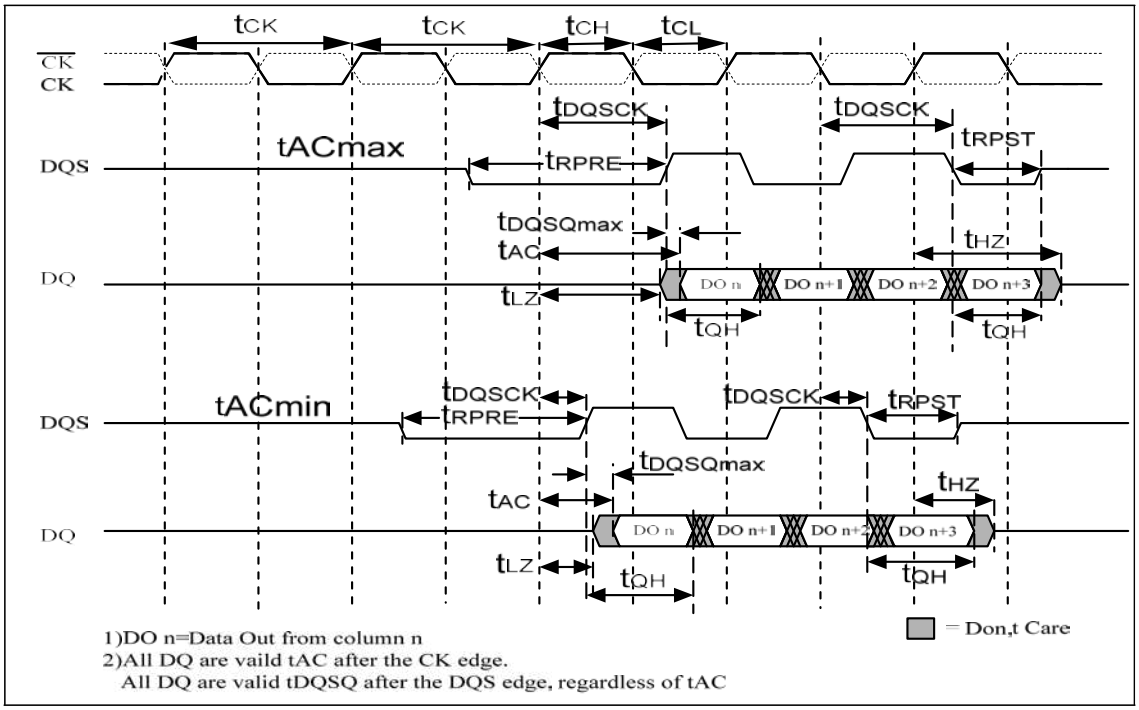


Figure 13 — Basic Read Timing Parameters

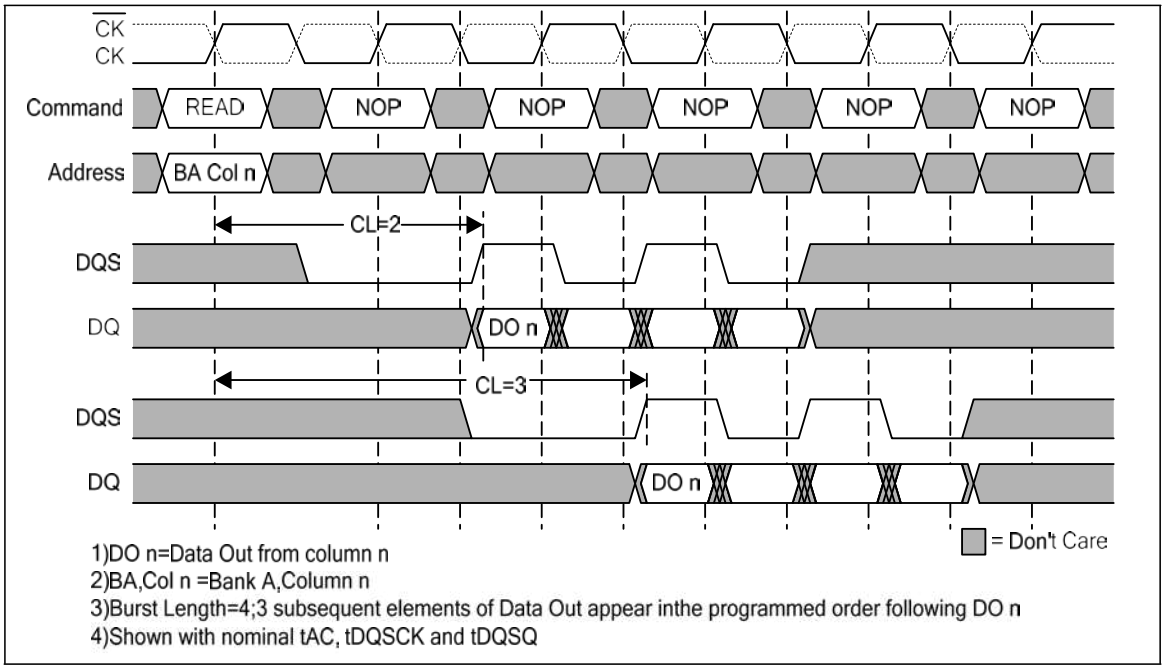


Figure 14 — Read Burst Showing CAS Latency

7.5.1 Read to Read

Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data-out element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 15.
A READ command can be initiated on any clock cycle following a previous READ command. Non-consecutive Reads are shown in Figure 16.
Full-speed random read accesses within a page or pages can be performed as shown in Figure 17.

7.5.2 Read Burst Terminate

Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 18. TheBURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element pairs.

7.5.3 Read to Write

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 19 for the case of nominal tDQSS .

5.5.4 Read to Precharge

A Read burst may be followed by or truncated with a PRECHARGE command to the same bank (provided Auto Precharge was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equal the number of desired data-out element pairs. This is shown in Figure 20. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data-out elements.
In the case of a Read being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from Read burst with Auto Precharge enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.