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Revision History

512M (16M x 32) Low Power SDRAM **AS4C16**M**32**MSA **90ball FBGA PACKAGE**

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Dec. 2017

512M(16Mx32) Low Power SDRAM

Features

- Functionality
- Standard SDRAM Functionality
- Programmable burst lengths : 1, 2, 4, 8 or full page
- 64ms refresh period (8K cycle)
- JEDEC Compatibility

- Low Power Features
- Auto TCSR(Temperature Compensated Self Refresh)
- Partial Array Self Refresh power-saving mode
- Deep Power Down Mode
- Driver Strength Control

- Operating Temperature Ranges:
- Industrial (-40℃ to +85℃)

- LVCMOS Compatible IO Interface

- 90 ball FBGA with 0.8 mm ball pitch (8mm x 13mm)
- AS4C16M32MSA : Pb-Free & Halogen Free

Functional Description

The AS4C16M32MSA Family is high-performance CMOS Dynamic RAMs (DRAM) organized as 16M x 32. These devices feature advanced circuit design to provide low active current and extremely low standby current.

The device is compatible with the JEDEC standard LP-SDRAM specifications.

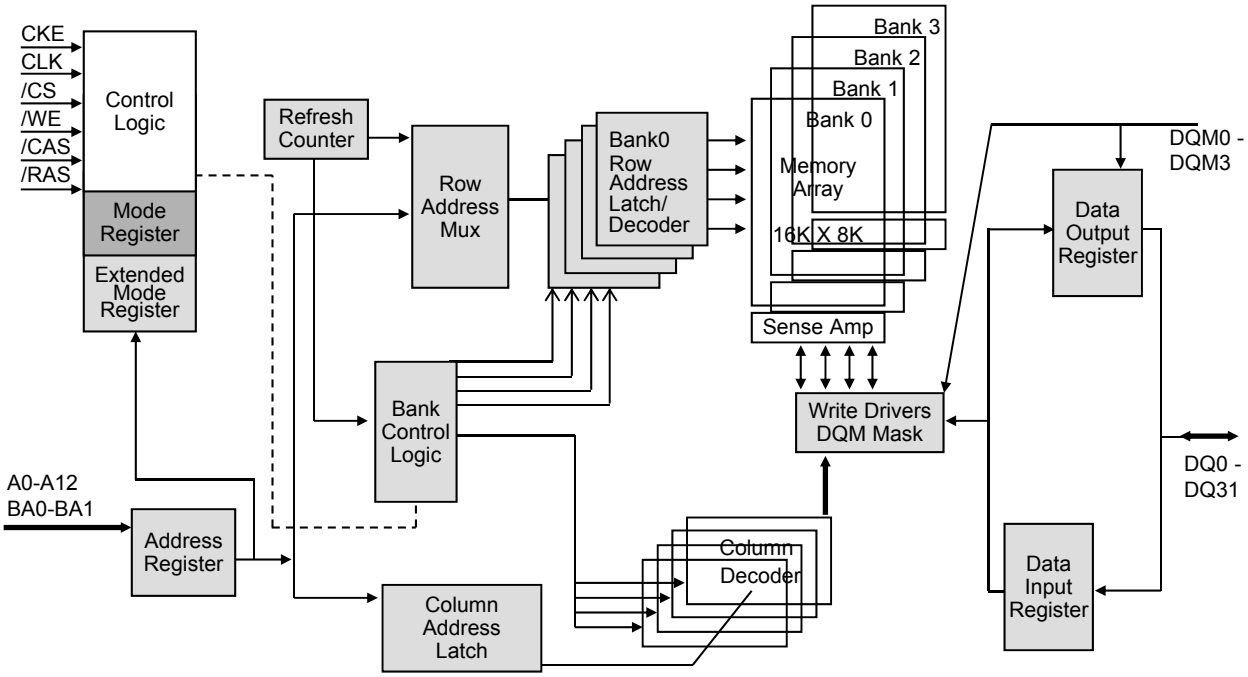
Table Ⅰ.Ordering Information

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C16M32MSA-6BIN	16M x 32	Industrial -40°C to 85°C	166MHz	90-ball FBGA

Table Ⅱ.Key Specifications

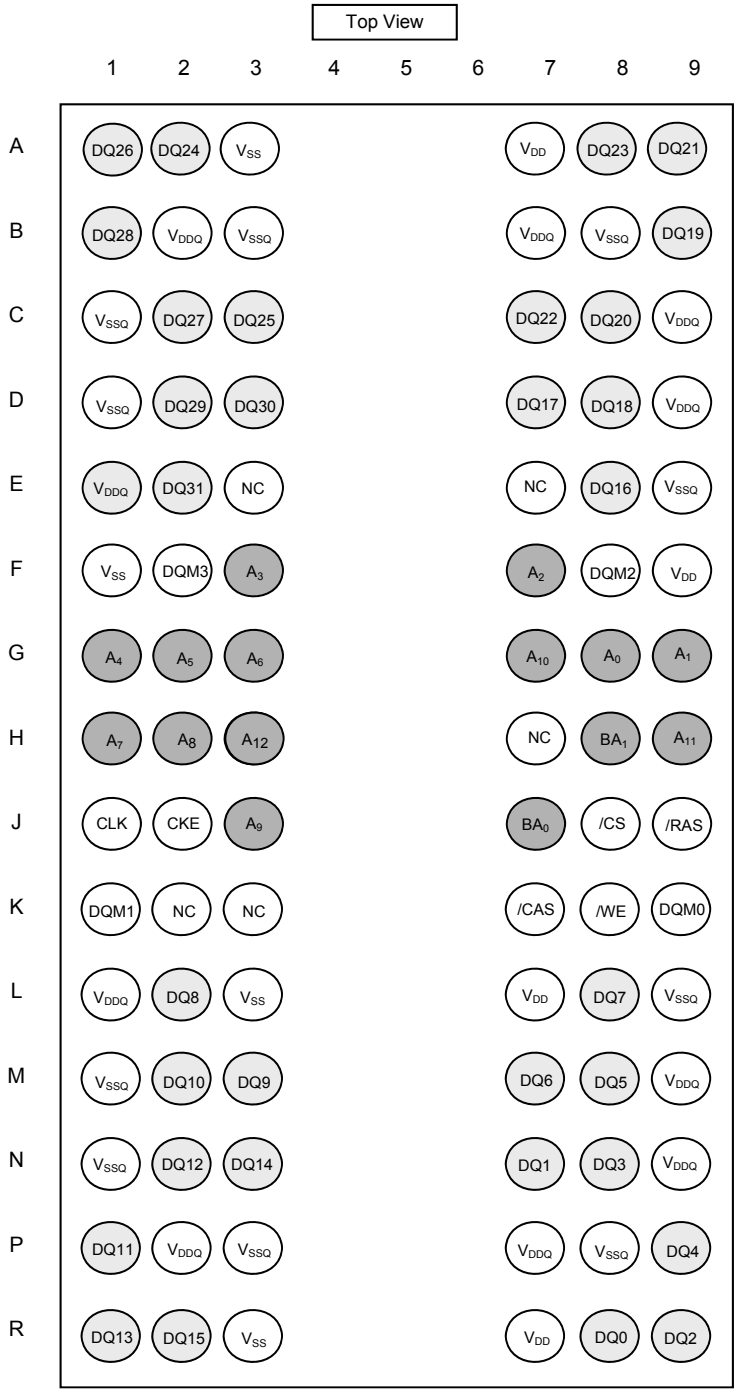
AS4C16M32MSA-6BIN		-6
tCK(3)	Clock Cycle time(min.)	6ns
tAC(3)	Access time from CLK (max.)	5.5ns
tRAS	Row Active time(min.)	48 ns
tRC	Row Cycle time(min.)	60ns

Logic Block Diagram



Pin Configuration

90 ball 0.8mm pitch FBGA(8mm x 13mm)



Pin Description

Symbol	Type	Description
CLK	Input	Clock : CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock Enable: CKE activates(HIGH) and deactivates(LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF Refresh operation(all banks idle), ACTIVE POWER-DOWN(row active in any bank) or CLOCK SUSPEND operation(burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
/CS	Input	Chip Select: /CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
/CAS, /RAS, /WE	Input	Command Inputs : /CAS, /RAS, and /WE (along with /CS) define the command being entered.
DQM0-3	Input	Input/Output Mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output disable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when during a READ cycle. DQM0 corresponds to DQ0 – DQ7, DQM1 corresponds to DQ8–DQ15, DQM2 corresponds to DQ16-DQ23, and DQM3 corresponds to DQ24-DQ31.
BA0, BA1	Input	Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. These pins also provide the op-code during a LOAD MODE REGISTER command.
A0-A12	Input	Address Inputs: A0–A12 are sampled during the ACTIVE command (row- address A0–A12) and READ/WRITE command (column-address A0–A8; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (A10 LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ	I/O	Data Input/Output : Data bus
NC	-	No Connect
V_{DDQ}	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
V_{SSQ}	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
V_{DD}	Supply	Power Supply: Voltage dependant on option.
V_{SS}	Supply	Ground.

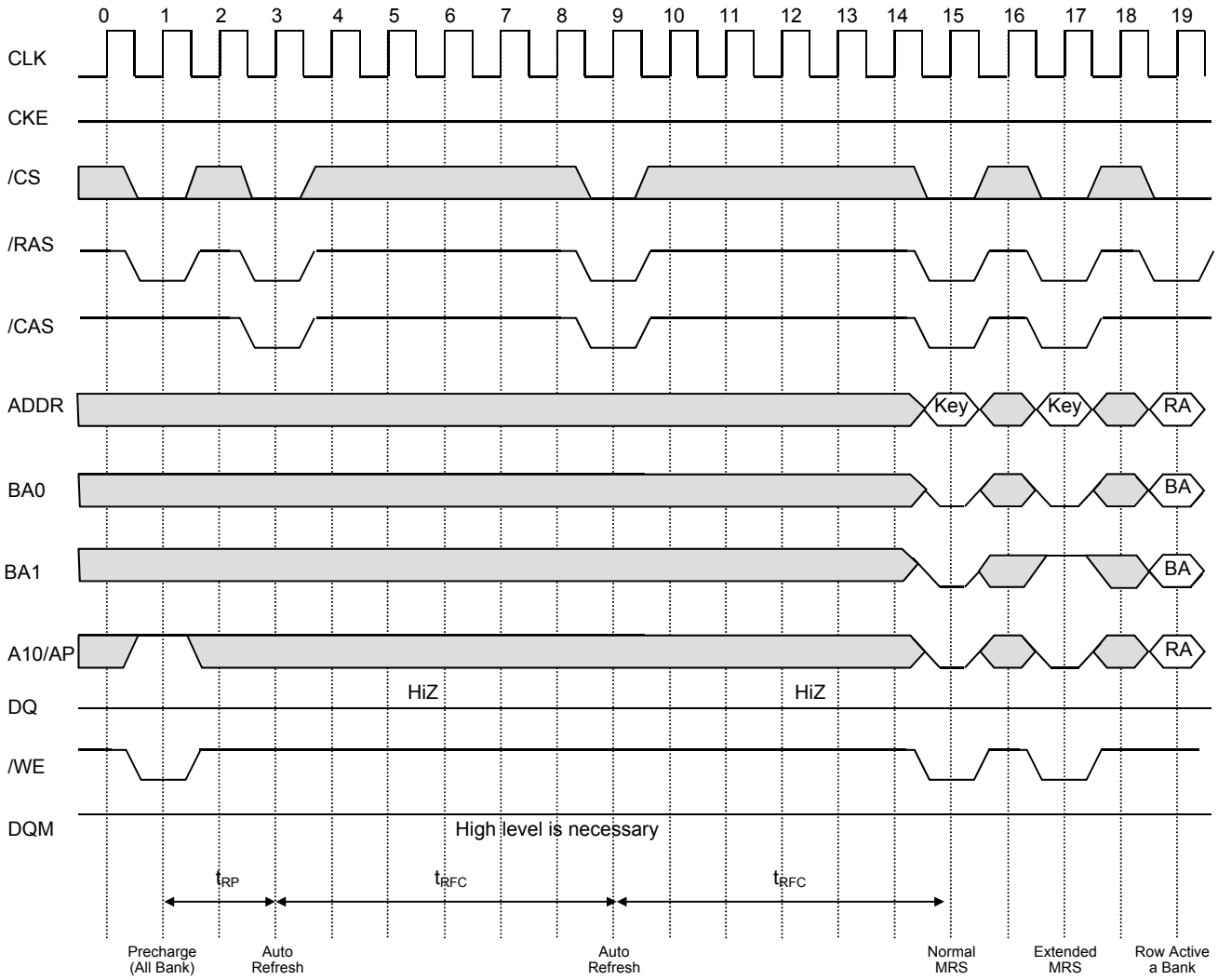
FUNCTIONAL DESCRIPTION

The Alliance 512Mb SDRAM is a quad-bank DRAM that operates at 1.8V and includes a synchronous inter-face (all signals are registered on the positive edge of the clock signal, CLK).
Read and write accesses accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0- A12 select the row). The address bits (A0-A8) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access. The SDRAM must be initialized prior to normal operation. The following sections provide detailed information regarding device initialization, register definition,command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V_{DD} and V_{DDQ}(simultaneously) and the clock is stable (meets the clock specifications in the AC characteristics), the SDRAM requires a 200µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. The COMMAND INHIBIT or NOP should be applied at least once during the 200µs delay. After the 200µs delay, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state. Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command. Refer Figure 1.

Figure 1. Initialize and Load Mode Register[1.2.3.]



Note :
1. The two AUTO REFRESH commands at T4 and T9 may be applied before either LOAD MODE REGISTER (LMR) command.
2. PRE = PRECHARGE command, LMR = LOAD MODE REGISTER command, AR = AUTO REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address
3. The Load Mode Register for both MR/EMR and 2 Auto Refresh commands can be in any order; However, all must occur prior to an Active command.

Register Definition

There are two mode registers which contain settings to achieve low power consumption. The two registers : Mode Register and Extended Mode Register are discussed below.

Mode Register

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Table 1. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power. Mode Register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the width burst mode, M10, M11, M12 and M13 should be set to zero. The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the SDRAM are burst oriented. The burst length is programmable, as shown in Table 2. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1,2, 4, or 8 locations are available for both the

sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths. Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A8 when the burst length is set to two; by A2-A8 when the burst length is set to four; and by A3-A8 when the burst length is set to eight.

The remaining(least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

The burst type can be set to either Sequential or Interleaved by using the M3 bit in the Mode register. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 2. [4.5.6.7.8.9.10.]

Table 1. Mode Register Definition.

M13-BA1	M12-BA0	M11-A11	M10-A10	M9-A9	M8-A8	M7-A7	M6-A6	M5-A5	M4-A4	M3-A3	M2-A2	M1-A1	M0-A0
Reserved(Set to '0')				WB	Op Mode		CAS Latency			BT	Burst Length		

M2 M1 M0	Burst Length	
	M3=0	M3=1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M9	Write Burst Mode
0	Prog. Burst Length
1	Single Mode Access

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

Note :

4. For full-page accesses: y =512
5. For a burst length of two, A1-A8 select the block-of-two burst; A0 selects the starting column within the block.
6. For a burst length of four, A2-A8 select the block-of-four burst; A0-A1 select the starting column within the block.
7. For a burst length of eight, A3-A8 select the block-of-eight burst; A0-A2 select the starting column within the block.
8. For a full-page burst, the full row is selected and A0-A8 select the starting column.
9. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
10. For a burst length of one, A0-A8 select the unique column to be accessed,and mode register bit M3 is ignored.

Table 2. Burst Length Definition.

Burst Length	Starting Column Address	Order of Accesses within a Burst	
		Type=Sequential	Type=Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page(y)	n=A0-A8(location 0-y)	Bn, Bn+1, Bn+2…..Bn,…	Not supported

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes.Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to one, two, or three clocks. If a READ command is registered at clock edge ***r***, and the latency is ***q*** clocks, the data will be available by clock edge ***r + q***. The DQs will start driving as a result of the clock edge one cycle earlier ***(r + q- 1)***, and provided that the relevant access times are met, the data will be valid by clock edge ***r + q.***

For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 2.

Table 3 indicates the operating frequencies at which each CAS latency setting can be used. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9=0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9=1, the programmed burst length applies to READ bursts, but write accesses are single-location (non-burst) accesses.

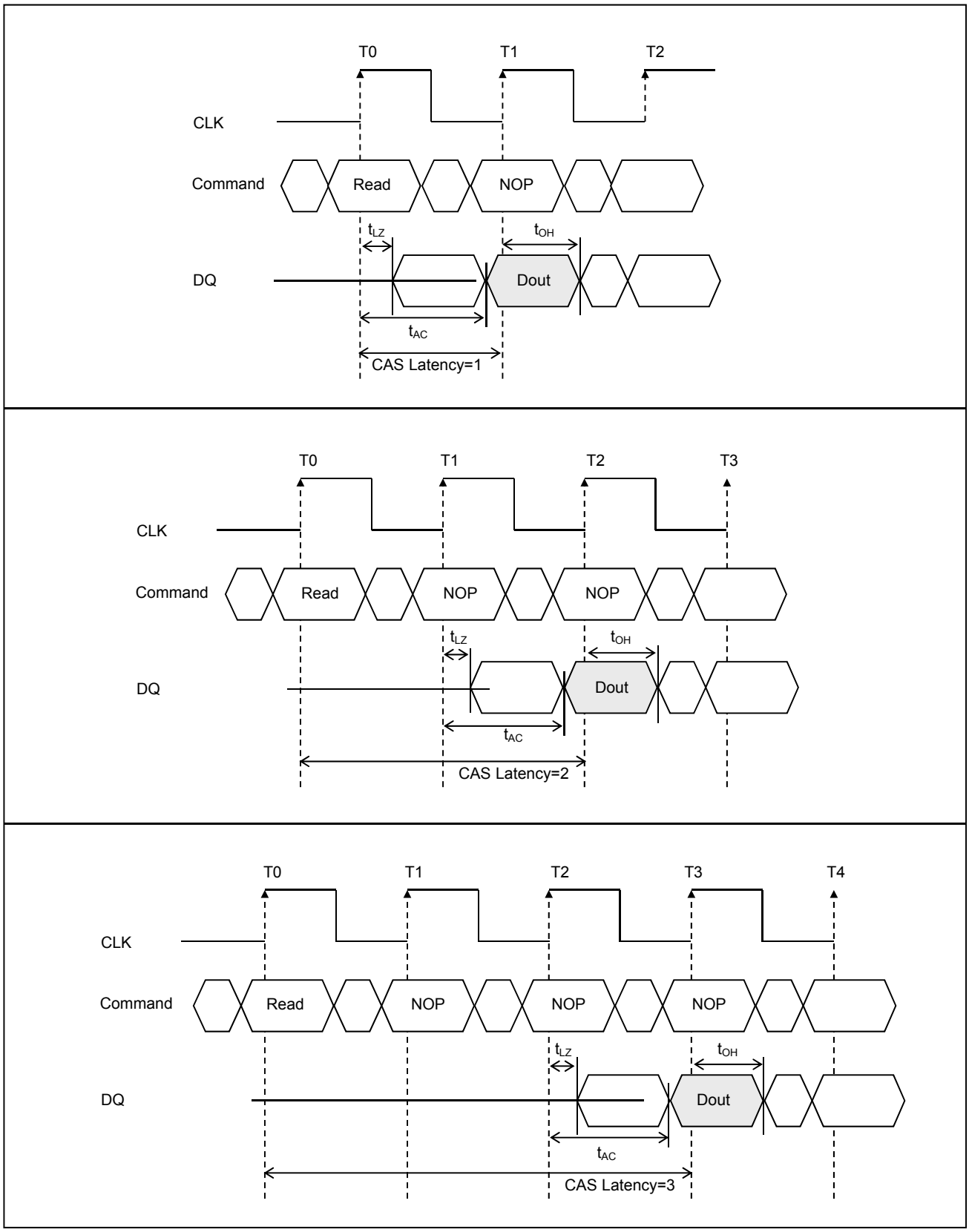


Figure 2. CAS Latency

Table 3. CAS Latency.

Speed	Allowable Operating Frequency (MHz)		
	CAS Latency = 1	CAS Latency = 2	CAS Latency = 3
166MHz	≤ 50	≤ 83	≤ 166

EXTENDED MODE REGISTER

The Extended Mode Register controls additional functions such as the Temperature Compensated Self Refresh (TCSR) Control, Partial Array Self Refresh (PASR), and Output Drive Strength.The Extended Mode Register is programmed via the Mode Register Set command (BA1=1, BA0=0) and retains the stored information until it is programmed again or the device loses power. The Extended Mode Register must be programmed with M8 through M11 set to "0". The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time initiating any subsequent operation. Violating either of these requirements results in unspecified operation.

AUTO TEMPERATURE COMPENSATED SELF REFRESH

Every cell in the DRAM requires refreshing due to the capacitor losing its charge over time. The refresh rate is dependent on temperature. At higher temperatures a capacitor loses charge quicker than at lower temperatures, requiring the cells to be refreshed more often. In order to save power consumption, according to the temperature, Mobile-SDRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically.

PARTIAL ARRAY SELF REFRESH

The Partial Array Self Refresh (PASR) feature allows the controller to select the amount of memory that will be refreshed during SELF REFRESH. The refresh options are full array (banks 0, 1, 2, and 3); half array(banks 0 and 1); and quarter array(bank 0). WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks in PASR will be refreshed during SELF REFRESH. The data in banks 2 and 3 will be lost when the half array option is used. Similarly the data will be lost in banks 1, 2, and 3 when the quarter array option is used.

Driver Strength Control

The driver strength feature allows one to reduce the drive strength of the I/O's on the device during low frequency operation. This allows systems to reduce the noise associated with the I/O's switching.

Table 4. Extended Mode Register Definition

EM13-BA1	EM12-BA0	EM11-A11	EM10-A10	EM9-A9	EM8-A8	EM7-A7	EM6-A6	EM5-A5	EM4-A4	EM3-A3	EM2-A2	EM1-A1	EM0-A0
1	0	All must be set to '0'				Driver Strength			0	0	PASR		

Table 5. Extended Mode Register Table[11.12.].

A2	A1	A0	Self Refresh Coverage
0	0	0	All Banks
0	0	1	Half of Total Bank(BA1=0)
0	1	0	Quarter of Total Bank(BA1=BA0=0)
0	1	1	RFU
1	0	0	RFU
1	0	1	One Eighth of Total Bank (BA1=BA0=Row Address MSB=0)
1	1	0	One Sixteenth of Total Bank (BA1=BA0=Row Address2 MSBs=0)
1	1	1	RFU

A7	A6	A5	Driver Strength
0	0	0	100%
0	0	1	50%
0	1	0	25%
0	1	1	12.5%
1	0	0	75%
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Note :

11. EM13 and EM12 (BA1 and BA0) must be "1, 0" to select the Extended Mode Register(vs. the base Mode Register).
12. RFU: Reserved for Future Use

Table 6. Commands[13.14.15.16.17.18.19.20.] .

Name(Function)	CKE	/CS	/RAS	/CAS	/WE	DQM	ADDR	DQ
COMMAND INHIBIT(NOP)	X	H	X	X	X	X	X	X
NO OPERATION(NOP)	H	L	H	H	H	X	X	X
ACTIVE(Select bank and activate row)[14]	H	L	L	H	H	X	Bank/ Row	X
READ(Select bank and column, and start READ burst)[15]	H	L	H	L	H	L/H[20]	Bank/ Col	X
WRITE(Select bank and column, and start WRITE burst)[15]	H	L	H	L	L	L/H[20]	Bank/ Col	Valid
BURST TERMINATE	H	L	H	H	L	X	X	Active
PRECHARGE(Deactivate row in bank or banks)[16]	H	L	L	H	L	X	Code	X
AUTO REFRESH or SELF REFRESH(Enter Self Refresh Mode)[17. 18]	H	L	L	L	H	X	X	X
LOAD MODE REGISTER[19]	H	L	L	L	L	X	Opcode	X
Write Enable/Output Enable[20]	H	-	-	-	-	L	-	Active
Write Inhibit/Output High-Z[20]	H	-	-	-	-	H		High Z
Deep Power Down(Enter DPD Mode)	L	L	H	H	L	X	X	X

Note :

13. CKE is HIGH for all commands shown except SELF REFRESH and Deep Power Down.
14. A0-A11 provide row address, and BA0, BA1 determine which bank is made active.
15. A0-A8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
16. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are "Don't Care."
17. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
18. This command is AUTO REFRESH if CKEn is HIGH, SELF REFRESH if CKEn is LOW.
19. A0-A9 define the op-code written to the mode register and BA0, BA1 determine Normal MRS and Extended MRS.
20. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay). DQM0 controls DQ0-7, DQM1 controls DQ8-15, DQM2 controls DQ16-23 and DQM3 controls DQ24-31.

Commands

Table 6. provides a reference of all the commands available with the state of the control signals for executing a specific command.

COMMAND INHIBIT
The COMMAND INHIBIT function effectively deselects the SDRAM by preventing new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. Operations already in progress are not affected.

NO OPERATION (NOP)
The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (/CS is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER
The mode register is loaded via inputs A0-A11, BA0, BA1. The LOAD MODE REGISTER and LOAD EXTENDED MODE REGISTER commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until t_{MRD} is met. Table 1, Table 4 And Table 5 provide the definition for the Mode Register and Extended Mode Register.

ACTIVE
The ACTIVE command is used to activate a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A11 selects the row. This row remains active for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ
READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. If auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQs subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

WRITE
The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst. If auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE
The PRECHARGE command is used to deactivate the active row in a particular bank or the active row in all banks. The bank(s) will be available for a subsequent row access after a specified time (t_{RP}) from the issued PRECHARGE command. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE
AUTO PRECHARGE is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. AUTO PRECHARGE thus performs the same PRECHARGE command described above , without requiring an explicit command. A PRECHARGE of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE does not apply in the full page mode burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.
Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (t_{RP}) is completed.

BURST TERMINATE
The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM. This command is non-persistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum t_{RP} has been met after the PRECHARGE command. The addressing is generated by the internal refresh controller. The address bits thus are a “Don’t Care” during an AUTO REFRESH command. The Alliance 512Mb SDRAM requires 8,192 AUTO REFRESH cycles every 64ms (t_{REF}), regardless of width option. Providing a distributed AUTO REFRESH command every 7.8125µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (t_{RFC}), once every 64ms.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM(without external clocking), even if the rest of the system is powered down. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care” with the exception of CKE, which must remain LOW. Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to t_{RAS} and may remain in self refresh mode for an indefinite period beyond that. The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (meet the clock specifications in the AC characteristics) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for t_{XSR} because time is required for the completion of any internal refresh in progress. Upon exiting the self refresh mode, AUTO REFRESH commands must be issued every 7.8125µs or less as both SELF REFRESH and AUTO REFRESH utilize he row refresh counter.

DEEP POWER DOWN

Deep Power Down Mode is an operating mode to achieve extreme power reduction by cutting the power of the whole memory array of the device. Data will not be retained once the device enters DPD Mode. Full initialization is required when the device exits from DPD Mode. [Figure 29.30]

Maximum Ratings

Voltage on V_{DD}/V_{DDQ} Supply
Relative to V_{SS} .....-0.5V to + 3.6V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} ..... –0.5V to +3.6V
Storage Temperature(plastic) ..... -55℃ to + 150℃
Power Dissipation 1W

*Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device.This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Device	Range	Ambient Temperature	V_{DD}	V_{DDQ}
AS4C16M32MSA	Industrial	-40℃ to +85℃	1.7V to 1.95V	1.7V to VDD

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS [21.22.]

Parameter / Condition	Symbol	Min	Max	Units
Supply Voltage	V_{DD}	1.7	1.95	V
I/O Supply Voltage	V_{DDQ}	1.7	VDD	V
Input High Voltage : Logic 1 All Inputs [23.]	V_{IH}	0.8* V_{DDQ}	V_{DDQ} +0.3	V
Input Low Voltage : Logic 0 All Inputs [23.]	V_{IL}	-0.3	0.2*V_{DDQ}	V
Data Output High Voltage : Logic 1 : All Inputs(-0.1mA)	V_{OH}	0.9* V_{DDQ}		V
Data Output Low Voltage : Logic 0 : All Inputs(0.1mA)	V_{OL}		0.1*V_{DDQ}	V
Input Leakage Current : Any Input 0V=V_{IN}=V_{DD} (All other pins not under test=0V)	IL	-5	5	μA
Output Leakage Current : DQs are disabled ; 0V= V_{OUT}=V_{DDQ}	I_{OZ}	-5	5	μA

Table 7. AC OPERATING CONDITIONS[21.22.23.24.25.26.]

Parameter / Condition	Symbol	Value	Units
Input High Voltage : Logic 1 All Inputs	V_{IH}	0.8* V_{DDQ}	V
Input Low Voltage : Logic 0 All Inputs	V_{IL}	0.2* V_{DDQ}	V
Input and Output Measurement Reference Level		0.5*V_{DDQ}	V

Table 8. I_{DD} Specifications and Conditions [21.22.26.27.].

Parameter	Description	-6	Units
$I_{DD}1$	Operating Current: Active Mode; Burst =2 ; Read or Write ; $t_{RC} \geq t_{RC}$(min); CAS Latency =3 [28.29.30.]	80	mA
$I_{DD}2P$	Precharge Standby Current in power down mode : CKE $\leq V_{IL}$(max)	0.3	mA
$I_{DD}2N$	Precharge Standby Current in non power down mode : CKE $\geq V_{IH}$(min), /CS $\geq V_{IH}$(min) [28.29.30,31.]	15	mA
$I_{DD}3P$	Active Standby Current in power down mode; CKE $\leq V_{IL}$(max) [28.29,30.31.],	5	mA
$I_{DD}3N$	Active Standby Current in non power down mode (One Bank Active); CKE $\geq V_{IH}$(min), /CS $\geq V_{IH}$(min) [28.29,30.31.]	15	mA
$I_{DD}4$	Operating Current: Burst Mode: Continuous Burst ; Read or Write : All banks Active, CAS Latency =3[28.29.30.]	100	mA
$I_{DD}5$	Auto Refresh Current : $t_{RFC} \geq t_{RFC}$(138ns)	110	mA
$I_{DD}6$	Self Refresh Current : CKE $\leq$ 0.2V, 4 Banks, t_{CLK}= ∞, 85°C	700	μA
	Self Refresh Current : CKE $\leq$ 0.2V, 2 Banks , t_{CLK}= ∞, 85°C	520	μA
	Self Refresh Current : CKE $\leq$ 0.2V, 1 Banks, t_{CLK}= ∞, 85°C	430	μA
$I_{DD}7$	Deep power down, t_{CLK}= ∞	10	μA

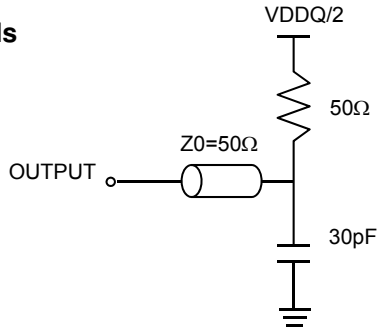
Note :

21. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-40°C = TA = +85°C for IT parts) is ensured.
22. An initial pause of 200μs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
23. All states and sequences not shown are illegal or reserved.
24. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
25. t_{HZ} defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet t_{OH} before going High-Z.
26. AC timing and I_{DD} tests have V_{IL} and V_{IH}, with timing referenced to $V_{IH/2}$ = crossover point. If the input transition time is longer than t_T (MAX), then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the $V_{IH/2}$ crossover point.
27. I_{DD} specifications are tested after the device is properly initialized.
28. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
29. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
30. Input signals are changed one time during 20ns.
31. Unless otherwise note, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).
32. CKE is HIGH during refresh command period t_{RFC} (MIN) else CKE is LOW. The I_{DD} 6 limit is actually a nominal value and does not result in a fail value

Capacitance

Parameter	Description	Test Conditions	Max	Units
C_{IN}	Input Capacitance	T_A=25℃, f=1Mhz, $V_{DD(typ)}$	4	pF
C_{OUT}	Output Capacitance		6	pF

AC Test Loads



AC Characteristics

AC Characteristics		Symbol	-6		Units
Parameter			Min	Max	
Clock Period[33.]		t_{CLKS3}	6.0		ns
		t_{CLKS2}	12		
Clock High Time		t_{CH}	2.5		ns
Clock Low Time		t_{CL}	2.5		ns
Address Setup Time to Clock		t_{CAS}	2.0		ns
Address Hold Time to Clock		t_{CAH}	1.0		ns
CKE Setup Time to Clock		t_{CKS}	2.0		ns
CKE Hold Time to Clock		t_{CKH}	1.0		ns
Clock Access Time[34, 35]	CL=3	$t_{AC}(3)$		5.5	ns
	CL=2	$t_{AC}(2)$		6	ns
	CL=1	$t_{AC}(1)$		22	ns
Output Hold Time from Clock		t_{OH}	2.5		ns
Data In Setup Time to Clock		t_{CDS}	2.0		ns
Data In Hold Time to Clock		t_{CDH}	1.0		ns
/CS, /RAS, /CAS, /WE, /DQM Setup Time to Clock		t_{CMS}	2.0		ns
/CS, /RAS, /CAS, /WE, /DQM Hold Time to Clock		t_{CMH}	1.0		ns
Data High Impedance Time[25.]		t_{HZ}		6	ns
Active to Precharge Command		t_{RAS}	48	100000	ns
Active to Active Command Period		t_{RC}	60		ns
Active to Read/Write Delay		t_{RCD}	18		ns
Refresh Period(8192 rows)		t_{REF}		64	ms
Auto Refresh Period		t_{RFC}	80		ns
Precharge Command Period		t_{RP}	18		ns
Active Bank ‘a’ to Active Bank ’b’ Command		t_{RRD}	12		ns
Transition Time[36.]		t_T	0.5	1.2	ns
Write Recovery Time[37.]		t_{WR}	15		ns
Exit Self Refresh to Active Command[38.]		t_{XSR}	80		ns
READ/WRITE command to READ/WRITE command[39.]		t_{CCD}	1		t_{CLK}
CKE to clock disable or power-down entry mode[40.]		t_{CKED}	1		t_{CLK}
CKE to clock enable or power-down exit setup mode[40.]		t_{PED}	1		t_{CLK}
DQM to input data delay[39.]		t_{DQD}	0		t_{CLK}
DQM to data mask during WRITEs[39.]		t_{DQM}	0		t_{CLK}
DQM to data high-impedance during READs[39.]		t_{DQZ}	2		t_{CLK}
WRITE command to input data delay[39.]		t_{DWD}	0		t_{CLK}
Data-in to ACTIVE command[41.]		t_{DAL}	5		t_{CLK}
Data-in to PRECHARGE command[42.]		t_{DPL}	2		t_{CLK}
Last data-in to burst STOP command[39.]		t_{BDL}	1		t_{CLK}

AC Characteristics

AC Characteristics		Symbol	-6		Units
Parameter			Min	Max	
Last data-in to new READ/WRITE command[39.]		t_{CDL}	1		t_{CLK}
Last data-in to PRECHARGE command[42.]		t_{RDL}	2		t_{CLK}
LOAD MODE REGISTER command to ACTIVE or REFRESH command[43.]		t_{MRD}	2		t_{CLK}
Data-out to high-impedance from PRECHARGE command[40.]	CL=3	$t_{ROH}(3)$	3		t_{CLK}
	CL=2	$t_{ROH}(2)$	2		t_{CLK}
	CL=1	$t_{ROH}(1)$	1		t_{CLK}

Note :

33. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including t_{WR}, and PRECHARGE commands). CKE may be used to reduce the data rate.
34. t_{AC} for -166Mhz at CL=3 with no load is 5ns and is guaranteed by design.
35. t_{AC} for -166Mhz at CL=3 and V_{DD} of 1.8V is 5.5ns.
36. AC characteristics assume t_T = 1ns.
37. Auto precharge mode only. The precharge timing budget (t_{RP}) begins at 3ns for -166Mhz after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
38. CLK must be toggled a minimum of two times during this period.
39. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
40. Timing actually specified by t_{CKS}; clock(s) specified as a reference only at minimum cycle rate.
41. Timing actually specified by t_{WR} plus t_{RP}; clock(s) specified as a reference only at minimum cycle rate.
42. Timing actually specified by t_{WR}.
43. JEDEC and PC100 specify three clocks.

Operation

BANK / ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened" (activated). This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated. A READ or WRITE command may then be issued to that row, subject to the t_{RCD} specification. t_{RCD} (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, t_{RCD} specification of 18ns with a 166MHz clock (6ns period) results in 3 clocks. (The same procedure is used to convert other specification limits from time units to clock cycles.) A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by t_{RC}. A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by t_{RRD}.

READs

READ bursts are initiated with a READ command, as shown in Figure 3. The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. For the generic READ commands used in the following illustrations, auto precharge is disabled. During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 2. shows general timing for each possible CAS latency setting.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A full-page burst will continue until terminated. (The burst will wrap around at the end of the page). A continuous flow of data can be maintained by having additional Read Burst or single Read Command. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated.

The new READ command should be issued ***x*** cycles before the clock edge at which the last desired data element is valid, where ***x*** equals the CAS latency minus one.

This is shown in Figure 4. for CAS latencies of one, two and three; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Full-speed random read accesses can be performed to the same bank, as shown in Figure 5. , or each subsequent READ may be performed to a different bank.

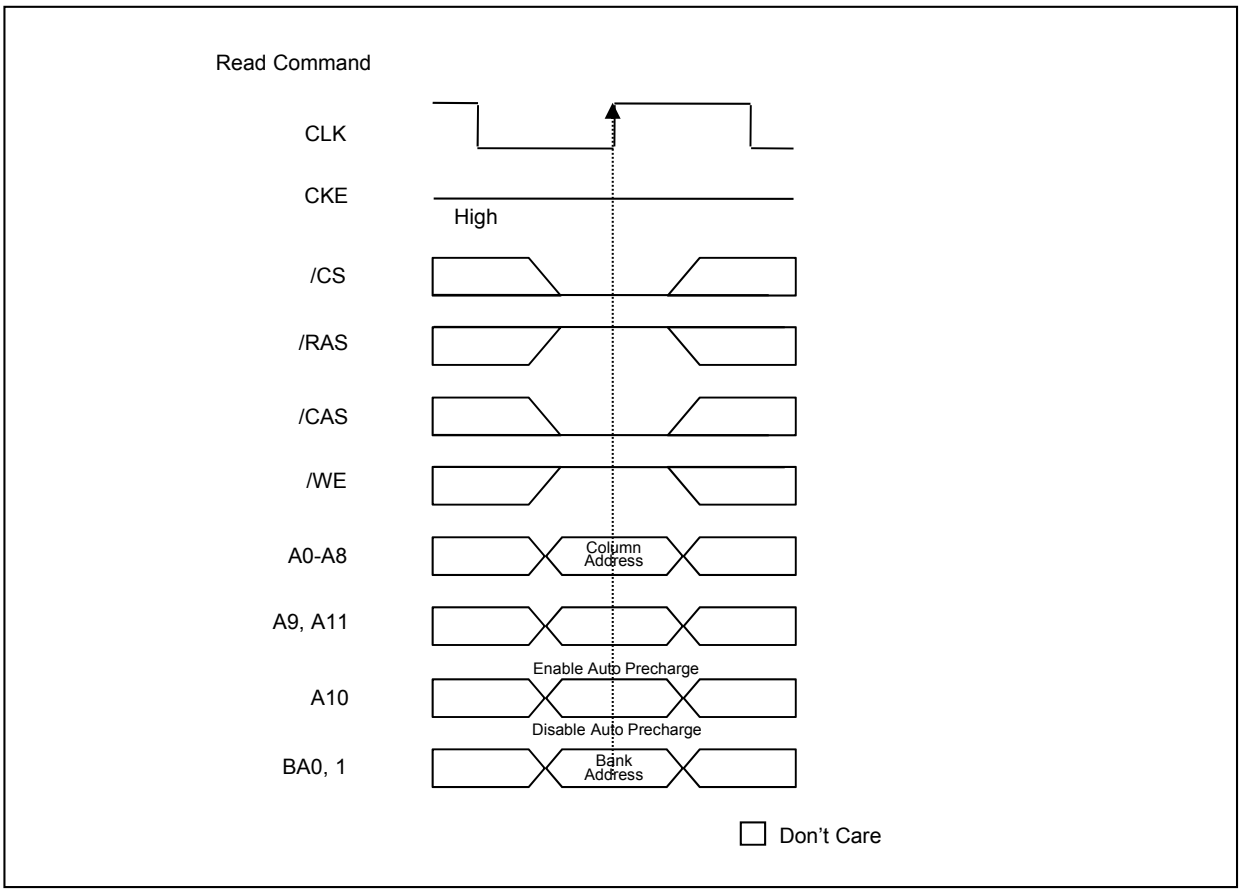


Figure 3. Read Command

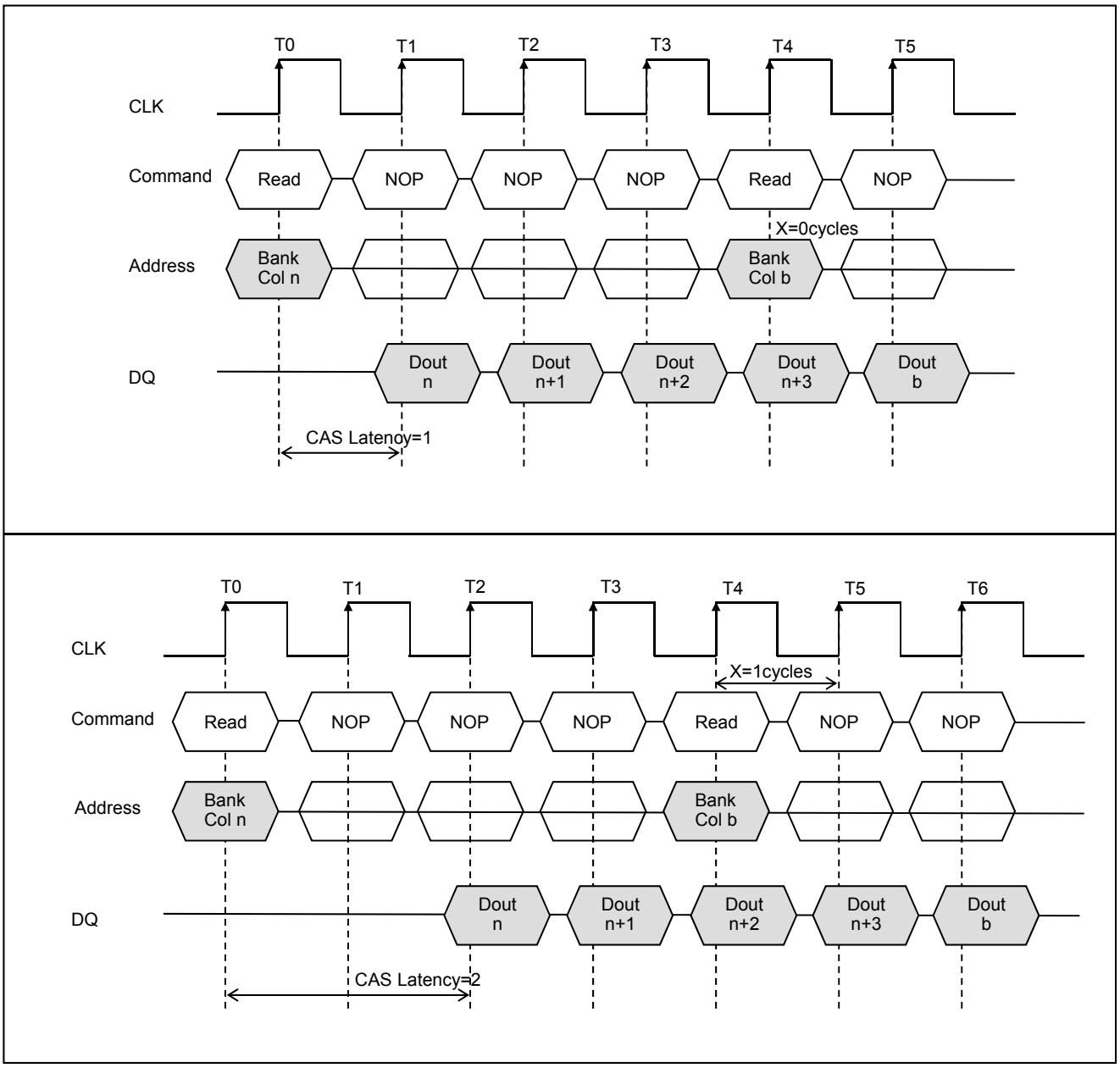


Figure 4. Consecutive Burst Reads -Transition from Burst of 4 Read to a Single read for CAS Latency 1,2,3

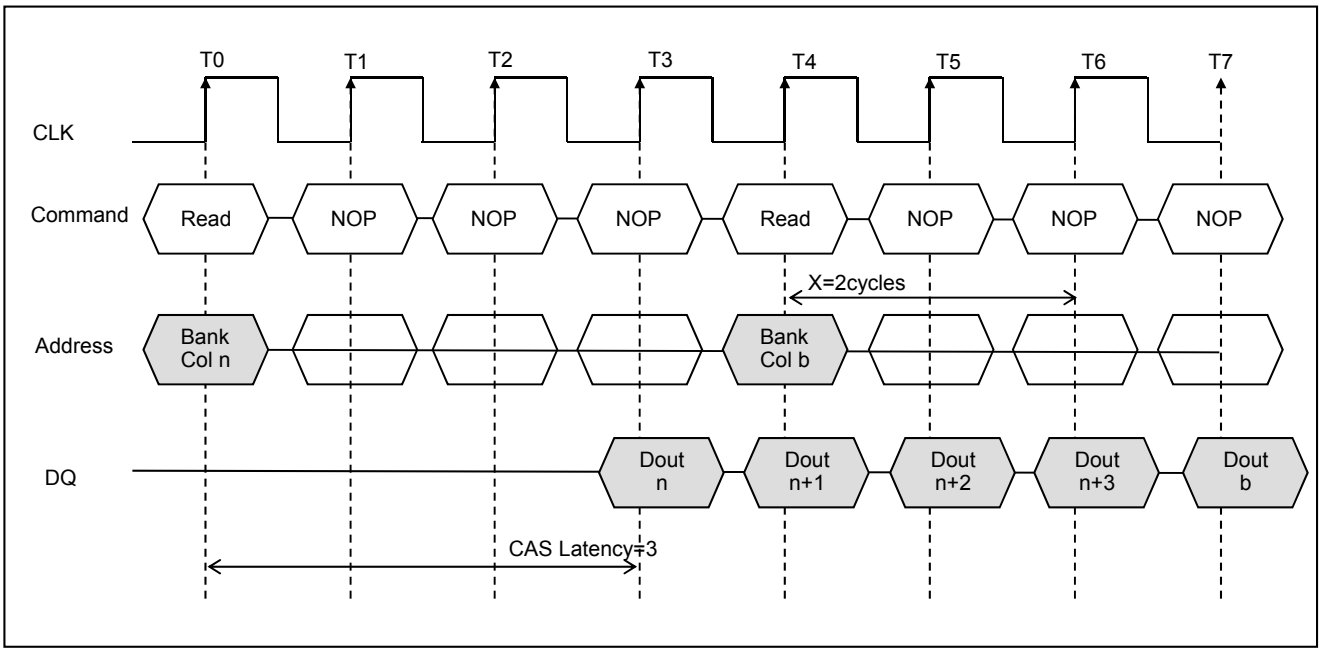


Figure 4. Consecutive Burst Reads -Transition from Burst of 4 Read to a Single read for CAS Latency 1,2,3

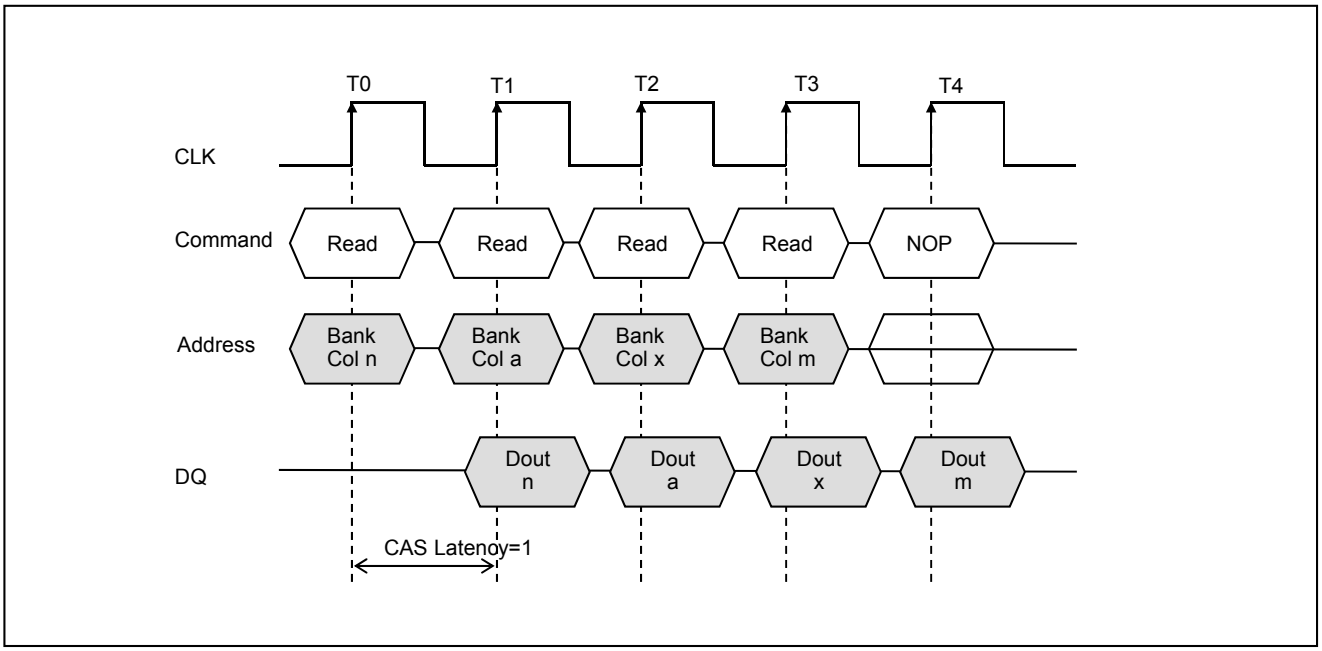


Figure 5. Random Read Accesses for CAS Latency =1,2,3

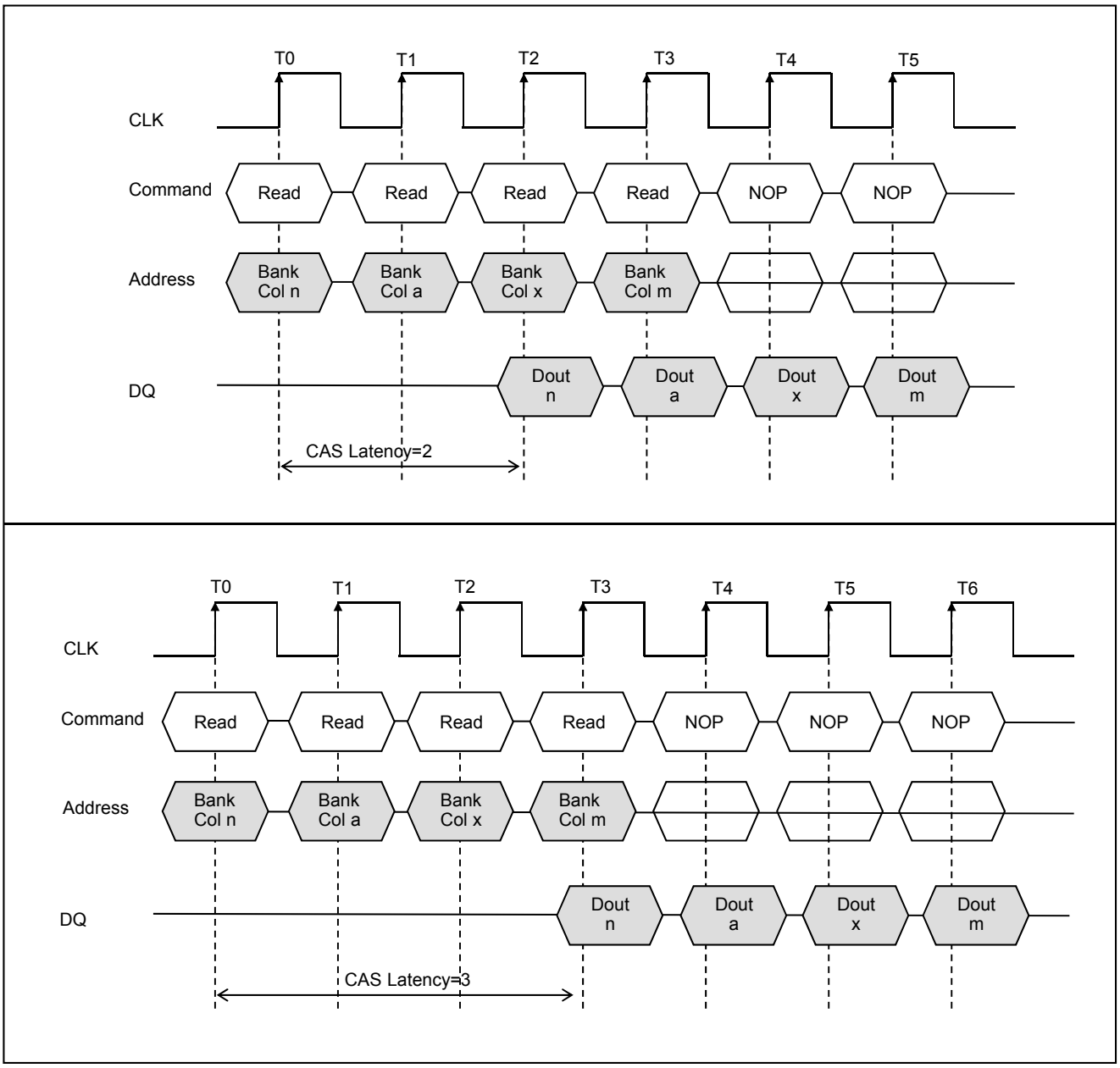


Figure 5. Random Read Accesses for CAS Latency =1,2,3

A Read Burst can be terminated by a subsequent Write command, and data from a fixed length READ burst may be immediately followed by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command. The DQM input is used to avoid I/O contention, as shown in Figure 6. and Figure 7. . The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM

was active on the clock just prior to the WRITE command that truncated the READ command. The DQM signal must be asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 6. shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 7. shows the case with the additional NOP cycle.

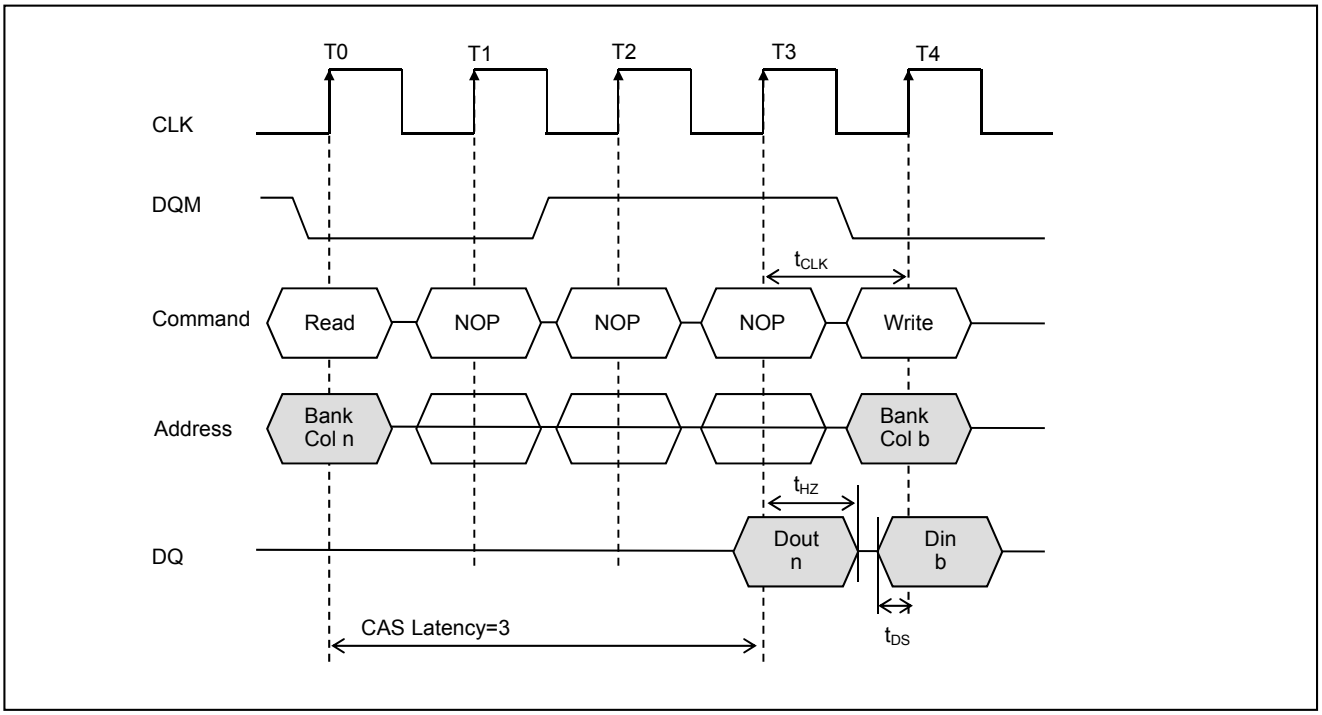


Figure 6. Read to Write

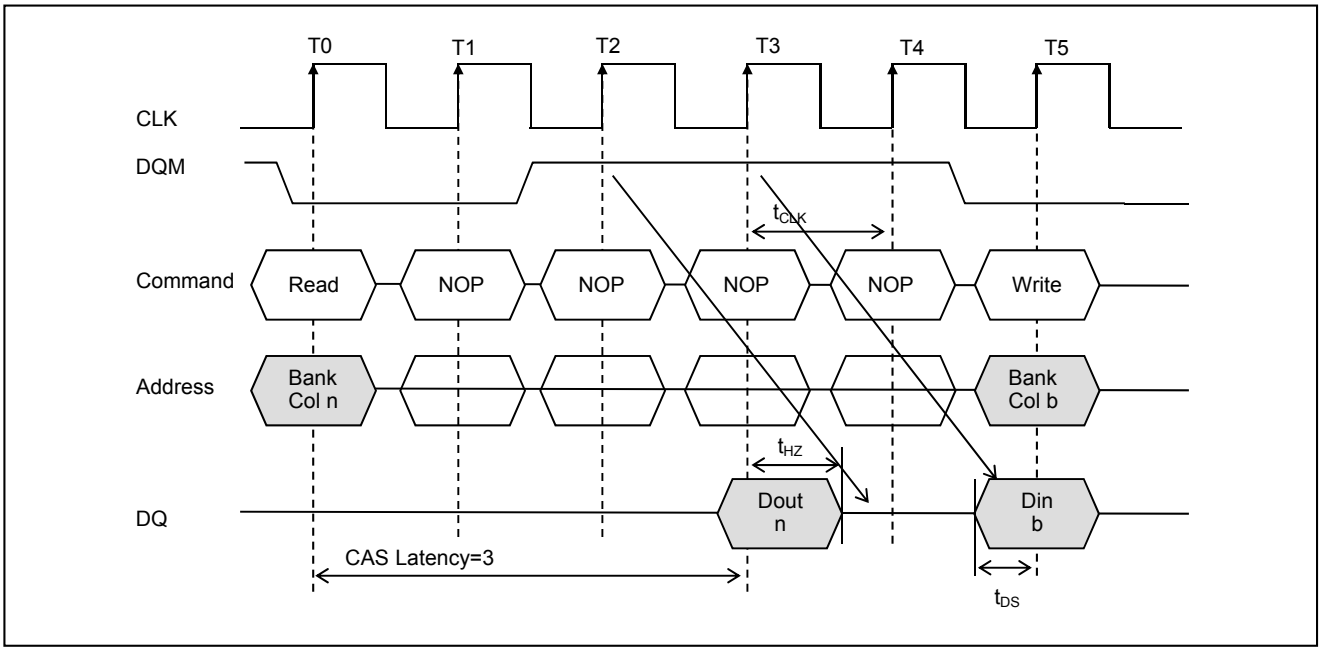


Figure 7. Read to Write with extra clock cycle

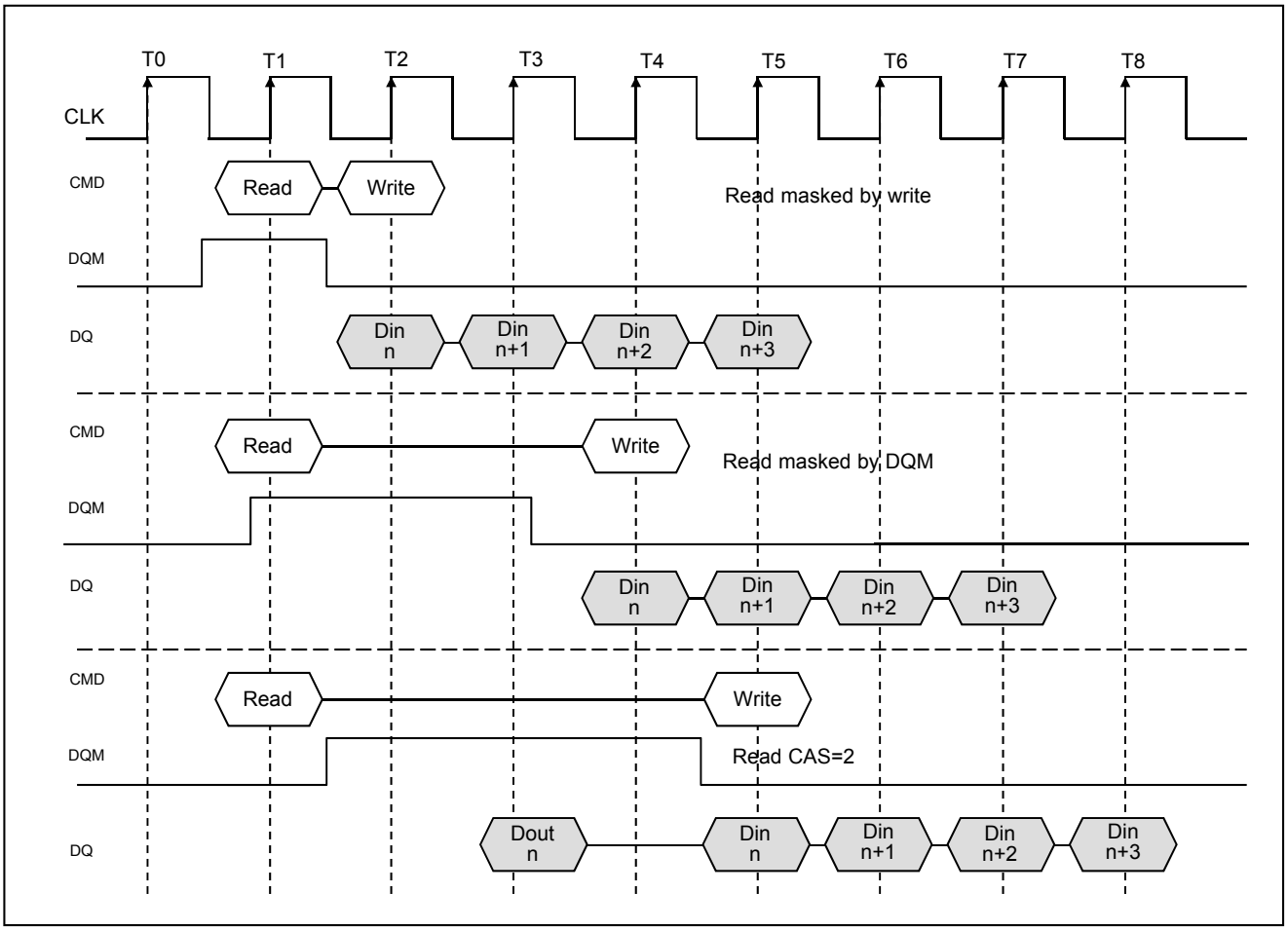


Figure 8. Read Interrupted by Write with DQM ; CAS Latency =2

A fixed-length READ burst or a full-page burst may be followed by, or truncated with, a PRECHARGE command to the same bank. The PRECHARGE command should be issued ***x*** cycles before the clock edge at which the last desired data element is valid, where ***x*** equals the CAS latency minus one. This is shown in Figure 9. for each possible CAS latency; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met. Note that part of the row precharge time is hidden during the access of the last data element(s). The BURST TERMINATE command should be issued ***x*** cycles before the clock edge at which the last desired data element is valid, where ***x*** equals the CAS latency minus one. This is shown in Figure 10. for each possible CAS latency; data element *n* + 3 is the last desired data element of a longer burst.

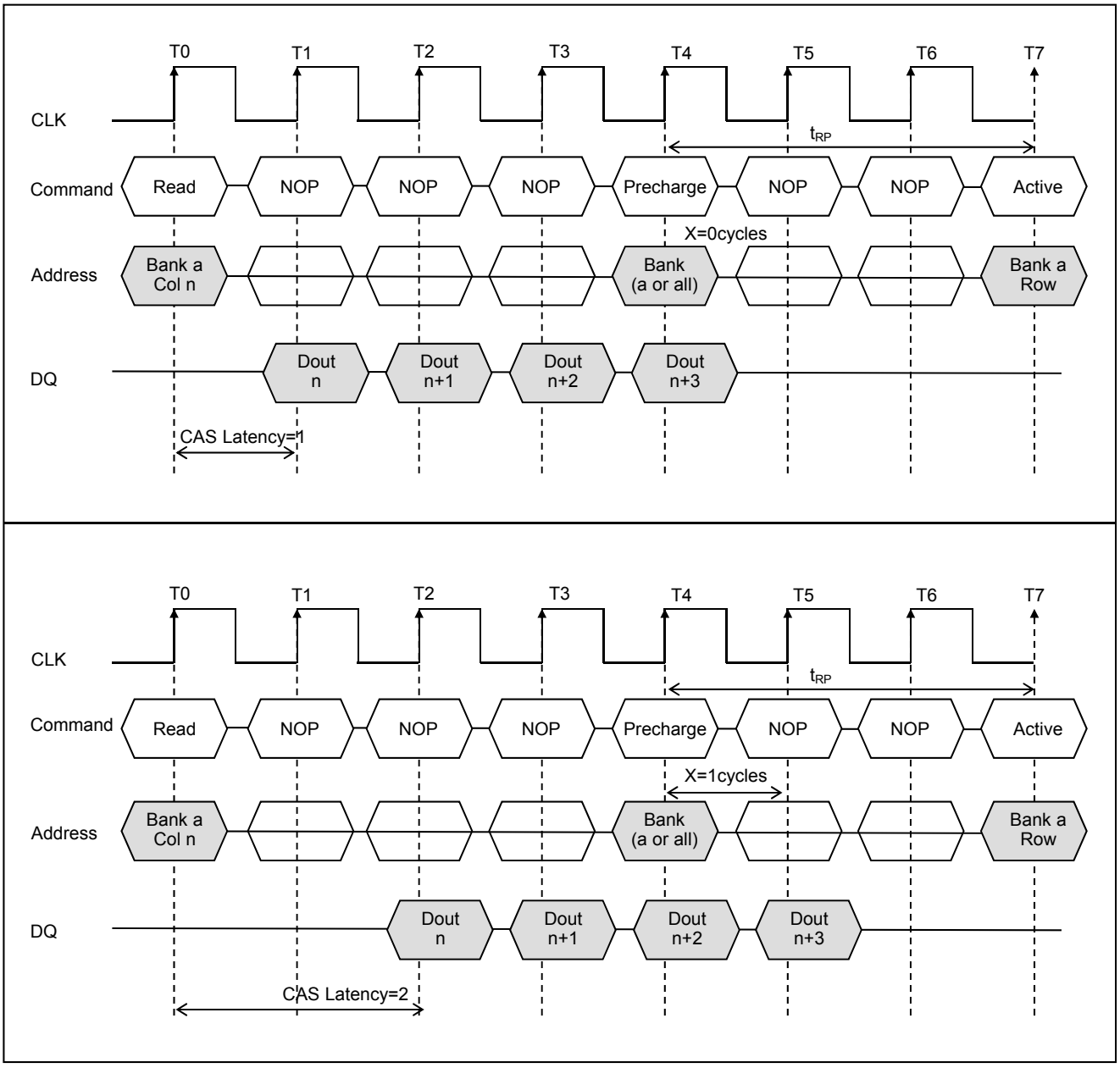


Figure 9. Read to Precharge