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Revision History

4Gb AS4C256M16D3B - 12BIN/BCN 96 ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Apr. 2016
Rev 1.1	Add Industrial part in datasheet	Apr. 2017

Specifications

- Density : 4G bits
- Organization : 32M words x 16 bits x 8 banks
- Package :
  - 96-ball FBGA
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply : VDD, VDDQ = 1.5V ± 0.075V
- Data rate :
  - 1600Mbps
- 2KB page size
  - Row address: A0 to A14
  - Column address: A0 to A9
- Eight internal banks for concurrent operation
- Burst lengths (BL) : 8 and 4 with Burst Chop (BC)
- Burst type (BT) :
  - Sequential (8, 4 with BC)
  - Interleave (8, 4 with BC)
- $\overline{\text{CAS}}$ Latency (CL) : 5, 6, 7, 8, 9, 10, 11
- CAS Write Latency (CWL) : 5, 6, 7, 8
- Precharge : auto precharge option for each burst access
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Refresh : auto-refresh, self-refresh
- Refresh cycles : - Average refresh period
  7.8 μs at -40°C ≤ Tc ≤ +85°C
  3.9 μs at +85°C < Tc ≤ +95°C
- Operating case temperature range
  - Commercial Tc = 0°C to +95°C
  - Industrial Tc = -40°C to +95°C

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and $\overline{\text{DQS}}$) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted $\overline{\text{CAS}}$ by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- $\overline{\text{RESET}}$ pin for Power-up sequence and reset function
- SRT range : Normal/extended
- Programmable Output driver impedance control

Table 1. Ordering Information

Part Number	Org	Temperature	MaxClock (MHz)	Package
AS4C256M16D3B-12BCN	256Mx16	Commercial 0°C to +95°C	800	96-ball FBGA
AS4C256M16D3B-12BIN	256Mx16	Industrial -40°C to +95°C	800	96-ball FBGA

Table 2. Speed Grade Information

Speed Grade	Clock Frequency	CAS Latency	tRCD (ns)	tRP (ns)
DDR3-1600	800MHz	11	13.75	13.75

Pin Configurations

96-ball FBGA (x16 configuration)

	1	2	3	4	5	6	7	8	9	
A	V_{DDQ}	DQU5	DQU7				DQU4	V_{DDQ}	V_{SS}	**A**
B	V_{SSQ}	V_{DD}	V_{SS}				$\overline{DQSU}$	DQU6	V_{SSQ}	**B**
C	V_{DDQ}	DQU3	DQU1				DQSU	DQU2	V_{DDQ}	**C**
D	V_{SSQ}	V_{DDQ}	DMU				DQU0	V_{SSQ}	V_{DD}	**D**
E	V_{SS}	V_{SSQ}	DQL0				DML	V_{SSQ}	V_{DDQ}	**E**
F	V_{DDQ}	DQL2	DQSL				DQL1	DQL3	V_{SSQ}	**F**
G	V_{SSQ}	DQL6	$\overline{DQSL}$				V_{DD}	V_{SS}	V_{SSQ}	**G**
H	V_{REFDQ}	V_{DDQ}	DQL4				DQL7	DQL5	V_{DDQ}	**H**
J	NC	V_{SS}	$\overline{RAS}$				CK	V_{SS}	NC	**J**
K	ODT	V_{DD}	$\overline{CAS}$				$\overline{CK}$	V_{DD}	CKE	**K**
L	NC	$\overline{CS}$	$\overline{WE}$				A10/AP	ZQ	NC	**L**
M	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}	**M**
N	V_{DD}	A3	A0				A12/$\overline{BC}$	BA1	V_{DD}	**N**
P	V_{SS}	A5	A2				A1	A4	V_{SS}	**P**
R	V_{DD}	A7	A9				A11	A6	V_{DD}	**R**
T	V_{SS}	$\overline{RESET}$	A13				A14	A8	V_{SS}	**T**

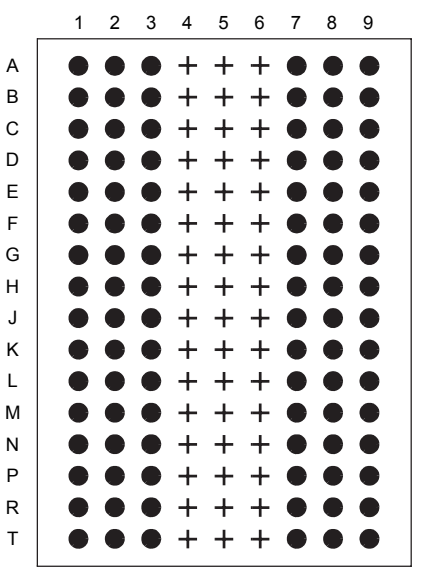
Ball Locations (x16)

● Populated ball

\+ Ball not populated

Top view

(See the balls through the package)

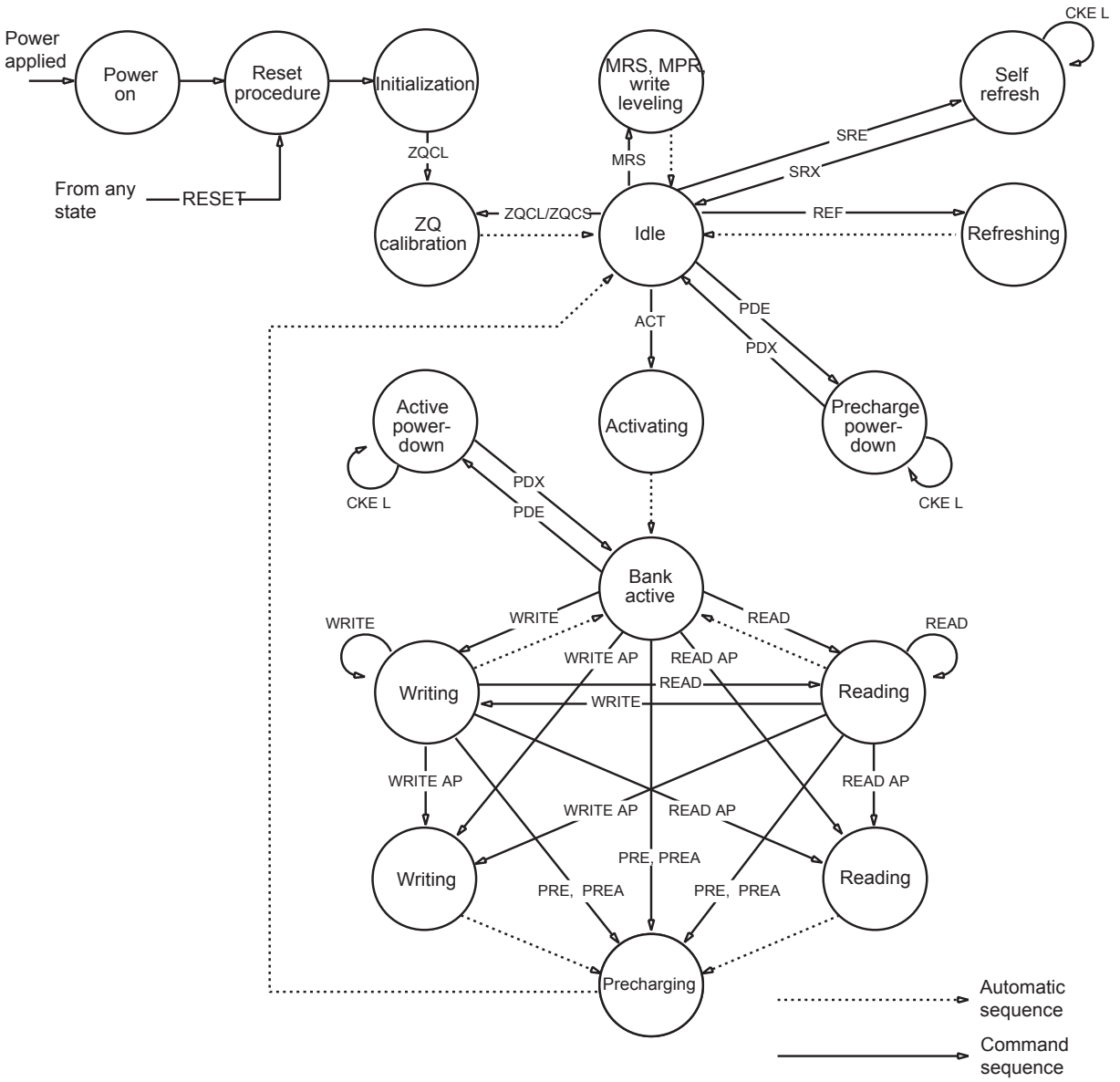


Signal Pin Description

Pin	Type	Function
CK, $\overline{CK}$	Input	**Clock :** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$
CKE	Input	**Clock Enable :** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self -Refresh.
$\overline{CS}$	Input	**Chip Select :** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination :** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if the Mode Register (MR1) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs :** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (DMU), (DML)	Input	**Input Data Mask :** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/$\overline{TDQS}$ is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	**Bank Address Inputs :** BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A14	Input	**Address Inputs :** Provided the row address for Active commands and the column address for Read / Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$ have additional functions, see below) The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	**Autoprecharge :** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH:Autoprecharge; LOW: No Autoprecharge)A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). if only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	**Burst Chop :** A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be performed. (HIGH : no burst chop, LOW : burst chopped). See command truth table for details.
$\overline{RESET}$	Input	**Active Low Asynchronous Reset :** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input/ Output	**Data Input/ Output :** Bi-directional data bus.
DQSL, $\overline{DQSL}$ DQSU, $\overline{DQSU}$	Input/ Output	**Data Strobe :** Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQSL and DQSU are paired with differential signals $\overline{DQSL}$ and $\overline{DQSU}$, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

Pin	Type	Function
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ power supply: 1.5V +/- 0.075V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.5V +/- 0.075V
VSS	Supply	Ground
VREFDQ	Supply	Reference Voltage for DQ
VREFCA	Supply	Reference Voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
NOTE : Input only pins (BA0-BA2, A0-A14, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT and $\overline{RESET}$) do not supply termination.		

Simplified State Diagram



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE

PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

Basic Functionality

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of four or eight in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row).The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10/AP), and the select BC4 or BL8 mode “on the fly” (via A12) if enabled in the mode register.

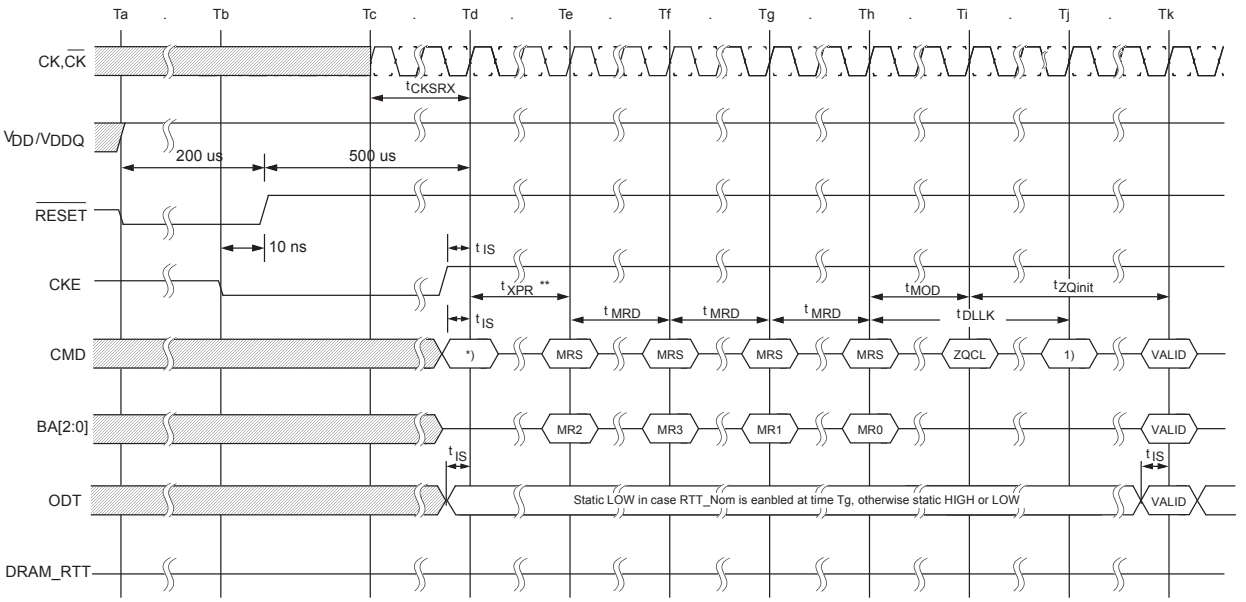
Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain $\overline{\text{RESET}}$ below 0.2 x VDD (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200μs with stable power. CKE is pulled “Low” anytime before $\overline{\text{RESET}}$ being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDD min must be no longer than 200ms; and during the ramp, VDD > VDDQ and VDD -VDDQ < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished, AND
   - Vref tracks VDDQ/2.

   or
   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
   - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will bedone independently of external clocks.
3. Clocks (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequenceis finished, including expiration of tDLLK and tZQinit.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 and the on-die termination is required to remain in the high impedance state, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register.(tXPR=Max(tXS, 5tCK)]
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue ”DLL Enable” command, provide “Low” to A0, ”High” to BA0 and “Low” to BA1-BA2)
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both tDLLK and tZQ init completed.
12. The DDR3 SDRAM is now ready for normal operation.

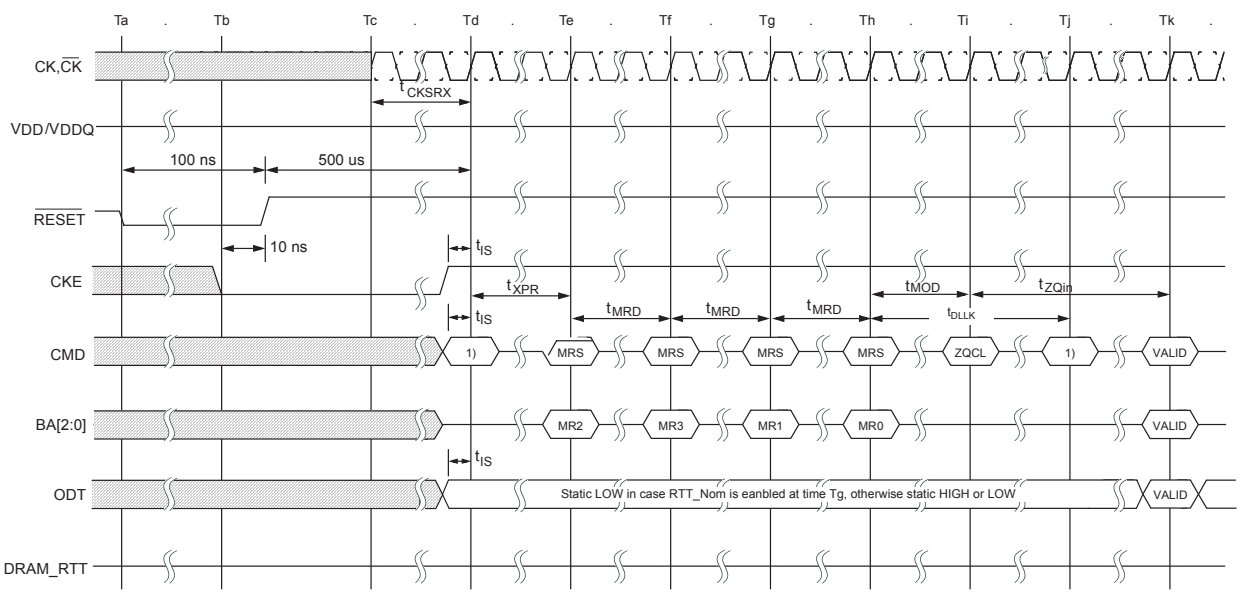


1) From time point 'Td' until 'Tk', NOP or DES commands must be applied between MRS and ZQCL commands

Reset and Initialization with Stable Power

The following sequence is required for /RESET at no power interruption initialization.

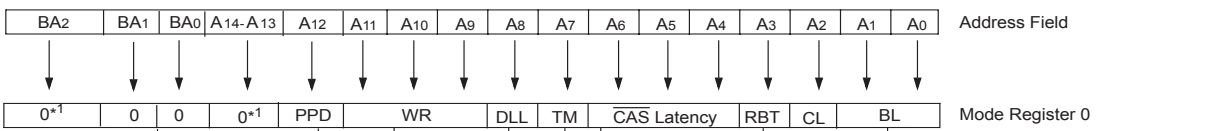
1. Assert /RESET below 0.2 x VDD anytime when reset is needed (all other inputs may be undefined). /RESET needs to be maintained for minimum 100ns. CKE is pulled low before /RESET being de-asserted (minimum time 10ns).
2. Follow Power-Up Initialization Sequence steps 2 to 11.
3. The reset sequence is now completed; DDR3 SDRAM is ready for normal operation.



1) From time point 'Td' until 'Tk', NOP or DES commands must be applied between MRS and ZQCL commands

Mode Register MR0

The Mode Register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS, RAS, CAS, WE, BA0, BA1 and BA2, while controlling the states of address pins according to the table below.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	4 or 8(on the fly)
1	0	4 (Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	Reserved

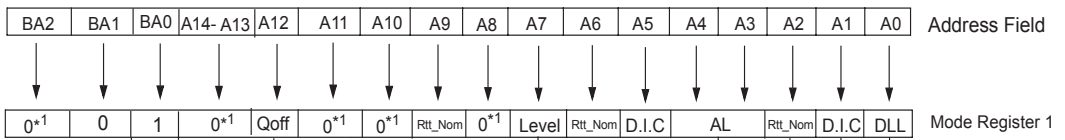
CAS Latency

A6	A5	A4	A2	Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11

*1 : BA2, A13 and A14 are reserved for future use and must be programmed to 0 during MRS.
*2 : WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, RTT_Nom impedance, additive latency, write leveling enable and Qoff.
The Mode Register 1 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0, low on BA1 and BA2, while controlling the states of address pins according to the table below.



A9	A6	A2	Rtt_Nom *3
0	0	0	ODT disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

Note : RZQ = 240 ohms

A0	DLL Enable
0	Enable
1	Disable

A7	Write leveling enable
0	Disabled
1	Enabled

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

*3: In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

*4: If RTT_Nom is used during Writes, only the values RZQ/2,RZQ/4 and RZQ/6 are allowed.

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled *2

*2: Outputs disabled - DQs, DQSs, $\overline{DQSs}$.

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

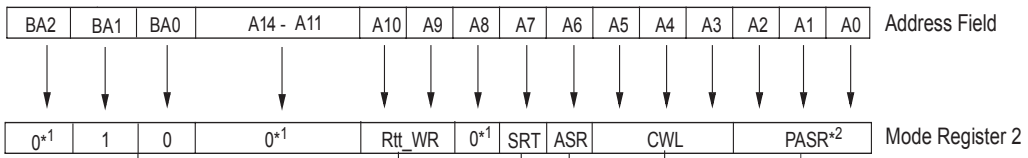
Note : RZQ = 240 ohms

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

* 1 : BA2, A8, A10, A11, A13 and A14 are reserved for future use (RFU) and must be programmed to 0 during MRS.

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, RTT_WR impedance and CAS write latency (CWL). The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1, low on BA0 and BA2, while controlling the states of address pins according to the table below.



A7	Self-refresh temperature range (SRT)
0	Normal operating temperature range
1	Extend temperature self-refresh (Optional)

A6	Auto Self-refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable (Optional)

A2	A1	A0	Partial Array Self Refresh (Optional)
0	0	0	Full Array
0	0	1	HalfArray (BA[2:0]=000,001,010, &011)
0	1	0	Quarter Array (BA[2:0]=000, & 001)
0	1	1	1/8th Array (BA[2:0] = 000)
1	0	0	3/4 Array (BA[2:0] = 010,011,100,101,110, & 111)
1	0	1	HalfArray (BA[2:0] = 100, 101, 110, &111)
1	1	0	Quarter Array (BA[2:0]=110, &111)
1	1	1	1/8th Array (BA[2:0]=111)

A10	A9	Rtt_WR*2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

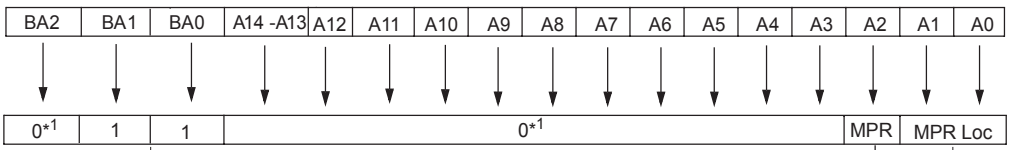
A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK(avg) ≥2.5ns)
0	0	1	6 (2.5ns >tCK(avg) ≥1.875ns)
0	1	0	7 (1.875ns>tCK(avg) ≥1.5ns)
0	1	1	8 (1.5ns>tCK(avg) ≥1.25ns)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

* 1 : BA2, A8, A11 ~ A14 are RFU and must be programmed to 0 during MRS.
* 2 : The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.
During write leveling, Dynamic ODT is not available.

Mode Register MR3

The Mode Register MR3 controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.



BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

MPR Operation

A2	MPR
0	Normal operation*3
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	RFU
1	0	RFU
1	1	RFU

* 1 : BA2, A3 - A14 are reserved for future use (RFU) and must be programmed to 0 during MRS.
* 2 : The predefined pattern will be used for read synchronization.
* 3 : When MPR control is set for normal operation, MR3 A[2] = 0, MR3 A[1:0] will be ignored

Burst Length (MR0)

Read and write accesses to the DDR3 are burst oriented, with the burst length being programmable, as shown in the figure MR0 Programming. The burst length determines the maximum number of column locations that can be accessed for a given read or write command. Burst length options include fixed BC4, fixed BL8, and on the fly which allows BC4 or BL8 to be selected coincident with the registration of a read on write command Via A12 ($\overline{BC}$). Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Burst Chop

In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on the fly via A12($\overline{BC}$), the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

Burst Type (MR0)

[Burst Length and Sequence]

Burst length	Operation	Starting address (A2, A1, A0)	Sequential addressing (decimal)	Interleave addressing (decimal)
4 (Burst chop)	READ	000	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T
		001	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T
		010	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T
		011	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T
		100	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T
		101	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T
		110	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T
		111	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T
	WRITE	0VV	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X
		1VV	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X
8	READ	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
		001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
		010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
		011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
		100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
		101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
		110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
		111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0
	WRITE	VVV	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7

Remark: T: Output driver for data and strobes are in high impedance.

V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins.

X: Don't Care.

Notes: 1. Page length is a function of I/O organization and column addressing

2. 0...7 bit number is value of CA [2:0] that causes this bit to be the first read during a burst.

Command Truth Table

(a) Note 1,2,3,4 apply to the entire Command truth table
(b) Note 5 applies to all Read/Write commands.
[BA=Bank Address, RA=Row Address, CA=Column Address, $\overline{BC}$=Burst Chop, X=Don't care, V=Valid]

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 - BA2	A13 - A15	A12 / $\overline{BC}$	A10 / AP	A0 - A9,A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
ZQ calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	

Note :
1. All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device density and configuration dependant
2. $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level"
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS
6. The Power Down Mode does not perform any refresh operations.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self refresh exit is asynchronous.
9. V_{REF}(Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation.
10. The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as a No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition

CKE Truth Table

(a) Note 1~7 apply to the entire Command truth table

(b) CKE low is allowed only if tMRD and tMOD are satisfied

Current State [2]	CKE		Command (N) [3]	Action (N)[3]	Notes
	Previous Cycle [1] (N-1)	Current Cycle [1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT or NOP	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT or NOP	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details with all signals See "Command Truth Table," on previous page					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh
6. CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.
7. DESELECT and NOP are defined in the Command truth table
8. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self Refresh Exit are NOP and DESELECT only.
13. Self Refresh can not be entered while Read or Write operations. See 'Self-Refresh Operation" and 'Power-Down Modes" on later section for a detailed list of restrictions.
14. The Power Down does not perform any refresh operations.
15. "X" means "don't care (including floating around V_{REF})" in Self Refresh and Power Down. It also applies to Address pins
16. V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power Down is entered, otherwise Active Power Down is entered
18. 'Idle state' means that all banks are closed(tRP,tDAL,etc. satisfied) and CKE is high and all timings from previous operations are satisfied (tMRD,tMOD,tRFC,tZQinit,tZQoper,tZQCS,etc)as well as all SRF exit and Power Down exit parameters are satisfied (tXS,tXP,tXPDLL,etc)

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
VIN, VOUT	Voltage on any pin relative to Vss	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE :

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
T_C	Operating case temperature (Commercial)	0 to +95	°C	1,2,3
T_C	Operating case temperature (Industrial)	-40 to +95	°C	1,2,3

NOTE :

1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9μs. (This double refresh requirement may not apply for some devices.)

   b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply voltage	1.425	1.5	1.575	V	1,2
VDDQ	Supply voltage for Output	1.425	1.5	1.575	V	1,2

NOTE :

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

AC and DC Input Measurement Levels

Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IHCA} (DC100)	DC input logic high	V_{REF} + 0.100	VDD	V	1
V_{ILCA} (DC100)	DC input logic low	VSS	V_{REF} - 0.100	V	1
V_{IHCA} (AC175)	AC input logic high	V_{REF} + 0.175	-	V	1,2
V_{ILCA} (AC175)	AC input logic low	-	V_{REF} - 0.175	V	1,2
V_{IHCA} (AC150)	AC input logic high	V_{REF} + 0.150	-	V	1,2
V_{ILCA} (AC150)	AC input logic low	-	V_{REF} - 0.150	V	1,2
V_{IHCA} (AC135)	AC input logic high	-	-	V	1,2
V_{ILCA} (AC135)	AC input logic low	-	-	V	1,2
V_{IHCA} (AC125)	AC input logic high	-	-	V	1,2
V_{ILCA} (AC125)	AC input logic low	-	-	V	1,2
V_{REFCA} (DC)	Reference voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3,4

NOTE :
1. For input only pins except /RESET : V_{REF} = V_{REFCA} (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REFCA} (DC) by more than ±1% VDD (for reference : approx. ±15 mV).
4. For reference : approx. VDD/2 ±15 mV.

Single-Ended AC and DC Input Levels for DQ and DM

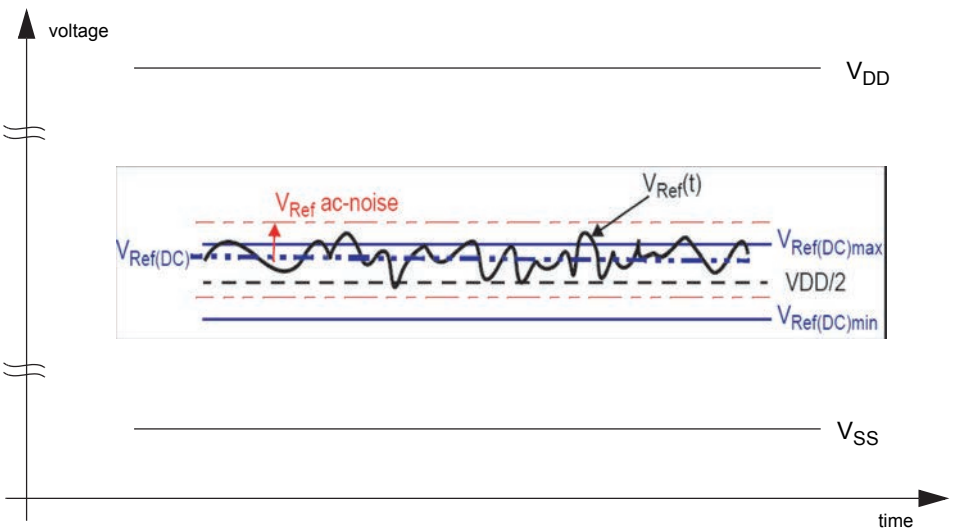
Symbol	Parameter	Min.	Max.	Units	Notes
V_{IHDQ} (DC100)	DC input logic high	V_{REF} + 0.100	VDD	V	1
V_{ILDQ} (DC100)	DC input logic low	VSS	V_{REF} - 0.100	V	1
V_{IHDQ} (AC175)	AC input logic high	-	-	V	1,2
V_{ILDQ} (AC175)	AC input logic low	-	-	V	1,2
V_{IHDQ} (AC150)	AC input logic high	V_{REF} + 0.150	-	V	1,2
V_{ILDQ} (AC150)	AC input logic low	-	V_{REF} - 0.150	V	1,2
V_{IHDQ} (AC135)	AC input logic high	-	-	V	1,2
V_{ILDQ} (AC135)	AC input logic low	-	-	V	1,2
V_{REFDQ} (DC)	Reference voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3,4

NOTE :
1. For DQ and DM : V_{REF} = V_{REFDQ} (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REFDQ} (DC) by more than ±1% VDD (for reference: approx. ±15 mV).
4. For reference: approx. VDD/2 ±15 mV.

VREF Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are illustrate in figure VREF(DC) tolerance and VREF AC-Noise limits. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise).

VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table of “Single-Ended AC and DC Input Levels for Command and Address”. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than +/- 1% VDD.



VREF(DC) tolerance and VREF AC-Noise limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF.

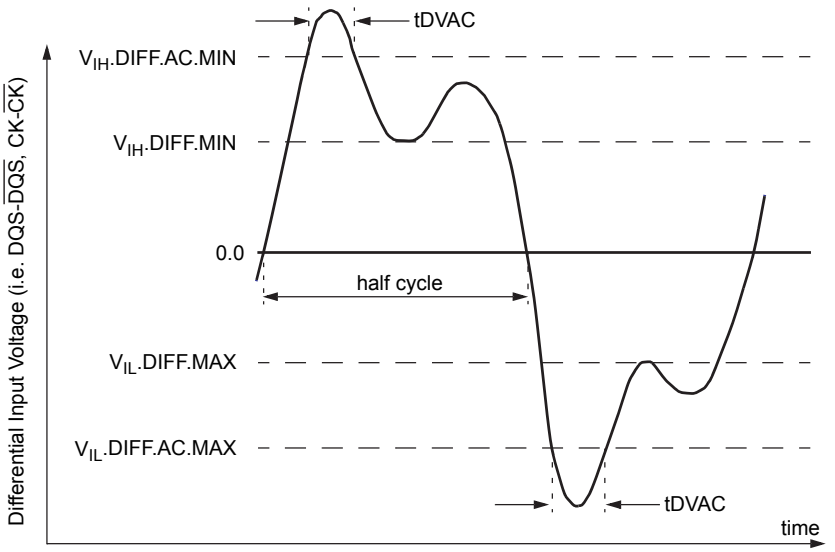
"VREF" shall be understood as VREF(DC), as defined in figure above, VREF(DC) tolerance and VREF AC-Noise limits.

This clarifies, that DC-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREF AC-noise. Timing and voltage effects due to AC-noise on VREF up to the specified limit (+/- 1% of VDD) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signals definition



Definition of differential ac-swing and "time above ac level" tDVAC

Differential swing requirement for clock (CK - $\overline{CK}$) and strobe (DQS - $\overline{DQS}$)

Differential AC and DC Input Levels

Symbol	Parameter	Min.	Max.	Units	Notes
VIHdiff	Differential input high	+0.2	NOTE 3	V	1
VILdiff	Differential input low	NOTE 3	-0.2	V	1
VIHdiff(AC)	Differential input high AC	2 x (VIH(AC) - VREF)	NOTE 3	V	2
VILdiff(AC)	Differential input low AC	NOTE 3	2 x (VIL(AC) - VREF)	V	2

NOTE :

1. Used to define a differential signal slew-rate.
2. for CK - $\overline{CK}$ use VIH/VIL(AC) of address/command and VREFCA; for strobes (DQS, $\overline{DQS}$) use VIH/VIL(AC) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$ need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot specification".

Allowed time before ringback (tDVAC) for CK - $\overline{CK}$ and DQS - $\overline{DQS}$

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(AC)| = 350mV		tDVAC [ps] @ |VIH/Ldiff(AC)| = 300mV	
	Min.	Max.	Min.	Max.
> 4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	-
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
< 1.0	0	-	150	-

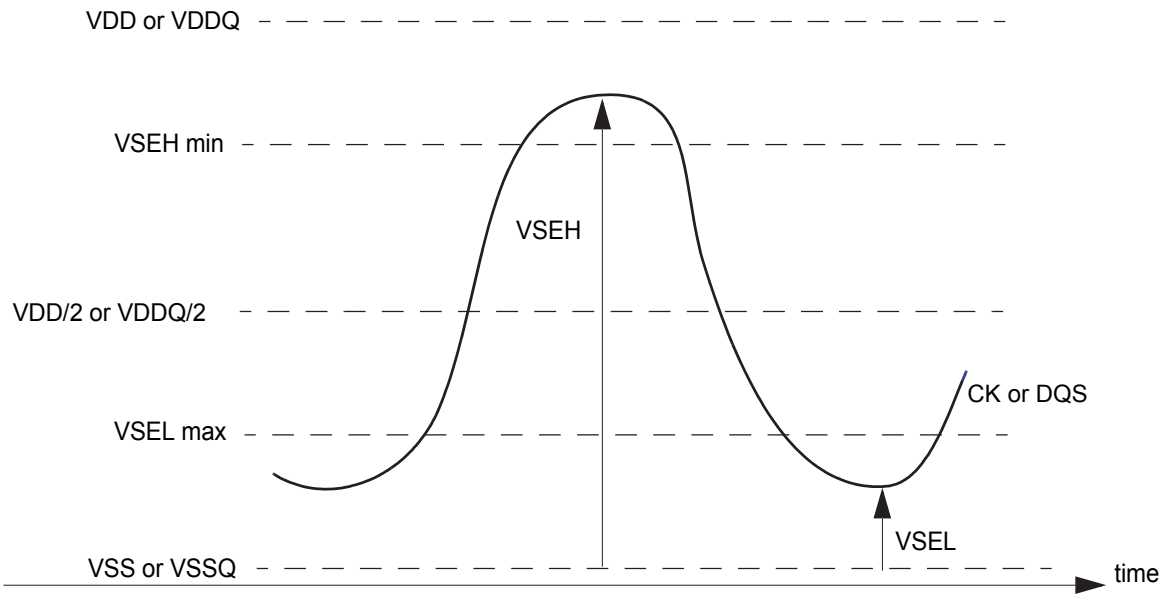
Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, $\overline{CK}$, $\overline{DQS}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{CK}$ have to approximately reach VSEH min / VSEL max [approximately equal to the AC-levels (VIH(AC) / VIL(AC)) for Address/command signals] in every half-cycle.

DQS, $\overline{DQS}$ have to reach VSEH min / VSEL max [approximately the ac-levels (VIH(AC) / VIL(AC)) for DQ signals] in every half-cycle proceeding and following a valid transition.

Note that the applicable AC-levels for Address/command and DQ's might be different per speed-bin etc. E.g. if VIH150(AC) / VIL150(AC) is used for Address/command signals, then these AC-levels apply also for the single-ended components of differential CK and $\overline{CK}$.



Single-ended requirement for differential signals

Note that while Address/command and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDD/2; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL max, VSEH min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

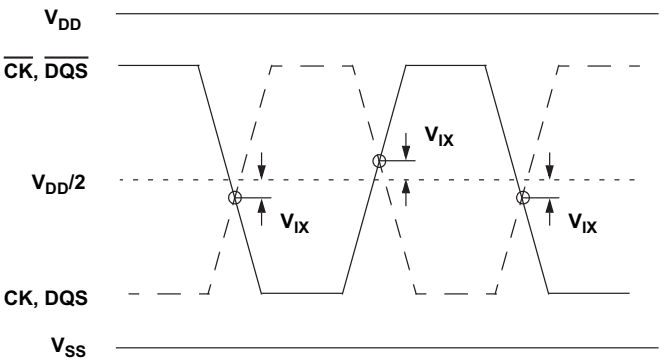
Single-ended levels for CK, DQS, $\overline{CK}$, $\overline{DQS}$

Symbol	Parameter	Min.	Max.	Units	Notes
VSEH	Single-ended high-level for strobes	(VDD/2) + 0.175	NOTE 3	V	1,2
	Single-ended high-level for CK, $\overline{CK}$	(VDD/2) + 0.175	NOTE 3	V	1,2
VSEL	Single-ended low-level for strobes	NOTE 3	(VDD/2) - 0.175	V	1,2
	Single-ended low-level for CK, $\overline{CK}$	NOTE 3	(VDD/2) - 0.175	V	1,2

NOTE :

1. For CK, $\overline{CK}$ use VIH/VIL(AC) of address/command; for strobes (DQS, $\overline{DQS}$) use VIH/VIL(AC) of DQs.
2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VIH(AC)/VIL(AC) for address/command is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended components of differential signals CK, $\overline{CK}$, DQS, $\overline{DQS}$ need to be within the respective limits (VIH(DC) max, VIL(DC) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot specifications".

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in below table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the mid level between of VDD and VSS.



VIX Definition

Cross point voltage for differential input signals (CK, DQS)

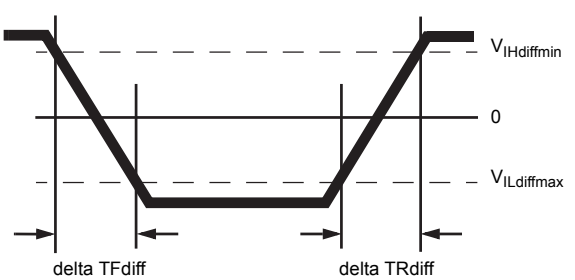
Symbol	Parameter	Min.	Max.	Units	Notes
VIX	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	-150	150	mV	
		-175	175	mV	1
VIX	Differential Input Cross Point Voltage relative to VDD/2 for DQS, $\overline{DQS}$	-150	150	mV	

NOTE :1. Extended range for VIX is only allowed for clock and if single-ended clock input signals CKand CK are monotonic, have a single-ended swing VSEL / VSEH of at least VDD/2 +/- 250 mV, and the differential slew rate of CK-$\overline{CK}$ is larger than 3 V/ ns. Refer to the table of Cross point voltage for differential input signals (CK, DQS) for VSEL and VSEH standard values.

Differential input slew rate definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VILdiff (max)	VIHdiff (min)	VIHdiff (min) - VILdiff (max) / Delta TRdiff
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VIHdiff (min)	VILdiff (max)	VIHdiff (min) - VILdiff (max) / Delta TFdiff

NOTE : The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be linear between these thresholds.



Differential Input Slew Rate definition for DQS, $\overline{DQS}$, and CK, $\overline{CK}$

AC and DC Output Measurement Levels

Single-ended AC & DC Output Levels

Symbol	Parameter	DDR3-1600	Units	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

NOTE : 1. The swing of +/-0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT=VDDQ/2.

Differential AC & DC Output Levels

Symbol	Parameter	DDR3-1600	Units	Notes
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.2 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.2 x VDDQ	V	1

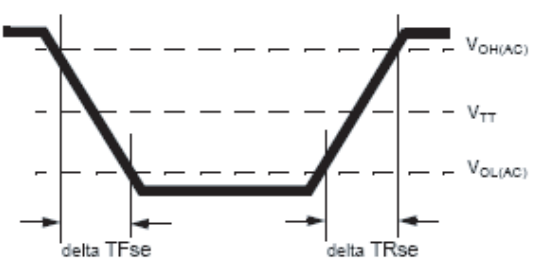
NOTE : 1. The swing of +/-0.2xVDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT=VDDQ/2 at each of the differential outputs.

Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals.

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	VOH(AC)-VOL(AC) / Delta TRse
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	VOH(AC)-VOL(AC) / Delta TRse

NOTE : Output slew rate is verified by design and characterization, and may not be subject to production test.



Single-ended Output Slew Rate definition

Parameter	Symbol	DDR3-1600		Units
		Min	Max	
Single ended output slew rate	SRQse	2.5	5	V/ns

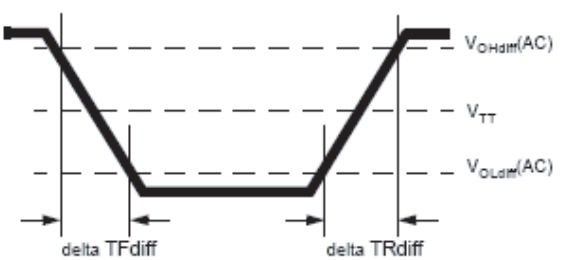
Description : SR : Slew Rate
Q : Query Output (like in DQ, which stands for Data-in, Query-Output)
se : Single-ended Signals For Ron = RZQ/7 setting
NOTE : (1) In two cased, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.
- Case_1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low of low to high) while all remaining DQ signals in the same byte lane are static (i.e they stay at either high or low).
- Case_2 is defined for a single DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.

Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOH-diff(AC) for differential signals.

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / Delta TRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	VOHdiff(AC)-VOLdiff(AC)) / Delta TFdiff

NOTE : Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output Slew Rate definition

Parameter	Symbol	DDR3-1600		Units
		Min	Max	
Differential output slew rate	SRQdiff	5	10	V/ns

Description : SR : Slew Rate
Q : Query Output (like in DQ, which stands for Data-in, Query-Output)
diff : Differential Signals
For Ron = RZQ/7 setting