Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

# Contact us


Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

## Revision History
## 2Gb DDR2 -AS4C256M8D2 - 60 ball FBGA PACKAGE

| Revision | Details | Date |
|---|---|---|
| Rev 1.0 | Preliminary datasheet | September 2014 |

### *Features*

- High speed data transfer rates with system frequency up to 400 MHz
- 8 internal banks for concurrent operation
- 4-bit prefetch architecture
- Programmable CAS Latency: 3, 4 ,5 , 6 and 7
- Programmable Additive Latency:0, 1, 2, 3 , 4, 5 and 6
- Write Latency = Read Latency -1
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 4 and 8
- Automatic and Controlled Precharge Command
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 7.8 us at -40$^{o}$C ≤ Tcase ≤ 85$^{o}$C, 3.9 us at 85$^{o}$C < Tcase ≤ 105$^{o}$C
- ODT (On-Die Termination)
- Weak Strength Data-Output Driver Option
- Bidirectional differential Data Strobe (Single-ended data-strobe is an optional feature)
- On-Chip DLL aligns DQ and DQs transitions with CK transitions
- DQS can be disabled for single-ended data strobe
- Read Data Strobe (RDQS) supported (x8 only)
- Differential clock inputs CK and CK
- JEDEC Power Supply 1.8V ± 0.1V
- VDDQ =1.8V ± 0.1V
- Available in 60-ball FBGA for x8 component
- RoHS compliant
- tRAS lockout supported

### *Description*

The AS4C256M8D2 is a eight bank DDR DRAM organized as 8 banks x 32Mbit x 8. The AS4C256M8D2 achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

The chip is designed to comply with the following key DDR2 SDRAM features:(1) posted CAS with additive latency, (2) write latency = read latency-1, (3) On Die Termination.

All of the control, address, circuits are synchronized with the positive edge of an externally supplied clock. I/O s are synchronized with a pair of bidirectional strobes (DQS, DQS) in a source synchronous fashion.

Operating the eight memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

## Table 1. Speed Grade Information

| Speed Grade | Clock Frequency | CAS Latency | $t_{RCD}$ (ns) | $t_{RP}$ (ns) |
|---|---|---|---|---|
| DDR2-800 | 400 MHz | 5 | 12.5 | 12.5 |

## Table 2. Ordering Information

| Product part No | Org | Temperature | Package |
|---|---|---|---|
| AS4C256M8D2-25BCN | 256M x 8 | Commercial (Extended) 0°C to +95°C | 60-ball FBGA |
| AS4C256M8D2-25BIN | 256M x 8 | Industrial -40°C to +95°C (Extended) | 60-ball FBGA |

### *256MX8 DDR2 PIN CONFIGURATION*

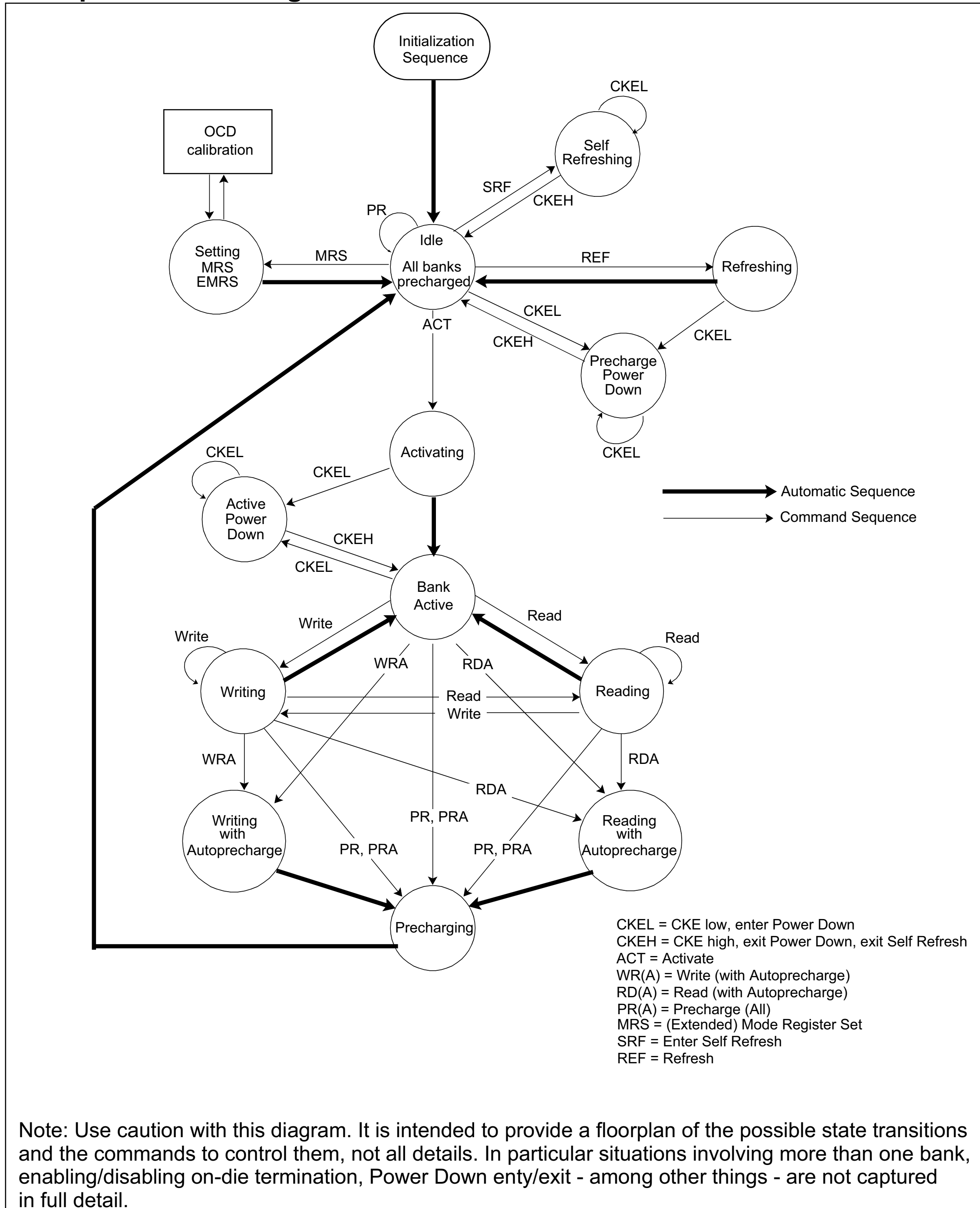
***<Top View>***

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| VDD | NU/$\overline{RDQS}$ | VSS | A | VSSQ | $\overline{DQS}$ | VDDQ |
| DQ6 | VSSQ | DM/RDQS | B | DQS | VSSQ | DQ7 |
| VDDQ | DQ1 | VDDQ | C | VDDQ | DQ0 | VDDQ |
| DQ4 | VSSQ | DQ3 | D | DQ2 | VSSQ | DQ5 |
| VDDL | VREF | VSS | E | VSSDL | CK | VDD |
| | CKE | $\overline{WE}$ | F | $\overline{RAS}$ | $\overline{CK}$ | ODT |
| BA2 | BA0 | BA1 | G | $\overline{CAS}$ | $\overline{CS}$ | |
| | A10/AP | A1 | H | A2 | A0 | VDD |
| VSS | A3 | A5 | J | A6 | A4 | |
| | A7 | A9 | K | A11 | A8 | VSS |
| VDD | A12 | A14 | L | NC | A13 | |

### *Signal Pin Description*

| Pin | Type | Function |
|---|---|---|
| CK, $\overline{CK}$ | Input | The system clock input. All inputs except DQs and DMs are sampled on the rising edge of CK. |
| CKE | Input | Activates the CK signal when high and deactivates the CK signal when low, thereby initiates either the Power Down mode, or the Self Refresh mode. |
| $\overline{CS}$ | Input | $\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Input | When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM. |
| A0 - A14 | Input | During a Bank Activate command cycle, A0-A14 defines the row address (RA0-RA14) when sampled at the rising clock edge for x8.<br>During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge.CAn depends on the SDRAM organization:<br>256M x 8 DDR CAn = CA9<br><br>In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If A10 is low, autoprecharge is disabled.<br>During a Precharge command cycle, A10(=AP) is used in conjunction with BA0, BA1and BA2 to control which bank(s) to precharge. If A10 is high, all eight banks will be precharged simultaneously regardless of state of BA0 , BA1 and BA2. |
| BA0-BA2 | Input | Selects which bank is to be active. |
| DQx | Input/ Output | Data Input/Output pins operate in the same manner as on conventional DRAMs.<br>DQ0-DQ7 for x8 device. |
| DQS, ($\overline{DQS}$)<br>RDQS, ($\overline{RDQS}$) | Input/ Output | Data Strobe, output with read data, input with write data. Edge-aligned with read data, centered in write data. For x8 device, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS and RDQS may be used in single ended mode or paired with optional complimentary signals $\overline{DQS}$ and $\overline{RDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals. |
| DM | Input | DM is an input mask signal for write data. Input data is masked when DM is sampled high along with that input data during a Write access. DM is sampled on both edges of DQS.<br>Although DM pins are input only, the DM loading is designed to match that of DQ and DQS pins.<br>For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command. |
| VDD, VSS | Supply | Power and ground for the input buffers and the core logic. |
| VDDQ, VSSQ | Supply | Isolated power supply and ground for the output buffers to provide improved noise immunity. |
| VREF | Input | SSTL Reference Voltage for Inputs |
| VDDL, VSSDL | Supply | Isolated power supply and ground for the DLL to provide improved noise immunity. |
| ODT | Input | On Die Termination Enable. It enables termination resistance internal to the DRAM. ODT is applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$ and DM for x8 device. ODT will be ignored if EMRS disable the function. |

## Simplified State Diagram




Note: Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down enty/exit - among other things - are not captured in full detail.

### *Basic Functionality*

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A14 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

### *Power up and Initialization*

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.)

   - VDD, VDDL and VDDQ are driven from a single power converter output, AND
   - VTT is limited to 0.95V max, AND
   - Vref tracks VDDQ/2.

   or

   - Apply VDD before or at the same time as VDDL.
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.

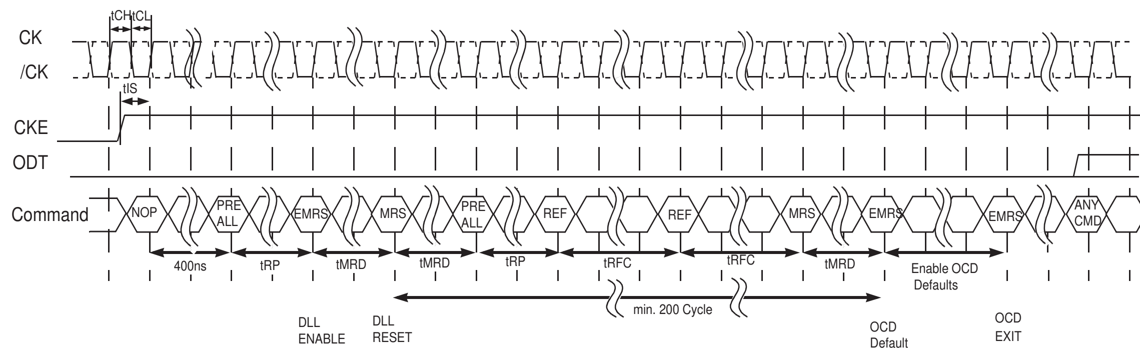
   at least one of these two sets of conditions must be met.

2. Start clock and maintain stable condition.
3. For the minimum of 200us after stable power and clock (CK, $\overline{CK}$), then apply NOP or deselect & take CKE high.
4. Wait minimum of 400ns then issue precharge all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide “Low” to BA0, “High” to BA1.)
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide “High” to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 and A12.)
8. Issue a Mode Register Set command for “DLL reset”.
   (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-1)
9. Issue precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with low to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.
12. At least 200 clocks after step 8, EMRS OCD Default command (A9=A8= A7=1) followed by EMRS OCD Exit command (A9=A8=A7=0) must be issued with other operating parameters of EMRS.

13. The DDR2 SDRAM is now ready for normal operation.

*1) To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.

## Initialization Sequence after Power Up



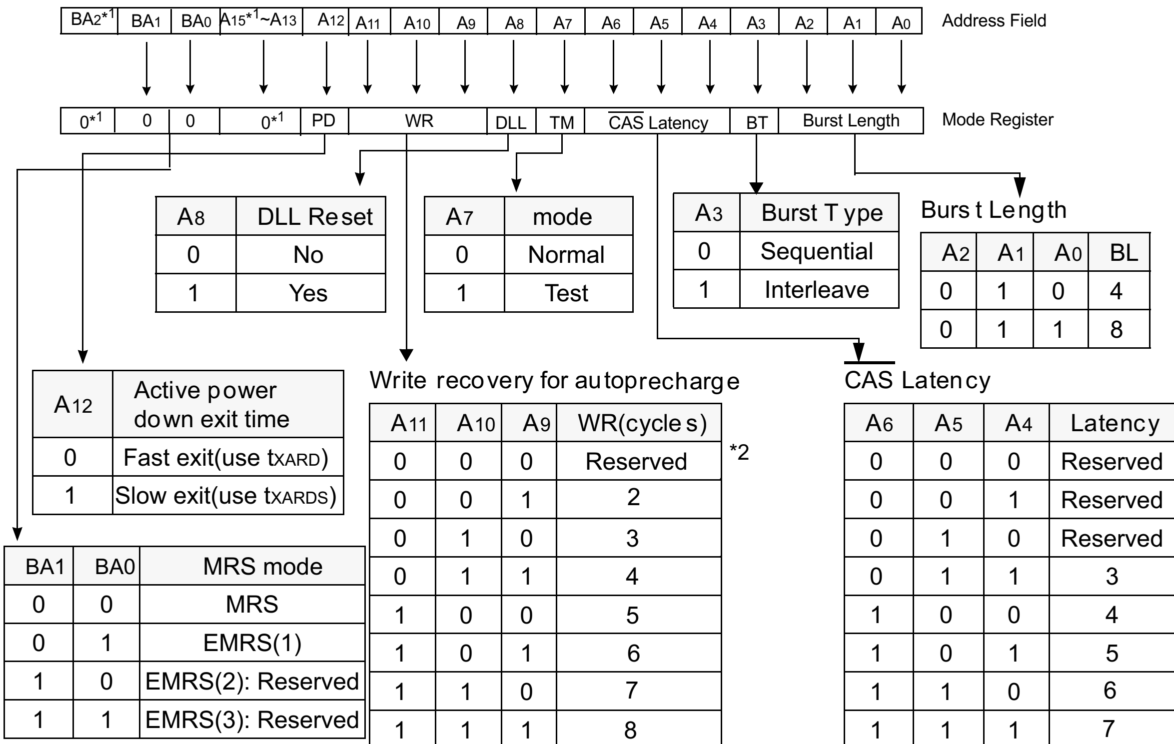

## Programming the Mode Register

For application flexibility, burst length, burst type, $\overline{\text{CAS}}$ latency, DLL reset function, write recovery time (tWR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, single-ended strobe and ODT (On Die Termination) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) or Extended Mode Registers (EMR(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

## DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on CS, RAS, CAS, WE, BA0 and BA1, while controlling the state of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4 ~ A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time tWR is defined by A9 ~ A11. Refer to the table for specific codes.




| A8 | DLL Reset |
|---|---|
| 0 | No |
| 1 | Yes |

| A7 | mode |
|---|---|
| 0 | Normal |
| 1 | Test |

| A3 | Burst Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

Burst Length

| A2 | A1 | A0 | BL |
|---|---|---|---|
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 8 |

| A12 | Active power down exit time |
|---|---|
| 0 | Fast exit(use tXARD) |
| 1 | Slow exit(use tXARDS) |

Write recovery for autoprecharge

| A11 | A10 | A9 | WR(cycles) |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8 |

*2

CAS Latency

| A6 | A5 | A4 | Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | MRS |
| 0 | 1 | EMRS(1) |
| 1 | 0 | EMRS(2): Reserved |
| 1 | 1 | EMRS(3): Reserved |

*1 : A13 is reserved for future use and must be programmed to 0 when setting the mode register.
BA2 and A14 are not used for 512Mb, but used for 1Gb and 2Gb DDR2 SDRAMs. A15 is reserved for future usage.

*2 : WR(write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up a non-integer value to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

## *DDR2 SDRAM Extended Mode Register Set*

### ***EMRS(1)***

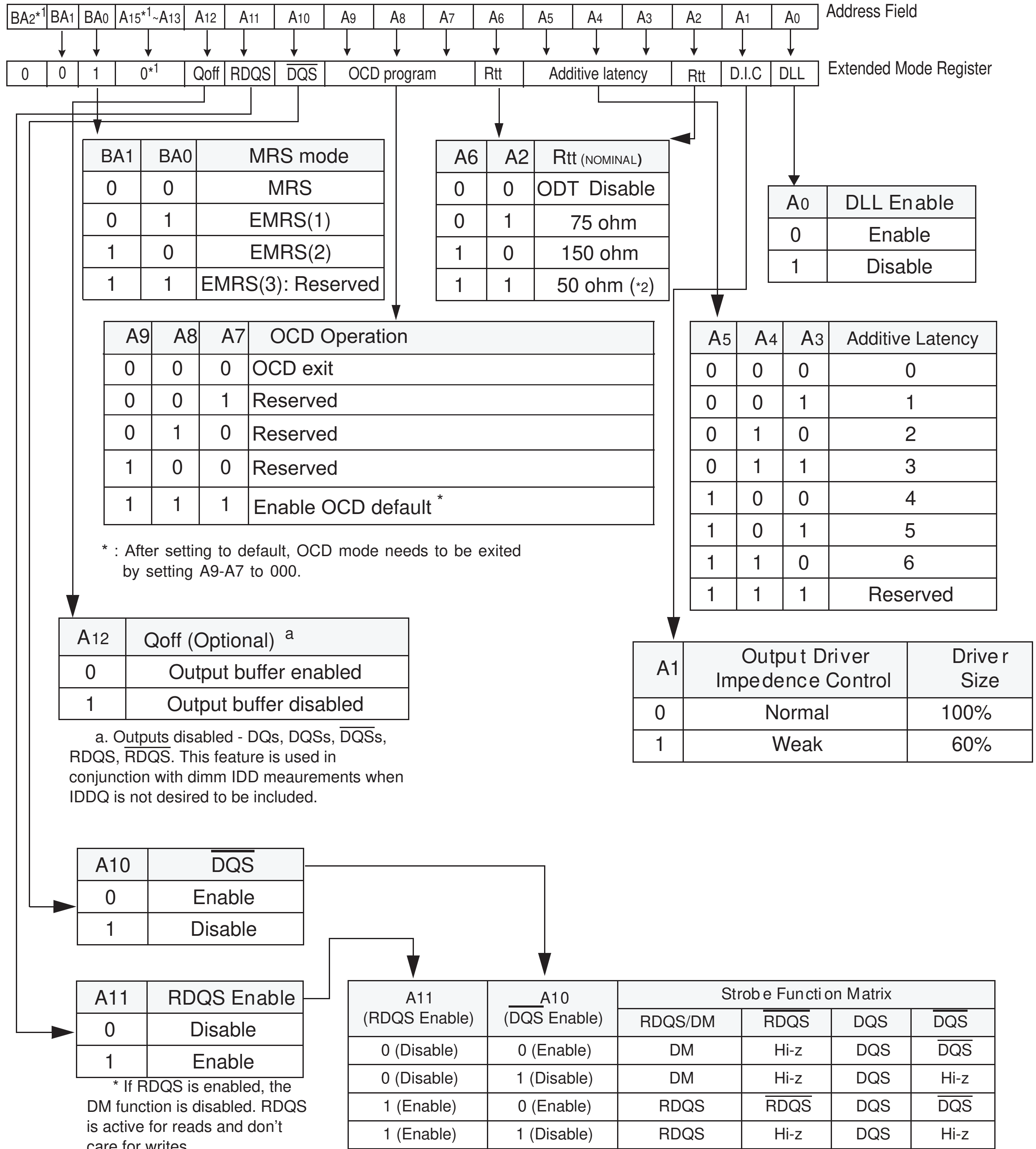
The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, ODT value selection and additive latency. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power-up for proper operation. Extended mode register(1) is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0 and low on BA1, and controlling rest of pins A0 ~ A14.

The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register. Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling reduced strength data-output drive. A3~A5 determines the additive latency. A2 and A6 are used for ODT value selection, A7~A9 are used for OCD control, A10 is used for $\overline{DQS}$ disable and A11 is used for RDQS enable.

### ***DLL Enable / Disable***

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

## EMRS(1) Programming




| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | MRS |
| 0 | 1 | EMRS(1) |
| 1 | 0 | EMRS(2) |
| 1 | 1 | EMRS(3): Reserved |

| A6 | A2 | Rtt (NOMINAL) |
|---|---|---|
| 0 | 0 | ODT Disable |
| 0 | 1 | 75 ohm |
| 1 | 0 | 150 ohm |
| 1 | 1 | 50 ohm (*2) |

| A0 | DLL Enable |
|---|---|
| 0 | Enable |
| 1 | Disable |

| A9 | A8 | A7 | OCD Operation |
|---|---|---|---|
| 0 | 0 | 0 | OCD exit |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 1 | 1 | Enable OCD default * |

* : After setting to default, OCD mode needs to be exited by setting A9-A7 to 000.

| A5 | A4 | A3 | Additive Latency |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | Reserved |

| A12 | Qoff (Optional) [a] |
|---|---|
| 0 | Output buffer enabled |
| 1 | Output buffer disabled |

a. Outputs disabled - DQs, DQSs, DQSs, RDQS, RDQS. This feature is used in conjunction with dimm IDD meaurements when IDDQ is not desired to be included.

| A1 | Output Driver Impedence Control | Driver Size |
|---|---|---|
| 0 | Normal | 100% |
| 1 | Weak | 60% |

| A10 | DQS |
|---|---|
| 0 | Enable |
| 1 | Disable |

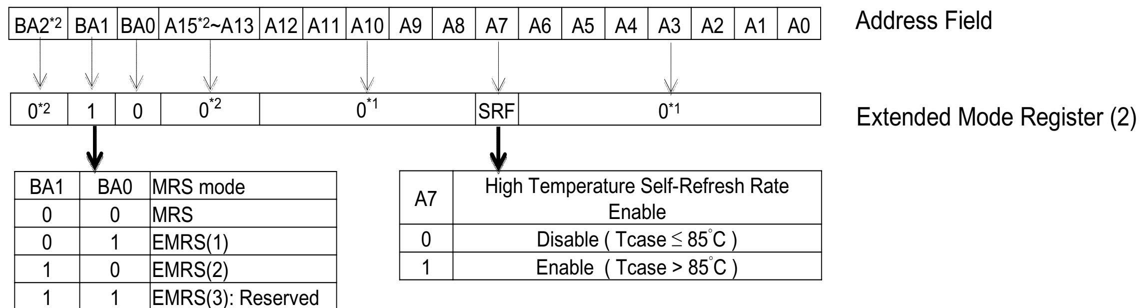
| A11 | RDQS Enable |
|---|---|
| 0 | Disable |
| 1 | Enable |

* If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.

| A11 (RDQS Enable) | A10 (DQS Enable) | Strobe Function Matrix | | | |
|---|---|---|---|---|---|
| | | RDQS/DM | RDQS | DQS | DQS |
| 0 (Disable) | 0 (Enable) | DM | Hi-z | DQS | DQS |
| 0 (Disable) | 1 (Disable) | DM | Hi-z | DQS | Hi-z |
| 1 (Enable) | 0 (Enable) | RDQS | RDQS | DQS | DQS |
| 1 (Enable) | 1 (Disable) | RDQS | Hi-z | DQS | Hi-z |

*1 : A13 is reserved for future use and must be programmed to 0 when setting the mode register.
BA2 and A14 are not used for 512Mb, but used for 1Gb and 2Gb DDR2 SDRAMs. A15 is reserved for future use.
*2 : Optional for DDR2-800

EMRS(2) Programming: *1

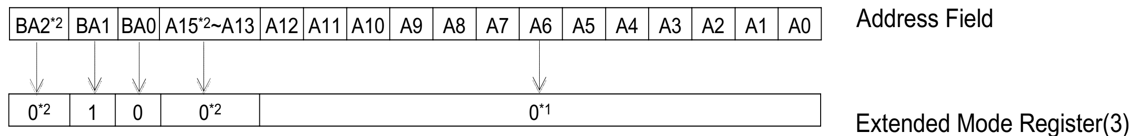



| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | MRS |
| 0 | 1 | EMRS(1) |
| 1 | 0 | EMRS(2) |
| 1 | 1 | EMRS(3): Reserved |

| A7 | High Temperature Self-Refresh Rate Enable |
|---|---|
| 0 | Disable ( Tcase ≤ 85°C ) |
| 1 | Enable ( Tcase > 85°C ) |

*1 : BA1 must be programmed to 0 setting the mode register during initialization.
*2 : BA2 and A14 are not used for 512Mb, but used for 1Gb and 2Gb DDR2 SDRAMs. A15 is reserved for future usage.

EMRS(3) Programming: Reserved*1

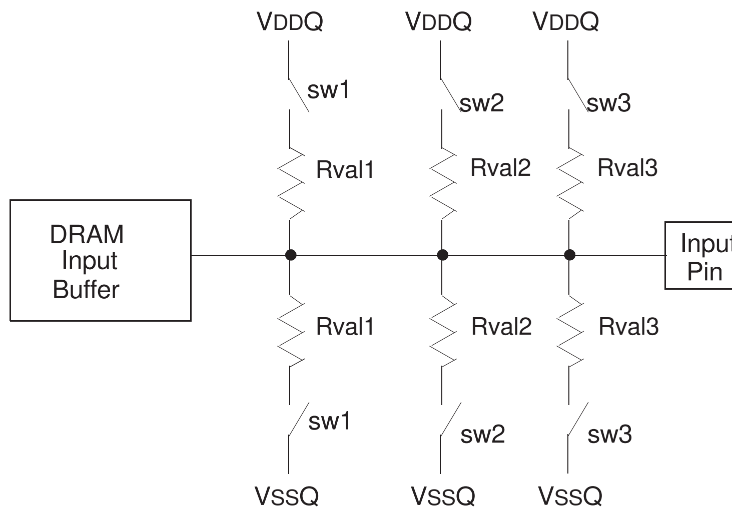



*1 : EMRS(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.
*2 : BA2 and A14 are not used for 512Mb, but used for 1Gb and 2Gb DDR2 SDRAMs. A15 is reserved for future usage.

### *ODT (on-die termination)*

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/$\overline{\text{DQS}}$, RDQS/$\overline{\text{RDQS}}$ and DM signal for x8 configurations via the ODT control pin.
The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is supported for ACTIVE and STANDBY modes. ODT is turned off and not supported in SELF REFRESH mode.




Switch (sw1, sw2, sw3) is enabled by ODT pin.
Selection among sw1, sw2, and sw3 is determined by “Rtt (nominal)” in EMR.
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.

**Functional representation of ODT**

### *ODT Truth Table*

The ODT Truth Table shows  which of the input pins are terminated depending on the state of address bit A10and A11 in the EMRS.

To activate termination of any ofthese pins, the ODT function has to be enabled in the EMRS by address bits A6 and A2.

| Input Pin | EMRS Adress Bit A10 | EMRS Adress Bit A11 |
|---|---|---|
| x8 components : | | |
| DQ0~DQ7 | X | X |
| DQS | X | X |
| $\overline{\text{DQS}}$ | 0 | X |
| RDQS | X | 1 |
| $\overline{\text{RDQS}}$ | 0 | 1 |
| DM | X | 0 |
| x16 components : | | |
| DQ0~DQ7 | X | X |
| DQ8~DQ15 | X | X |
| LDQS | X | X |
| $\overline{\text{LDQS}}$ | 0 | X |
| UDQS | X | X |
| $\overline{\text{UDQS}}$ | 0 | X |
| LDM | X | X |
| UDM | X | X |

X=Don’t Care
0=Signal Low
1=Signal High

### DC Electrical Characteristics and Operation Conditions :

| Parameter / Condition | Symbol | min. | nom. | max. | Units | Notes |
|---|---|---|---|---|---|---|
| Rtt eff. impedance value for EMRS(A6,A2)= 0,1; 75 ohm | Rtt1(eff) | 60 | 75 | 90 | ohm | 1 |
| Rtt eff. impedance value for EMRS(A6,A2)= 1,0; 150 ohm | Rtt2(eff) | 120 | 150 | 180 | ohm | 1 |
| Rtt eff. impedance value for EMRS(A6,A2)= 1,1; 50 ohm | Rtt3(eff) | 40 | 50 | 60 | ohm | 1 |
| Deviation of VM with respect to $V_{DDQ}/2$ | delta VM | -6 | | +6 | % | 2 |

1) Measurement Definition for Rtt(eff) :

Apply VIHac and VILac to test pin seperately, then measure current I(VIHac) and I(VILac) respectively

Rtt(eff) = (VIHac - VILac) /( I(VIHac) - I(VILac))

2) Measurement Definition for VM :

Measure voltage (VM) at test pin (midpoint) with no load:

delta VM = (( 2* VM / $V_{DDQ}$) - 1 ) x 100%

### AC Electrical Characteristics and Operation Conditions : For speed 800

| Symbol | Parameter / Condition | min. | max. | Units | Notes |
|---|---|---|---|---|---|
| $t_{AOND}$ | ODT turn-on delay | 2 | 2 | $t_{CK}$ | |
| $t_{AON}$ | ODT turn-on | $t_{AC}$(min) | $t_{AC}$(max) + 0.7 | ns | 1 |
| $t_{AONPD}$ | ODT turn-on (Power-Down Mode) | $t_{AC}$(min) + 2 | 2 $t_{CK}$ + $t_{AC}$(max) + 1 | ns | 3 |
| $t_{AOFD}$ | ODT turn-off delay | 2.5 | 2.5 | $t_{CK}$ | |
| $t_{AOF}$ | ODT turn-off | $t_{AC}$(min) | $t_{AC}$(max) + 0.6 | ns | 2 |
| $t_{AOFPD}$ | ODT turn-off (Power-Down Mode) | $t_{AC}$(min) + 2 | 2.5 $t_{CK}$ + $t_{AC}$(max) + 1 | ns | 3 |
| $t_{ANPD}$ | ODT to Power Down Mode Entry Latency | 3 | X | $t_{CK}$ | 4 |
| $t_{AXPD}$ | ODT Power Down Exit Latency | 8 | | $t_{CK}$ | 4 |

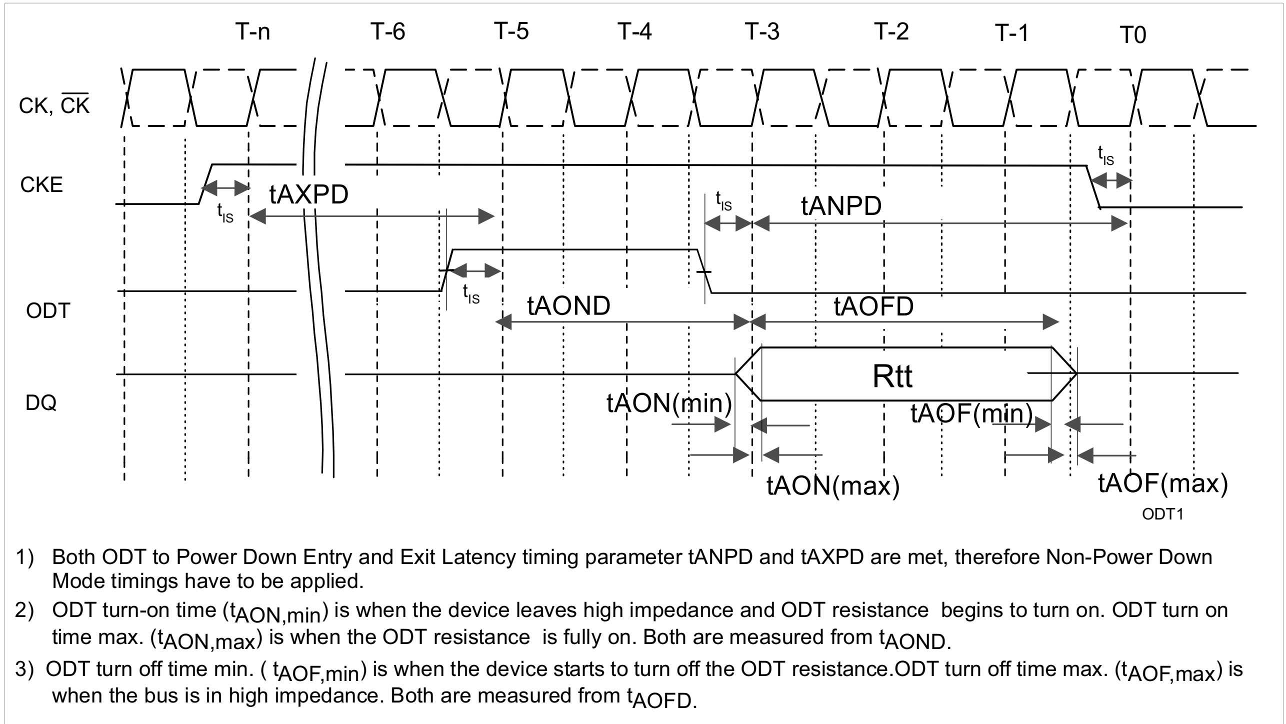
1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max. is when the ODT resistance is fully on. Both are measured from $t_{AOND}$.

2) ODT turn off time min. is when the device stars to turn-off ODT resistance.
ODT turn off time max. is when the bus is in high impedance. Both are measured from $t_{AOFD}$.

3) For Standard Active Power-down - with MRS A12 ="0" - the non power-down timings ( $t_{AOND}$, $t_{AON}$, $t_{AOFD}$ and $t_{AOF}$ ) apply

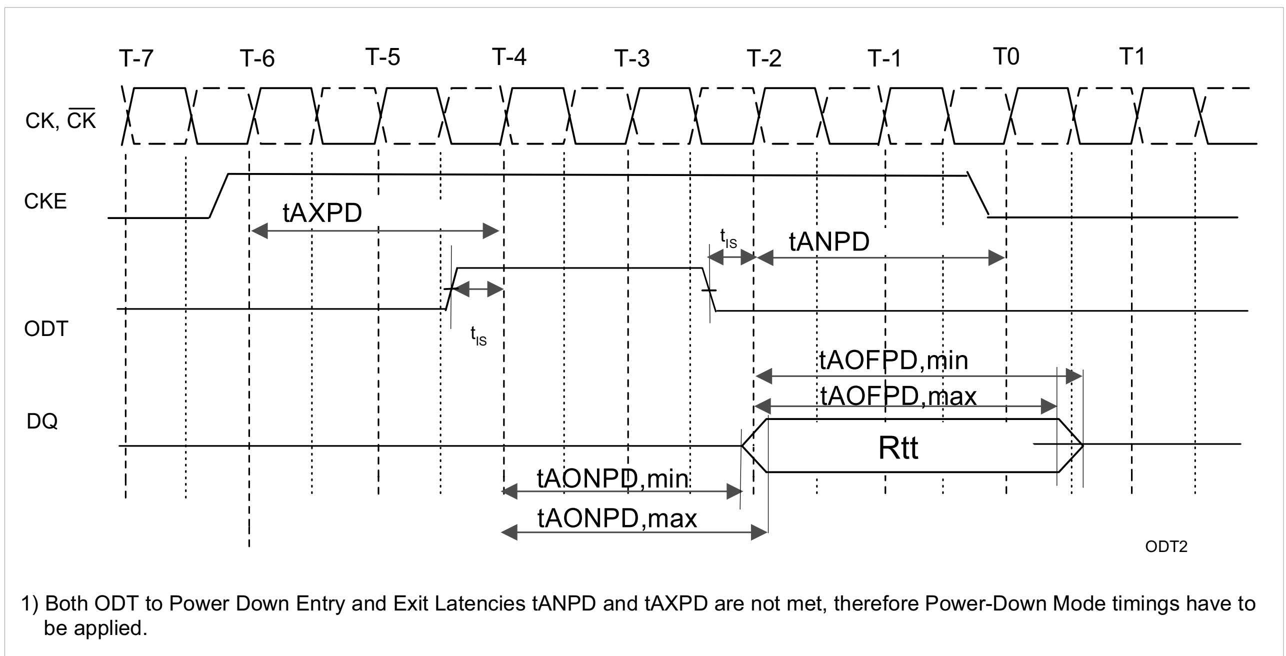
4) $t_{ANPD}$ and $t_{AXPD}$ define the timing limit when either Power Down Mode Timings ($t_{AONPD}$, $t_{AOFPD}$) or Non-Power Down Mode timings ($t_{AOND}$, $t_{AOFD}$) have to be applied.

ODT Timing for Active / Standby (Idle) Mode and Standard Active Power-Down Mode




1) Both ODT to Power Down Entry and Exit Latency timing parameter tANPD and tAXPD are met, therefore Non-Power Down Mode timings have to be applied.
2) ODT turn-on time ($t_{AON,min}$) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max. ($t_{AON,max}$) is when the ODT resistance is fully on. Both are measured from $t_{AOND}$.
3) ODT turn off time min. ( $t_{AOF,min}$) is when the device starts to turn off the ODT resistance.ODT turn off time max. ($t_{AOF,max}$) is when the bus is in high impedance. Both are measured from $t_{AOFD}$.

ODT Timing for Precharge Power-Down and Low Power Power-Down Mode




1) Both ODT to Power Down Entry and Exit Latencies tANPD and tAXPD are not met, therefore Power-Down Mode timings have to be applied.

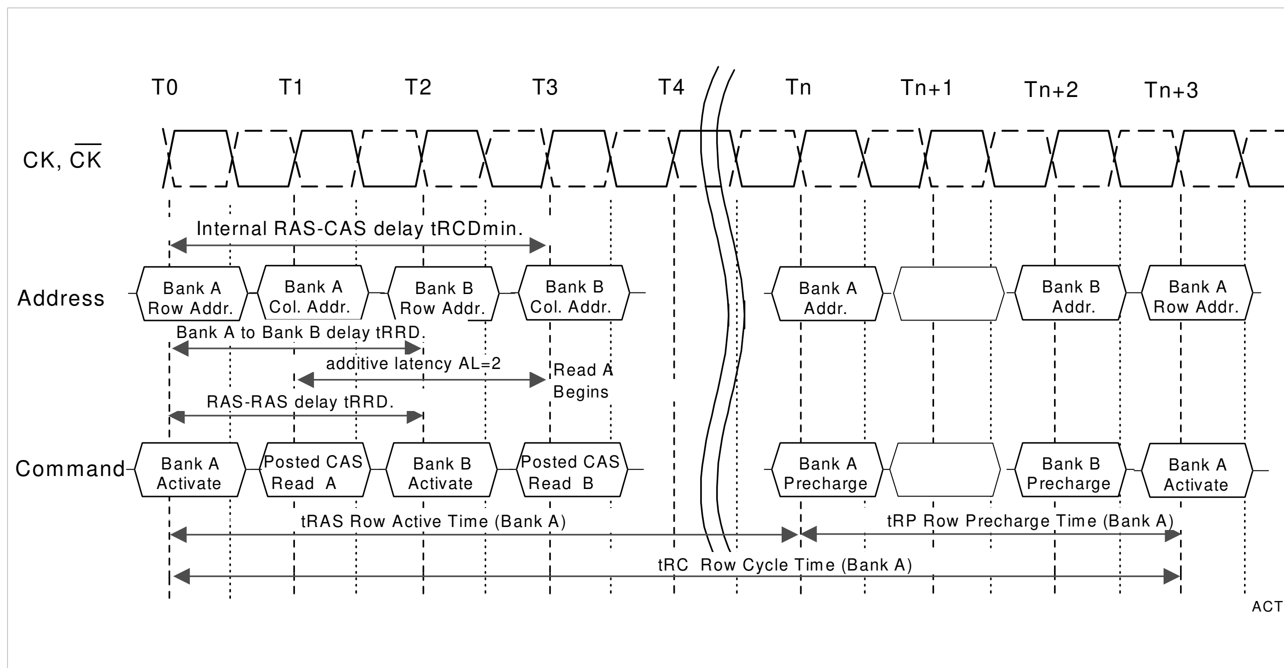
### *Bank Activate Command*

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses of BA0 - BA2 are used to select the desired bank. The row addresses A0 through A14 are used to determine which row to activate in the selected bank for x8 organised components.

The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command (with or without Auto-Precharge) on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0,1,2,3,4,5 and 6 are supported.

Once a bank has been activated, it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined (tRC). The minimum time interval between Bank Active commands, to any other bank, is the Bank A to Bank B delay time (tRRD).

Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2



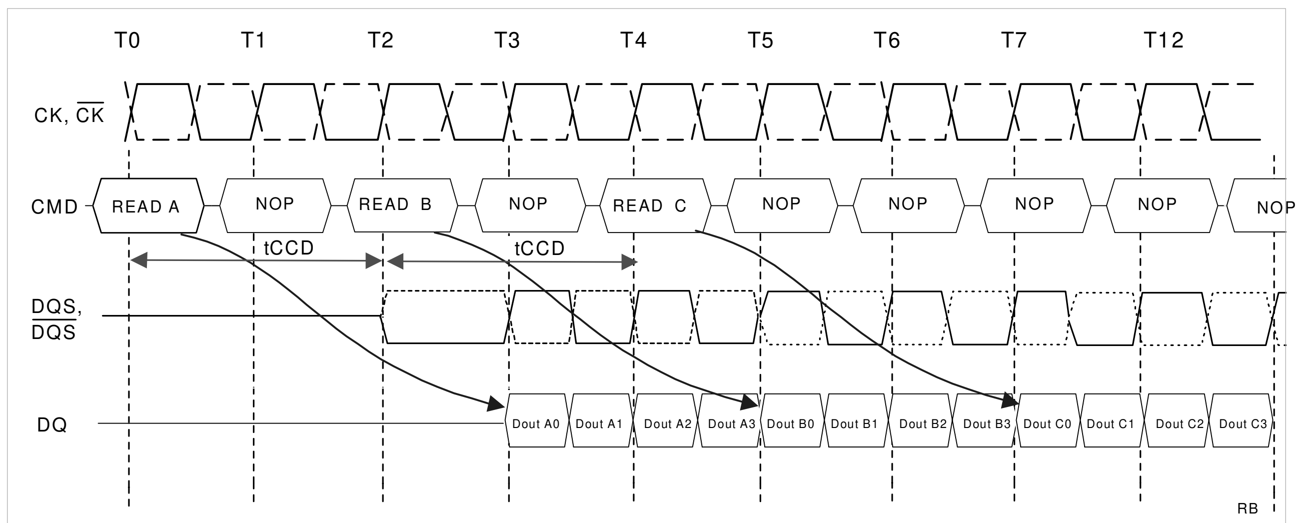
### *Read and Write Commands and Access Modes*

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ( $\overline{WE}$ high ) or a write operation ( $\overline{WE}$ low ). The DDR2 SDRAM provides a wide variety of fast access modes. The boundary of the burst cycle is restricted to specific segments of the page length.

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. Therefore the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (tCCD) is a minimum of 2 clocks for read or write cycles.

For 8 bit burst operation ( BL = 8 ) the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (tCCD) is 4 clocks for read or write cycles. Burst interruption is allowed with 8 bit burst operation. For details see the “Burst Interrupt” - Section of this datasheet.

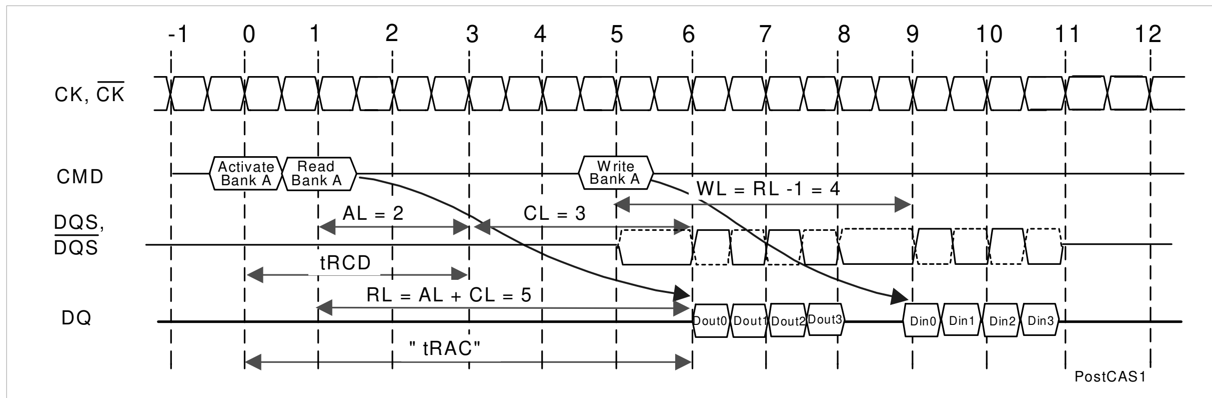
**Read Burst Timing Example : (CL = 3, AL = 0, RL = 3, BL = 4)**



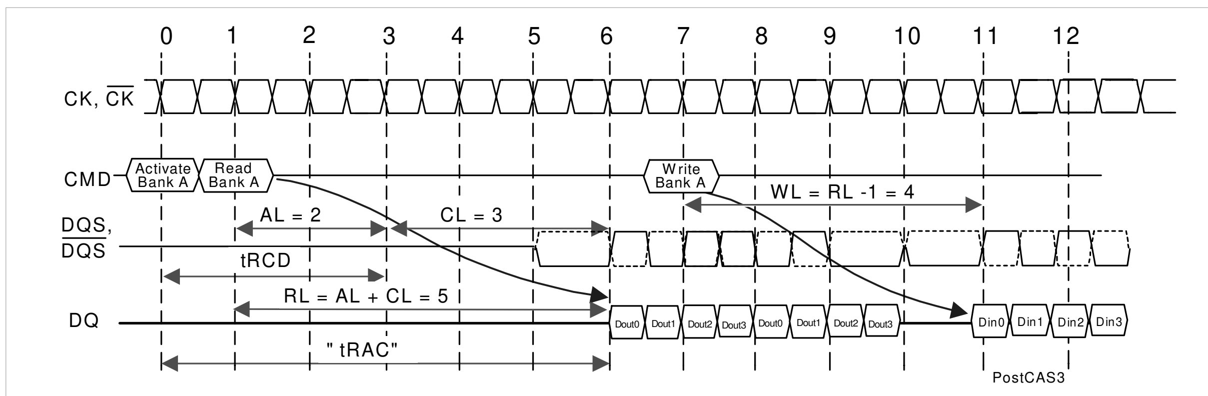
## Posted $\overline{CAS}$

Posted $\overline{CAS}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a Read or Write command to be issued immediately after the $\overline{RAS}$ bank activate command (or any time during the $\overline{RAS}$ to $\overline{CAS}$ delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is the sum of AL and the $\overline{CAS}$ latency (CL). Therefore if a user chooses to issue a Read/Write command before the tRCDmin, then AL greater than 0 must be written into the EMRS. The Write Latency (WL) is always defined as RL - 1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus $\overline{CAS}$ latency (RL=AL+CL). If a user chooses to issue a Read command after the tRCDmin period, the Read Latency is also defined as RL = AL + CL.

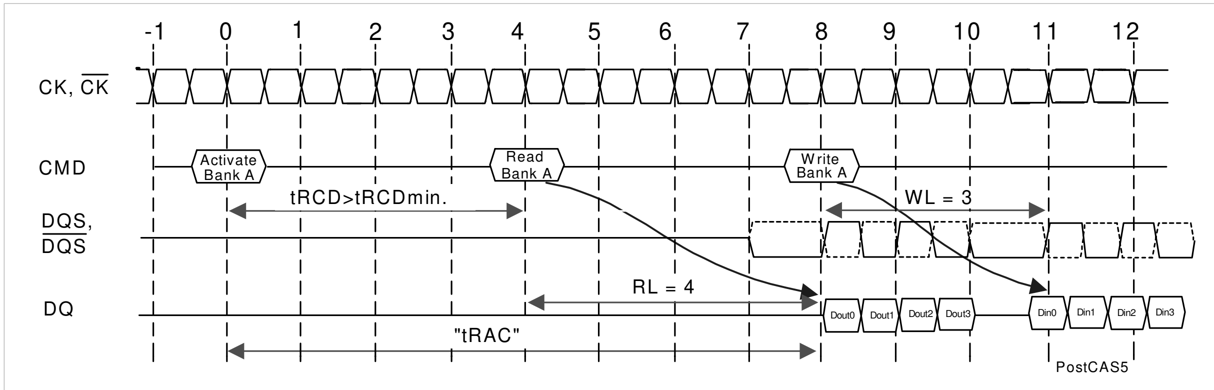
**Read followed by a write to the same bank, Activate to Read delay < tRCDmin:**
**AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 4**




**Read followed by a write to the same bank, Activate to Read delay < tRCDmin:**
**AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 8**



Read followed by a write to the same bank, Activate to Read delay > tRCDmin:
AL = 1, CL = 3, RL = 4, WL = 3, BL = 4



### Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations ( write cycle ), or from memory locations ( read cycle ). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst-mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by the addresses A0 ~ A2 of the MRS. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS. Seamless burst read or write operations are supported. Interruption of a burst read or write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a read or write burst when burst length = 8 is used, see the “Burst Interruption” section of this datasheet. A Burst Stop command is not supported on DDR2 SDRAM devices.

### Burst Length and Sequence

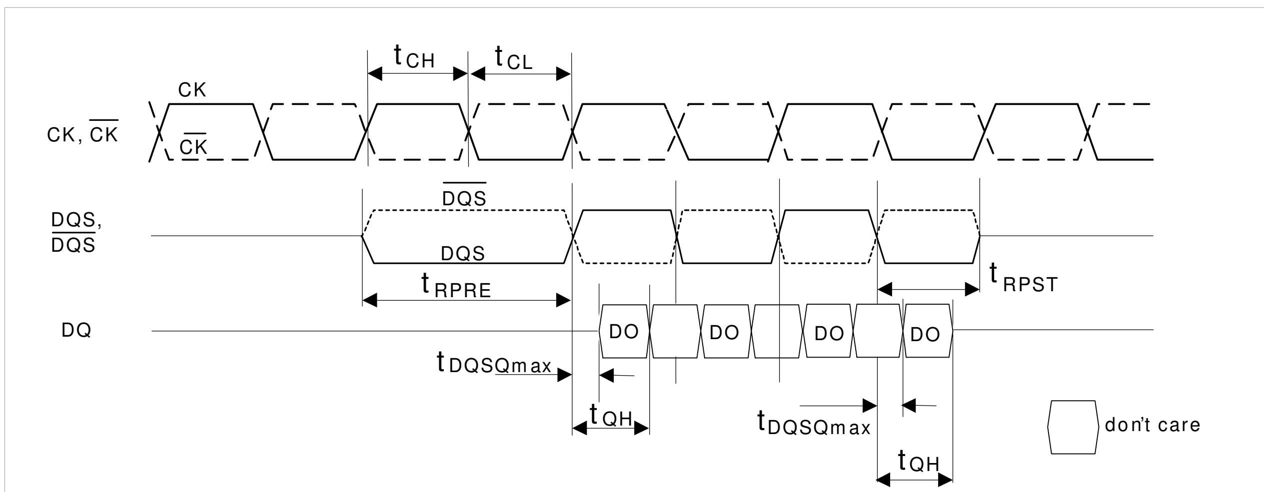
| Burst Length | Starting Address ( A2 A1 A0 ) | Sequential Addressing (decimal) | Interleave Addressing (decimal) |
|---|---|---|---|
| 4 | x 0 0 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| | x 0 1 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| | x 1 0 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| | x 1 1 | 3, 0, 1, 2 | 3, 2, 1, 0 |
| 8 | 0 0 0 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 |
| | 0 0 1 | 1, 2, 3, 0, 5, 6, 7, 4 | 1, 0, 3, 2, 5, 4, 7, 6 |
| | 0 1 0 | 2, 3, 0, 1, 6, 7, 4, 5 | 2, 3, 0, 1, 6, 7, 4, 5 |
| | 0 1 1 | 3, 0, 1, 2, 7, 4, 5, 6 | 3, 2, 1, 0, 7, 6, 5, 4 |
| | 1 0 0 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| | 1 0 1 | 5, 6, 7, 4, 1, 2, 3, 0 | 5, 4, 7, 6, 1, 0, 3, 2 |
| | 1 1 0 | 6, 7, 4, 5, 2, 3, 0, 1 | 6, 7, 4, 5, 2, 3, 0, 1 |
| | 1 1 1 | 7, 4, 5, 6, 3, 0, 1, 2 | 7, 6, 5, 4, 3, 2, 1, 0 |

Note: 1) Page length is a function of I/O organization and column addressing.
2) Order of burst access for sequential addressing is “nibble-based” and therefore different from SDR or DDR components.

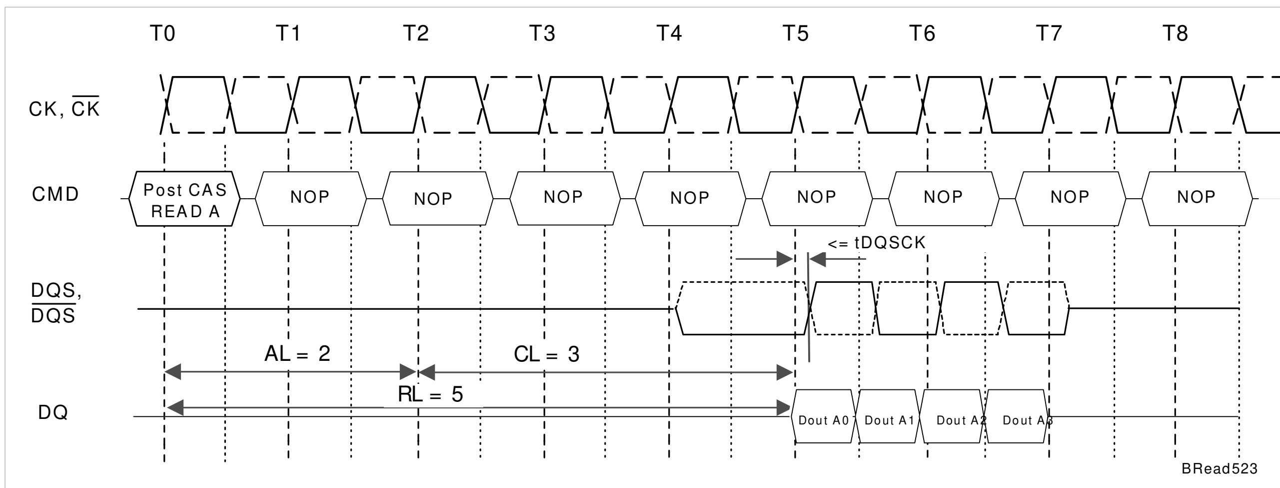
## Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command until the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register Set (EMRS).

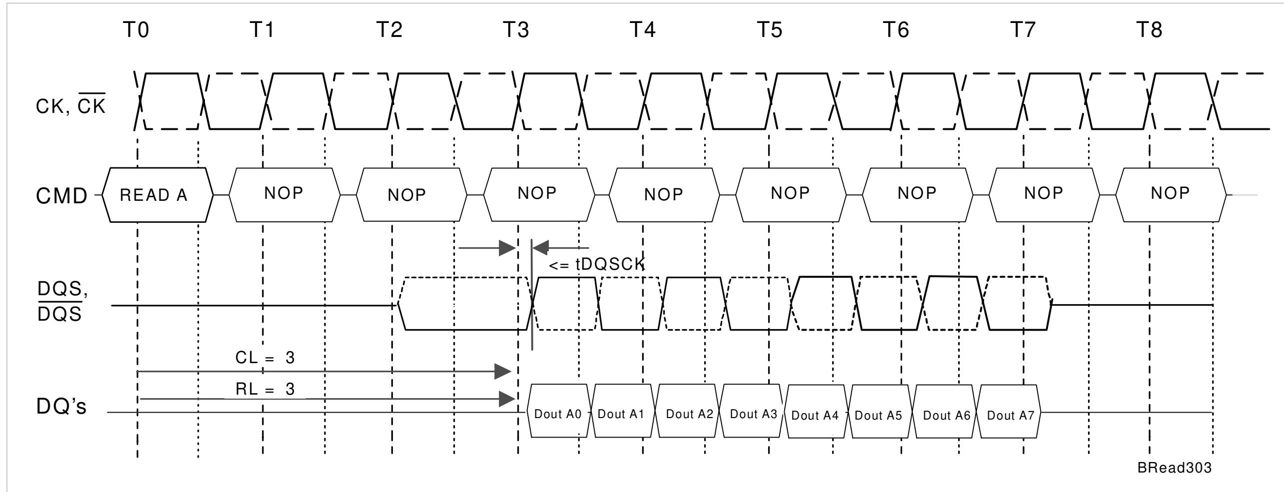
### Basic Burst Read Timing



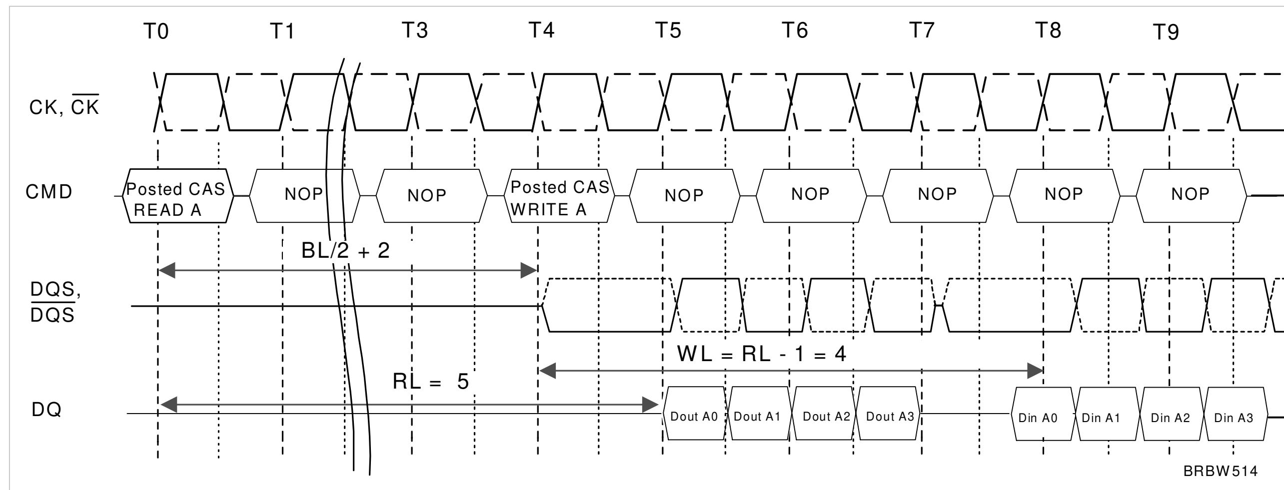

### Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)



**Burst Read Operation: RL = 3 (AL = 0, CL = 3, BL = 8)**

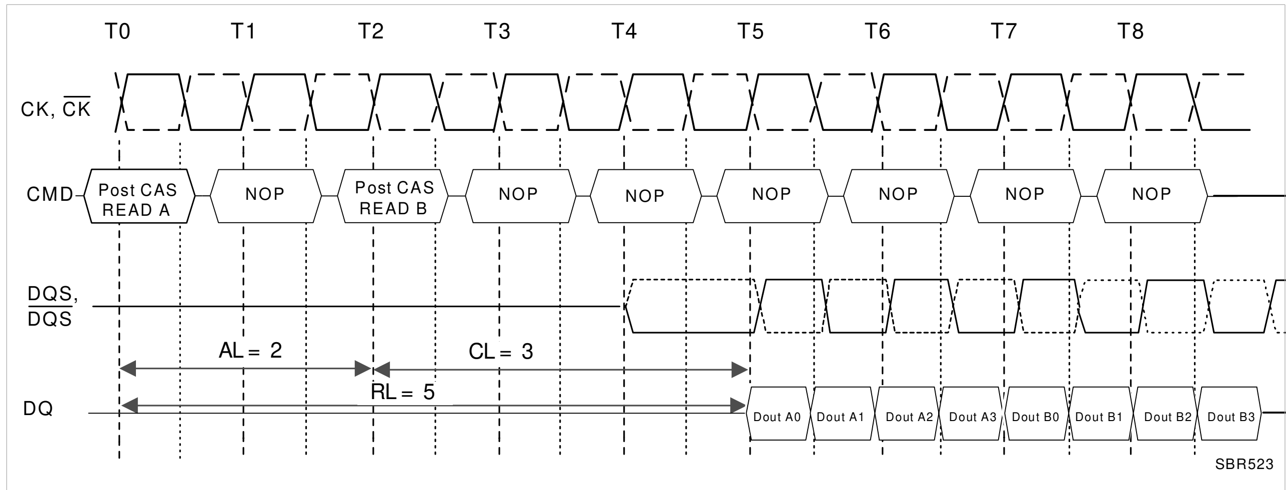



Burst Read followed by Burst Write : RL = 5, WL = (RL-1) = 4, BL = 4



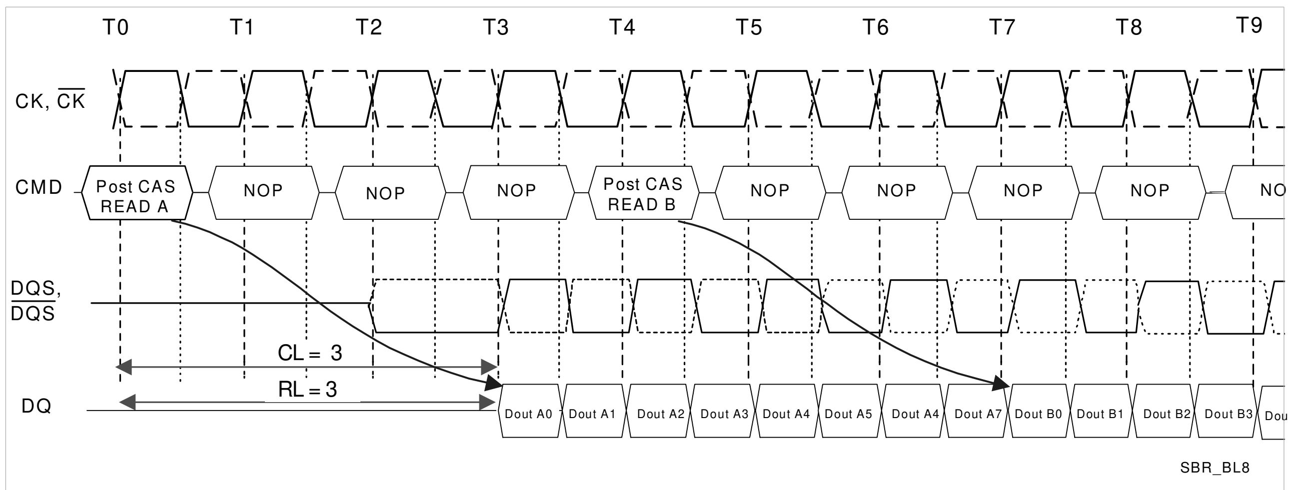

The minimum time from the burst read command to the burst write command is defined by a read-to-write turn-around time, which is BL/2 + 2 clocks.

Seamless Burst Read Operation : RL = 5, AL = 2, CL = 3, BL = 4




The seamless burst read operation is supported by enabling a read command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

**Seamless Burst Read Operation : RL = 3, AL = 0, CL = 3, BL = 8 (non interrupting)**

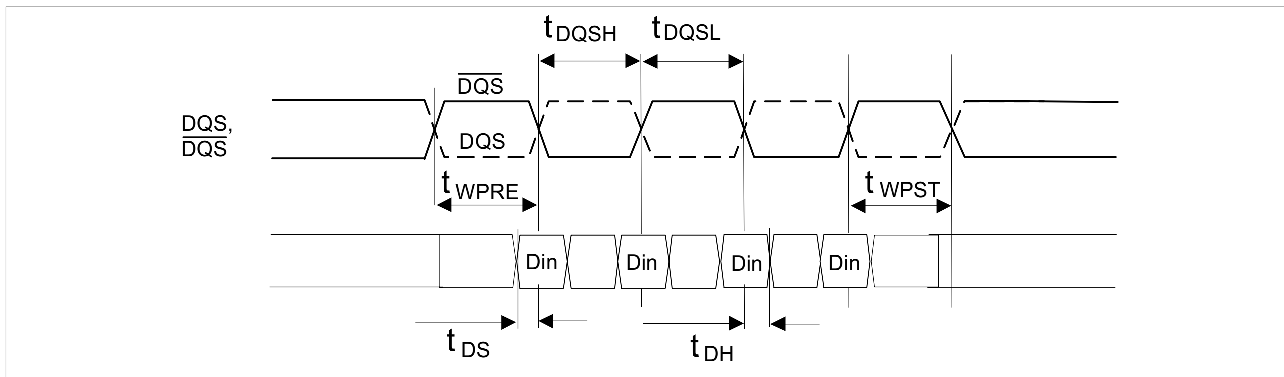



The seamless, non interrupting 8-bit burst read operation is supported by enabling a read command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

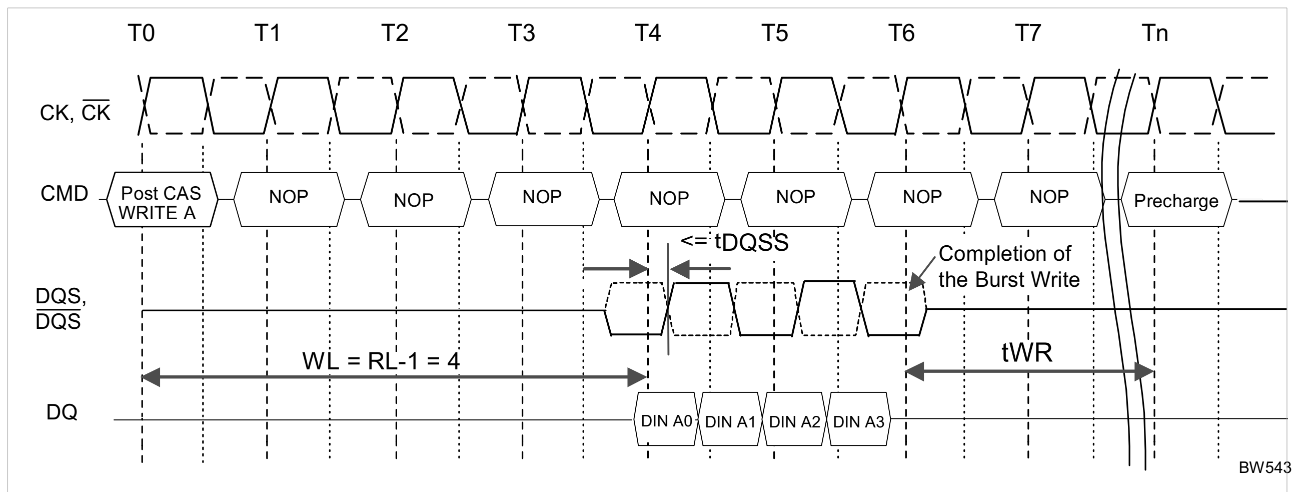
## Burst Write Command

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is named “write recovery time” (tWR) and is the time needed to store the write data into the memory array. tWR is an analog timing parameter (see the AC table in this specification) and is not the programmed value for WR in the MRS.

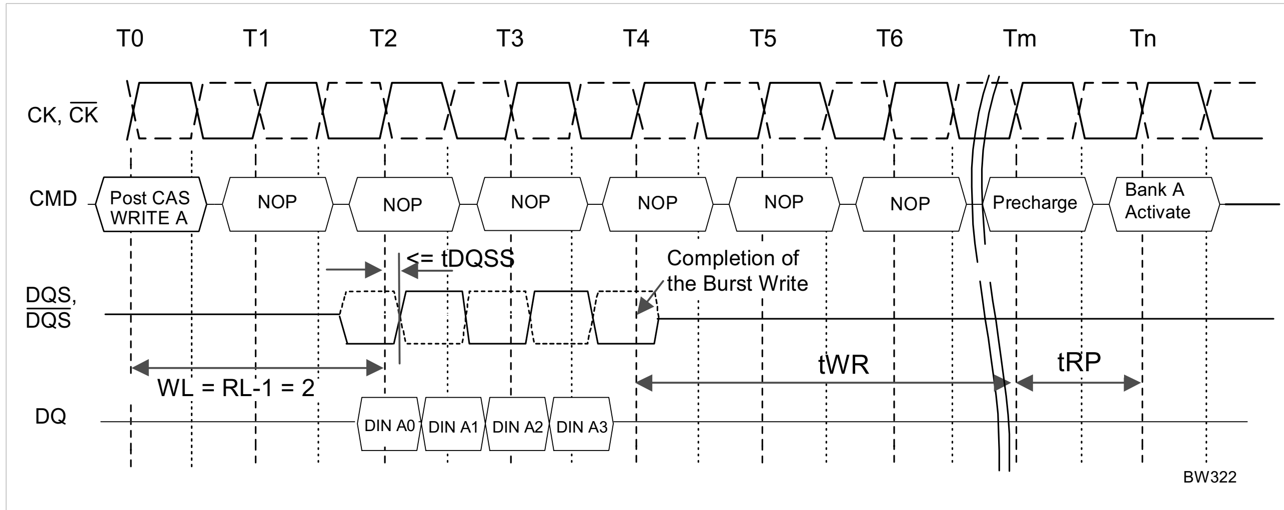
### Basic Burst Write Timing



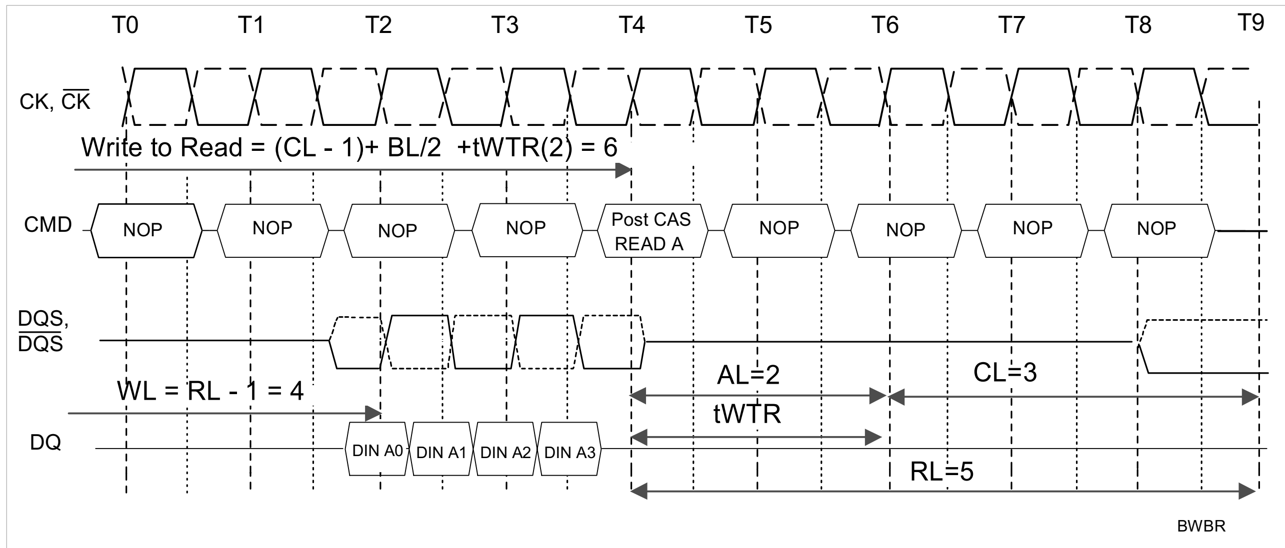

### Burst Write Operation : RL = 5 (AL = 2, CL = 3), WL = 4, BL = 4



**Burst Write Operation : RL = 3 (AL = 0, CL = 3), WL = 2, BL = 4**




**Burst Write followed by Burst Read : RL = 5 (AL = 2, CL = 3), WL = 4, tWTR = 2, BL = 4**




The minimum number of clocks from the burst write command to the burst read command is

(CL - 1) +BL/2 + tWTR

where tWTR is the write-to-read turn-around time tWTR expressed in clock cycles. The tWTR is not a write recovery time (tWR) but the time required to transfer 4 bit write data from the input buffer into sense amplifiers in the array.