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Revision History

AS4C32M8D1 - 66pin TSOPII PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Jun 2016

Features

- High speed data transfer rates with system frequency up to 200 MHz
- Data Mask for Write Control
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 2.5, 3, 4
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  2, 4, 8 for Sequential Type
  2, 4, 8 for Interleave Type
- Automatic and Controlled Precharge Command
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 8192 cycles/64 ms
- Available in 66-pin 400 mil TSOP
- SSTL-2 Compatible I/Os
- Double Data Rate (DDR)
- Bidirectional Data Strobe (DQS) for input and output data, active on both edges
- On-Chip DLL aligns DQ and DQs transitions with CK transitions
- Differential clock inputs CK and $\overline{CK}$
- Power Supply 2.5V ± 0.2V for DDR333, 2.6V ± 0.1V for DDR400
- tRAS lockout supported
- Concurrent auto precharge option is supported

Description

The AS4C32M8D1 is a four bank DDR DRAM organized as 4 banks x 8Mbit x 8. The AS4C32M8D1 achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

All of the control, address, circuits are synchronized with the positive edge of an externally supplied clock. I/O transactions are occurring on both edges of DQS.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

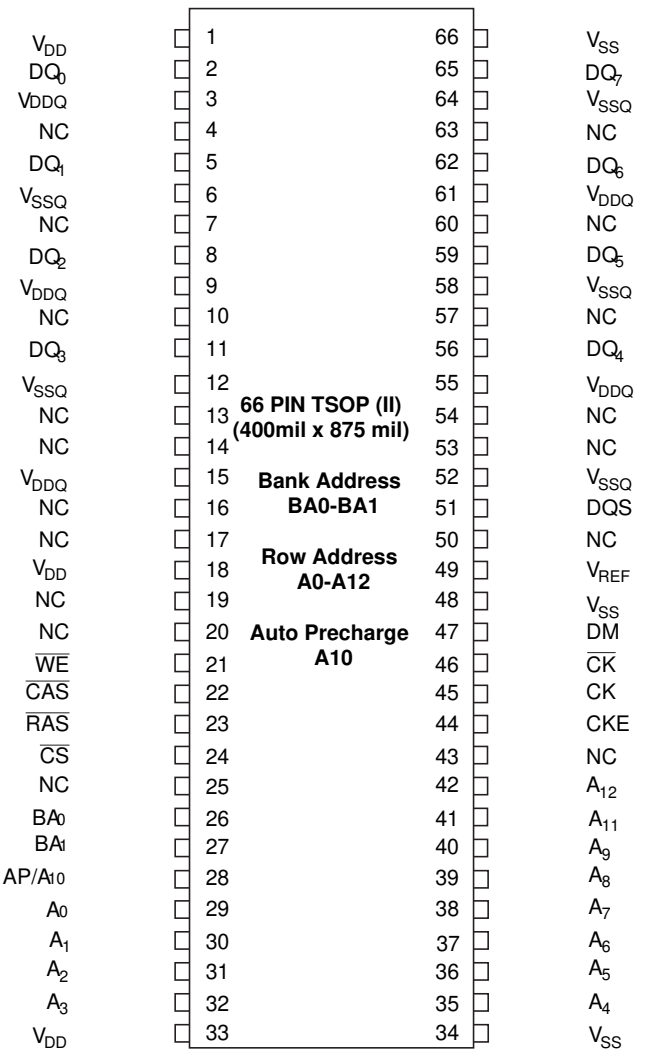
Table 1. Ordering Information

Part Number	Org	Temperature	MaxClock (MHz)	Package
AS4C32M8D1-5TCN	32Mx8	Commercial 0°C to 70°C	200	66-pin TSOPII
AS4C32M8D1-5TIN	32Mx8	Industrial -40°C to 85°C	200	66-pin TSOPII

Table 2. Speed Grade Information

Speed Grade	Clock Frequency	CAS Latency	tRCD (ns)	tRP (ns)
DDR1-400	200MHz	3	15	15

66 Pin Plastic TSOP-II



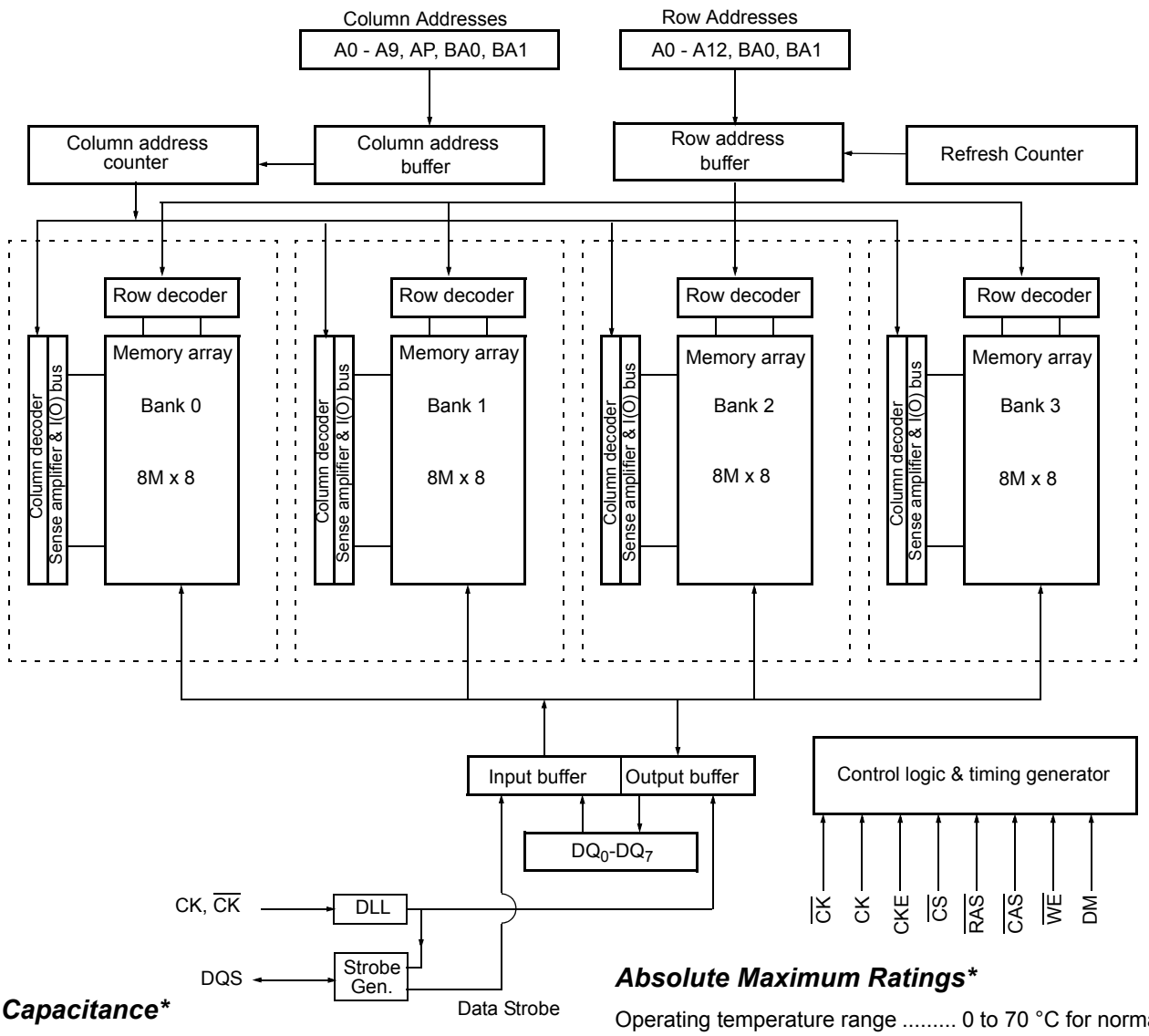
Pin Names

CK, $\overline{CK}$	Differential Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQS (UDQS, LDQS)	Data Strobe (Bidirectional)
A_0–A_{12}	Address Inputs
BA0, BA1	Bank Select

DQ's	Data Input/Output
DM	Data Mask
V_{DD}	Power (+2.5V and +2.6V for DDR400)
V_{SS}	Ground
V_{DDQ}	Power for I/O's (+2.5V and +2.6V for DDR400)
V_{SSQ}	Ground for I/O's
NC	Not connected
VREF	Reference Voltage for Inputs

Block Diagram

32M x 8



*Capacitance**

V_{CC} = 2.5V ± 0.2V, f = 1 MHz

Input Capacitance	Symbol	Min	Max	Unit
BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, ($\overline{CAS}$, A0-A11, $\overline{WE}$)	C_{INI}	2	3.0	pF
Input Capacitance (CK, $\overline{CK}$)	C_{IN2}	2	3.0	pF
Data & DQS I/O Capacitance	C_{OUT}	4	5	pF
Input Capacitance (DM)	C_{IN3}	4	5.0	pF

***Note:** Capacitance is sampled and not 100% tested.

*Absolute Maximum Ratings**

Operating temperature range ..... 0 to 70 °C for normal
-40 to 85 °C for Industrial
Storage temperature range..... -55 to 150 °C
V_{DD}Supply Voltage Relative to V_{SS}.....-1V to +3.6V
V_{DDQ} Supply Voltage Relative to V_{SS}
.....-1V to +3.6V
VREF and Inputs Voltage Relative to V_{SS}
.....-1V to +3.6V
I/O Pins Voltage Relative to V_{SS}
.....-0.5V to V_{DDQ}+0.5V
Power dissipation..... 1.6 W
Data out current (short circuit) ..... 50 mA

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Signal Pin Description

Pin	Type	Signal	Polarity	Function
CK $\overline{CK}$	Input	Pulse	Positive Edge	The system clock input. All inputs except DQs and DMs are sampled on the rising edge of CK.
CKE	Input	Level	Active High	Activates the CK signal when high and deactivates the CK signal when low, thereby initiates either the Power Down mode, or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
DQS	Input/ Output	Pulse	Active High	Active on both edges for data input and output. Center aligned to input data Edge aligned to output data
A0 - A12	Input	Level	—	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge.CAn depends on the SDRAM organization: 32M x 8 DDR CAn = CA9 In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged simultaneously regardless of state of BA0 and BA1.
BA0, BA1	Input	Level	—	Selects which bank is to be active.
DQx	Input/ Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DM,	Input	Pulse	Active High	In Write mode, DM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation .
VDD, VSS	Supply			Power and ground for the input buffers and the core logic.
VDDQ VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.
VREF	Input	Level	—	SSTL Reference Voltage for Inputs

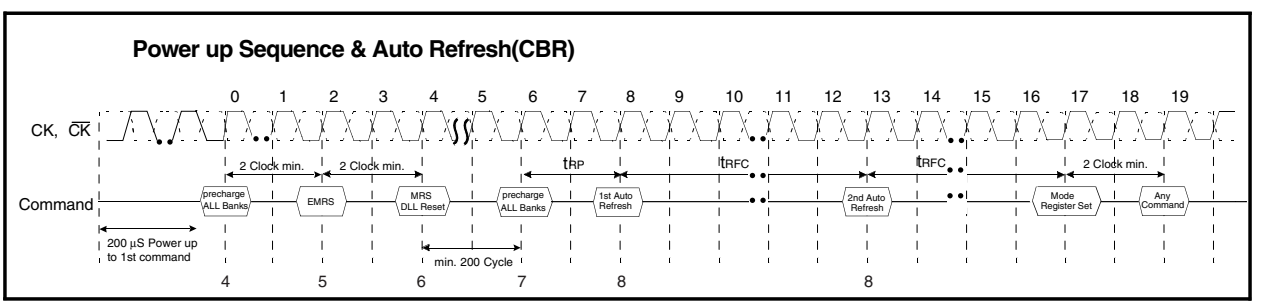
Functional Description

- Power-Up Sequence

  The following sequence is required for POWER UP.

  1. Apply power and attempt to maintain CKE at a low state (all other inputs may be undefined.)
     - Apply VDD before or at the same time as VDDQ.
     - Apply VDDQ before or at the same time as VTT & Vref.
  2. Start clock and maintain stable condition for a minimum of 200us.
  3. The minimum of 200us after stable power and clock (CLK, $\overline{CLK}$), apply NOP & take CKE high.
  4. Precharge all banks.
  5. Issue EMRS to enable DLL.(To issue “DLL Enable” command, provide “Low” to A0, “High” to BA0 and “Low” to all of the rest address pins, A1~A11 and BA1)
  6. Issue a mode register set command for “DLL reset”. The additional 200 cycles of clock input is required to lock the DLL. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0)
  7. Issue precharge commands for all banks of the device.
  8. Issue 2 or more auto-refresh commands.
  9. Issue a mode register set command to initialize device operation.

Note1 Every “DLL enable” command resets DLL. Therefore sequence 6 can be skipped during power up. Instead of it, the additional 200 cycles of clock input is required to lock the DLL after enabling DLL.



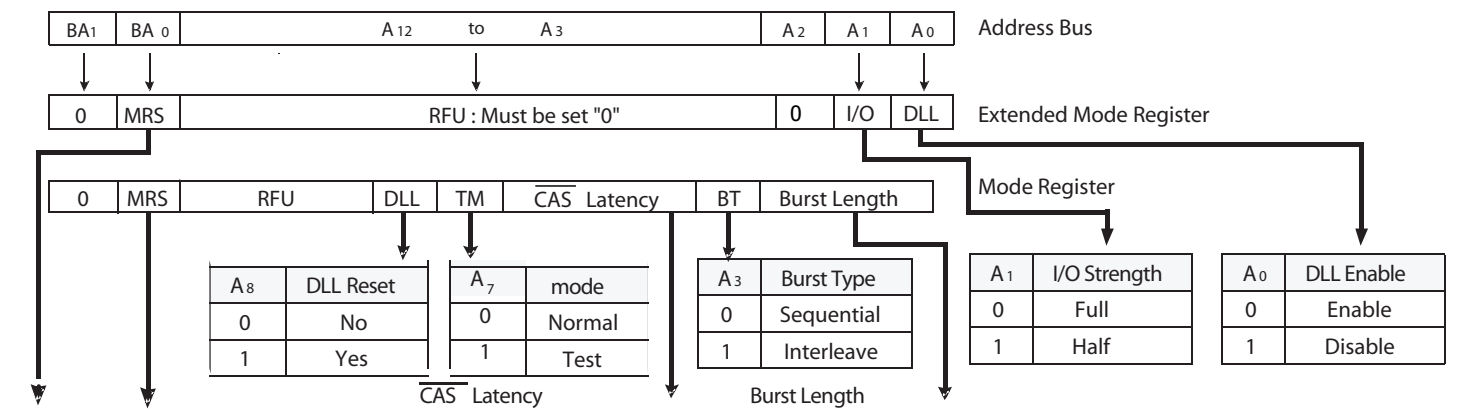
Extended Mode Register Set (EMRS)

The extended mode register stores the data for enabling or disabling DLL. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on $\overline{CS}$, RAS, $\overline{CAS}$, $\overline{WE}$ and high on BA_0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A_0 ~ A_{12} and BA_1 in the same cycle as $\overline{CS}$, RAS, $\overline{CAS}$ and $\overline{WE}$ low is written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A_0 is used for DLL enable or disable. “High” on BA_0 is used for EMRS. All the other address pins except A_0 and BA_0 must be set to low for proper EMRS operation. A_1 is used at EMRS to indicate I/O strength A_1 = 0 full strength, A_1 = 1 half strength. Refer to the table for specific codes.

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs $\overline{CAS}$ latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for a variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA_0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register). The state of address pins A_0 ~ A_{12} in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0 low is written in the mode register. Two clock cycles are required to meet t_{MRD} spec. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A_0 ~ A_2, addressing mode uses A_3, $\overline{CAS}$ latency (read latency from column address) uses A_4 ~ A_6. A_7 is a Alliance specific test mode during production test. A_8 is used for DLL reset. A_7 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and $\overline{CAS}$ latencies.

1. MRS can be issued only at all banks precharge state.
2. Minimum tRP is required to issue MRS command.



A_8	DLL Reset
0	No
1	Yes

A_7	mode
0	Normal
1	Test

A_3	Burst Type
0	Sequential
1	Interleave

A_1	I/O Strength
0	Full
1	Half

A_0	DLL Enable
0	Enable
1	Disable

BA_0	A_n ~ A_0
0	(Existing)MRS Cycle
1	Extended Funtions(EMRS)

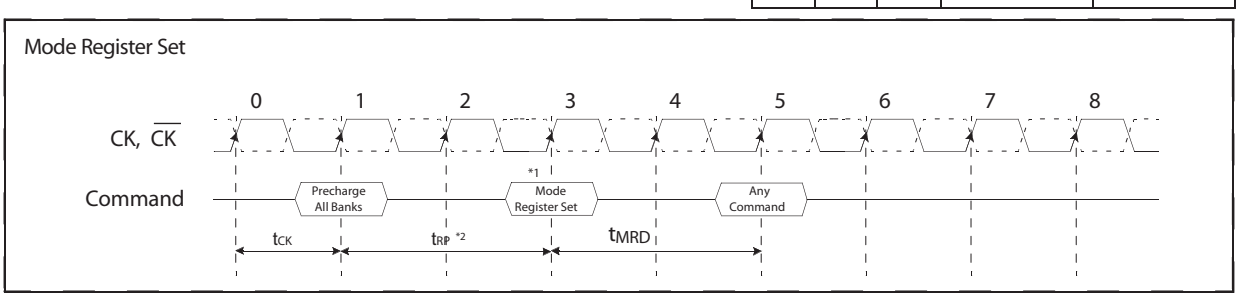
* RFU(Reserved for future use) should stay "0" during MRS cycle.

$\overline{CAS}$ Latency

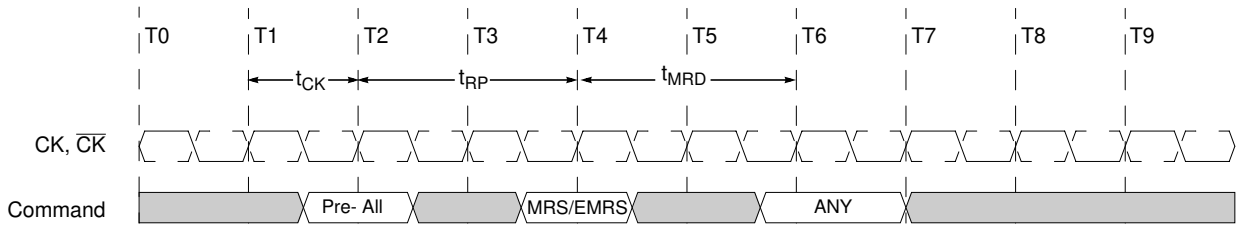
A_6	A_5	A_4	Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	Reserve
0	1	1	3
1	0	0	4
1	0	1	Reserve
1	1	0	2.5
1	1	1	Reserve

Burst Length

A_2	A_1	A_0	Latency	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Reserve	Reserve



Mode Register Set Timing



Mode Register set (MRS) or Extended Mode Register Set (EMRS) can be issued only when all banks are in the idle state.

If a MRS command is issued to reset the DLL, then an additional 200 clocks must occur prior to issuing any new command to allow time for the DLL to lock onto the clock.

Burst Mode Operation

Burst Mode Operation is used to provide a constant flow of data to memory locations (Write cycle), or from memory locations (Read cycle). Two parameters define how the burst mode will operate: burst sequence and burst length. These parameters are programmable and are determined by address bits A_0—A_3 during the Mode Register Set command. Burst type defines the sequence in which the burst data will be delivered or stored to the SDRAM. Two types of burst sequence are supported: sequential and interleave. The burst length controls the number of bits that will be output after a Read command, or the number of bits to be input after a Write command. The burst length can be programmed to values of 2, 4, or 8. See the Burst Length and Sequence table below for programming information.

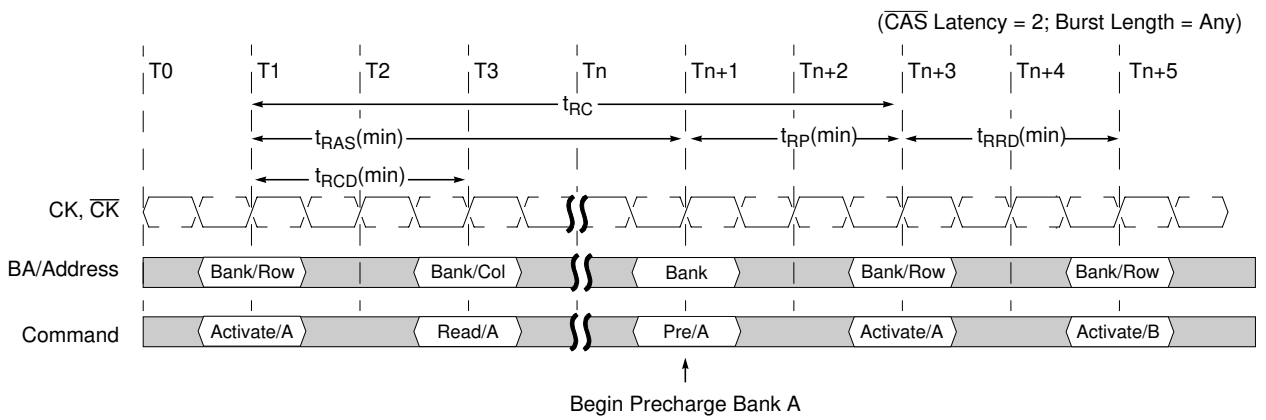
Burst Length and Sequence

Burst Length	Starting Length (A_2, A_1, A_0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0,1, 2, 3, 4, 5, 6, 7	0,1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The DDR SDRAM has four independent banks, so two Bank Select addresses (BA_0 and BA_1) are supported. The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from the Bank Activate command to the first Read or Write command must meet or exceed the minimum $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD} min). Once a bank has been activated, it must be pre-charged before another Bank Activate command can be applied to the same bank. The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD} min).

Bank Activation Timing



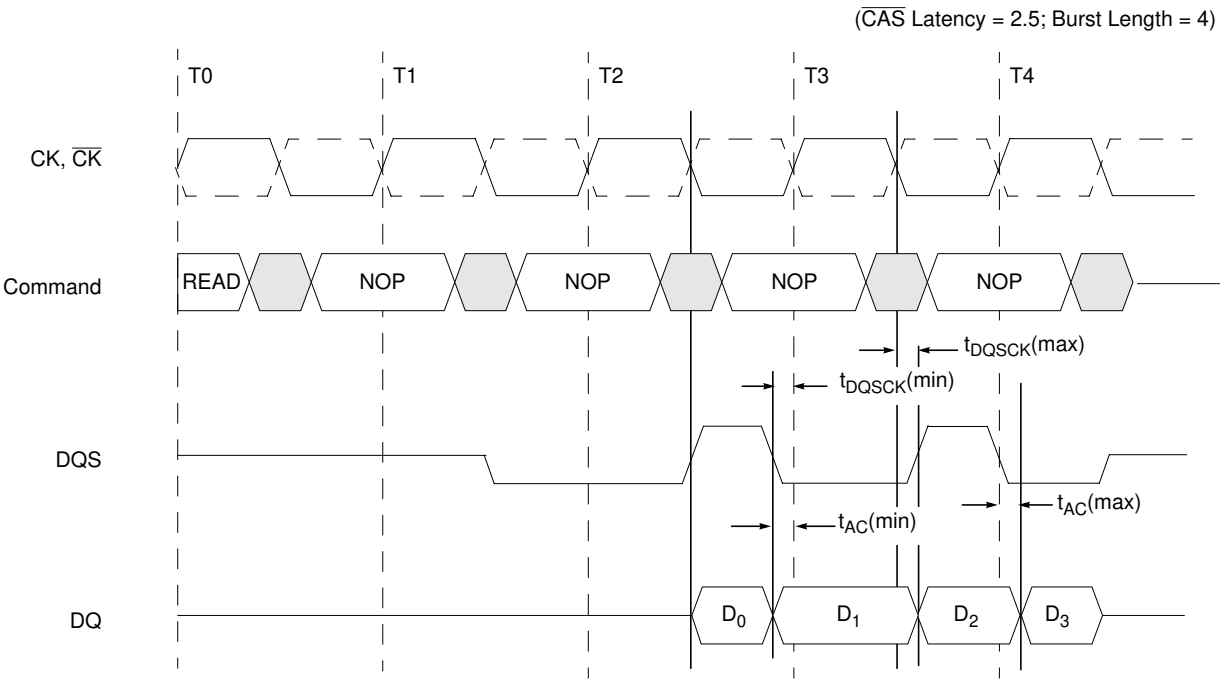
Read Operation

With the DLL enabled, all devices operating at the same frequency within a system are ensured to have the same timing relationship between DQ and DQS relative to the CK input regardless of device density, process variation, or technology generation.

The data strobe signal (DQS) is driven off chip simultaneously with the output data (DQ) during each read cycle. The same internal clock phase is used to drive both the output data and data strobe signal off chip to minimize skew between data strobe and output data. This internal clock phase is nominally aligned to the input differential clock (CK, $\overline{CK}$) by the on-chip DLL. Therefore, when the DLL is enabled and the clock frequency is within the specified range for proper DLL operation, the data strobe (DQS), output data (DQ), and the system clock (CK) are all nominally aligned.

Since the data strobe and output data are tightly coupled in the system, the data strobe signal may be delayed and used to latch the output data into the receiving device. The tolerance for skew between DQS and DQ (t_{DQSQ}) is tighter than that possible for CK to DQ (t_{AC}) or DQS to CK (t_{DQSCK}).

Output Data (DQ) and Data Strobe (DQS) Timing Relative to the Clock (CK) During Read Cycles



The minimum time during which the output data (DQ) is valid is critical for the receiving device (i.e., a memory controller device). This also applies to the data strobe during the read cycle since it is tightly coupled to the output data. The minimum data output valid time (t_{DV}) and minimum data strobe valid time (t_{DQSV}) are derived from the minimum clock high/low time minus a margin for variation in data access and hold time due to DLL jitter and power supply noise.

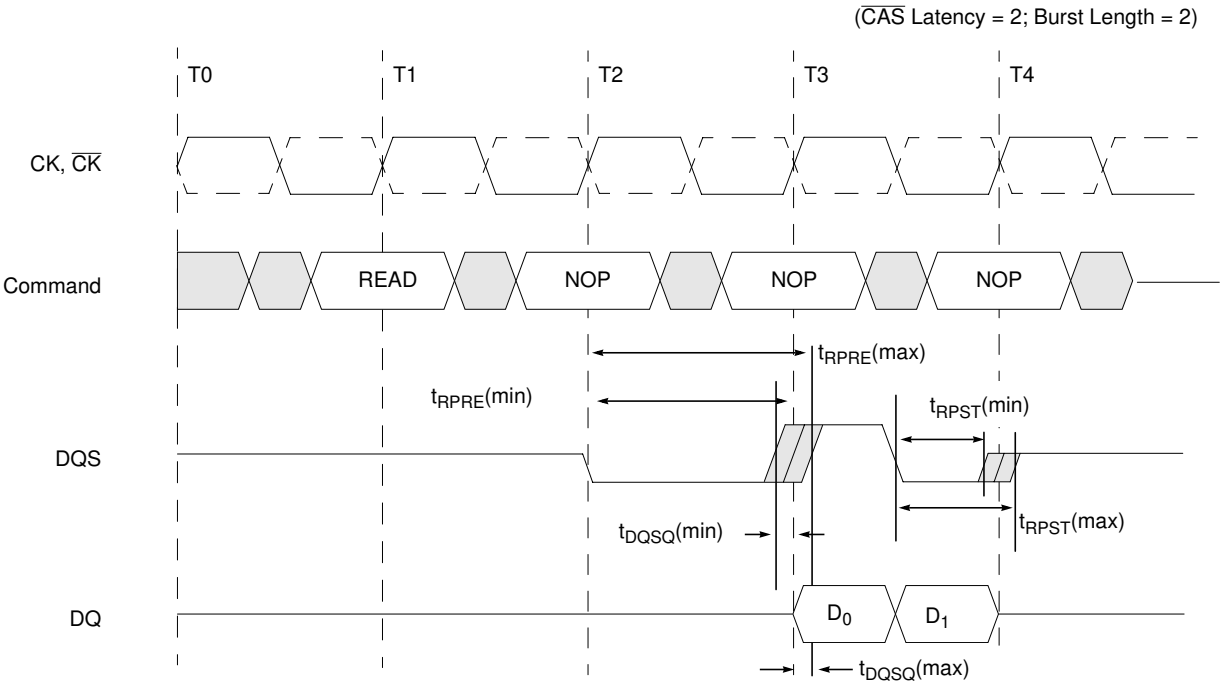
Read Preamble and Postamble Operation

Prior to a burst of read data and given that the controller is not currently in burst read mode, the data strobe signal(DQS), must transition from Hi-Z to a valid logic low. The is referred to as the data strobe “read preamble” (t_{RPRE}). This transition from Hi-Z to logic low nominally happens one clock cycle prior to the first edge of valid data.

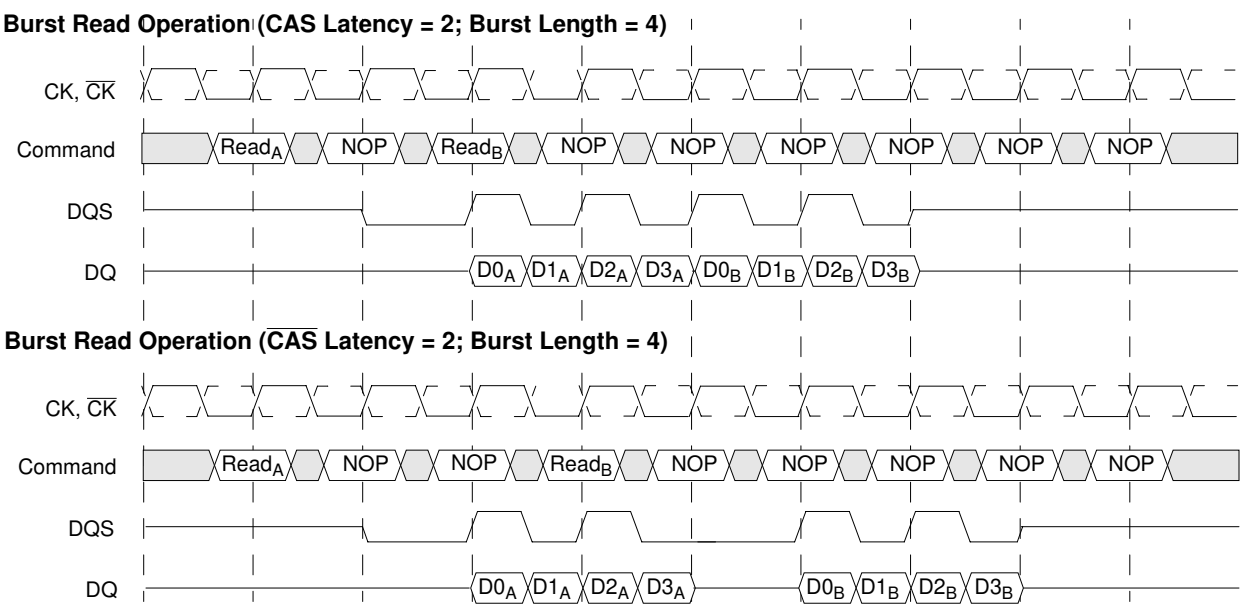
Once the burst of read data is concluded and given that no subsequent burst read operations are initiated, the data strobe signal (DQS) transitions from a logic low level back to Hi-Z. This is referred to as the data strobe “read postamble” (t_{RPST}). This transition happens nominally one-half clock period after the last edge of valid data.

Consecutive or “gapless” burst read operations are possible from the same DDR SDRAM device with no requirement for a data strobe “read” preamble or postamble in between the groups of burst data. The data strobe read preamble is required before the DDR device drives the first output data off chip. Similarly, the data strobe postamble is initiated when the device stops driving DQ data at the termination of read burst cycles.

Data Strobe Preamble and Postamble Timings for DDR Read Cycles



Consecutive Burst Read Operation and Effects on the Data Strobe Preamble and Postamble



Precharge Operation

The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank (s) will be available for a subsequent row access a specified time (t_{RP}) after the precharge command is issued. Except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A Precharge command will be treated as NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

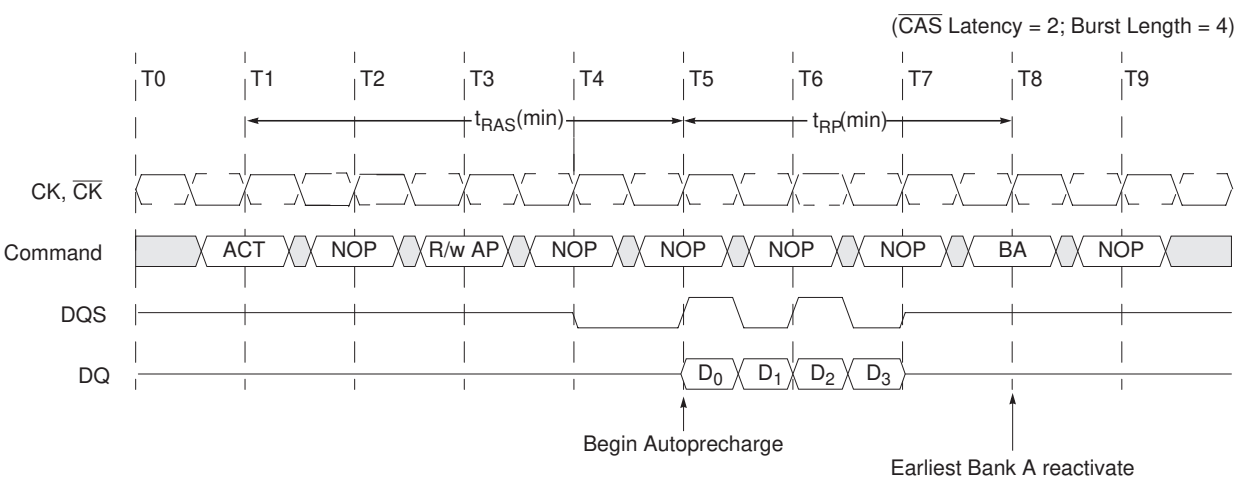
Auto Precharge Operation

The Auto Precharge operation can be issued by having column address A_{10} high when a Read or Write command is issued. If A_{10} is low when a Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. When the Auto Precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during the Read or Write cycle once t_{RAS}(min) is satisfied. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

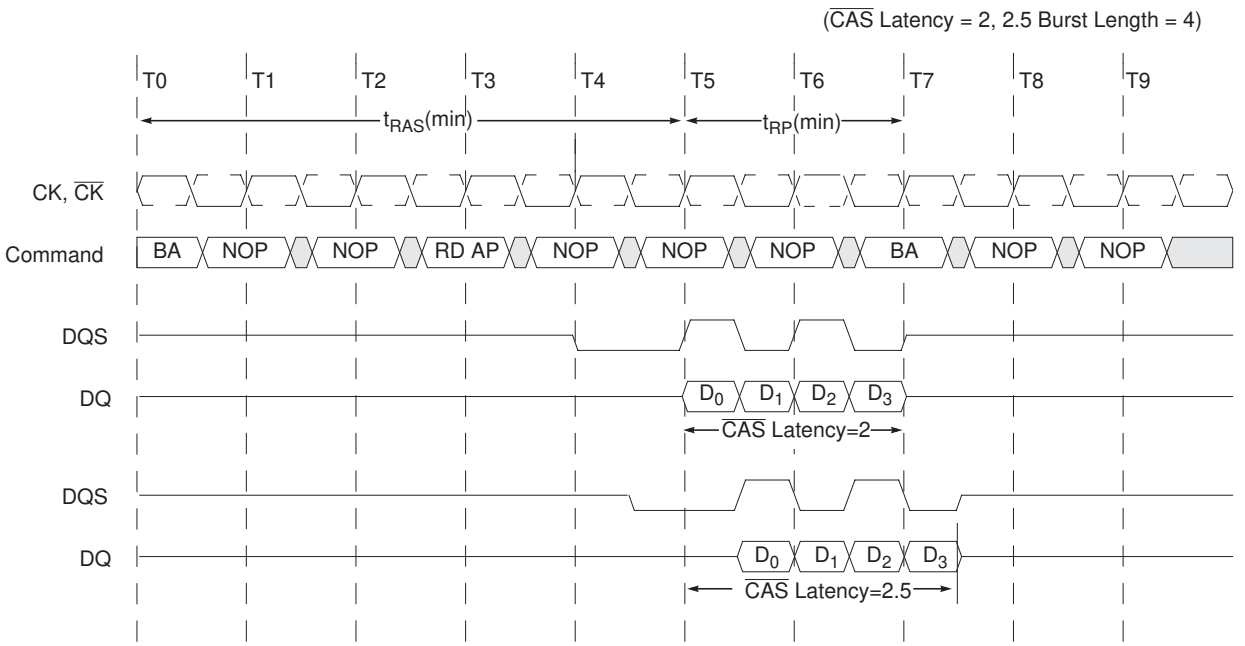
Read with Auto Precharge

If a Read with Auto Precharge command is initiated, the DDR SDRAM will enter the precharge operation N-clock cycles measured from the last data of the burst read cycle where N is equal to the $\overline{\text{CAS}}$ latency programmed into the device. Once the autoprecharge operation has begun, the bank cannot be reactivated until the minimum precharge time (t_{RP}) has been satisfied.

Read with Autoprecharge Timing



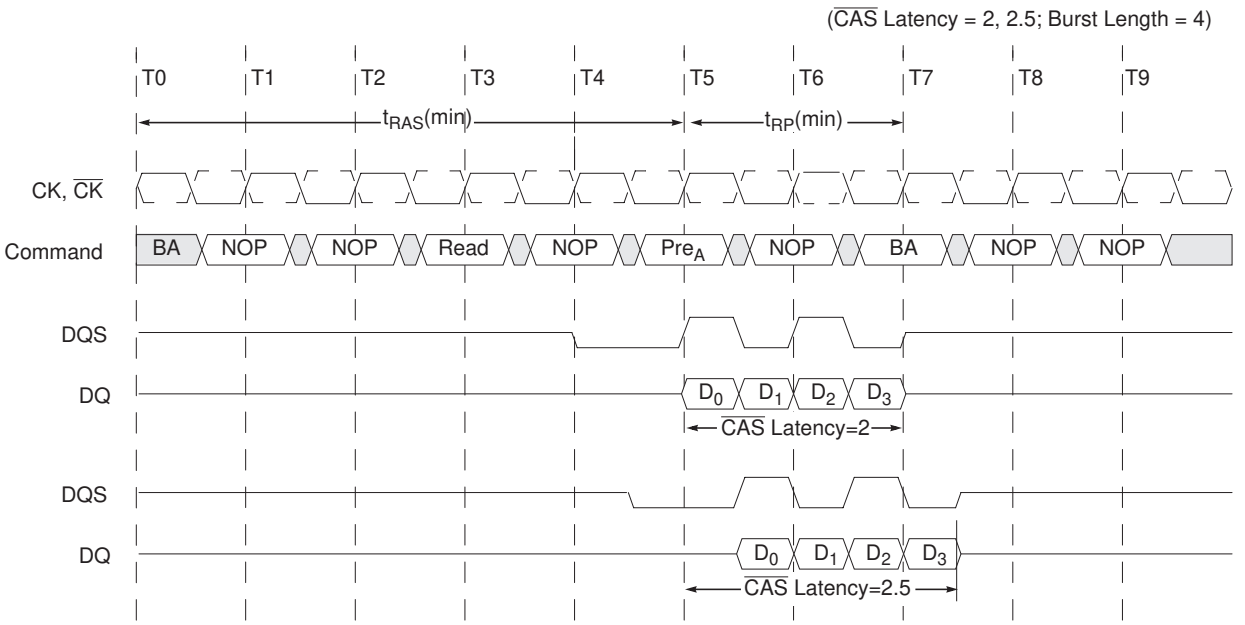
Read with Autoprecharge Timing as a Function of $\overline{CAS}$ Latency



Precharge Timing During Read Operation

For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be issued on the rising clock edge which is $\overline{\text{CAS}}$ latency (CL) clock cycles before the end of the Read burst. A new Bank Activate (BA) command may be issued to the same bank after the $\overline{\text{RAS}}$ precharge time (t_{RP}). A Precharge command can not be issued until t_{RAS}(min) is satisfied.

Read with Precharge Timing as a Function of $\overline{\text{CAS}}$ Latency

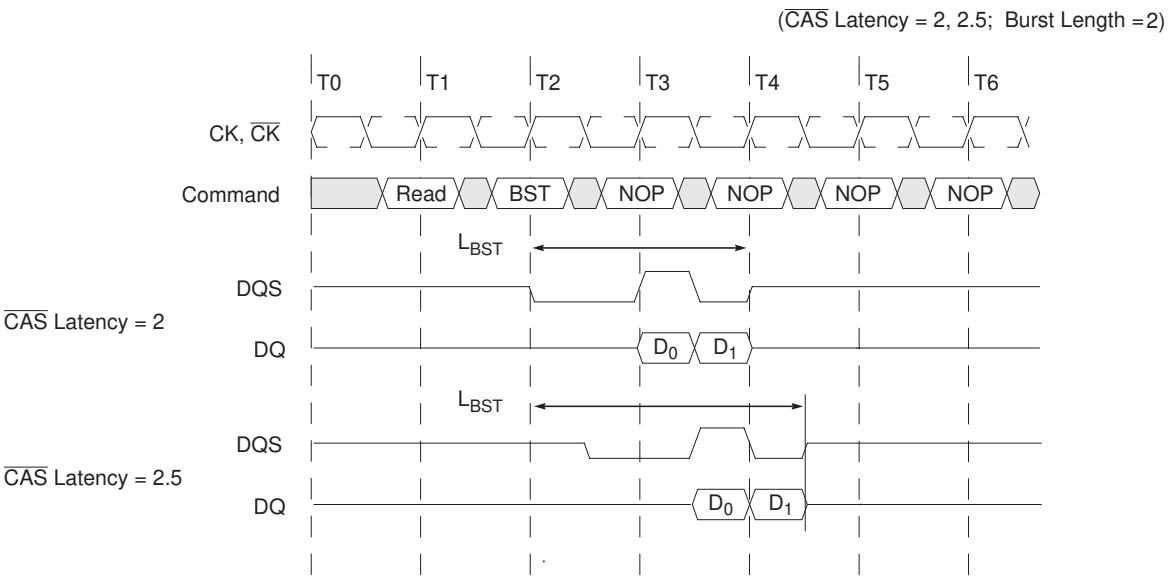


Burst Stop Command

The Burst Stop command is valid only during burst read cycles and is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock. When the Burst Stop command is issued during a burst Read cycle, both the output data (DQ) and data strobe (DQS) go to a high impedance state after a delay (L_{BST}) equal to the $\overline{CAS}$ latency programmed into the device. If the Burst Stop command is issued during a burst Write cycle, the command will be treated as a NOP command.

Read Terminated by Burst Stop Command Timing

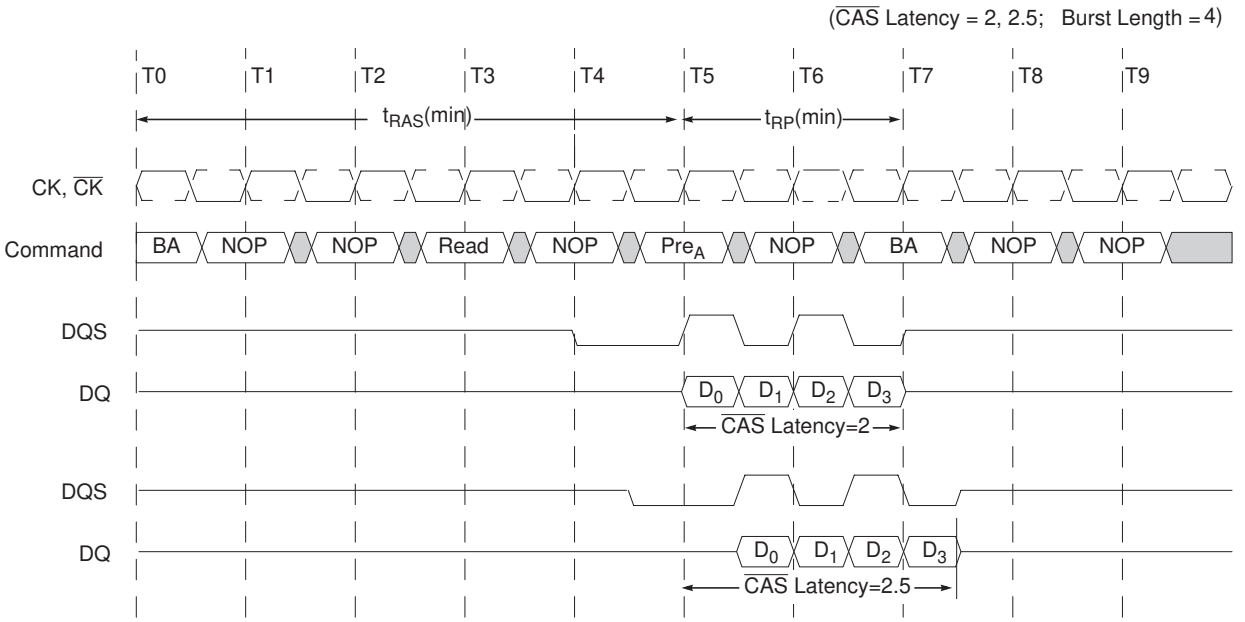
($\overline{CAS}$ Latency = 2, 2.5; Burst Length =2)



Read Interrupted by a Precharge

A Burst Read operation can be interrupted by a precharge of the same bank. The Precharge command to Output Disable latency is equivalent to the $\overline{CAS}$ latency.

Read Interrupted by a Precharge Timing



Burst Write Operation

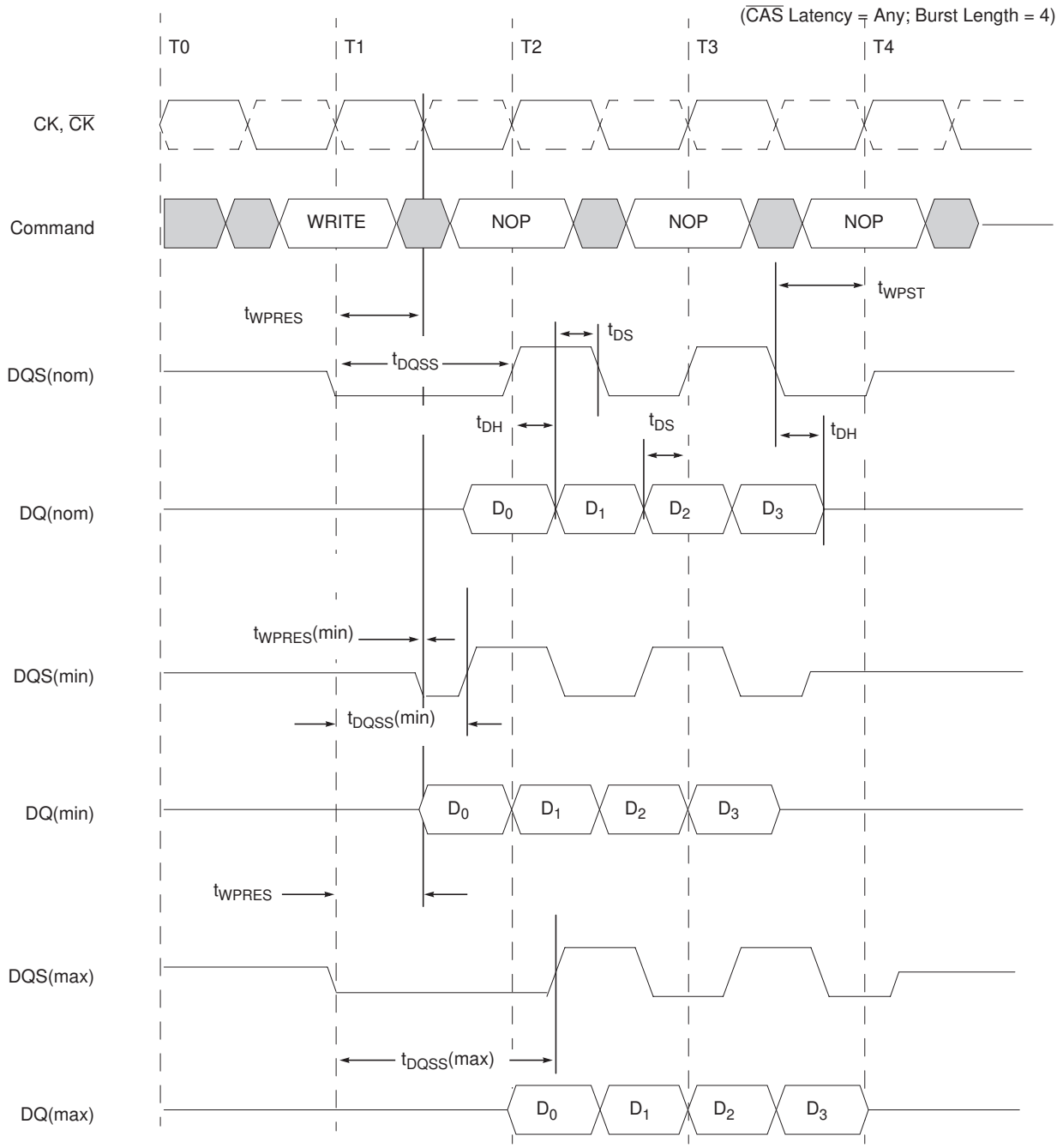
The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. The memory controller is required to provide an input data strobe (DQS) to the DDR SDRAM to strobe or latch the input data (DQ) and data mask (DM) into the device. During Write cycles, the data strobe applied to the DDR SDRAM is required to be nominally centered within the data (DQ) and data mask (DM) valid windows. The data strobe must be driven high nominally one clock after the write command has been registered. Timing parameters t_{DQSS}(min) and t_{DQSS}(max) define the allowable window when the data strobe must be driven high.

Input data for the first Burst Write cycle must be applied one clock cycle after the Write command is registered into the device (WL=1). The input data valid window is nominally centered around the midpoint of the data strobe signal. The data window is defined by DQ to DQS setup time (t_{QDQSS}) and DQ to DQS hold time (t_{QDQSH}). All data inputs must be supplied on each rising and falling edge of the data strobe until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

Write Preamble and Postamble Operation

Prior to a burst of write data and given that the controller is not currently in burst write mode, the data strobe signal (DQS), must transition from Hi-Z to a valid logic low. This is referred to as the data strobe “write preamble”. This transition from Hi-Z to logic low nominally happens on the falling edge of the clock after the write command has been registered by the device. The preamble is explicitly defined by a setup time (t_{WPRES}(min)) and hold time (t_{WPREH}(min)) referenced to the first falling edge of CK after the write command.

Burst Write Timing

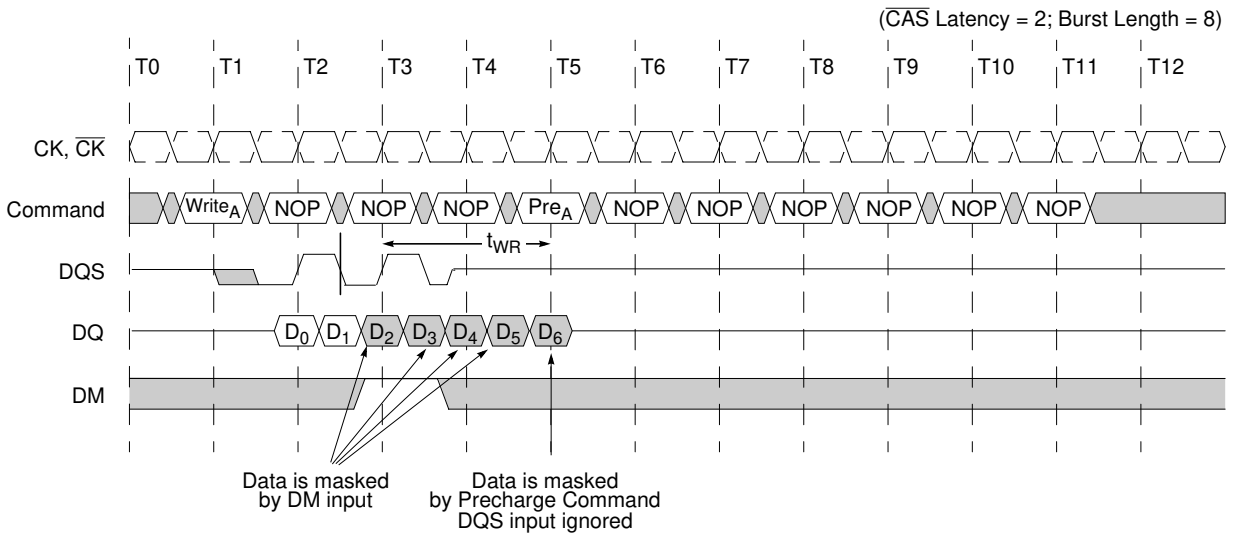


Once the burst of write data is concluded and given that no subsequent burst write operations are initiated, the data strobe signal (DQS) transitions from a logic low level back to Hi-Z. This is referred to as the data strobe “write postamble”. This transition happens nominally one-half clock period after the last data of the burst cycle is latched into the device.

Write Interrupted by a Precharge

A Burst Write can be interrupted before completion of the burst by a Precharge command, with the only restriction being that the interval that separates the commands be at least one clock cycle.

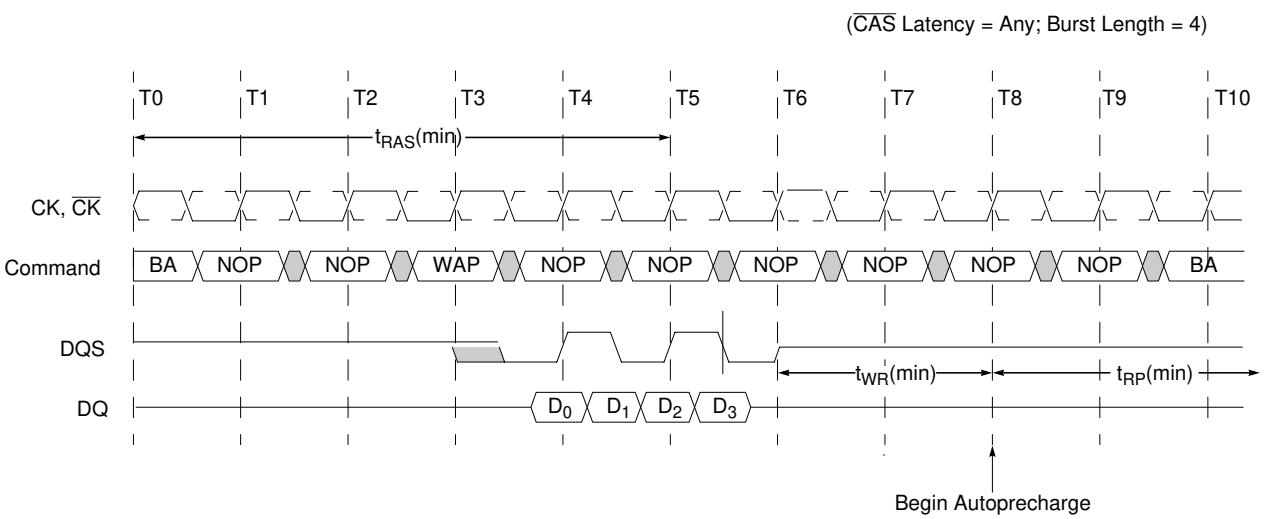
Write Interrupted by a Precharge Timing



Write with Auto Precharge

If A_{10} is high when a Write command is issued, the Write with auto Precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping t_{WR} (min.).

Write with Auto Precharge Timing



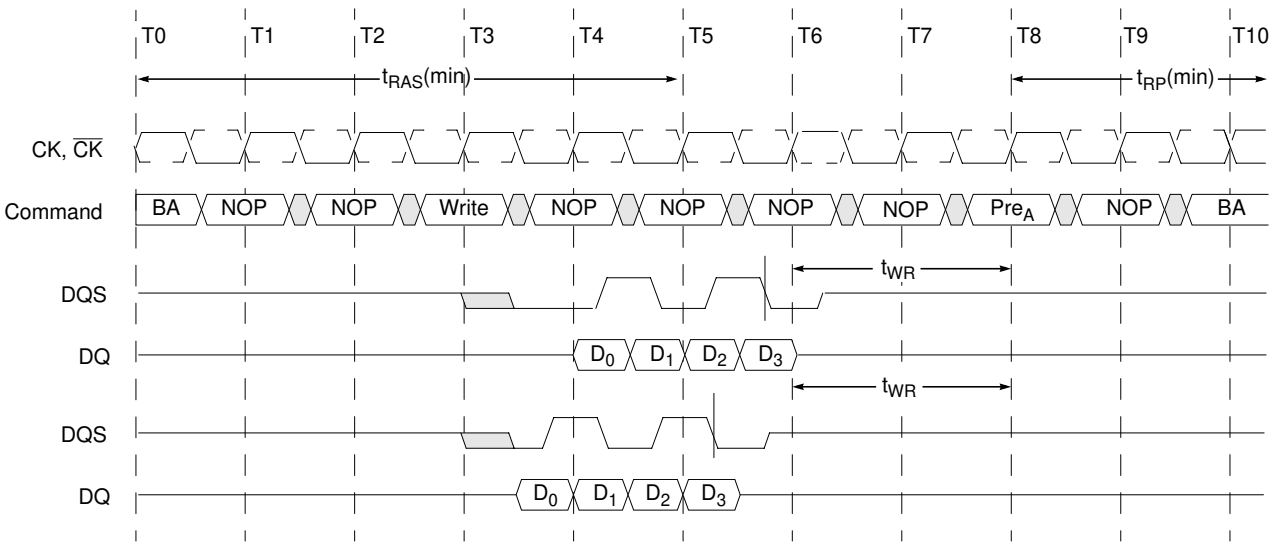
Precharge Timing During Write Operation

Precharge timing for Write operations in DRAMs requires enough time to satisfy the write recovery requirement. This is the time required by a DRAM sense amp to fully store the voltage level. For DDR SDRAMs, a timing parameter (t_{WR}) is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The “write recovery” operation begins on the rising clock edge after the last DQS edge that is used to strobe in the last valid write data. “Write recovery” is complete on the next 2nd rising clock edge that is used to strobe in the Precharge command.

Write with Precharge Timing

($\overline{CAS}$ Latency = Any; Burst Length = 4)

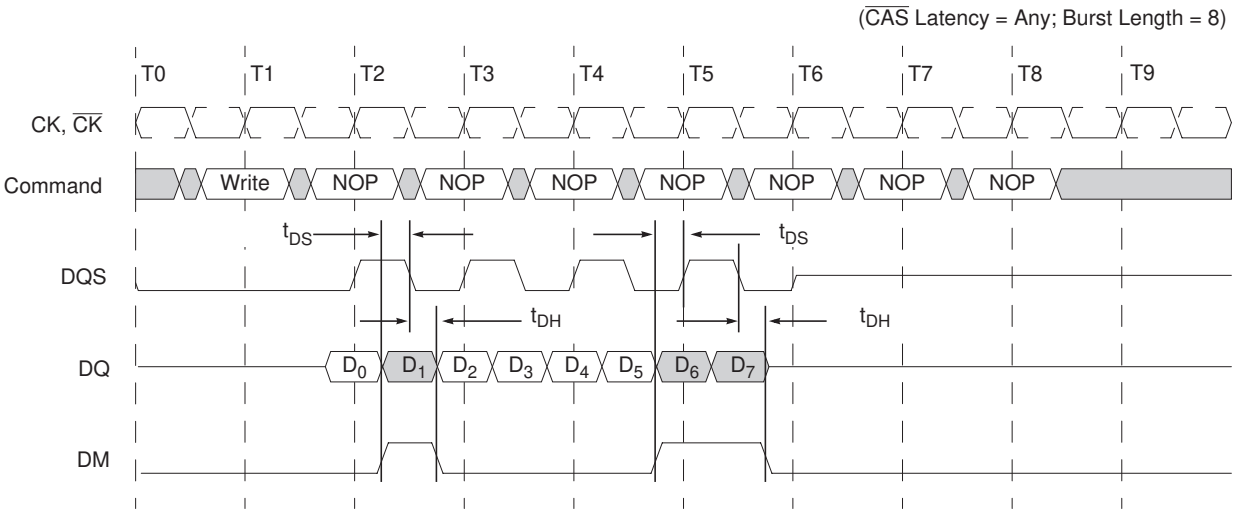


Data Mask Function

The DDR SDRAM has a Data Mask function that is used in conjunction with the Write cycle, but not the Read cycle. When the Data Mask is activated (DM high) during a Write operation, the Write is blocked (Mask to Data Latency = 0).

When issued, the Data Mask must be referenced to both the rising and falling edges of Data Strobe.

Data Mask Timing

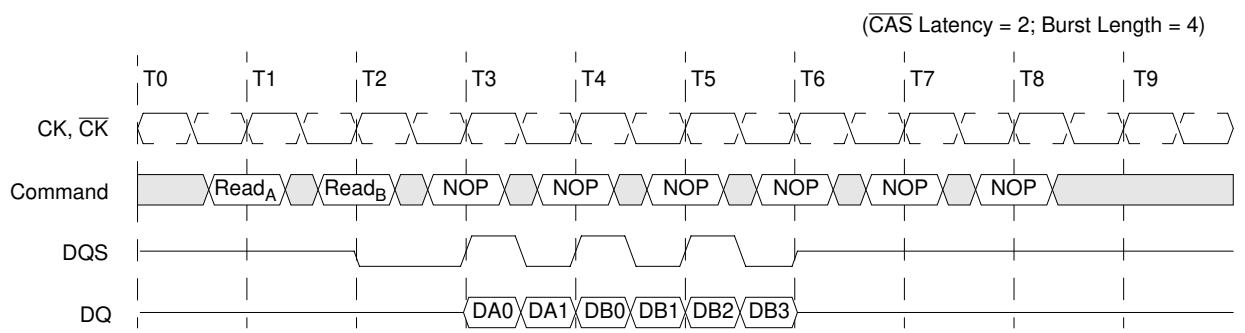


Burst Interruption

Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by issuing a new Read command to any bank. When the previous burst is interrupted, the remaining addresses are overridden with a full burst length starting with the new address. The data from the first Read command continues to appear on the outputs until the CAS latency from the interrupting Read command is satisfied. At this point, the data from the interrupting Read command appears on the bus. Read commands can be issued on each rising edge of the system clock. It is illegal to interrupt a Read with autoprecharge command with a Read command.

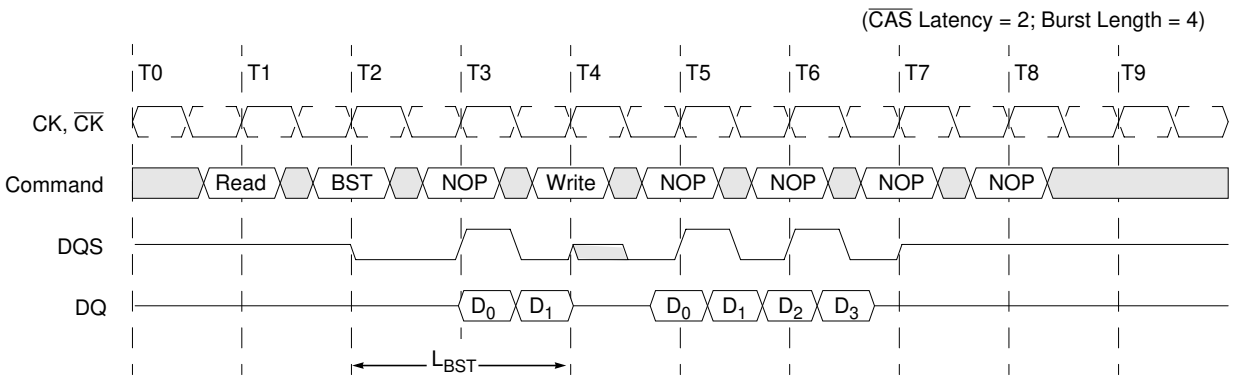
Read Interrupted by a Read Command Timing



Read Interrupted by a Write

To interrupt a Burst Read with a Write command, a Burst Stop command must be asserted to stop the burst read operation and 3-state the DQ bus. Additionally, control of the DQS bus must be turned around to allow the memory controller to drive the data strobe signal (DQS) into the DDR SDRAM for the write cycles. Once the Burst Stop command has been issued, a Write command can not be issued until a minimum delay or latency (L_{BST}) has been satisfied. This latency is measured from the Burst Stop command and is equivalent to the CAS latency programmed into the mode register. In instances where CAS latency is measured in half clock cycles, the minimum delay (L_{BST}) is rounded up to the next full clock cycle (i.e., if CL=2 then L_{BST}=2, if CL=2.5 then L_{BST}=3). It is illegal to interrupt a Read with autoprecharge command with a Write command.

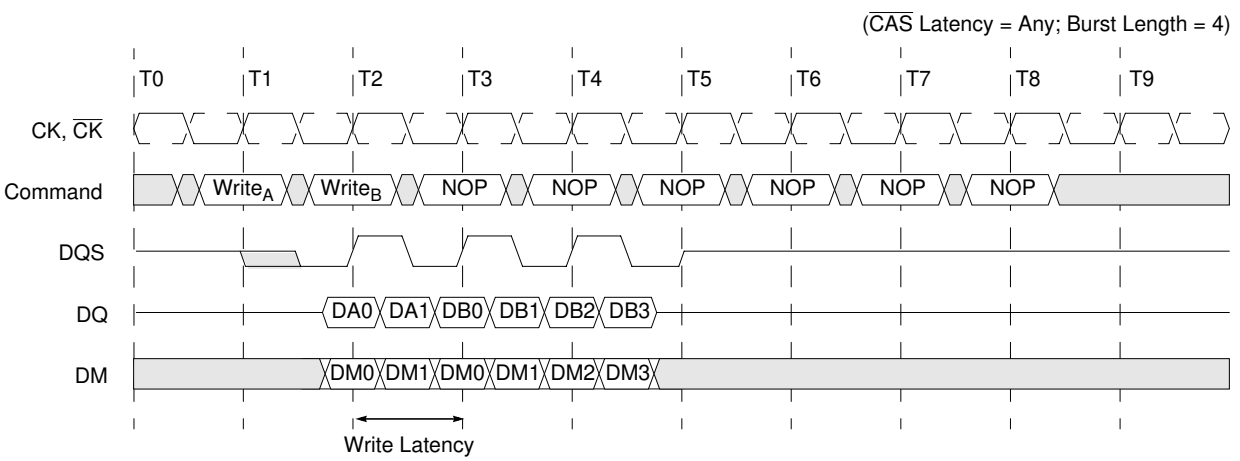
Read Interrupted by Burst Stop Command Followed by a Write Command Timing



Write Interrupted by a Write

A Burst Write can be interrupted before completion by a new Write command to any bank. When the previous burst is interrupted, the remaining addresses are overridden with a full burst length starting with the new address. The data from the first Write command continues to be input into the device until the Write Latency of the interrupting Write command is satisfied (WL=1) At this point, the data from the interrupting Write command is input into the device. Write commands can be issued on each rising edge of the system clock. It is illegal to interrupt a Write with autoprecharge command with a Write command.

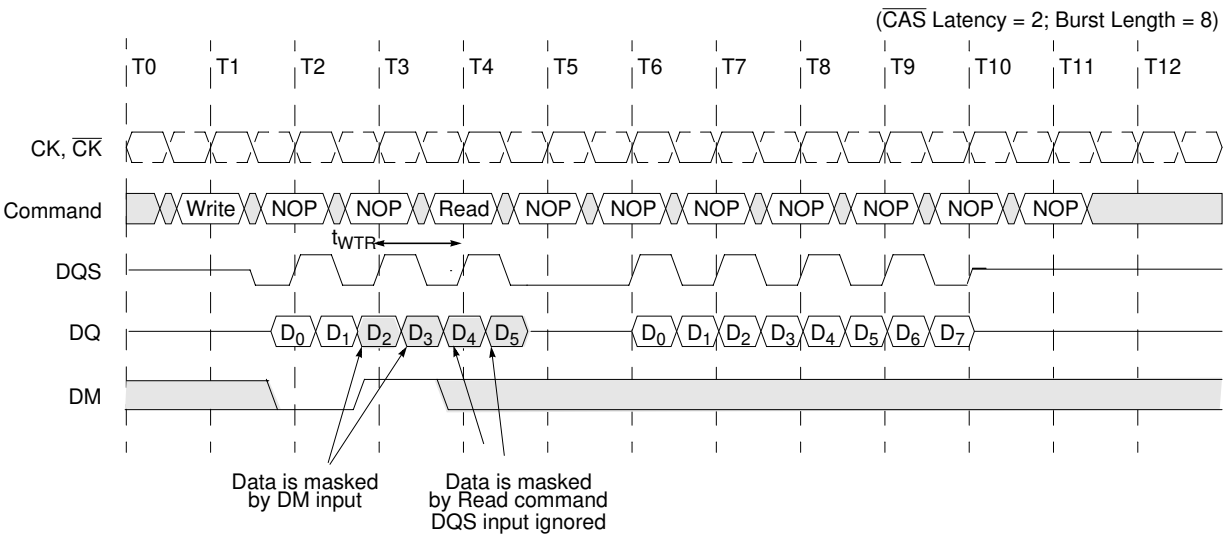
Write Interrupted by a Write Command Timing



Write Interrupted by a Read

A Burst Write can be interrupted by a Read command to any bank. If a burst write operation is interrupted prior to the end of the burst operation, then the last two pieces of input data prior to the Read command must be masked off with the data mask (DM) input pin to prevent invalid data from being written into the memory array. Any data that is present on the DQ pins coincident with or following the Read command will be masked off by the Read command and will not be written to the array. The memory controller must give up control of both the DQ bus and the DQS bus at least one clock cycle before the read data appears on the outputs in order to avoid contention. In order to avoid data contention within the device, a delay is required (t_{WTR}) from the first positive CK edge after the last desired data in the pair t_{WTR} before a Read command can be issued to the device. It is illegal to interrupt a Write with autoprecharge command with a Read command.

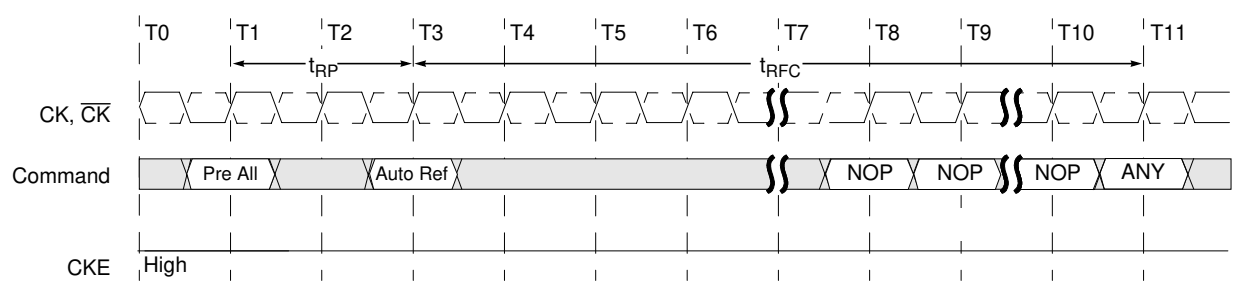
Write Interrupted by a Read Command Timing



Auto Refresh

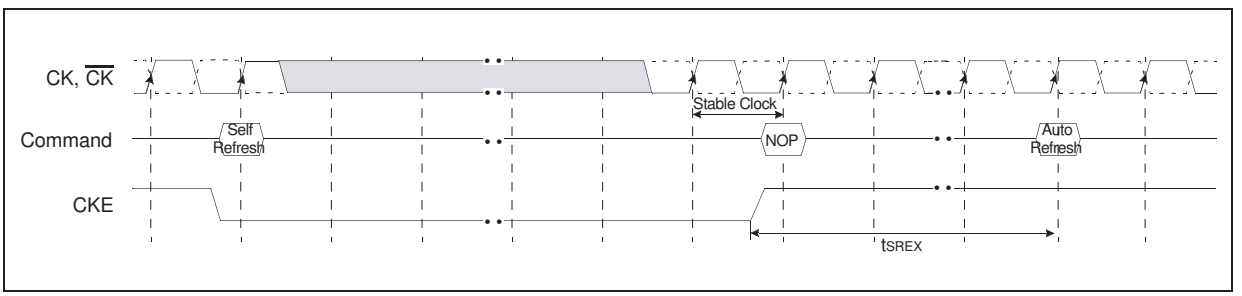
The Auto Refresh command is issued by having $\overline{CS}$, $\overline{RAS}$, and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock. All banks must be precharged and idle for a t_{RP}(min) before the Auto Refresh command is applied. No control of the address pins is required once this cycle has started because of the internal address counter. When the Auto Refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate command or subsequent Auto Refresh command must be greater than or equal to the t_{RFC}(min). Commands may not be issued to the device once an Auto Refresh cycle has begun. $\overline{CS}$ input must remain high during the refresh period or NOP commands must be registered on each rising edge of the CK input until the refresh period is satisfied.

Auto Refresh Timing



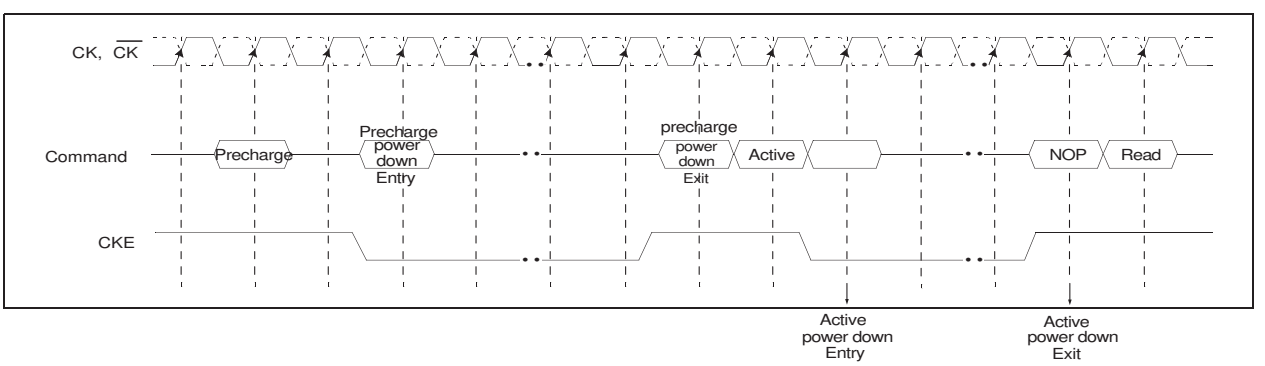
Self Refresh

A self refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock (CK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than t_{SREX} for locking of DLL. The auto refresh is required before self refresh entry and after self refresh exit.



Power Down Mode

The power down mode is entered when CKE is low and exited when CKE is high. Once the power down mode is initiated, all of the receiver circuits except clock, CKE and DLL circuit are gated off to reduce power consumption. All banks should be in idle state prior to entering the precharge power down mode and CKE should be set high at least 1tck+tIS prior to row active command. During power down mode, refresh operations cannot be performed, therefore the device cannot remain in power down mode longer than the refresh period (t_{REF}) of the device.



TRUTH TABLE 2 – CKE

(Notes: 1-4)

CKEn-1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	
		Self Refresh	DESELECT or NOP	Exit Self Refresh	5
H	L	All Banks Idle	DESELECT or NOP	Precharge Power-Down Entry	
		Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
		All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See Truth Table 3		

NOTE:

1. CKE_n is the logic state of CKE at clock edge *n*; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge *n*.
3. COMMANDn is the command registered at clock edge *n*, and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on any clock edges occurring during the ^{t}XSR period. A minimum of 200 clock cycles is needed before applying a read command, for the DLL to lock.

DDR SDRAM SIMPLIFIED COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	ADDR	A10/AP	BA	Note
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge									H		1,3,6
Write		H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge									H		1,4,6
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

1. LDM/UDM states are Don't Care. Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Register setting during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
4. If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tDPL+tRP). Last Data-In to Prechage delay(tDPL) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
5. If A10/AP is High when Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.
6. This device supports concurrent auto precharge such that when a READ with auto precharge is enabled or a WRITE with auto precharge is enabled any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).