Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Revision History
4Gb AS4C512M8D3A-12BCN - 78 ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	May. 2016

Alliance Memory Inc. 511 Taylor Way, San Carlos, CA 94070 TEL: (650) 610-6800 FAX: (650) 620-9211

512M x 8 bit DDR3 Synchronous DRAM (SDRAM)

Features

- JEDEC Standard Compliant
- Power supplies: V_{DD} & V_{DDQ} = +1.5V ± 0.075V
- Operating temperature: 0~95°C (TC)
- Supports JEDEC clock jitter specification
- Fully synchronous operation
- Fast clock rate: 800MHz
- Differential Clock, CK & CK#
- Bidirectional differential data strobe
  - DQS & DQS#
- 8 internal banks for concurrent operation
- 8n-bit prefetch architecture
- Pipelined internal architecture
- Precharge & active power down
- Programmable Mode & Extended Mode registers
- Additive Latency (AL): 0, CL-1, CL-2
- Programmable Burst lengths: 4, 8
- Burst type: Sequential / Interleave
- Output Driver Impedance Control
- 8192 refresh cycles / 64ms
  - Average refresh period
  7.8μs @ 0°C ≦TC≦ +85°C
  3.9μs @ +85°C ＜TC≦ +95°C
- Write Leveling
- ZQ Calibration
- Dynamic ODT (Rtt_Nom & Rtt_WR)
- RoHS compliant
- Auto Refresh and Self Refresh
- 78-ball 9 x 10.5 x 1.0mm FBGA package
  - Pb and Halogen Free

Overview

The 4Gb Double-Data-Rate-3 DRAMs is double data rate architecture to achieve high-speed operation. It is internally configured as an eight bank DRAM.
The 4Gb chip is organized as 64Mbit x 8 I/Os x 8 bank devices. These synchronous devices achieve high speed double-data-rate transfer rates of up to 1866 Mb/sec/pin for general applications.
The chip is designed to comply with all key DDR3 DRAM key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK# falling). All I/Os are synchronized with differential DQS pair in a source synchronous fashion.
These devices operate with a single 1.5V ± 0.075V power supply and are available in BGA packages.

Table 1. Ordering Information

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C512M8D3A-12BCN	512M x 8	Commercial 0°C to 95°C	800	78-ball FBGA

Table 2. Speed Grade Information

Speed Grade	Clock Frequency	CAS Latency	t_{RCD} (ns)	t_{RP} (ns)
DDR3-1600	800 MHz	11	13.75	13.75

Figure 1. Ball Assignment (FBGA Top View)

	1	2	3	…	7	8	9
A	VSS	VDD	NC		TDQS#	VSS	VDD
B	VSS	VSSQ	DQ0		DM/ TDQS	VSSQ	VDDQ
C	VDDQ	DQ2	DQS		DQ1	DQ3	VSSQ
D	VSSQ	DQ6	DQS#		VDD	VSS	VSSQ
E	VREFDQ	VDDQ	DQ4		DQ7	DQ5	VDDQ
F	NC	VSS	RAS#		CK	VSS	NC
G	ODT	VDD	CAS#		CK#	VDD	CKE
H	NC	CS#	WE#		A10/AP	ZQ	NC
J	VSS	BA0	BA2		A15	VREFCA	VSS
K	VDD	A3	A0		A12/BC#	BA1	VDD
L	VSS	A5	A2		A1	A4	VSS
M	VDD	A7	A9		A11	A6	VDD
N	VSS	RESET#	A13		A14	A8	VSS

Figure 2. Block Diagram

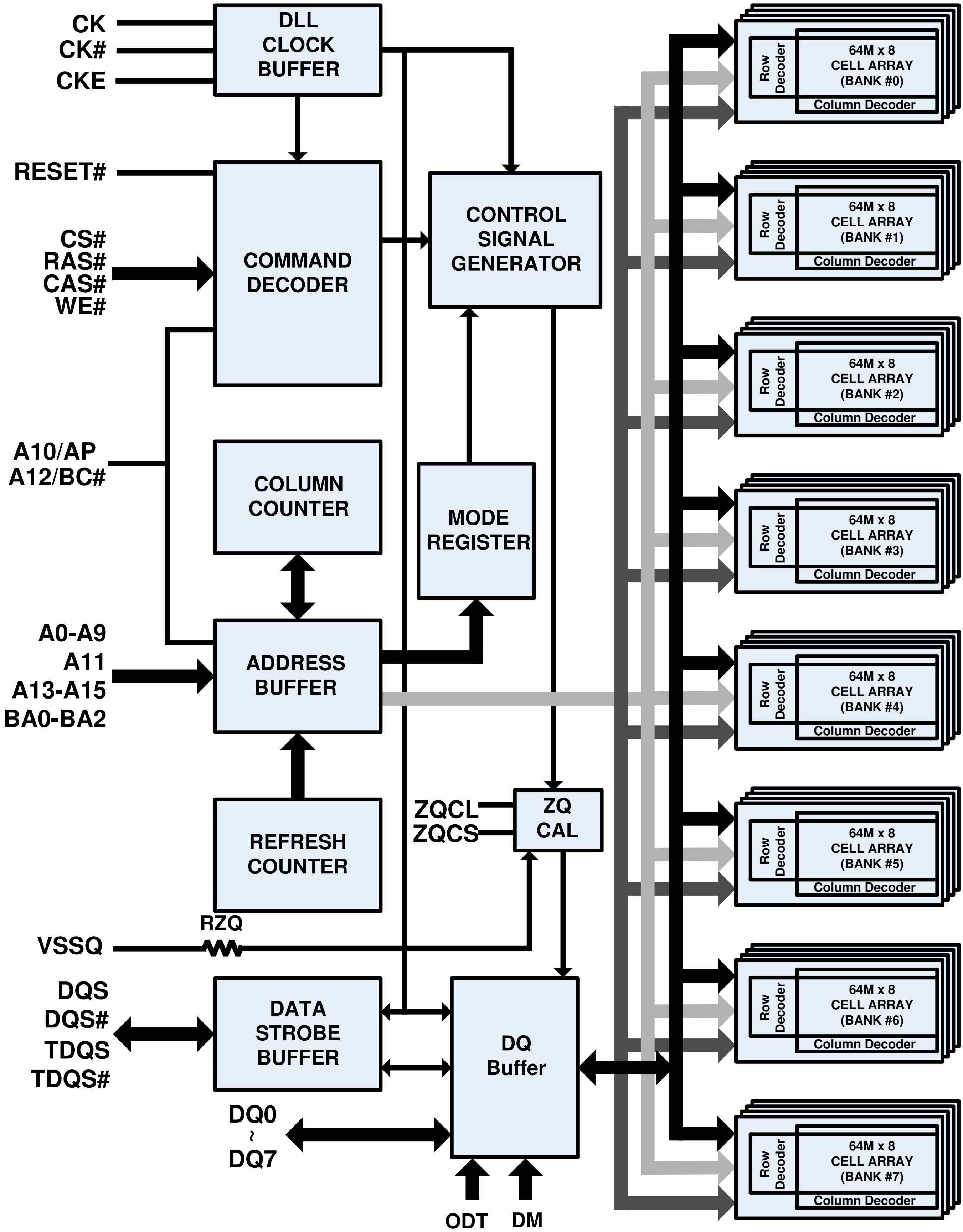
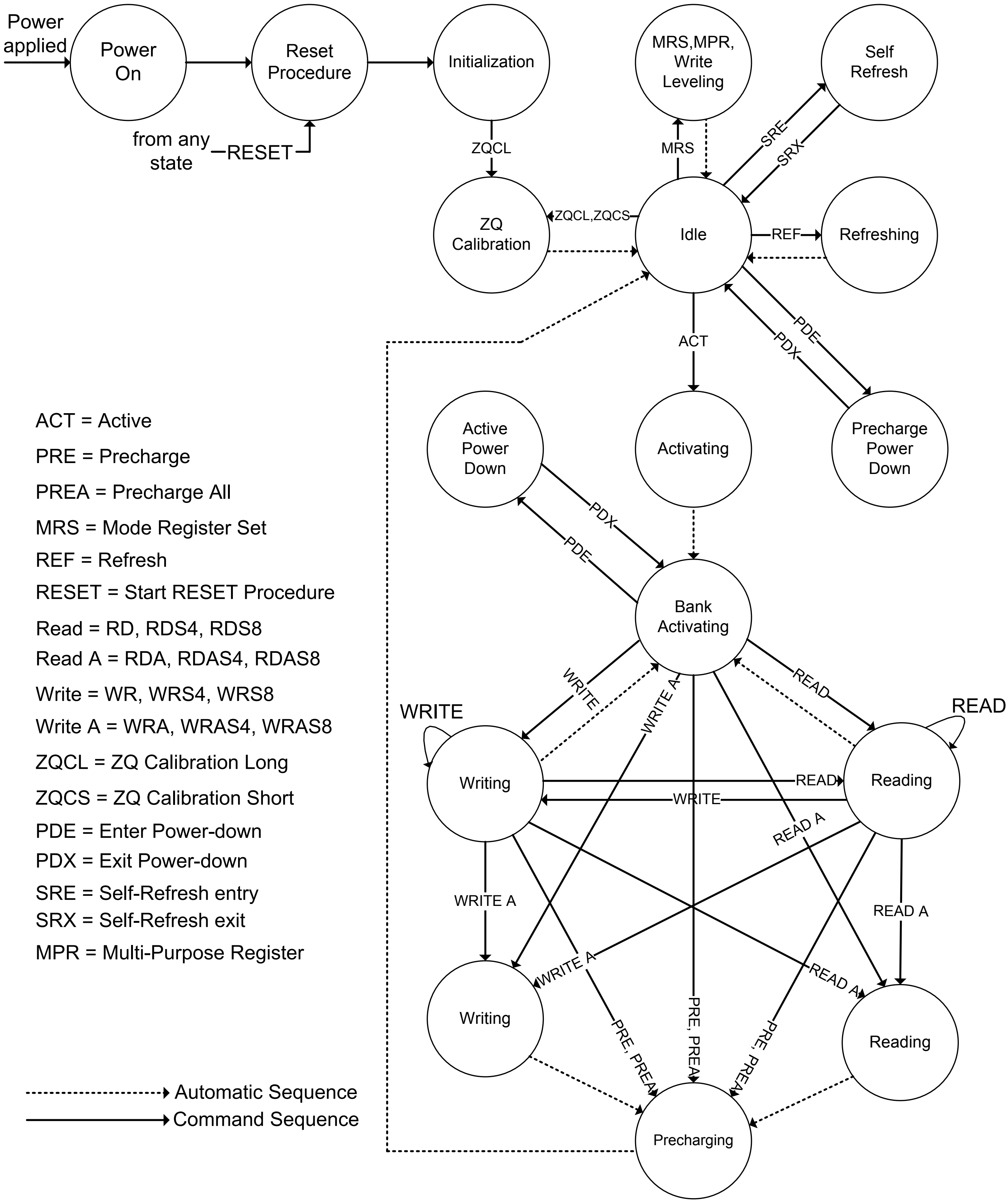


Figure 3. State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.



Ball Descriptions

Table 3. Ball Descriptions

Symbol	Type	Description
CK, CK#	Input	**Differential Clock:** CK and CK# are driven by the system clock. All SDRAM input signals are sampled on the crossing of positive edge of CK and negative edge of CK#. Output (Read) data is referenced to the crossings of CK and CK# (both directions of crossing).
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes LOW synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains LOW. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0-BA2	Input	**Bank Address:** BA0-BA2 define to which bank the BankActivate, Read, Write, or Bank Precharge command is being applied.
A0-A15	Input	**Address Inputs:** A0-A15 are sampled during the BankActivate command (row address A0-A15) and Read/Write command (column address A0-A9 with A10 defining Auto Precharge).
A10/AP	Input	**Auto-Precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH).
A12/BC#	Input	**Burst Chop:** A12/BC# is sampled during Read and Write commands to determine if burst chop (on the fly) will be performed. (HIGH - no burst chop; LOW - burst chopped).
CS#	Input	**Chip Select:** CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. It is considered part of the command code.
RAS#	Input	**Row Address Strobe:** The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
CAS#	Input	**Column Address Strobe:** The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# “HIGH " or “LOW".
WE#	Input	**Write Enable:** The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
DQS, DQS#	Input / Output	**Bidirectional Data Strobe:** Specifies timing for Input and Output data. Read Data Strobe is edge triggered. Write Data Strobe provides a setup and hold time for data and DM. The data strobes DOS is paired with DQS# to provide differential pair signaling to the system during both reads and writes.
TDQS TDQS#	Output	**Termination Data Strobe:** When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
DM	Input	**Data Input Mask:** Input data is masked when DM is sampled HIGH during a write cycle. DM has an optional use as TDQS on the x8.

DQ0 – DQ7	Input / Output	**Data I/O:** The DQ0-DQ7 input and output data are synchronized with positive and negative edges of DQS and DQS#. The I/Os are byte-maskable during Writes.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, DQS#, DM/TDQS and TDQS# signal. (When TDQS is enabled via Mode Register A11=1 in MR1) The ODT pin will be ignored if Mode-registers, MR1and MR2, are programmed to disable RTT.
RESET#	Input	**Active Low Asynchronous Reset:** Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD
V_{DD}	Supply	**Power Supply:** +1.5V ±0.075V
V_{SS}	Supply	**Ground**
V_{DDQ}	Supply	**DQ Power:** +1.5V ±0.075V.
V_{SSQ}	Supply	**DQ Ground**
V_{REFCA}	Supply	**Reference voltage for CA**
V_{REFDQ}	Supply	**Reference voltage for DQ**
ZQ	Supply	**Reference pin for ZQ calibration.**
NC	-	**No Connect:** These pins should be left unconnected.

Operation Mode Truth Table

Table 4. Truth Table (Note (1), (2))

Command	State	CKE_{n-1}(3)	CKE_n	DM	BA0-2	A10/AP	A0-9, 11, 13-15	A12/BC#	CS#	RAS#	CAS#	WE#
BankActivate	Idle(4)	H	H	X	V	Row address			L	L	H	H
Single Bank Precharge	Any	H	H	X	V	L	V	V	L	L	H	L
All Banks Precharge	Any	H	H	X	V	H	V	V	L	L	H	L
Write (Fixed BL8 or BC4)	Active(4)	H	H	X	V	L	V	V	L	H	L	L
Write (BC4, on the fly)	Active(4)	H	H	X	V	L	V	L	L	H	L	L
Write (BL8, on the fly)	Active(4)	H	H	X	V	L	V	H	L	H	L	L
Write with Autoprecharge (Fixed BL8 or BC4)	Active(4)	H	H	X	V	H	V	V	L	H	L	L
Write with Autoprecharge (BC4, on the fly)	Active(4)	H	H	X	V	H	V	L	L	H	L	L
Write with Autoprecharge (BL8, on the fly)	Active(4)	H	H	X	V	H	V	H	L	H	L	L
Read (Fixed BL8 or BC4)	Active(4)	H	H	X	V	L	V	V	L	H	L	H
Read (BC4, on the fly)	Active(4)	H	H	X	V	L	V	L	L	H	L	H
Read (BL8, on the fly)	Active(4)	H	H	X	V	L	V	H	L	H	L	H
Read with Autoprecharge (Fixed BL8 or BC4)	Active(4)	H	H	X	V	H	V	V	L	H	L	H
Read with Autoprecharge (BC4, on the fly)	Active(4)	H	H	X	V	H	V	L	L	H	L	H
Read with Autoprecharge (BL8, on the fly)	Active(4)	H	H	X	V	H	V	H	L	H	L	H
(Extended) Mode Register Set	Idle	H	H	X	V	OP code			L	L	L	L
No-Operation	Any	H	H	X	V	V	V	V	L	H	H	H
Device Deselect	Any	H	H	X	X	X	X	X	H	X	X	X
Refresh	Idle	H	H	X	V	V	V	V	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	V	V	V	V	L	L	L	H
SelfRefresh Exit	Idle	L	H	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H
Power Down Mode Entry	Idle	H	L	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H
Power Down Mode Exit	Any	L	H	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H
Data Input Mask Disable	Active	H	X	L	X	X	X	X	X	X	X	X
Data Input Mask Enable(5)	Active	H	X	H	X	X	X	X	X	X	X	X
ZQ Calibration Long	Idle	H	H	X	X	H	X	X	L	H	H	L
ZQ Calibration Short	Idle	H	H	X	X	L	X	X	L	H	H	L

NOTE 1: V=Valid data, X=Don't Care, L=Low level, H=High level
NOTE 2: CKEn signal is input level when commands are provided.
NOTE 3: CKEn-1 signal is input level one clock cycle before the commands are provided.
NOTE 4: These are states of bank designated by BA signal.
NOTE 5: DM can be enabled respectively.

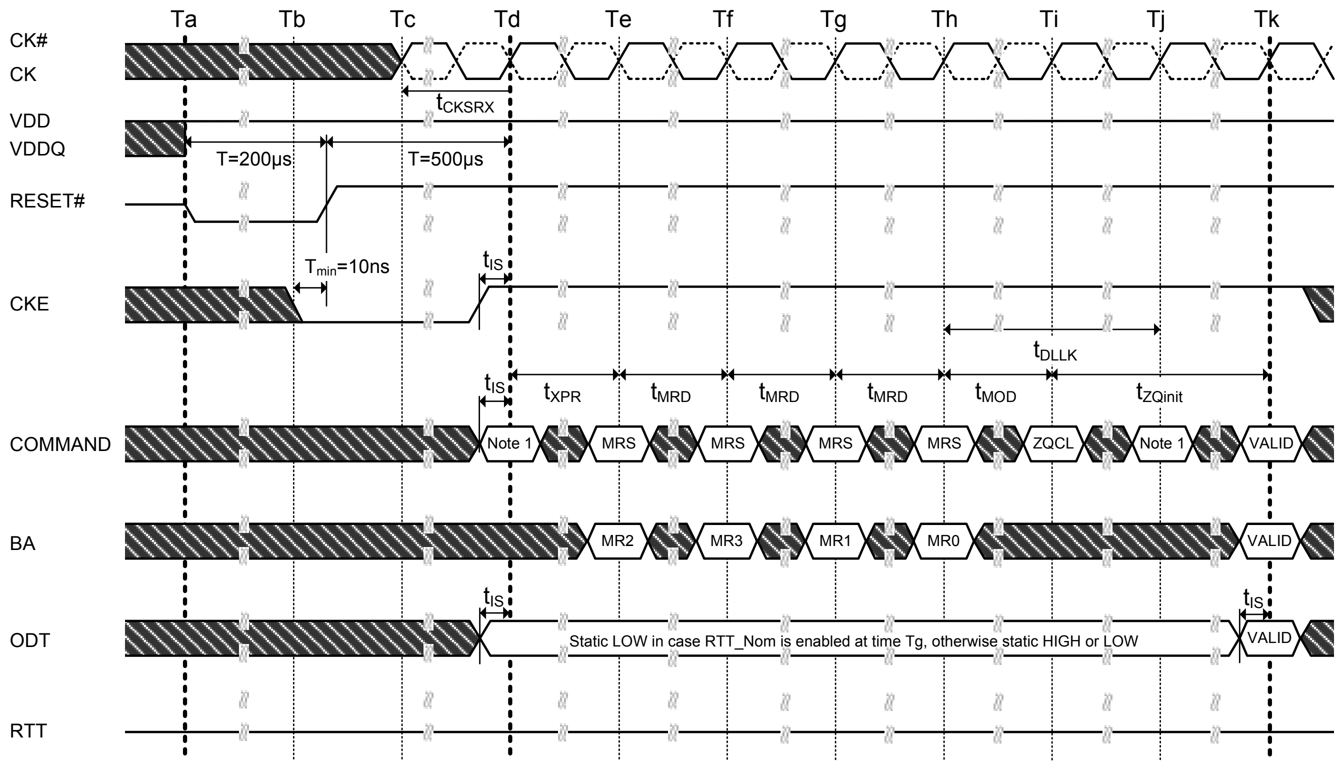
Functional Description

The DDR3 SDRAM is a high-speed dynamic random access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation. The 8n Prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A15 select the row). The address bit registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

Figure 4. Reset and Initialization Sequence at Power-on Ramping



NOTE 1. From time point Td until Tk NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK Don't Care

Power-up and Initialization

The Following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD, all other inputs may be undefined). RESET# needs to be maintained for minimum 200us with stable power. CKE is pulled “Low” anytime before RESET# being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDDmin must be no greater than 200ms; and during the ramp, VDD>VDDQ and (VDD-VDDQ) <0.3 Volts.
- VDD and VDDQ are driven from a single power converter output, AND
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished, AND
- Vref tracks VDDQ/2.

OR
- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After RESET# is de-asserted, wait for another 500us until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

3. Clock (CK, CK#) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be meeting. Also a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit.

4. The DDR3 DRAM will keep its on-die termination in high impedance state as long as RESET# is asserted. Further, the DRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register.(tXPR=max (tXS, 5tCK))

6. Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1)

7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1)

8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue “DLL Enable” command, provide “Low” to A0, “High” to BA0 and “Low” to BA1 and BA2)

9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command provide “High” to A8 and “Low” to BA0-BA2)

10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both tDLLK and tZQinit completed.

12. The DDR3 SDRAM is now ready for normal operation.

Reset Procedure at Stable Power

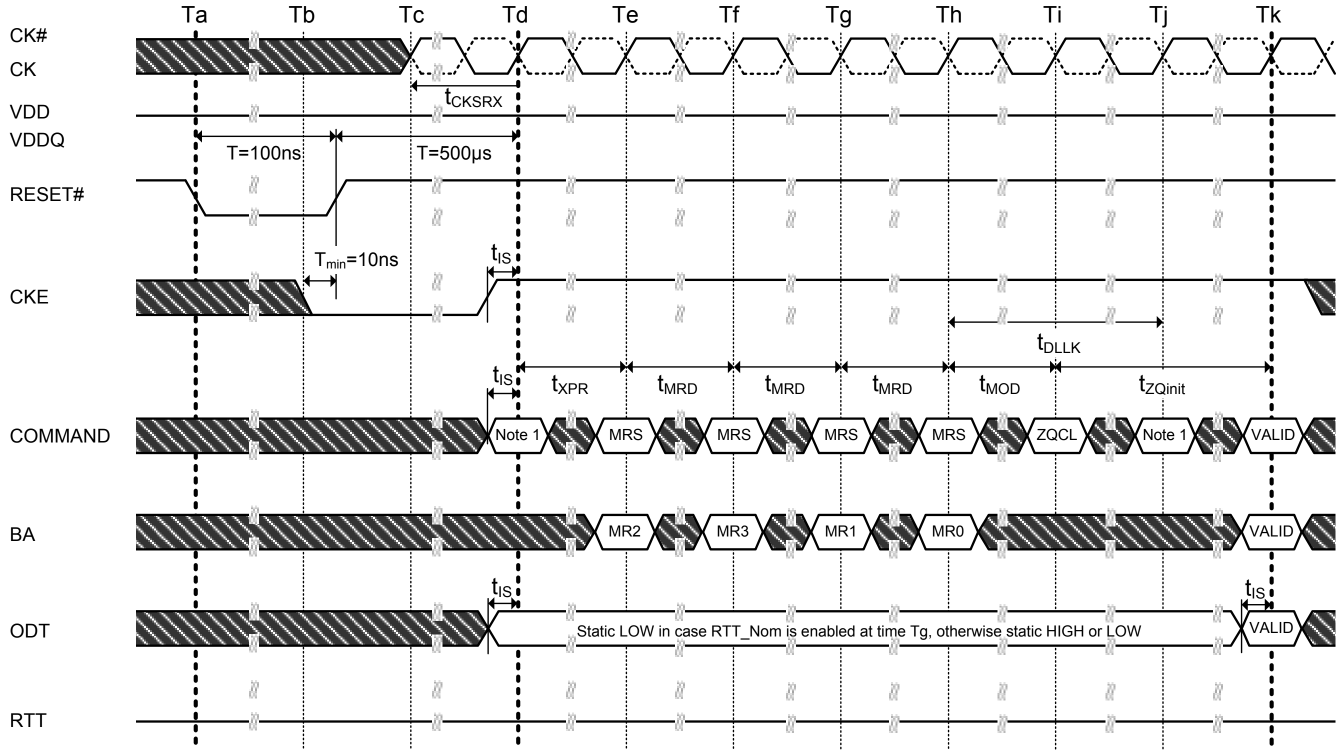
The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2*VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100ns. CKE is pulled "Low" before RESET being de-asserted (min. time 10ns).

2. Follow Power-up Initialization Sequence step 2 to 11.

3. The Reset sequence is now completed. DDR3 SDRAM is ready for normal operation.

Figure 5. Reset Procedure at Power Stable Condition



NOTE 1. From time point Td until Tk NOP or DES commands must be applied between MRS and ZQCL commands.

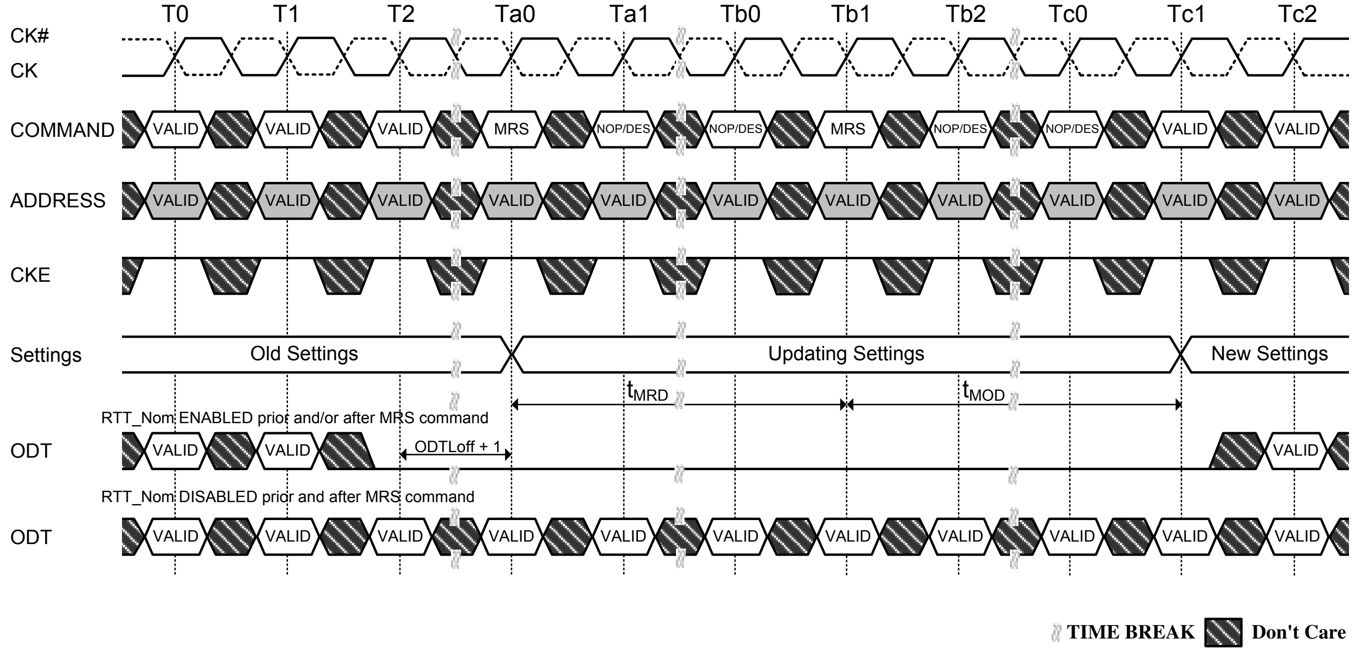
TIME BREAK Don't Care

Register Definition

● Programming the Mode Registers

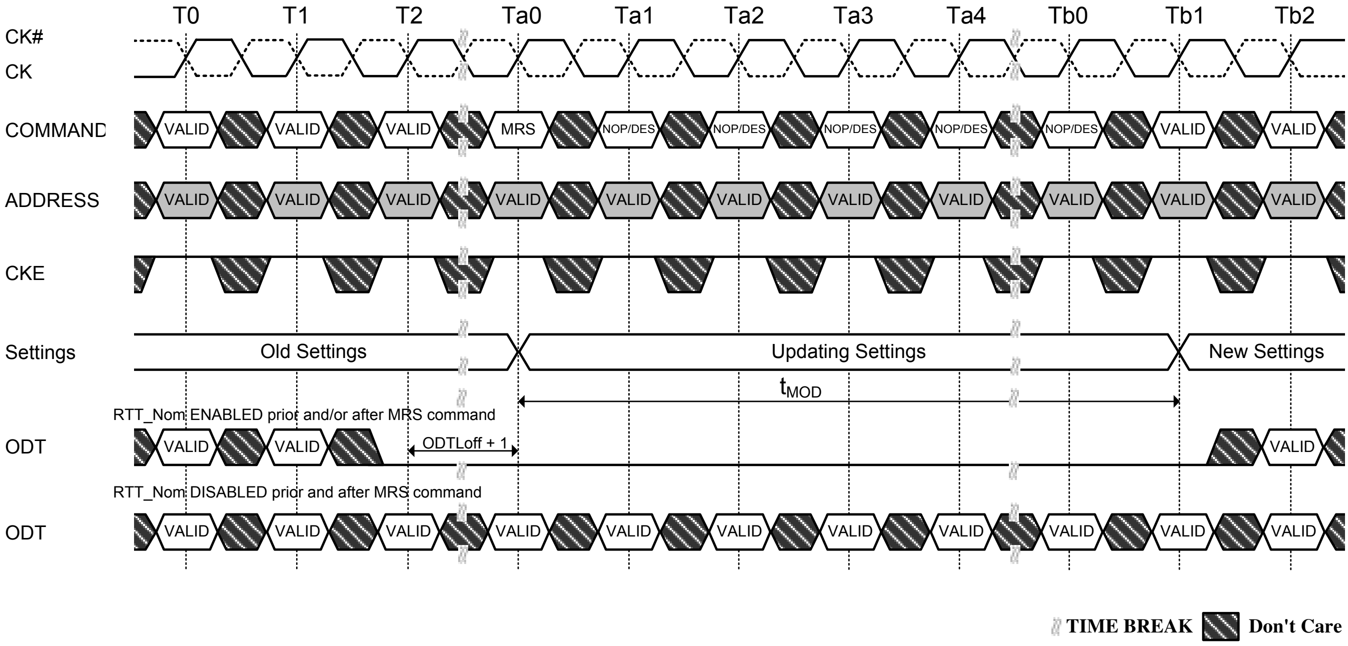
For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which mean these commands can be executed any time after power-up without affecting the array contents.
The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure of tMRD timing.

Figure 6. tMRD timing



The MRS command to Non-MRS command delay, tMOD, is require for the DRAM to update the features except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure of tMOD timing.

Figure 7. tMOD timing



The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

Mode Register MR0

The mode-register MR0 stores data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR, and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 DRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to the following figure.

Table 5. Mode Register Bitmap

Address Field	BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register (0)	0*1	0	0	0*1	0*1	0*1	PPD	WR			DLL	TM	CAS Latency			RBT	CL	BL	

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A7	Mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

A11	A10	A9	WR (cycles)
0	0	0	Reserved
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	14*2

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	Reserved
0	0	1	1	Reserved
0	1	0	1	Reserved
0	1	1	1	Reserved
1	0	0	1	Reserved
1	0	1	1	Reserved
1	1	0	1	Reserved
1	1	1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

A8	DLL Reset
0	No
1	Yes

Note 1: Reserved for future use and must be set to 0 when programming the MR.
Note 2: WR (write recovery for autoprecharge) min in clock cycles is calculated by dividing tWR (ns) by tCK (ns) and rounding up to the next integer WRmin [cycles] =Roundup (tWR / tCK). The value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

- Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in the MR0 Definition as above figure. The ordering of access within a burst is determined by the burst length, burst type, and the starting column address. The burst length is defined by bits A0-A1. Burst lengths options include fix BC4, fixed BL8, and on the fly which allow BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#

Table 6. Burst Type and Burst Order

Burst Length	Read Write	Starting Column Address			Sequential A3=0	Interleave A3=1	Note
		A2	A1	A0			
4 Chop	Read	0	0	0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	1, 2, 3
		0	0	1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	
		0	1	0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	
		0	1	1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	
		1	0	0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	
		1	0	1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	
		1	1	0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	
		1	1	1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	
	Write	0	V	V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 2, 4, 5
		1	V	V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	
8	Read	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2
		0	0	1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0	1	0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0	1	1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1	0	1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1	1	0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		1	1	1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
	Write	V	V	V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2, 4

Note 1: In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

Note 2: 0~7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

Note 3: T: Output driver for data and strobes are in high impedance.

Note 4: V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.

Note 5: X: Don't Care.

- CAS Latency

The CAS Latency is defined by MR0 (bit A2, A4~A6) as shown in the MR0 Definition figure. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

- Test Mode

The normal operating mode is selected by MR0 (bit7=0) and all other bits set to the desired values shown in the MR0 definition figure. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM manufacturer and should not be used. No operations or functionality is guaranteed if A7=1.

- DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Anytime the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations.)

- Write Recovery

The programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (ns) by tCK (ns) and rounding up to the next integer: WR min [cycles] = Roundup (tWR [ns]/tCK [ns]). The WR must be programmed to be equal or larger than tWR (min).

- Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12=0), or ‘slow-exit’, the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12=1), or ‘fast-exit’, the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

● Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output strength, Rtt_Nom impedance, additive latency, WRITE leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to the following figure.

Table 7. Extended Mode Register EMR (1) Bitmap

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0[*1]	0	1	0[*1]	0[*1]	0[*1]	Qoff	TDQS	0[*1]	Rtt_Nom	0[*1]	Level	Rtt_Nom	D.I.C	AL		Rtt_Nom	D.I.C	DLL	Mode Register (1)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL – 1
1	0	CL – 2
1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

A12	Qoff [*2]
0	Output buffer enabled
1	Output buffer disabled

A9	A6	A2	Rtt_Nom [*3]
0	0	0	Rtt_Nom disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12 [*4]
1	0	1	RZQ/8 [*4]
1	1	0	Reserved
1	1	1	Reserved

Note: RZQ = 240 Ω

A11	TDQS
0	Disable
1	Enable

A7	Write leveling enable
0	Disabled
1	Enabled

Note: RZQ = 240 Ω

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

Note 1: Reserved for future use and must be set to 0 when programming the MR.
Note 2: Outputs disabled - DQs, DQSs, DQS#s.
Note 3: In Write leveling Mode (MR1 [bit7] = 1) with MR1 [bit12] =1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1 [bit7] = 1) with MR1 [bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
Note 4: If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

- DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0=0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enable upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, expect when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation are described in DLL-off Mode. The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0, 0}, to disable Dynamic ODT externally

- Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bit A1 and A5) as shown in MR1 definition figure.

- ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmable in MR1. A separate value (Rtt_WR) may be programmable in MR2 to enable a unique Rtt value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

- Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidth in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in MR.

- Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the controller should support ‘write leveling’ in DDR3 SDRAM to compensate for skew.

- Output Disable

The DDR3 SDRAM outputs maybe enable/disabled by MR1 (bit 12) as shown in MR1 definition. When this feature is enabled (A12=1) all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring modules power for example. For normal operation A12 should be set to ‘0’.

- TDQS enable

TDQS (Termination Data Strobe) is a feature of DDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations. In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS. The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the TDQS# pin is not used. The TDQS function is available in X8 DDR3 SDRAM only

- ## Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

Table 8. Extended Mode Register EMR (2) Bitmap

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0*1	1	0	0*1					Rtt_WR		0*1	SRT	ASR	CWL			PASR			Mode Register (2)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A6	Auto Self-Refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable (Optional)

A10	A9	RTT_WR *2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A2	A1	A0	Partial Array Self-Refresh (Optional)
0	0	0	Full Array
0	0	1	HalfArray (BA[2:0]=000,001,010,&011)
0	1	0	Quarter Array (BA[2:0]=000,&001)
0	1	1	1/8th Array (BA[2:0]=000)
1	0	0	3/4 Array (BA[2:0]=010,011,100.101,110,&111)
1	0	1	HalfArray (BA[2:0]=100,101,110,&111)
1	1	0	Quarter Array (BA[2:0]=110,&111)
1	1	1	1/8th Array (BA[2:0]=111)

A7	Self-Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended (optional) operating temperature range

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK(avg) ≧ 2.5ns)
0	0	1	6 (2.5ns > tCK(avg) ≧ 1.875ns)
0	1	0	7 (1.875ns > tCK(avg) ≧ 1.5ns)
0	1	1	8 (1.5ns > tCK(avg) ≧ 1.25ns)
1	0	0	9 (1.25ns > tCK(avg) ≧ 1.07ns)
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Note 1: BA2 and A8, A11~ A15 are RFU and must be programmed to 0 during MRS.
Note 2: The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.
During write leveling, Dynamic ODT is not available.

- Partial Array Self-Refresh (PASR)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.
If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

- CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5) shown in MR2. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 DRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL=AL+CWL.
For more information on the supported CWL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins". For detailed Write operation refer to "WRITE Operation".

- Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

DDR3 SDRAM must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the ASR function or program the SRT bit appropriately.
Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. For more details refer to "Extended Temperature Usage". DDR3 SDRAMs must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

- Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings.
DDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to "Dynamic ODT".

Mode Register MR3

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below

Table 9. Extended Mode Register EMR (3) Bitmap

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0 *1	1	1	0 *1													MPR	MPR Loc		Mode Register (3)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A2	MPR
0	Normal operation *3
1	Dataflow from MPR

A1	A0	MPR location
0	0	Predefined pattern *2
0	1	RFU
1	0	RFU
1	1	RFU

Note 1: BA2, A3 - A15 are RFU and must be programmed to 0 during MRS.
Note 2: The predefined pattern will be used for read synchronization.
Note 3: When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.

Table 10. Absolute Maximum DC Ratings

Symbol	Parameter	Values	Unit	Note
V_{DD}	Voltage on VDD pin relative to Vss	-0.4 ~ 1.8	V	1,3
V_{DDQ}	Voltage on VDDQ pin relative to Vss	-0.4 ~ 1.8	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.4 ~ 1.8	V	1
T_{STG}	Storage temperature	-55~100	°C	1,2

NOTE1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
NOTE2: Storage Temperature is the case surface temperature on the center/top side of the DRAM.
NOTE3: VDD and VDDQ must be within 300mV of each other at all times; and Vref must be not greater than 0.6VDDQ, when VDD and VDDQ are less than 500mV; Vref may be equal to or less than 300mV.

Table 11. Temperature Range

Symbol	Parameter	Values	Unit	Note
T_{OPER}	Operating case temperature Range	0~85	°C	1,2
	Extended Temperature Range	85~95	°C	1,3

NOTE1: Operating temperature is the case surface temperature on center/top of the DRAM.
NOTE2: The operating temperature range is the temperature where all DRAM specification will be supported. Outside of this temperature range, even if it is still within the limit of stress condition, some deviation on portion of operating specification may be required. During operation, the DRAM case temperature must be maintained between 0-85°C under all other specification parameter. Supporting 0 - 85 °C with full JEDEC AC & DC specifications.
NOTE3: Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are guaranteed in this range, but the following additional apply.
a) Refresh commands must be doubled in frequency, therefore, reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1x refresh (tREFI to 7.8us) in the Extended Temperature Range.
b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0 and MR2 A7=1) or enable the optional Auto Self-Refresh mode (MR2 A6=1 and MR2 A7=0).

Table 12. Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{DD}	Power supply voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Power supply voltage for output	1.425	1.5	1.575	V	1,2

NOTE1: Under all conditions VDDQ must be less than or equal to VDD.
NOTE2: VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Table 13. Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	-12		Unit	Note
		Min.	Max.		
V_{IH}.CA(DC100)	DC input logic high	V_{REF}+0.1	V_{DD}	V	1,5
V_{IL}.CA(DC100)	DC input logic low	V_{SS}	V_{REF}-0.1	V	1,6
V_{IH}.CA(AC175)	AC input logic high	V_{REF}+0.175	-	V	1,2
V_{IL}.CA(AC175)	AC input logic low	-	V_{REF}-0.175	V	1,2
V_{IH}.CA(AC150)	AC input logic high	V_{REF}+0.15	-	V	1,2
V_{IL}.CA(AC150)	AC input logic low	-	V_{REF}-0.15	V	1,2
V_{IH}.CA(AC135)	AC input logic high	-	-	V	1,2
V_{IL}.CA(AC135)	AC input logic low	-	-	V	1,2
V_{RefCA}(DC)	Reference Voltage for ADD, CMD inputs	0.49xV_{DD}	0.51xV_{DD}	V	3,4

NOTE 1: For input only pins except RESET#. Vref = VrefCA(DC).
NOTE 2: See "Overshoot and Undershoot Specifications".
NOTE 3: The ac peak noise on VRef may not allow VRef to deviate from VRefCA(DC) by more than +/-1% VDD.
NOTE 4: For reference: approx. VDD/2 +/- 15 mV.
NOTE 5: VIH(dc) is used as a simplified symbol for VIH.CA(DC100)
NOTE 6: VIL(dc) is used as a simplified symbol for VIL.CA(DC100)
NOTE 7: VIH(ac) is used as a simplified symbol for VIH.CA(AC175), VIH.CA(AC150), VIH.CA(AC135) and VIH.CA(AC175) value is used when Vref + 0.175V is referenced, VIH.CA(AC150) value is used when Vref + 0.150V is referenced, VIH.CA(AC135) value is used when Vref + 0.135V is referenced.
NOTE 8: VIL(ac) is used as a simplified symbol for VIL.CA(AC175), VIL.CA(AC150), VIL.CA(AC135) and VIL.CA(AC175) value is used when Vref - 0.175V is referenced, VIL.CA(AC150) value is used when Vref - 0.150V is referenced, VIL.CA(AC135) value is used when Vref - 0.135V is referenced.

Table 14. Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	-12		Unit	Note
		Min.	Max.		
V_{IH}.DQ(DC100)	DC input logic high	V_{REF}+0.1	V_{DD}	V	1,5
V_{IL}.DQ(DC100)	DC input logic low	V_{SS}	V_{REF}-0.1	V	1,6
V_{IH}.DQ(AC150)	AC input logic high	V_{REF}+0.15	-	V	1,2
V_{IL}.DQ(AC150)	AC input logic low	-	V_{REF}-0.15	V	1,2
V_{IH}.DQ(AC135)	AC input logic high	-	-	V	1,2
V_{IL}.DQ(AC135)	AC input logic low	-	-	V	1,2
V_{RefDQ}(DC)	Reference Voltage for DQ, DM inputs	0.49xV_{DD}	0.51xV_{DD}	V	3,4

NOTE 1: Vref = VrefDQ(DC).
NOTE 2: See "Overshoot and Undershoot Specifications".
NOTE 3: The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD.
NOTE 4: For reference: approx. VDD/2 +/- 15 mV.
NOTE 5: VIH(dc) is used as a simplified symbol for VIH.DQ(DC100)
NOTE 6: VIL(dc) is used as a simplified symbol for VIL.DQ(DC100)
NOTE 7: VIH(ac) is used as a simplified symbol for VIH.DQ(AC150), VIH.DQ(AC135) and VIH.DQ(AC150) value is used when Vref + 0.150V is referenced, VIH.DQ(AC135) value is used when Vref + 0.135V is referenced.
NOTE 8: VIL(ac) is used as a simplified symbol for VIL.DQ(AC150), VIL.DQ(AC135) and VIL.DQ(AC150) value is used when Vref - 0.150V is referenced, VIL.DQ(AC135) value is used when Vref - 0.135V is referenced.

Table 15. Differential AC and DC Input Levels

Symbol	Parameter	Min.	Max.	Unit	Note
$V_{IH}diff$	Differential input high	0.2	-	V	1, 3
$V_{IL}diff$	Differential input logic low	-	- 0.2	V	1, 3
$V_{IH}diff(AC)$	Differential input high ac	2 x ($V_{IH}(AC)$ - V_{REF})	-	V	2, 3
$V_{IL}diff(AC)$	Differential input low ac	-	2 x ($V_{IL}(AC)$ - V_{REF})	V	2, 3

NOTE 1: Used to define a differential signal slew-rate.
NOTE 2: For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS, DQS# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
NOTE 3: These values are not defined; however, the single-ended signals CK, CK#, DQS, DQS# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Table 16. Capacitance (V_{DD} = 1.5V, f = 1MHz, T_{OPER} = 25 °C)

Symbol	Parameter	-12		Unit	Note
		Min.	Max.		
C_{IO}	Input/output capacitance, (DQ, DM, DQS, DQS#, TDQS, TDQS#)	1.4	2.3	pF	1, 2, 3
C_{CK}	Input capacitance, CK and CK#	0.8	1.4	pF	2, 3
C_{DCK}	Input capacitance delta, CK and CK#	0	0.15	pF	2, 3, 4
C_{DDQS}	Input/output capacitance delta, DQS and DQS#	0	0.15	pF	2, 3, 5
C_{I}	Input capacitance, (CTRL, ADD, CMD input-only pins)	0.75	1.3	pF	2, 3, 6
C_{DI_CTRL}	Input capacitance delta, (All CTRL input-only pins)	-0.4	0.2	pF	2, 3, 7, 8
$C_{DI\_ADD\_CMD}$	Input capacitance delta, (All ADD, CMD input-only pins)	-0.4	0.4	pF	2, 3, 9, 10
C_{DIO}	Input/output capacitance delta, (DQ, DM, DQS, DQS#, TDQS, TDQS#)	-0.5	0.3	pF	2, 3, 11
C_{ZQ}	Input/output capacitance of ZQ pin	-	3	pF	2, 3, 12

NOTE 1: Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS.
NOTE 2: This parameter is not subject to production test. It is verified by design and characterization. VDD=VDDQ=1.5V, VBIAS=VDD/2 and ondie termination off.
NOTE 3: This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
NOTE 4: Absolute value of CCK-CCK#.
NOTE 5: Absolute value of CIO(DQS)-CIO(DQS#).
NOTE 6: CI applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.
NOTE 7: CDI_CTRL applies to ODT, CS# and CKE.
NOTE 8: CDI_CTRL=CI(CTRL)-0.5*(CI(CK)+CI(CK#)).
NOTE 9: CDI_ADD_CMD applies to A0-A12, BA0-BA2, RAS#, CAS# and WE#.
NOTE 10: CDI_ADD_CMD=CI(ADD_CMD) - 0.5*(CI(CK)+CI(CK#)).
NOTE 11: CDIO=CIO(DQ,DM) - 0.5*(CIO(DQS)+CIO(DQS#)).
NOTE 12: Maximum external load capacitance on ZQ pin: 5 pF.

Table 17. IDD specification parameters and test conditions (V_{DD} = 1.5V ± 0.075V, T_{OPER} = 0~85 °C)

Parameter & Test Condition	Symbol	-12 Max.	Unit
Operating One Bank Active-Precharge Current **CKE:** High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: High between ACT and PRE; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,...;**Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD0}	54	mA
Operating One Bank Active-Read-Precharge Current **CKE:** High; **External clock:** On; **BL:** 8[*1, 7]; **AL:**0; **CS#**: High between ACT, RD and PRE; **Command, Address, Bank Address Inputs, Data IO:** partially toggling; **DM**:stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,...; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD1}	61	mA
Precharge Standby Current **CKE**: High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD2N}	30	mA
Precharge Power-Down Current Slow Exit **CKE:** Low; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0; **Pecharge Power Down Mode**: Slow Exit.[*3]	I_{DD2P0}	17	mA
Precharge Power-Down Current Fast Exit **CKE:** Low; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0; **Pecharge Power Down Mode**: Fast Exit.[*3]	I_{DD2P1}	25	mA
Precharge Quiet Standby Current **CKE**: High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD2Q}	30	mA
Active Standby Current **CKE**: High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD3N}	55	mA
Active Power-Down Current **CKE:** Low; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0	I_{DD3P}	34	mA
Operating Burst Read Current **CKE:** High; **External clock:** On; **BL:** 8[*1, 7]; **AL:** 0; **CS#**: High between RD; **Command, Address, Bank Address Inputs:** partially toggling; **DM**:stable at 0; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; **tput Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at 0.	I_{DD4R}	133	mA
Operating Burst Write Current **CKE:** High; **External clock:** On; **BL:** 8[*1]; **AL:** 0; **CS#**: High between WR; **Command, Address, Bank Address Inputs:** partially toggling; **DM:** stable at 0; **Bank Activity:** all banks open. **Output Buffer and RTT:** Enabled in Mode Registers[*2]; **ODT Signal:** stable at HIGH.	I_{DD4W}	120	mA

Burst Refresh Current **CKE:** High; **External clock:** On; **BL:** 8*1; **AL:** 0; **CS#**: High between tREF; **Command, Address, Bank Address Inputs:** partially toggling; **Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** REF command every tRFC; **Output Buffer and RTT:** Enabled in Mode Registers*2; **ODT Signal:** stable at 0.		I_{DD5B}	185	mA
Self Refresh Current: **Auto Self-Refresh (ASR)**: Disabled*4; **Self-Refresh Temperature Range (SRT):** Normal*5; **CKE:** Low; **External clock:** Off; CK and CK#: LOW; **BL:** 8*1; **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers*2; **ODT Signal:** MID-LEVEL	**TCASE:** 0 - 85°C	I_{DD6}	19	mA
	TCASE: 0 - 95°C	I_{DD6ET}	25	mA
Operating Bank Interleave Read Current **CKE:** High; **External clock:** On; **BL:** 8*1, 7; **AL:** CL-1; **CS#**: High between ACT and RDA; **Command, Address, Bank Address Inputs:** partially toggling; **DM**:stable at 0; **Output Buffer and RTT:** Enabled in Mode Registers*2; **ODT Signal:** stable at 0.		I_{DD7}	188	mA
RESET Low Current **RESET:** LOW; **External clock:** Off; **CK and CK#:** LOW; **CKE:** FLOATING; **CS#**, **Command, Address, Bank Address, Data IO:** FLOATING; **ODT Signal:** FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.		I_{DD8}	19	mA

NOTE 1: Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
NOTE 2: Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
NOTE 3: Pecharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
NOTE 4: Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
NOTE 5: Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
NOTE 6: Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B