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Revision History

1Gb Auto-AS4C64M16D2 - 84 ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Dec 2015
Rev 2.0	1 Delete Truth Table Note 5 'Device state is 4 and 8 burst operation.' 2 Add follow information in Absolute Maximum DC Ratings note2 'Recommended storage temperature is not exceeding 105°C. Do not store at 150°C for more than 1000 hours.	Apr 2016

Features

- JEDEC Standard Compliant
- AEC-Q100 Compliant
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Power supplies: V_{DD} & V_{DDQ} = +1.8V ± 0.1V
- Automotive Temperature: T_C = -40°C~105°C
- Supports JEDEC clock jitter specification
- Fully synchronous operation
- Fast clock rate: 400 MHz
- Differential Clock, CK & CK#
- Bidirectional single/differential data strobe
  - DQS & DQS#
- 8 internal banks for concurrent operation
- 4-bit prefetch architecture
- Internal pipeline architecture
- Precharge & active power down
- Programmable Mode & Extended Mode registers
- Posted CAS# additive latency (AL): 0, 1, 2, 3, 4, 5
- WRITE latency = READ latency - 1 t_{CK}
- Burst lengths: 4 or 8
- Burst type: Sequential / Interleave
- DLL enable/disable
- On-die termination (ODT)
- RoHS compliant
- Auto Refresh and Self Refresh
- 8192 refresh cycles / 64ms
  - Average refresh period
  7.8μs @ -40°C ≦T_C≦ +85°C
  3.9μs @ +85°C ＜T_C≦ +105°C
- 84-ball 8 x 12.5 x 1.2mm (max) FBGA package
  - Pb and Halogen Free

Overview

The 1Gb DDR2 is a high-speed CMOS Double-Data-Rate-Two (DDR2), synchronous dynamic random - access memory (SDRAM) containing 1024 Mbits in a 16-bit wide data I/Os. It is internally configured as a 8-bank DRAM, 8 banks x 8Mb addresses x 16 I/Os.

The device is designed to comply with DDR2 DRAM key features such as posted CAS# with additive latency, Write latency = Read latency -1 and On Die Termination(ODT).

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK# falling)
All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS#) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in RAS #, CAS# multiplexing style. Accesses begin with the registration of a Bank Activate command, and then it is followed by a Read or Write command. Read and write accesses to the DDR2 SDRAM are 4 or 8-bit burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.
Operating the eight memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. A sequential and gapless data rate is possible depending on burst length, CAS latency, and speed grade of the device.

Table 1. Ordering Information

Part Number	Org	Temperature	MaxClock (MHz)	Package
AS4C64M16D2-25BAN	64Mx16	Automotive -40°C to +105°C	400	84-ball FBGA

Table 2. Speed Grade Information

Speed Grade	Clock Frequency	CAS Latency	tRCD (ns)	tRP (ns)
DDR2-800	400MHz	5	12.5	12.5

Figure 1. Ball Assignment (FBGA Top View)

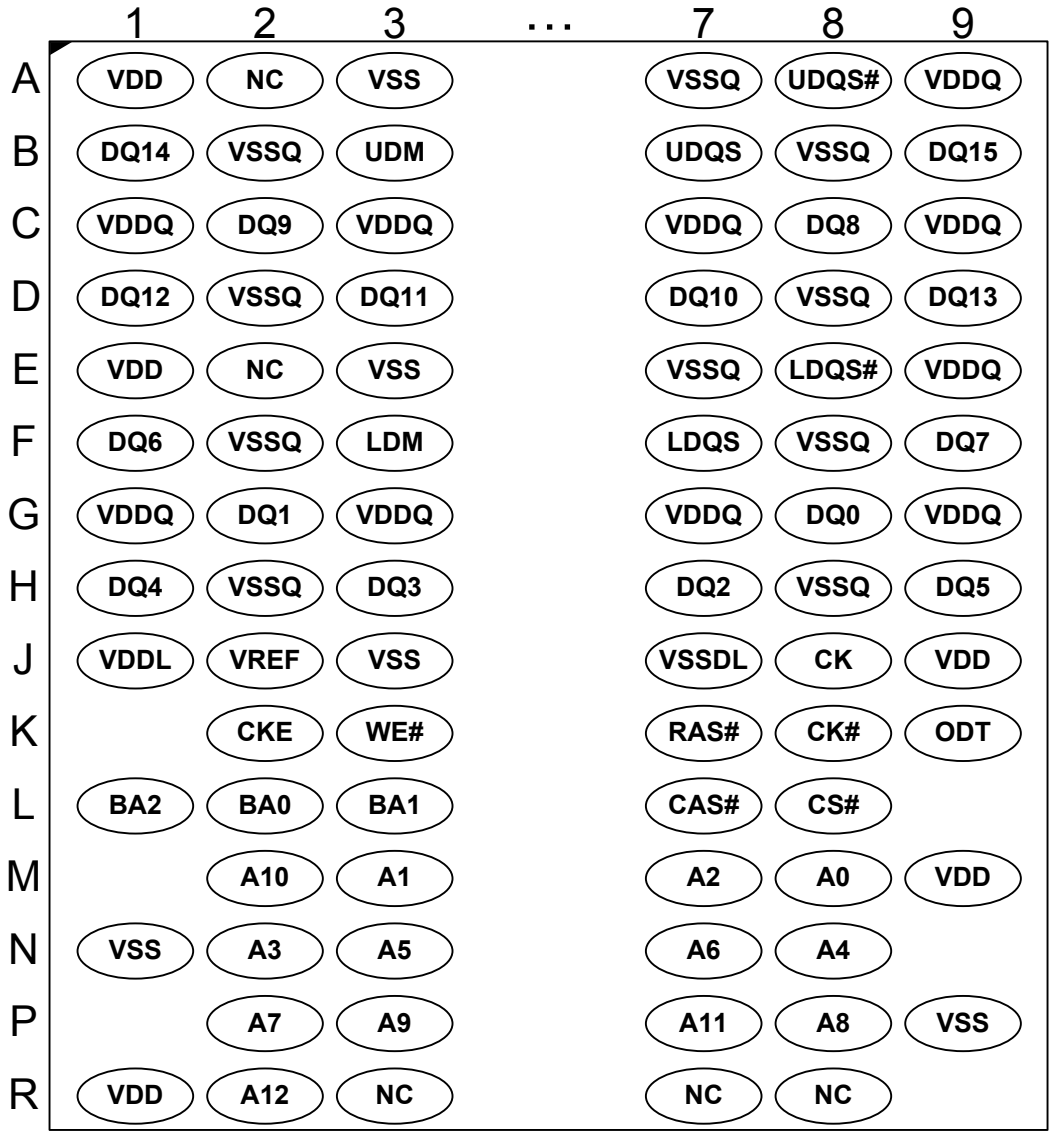


Figure 2. Block Diagram

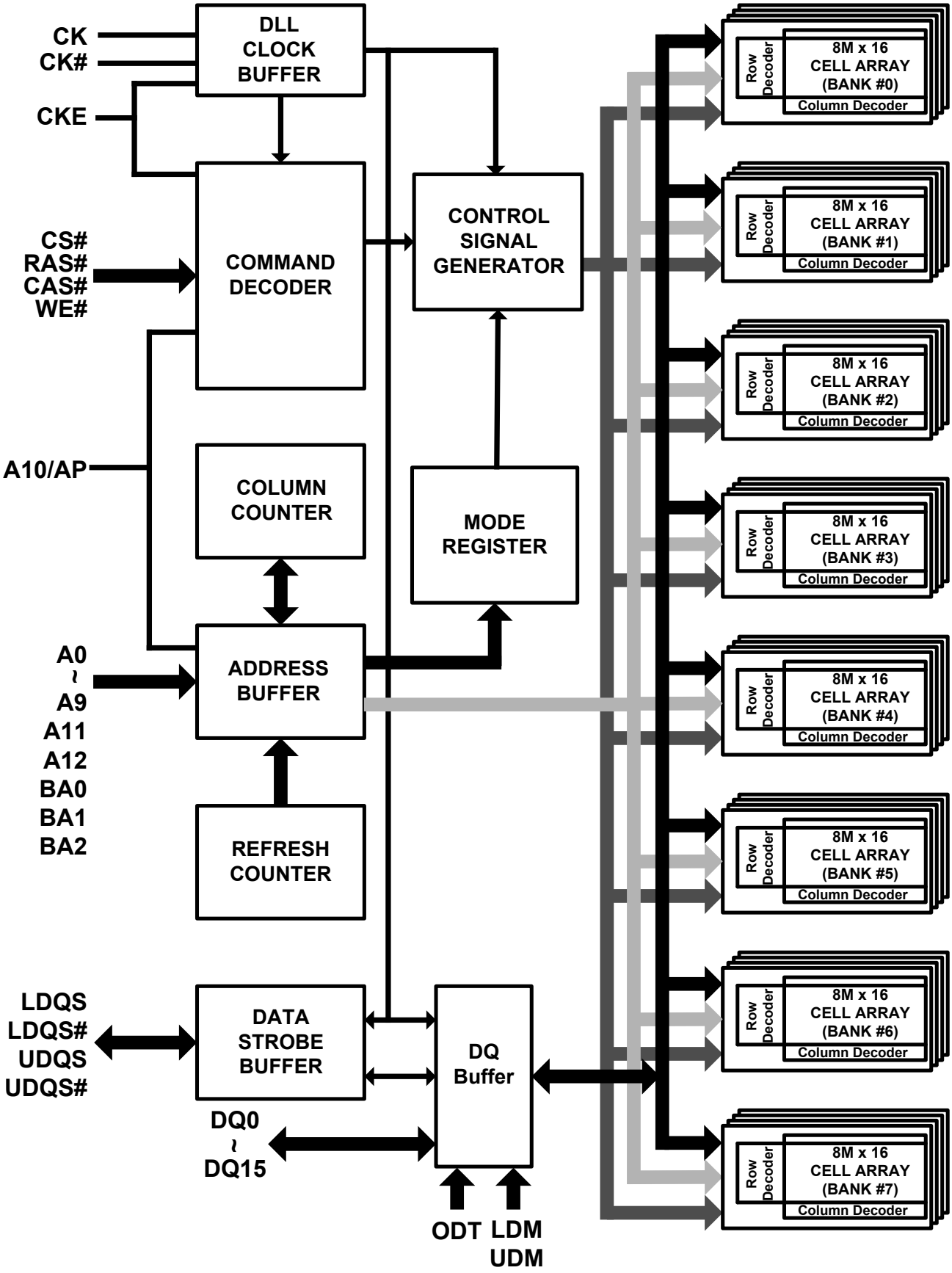
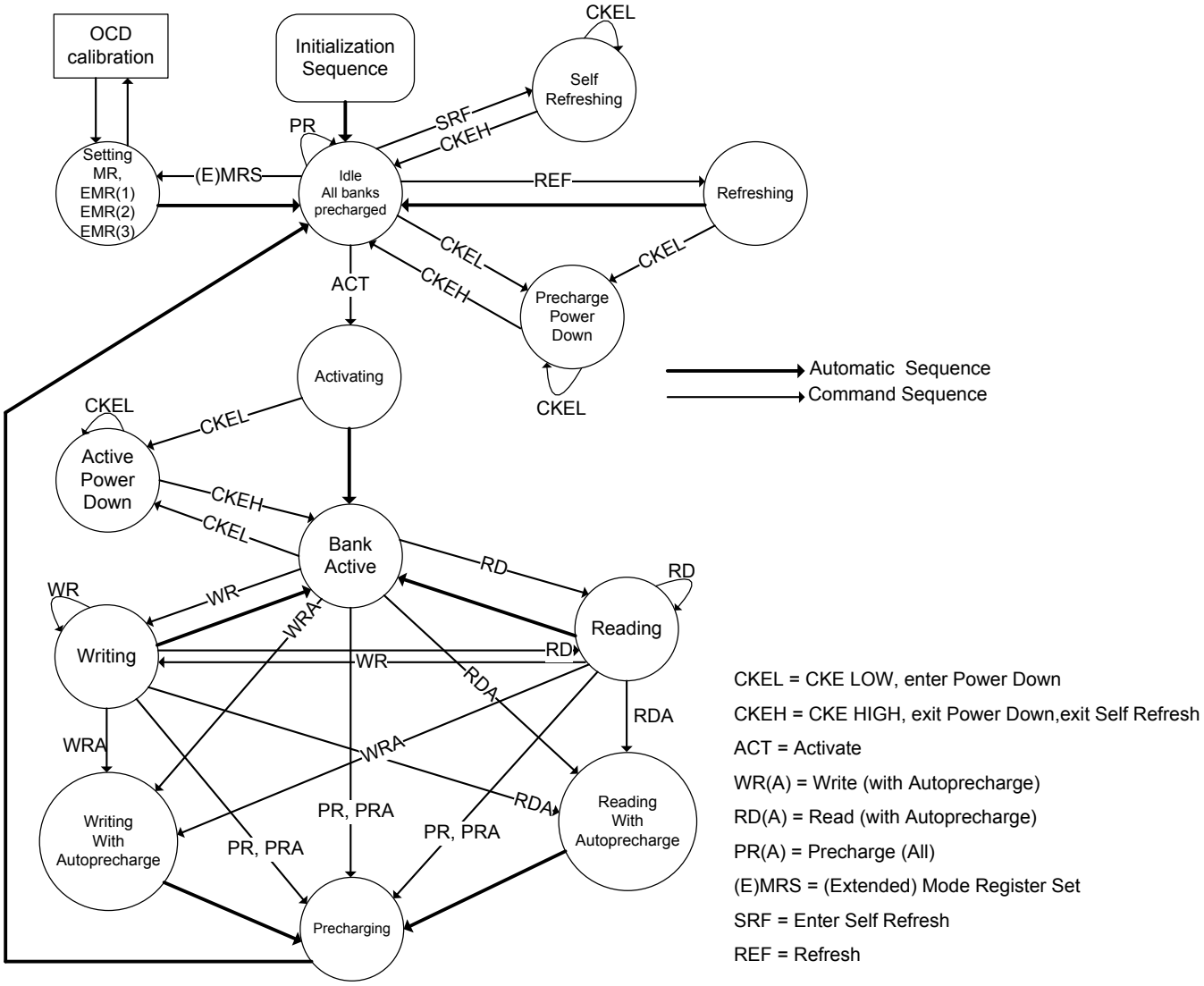


Figure 3. State Diagram



Note: Use caution with this diagram. It is indented to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down entry/exit, timing restrictions during state transitions, among other things, are not captured in full detail.

Ball Descriptions

Table 3. Ball Descriptions

Symbol	Type	Description
CK, CK#	Input	**Differential Clock:** CK, CK# are driven by the system clock. All SDRAM input signals are sampled on the crossing of positive edge of CK and negative edge of CK#. Output (Read) data is referenced to the crossings of CK and CK# (both directions of crossing).
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes LOW synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains LOW. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0-BA2	Input	**Bank Address:** BA0-BA2 define to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied.
A0-A12	Input	**Address Inputs:** A0-A12 are sampled during the BankActivate command (row address A0-A12) and Read/Write command (column address A0-A9 with A10 defining Auto Precharge).
CS#	Input	**Chip Select:** CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.
RAS#	Input	**Row Address Strobe:** The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
CAS#	Input	**Column Address Strobe:** The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# “HIGH " or “LOW".
WE#	Input	**Write Enable:** The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
LDQS, LDQS# UDQS UDQS#	Input / Output	**Bidirectional Data Strobe:** Specifies timing for Input and Output data. Read Data Strobe is edge triggered. Write Data Strobe provides a setup and hold time for data and DQM. LDQS is for DQ0~7, UDQS is for DQ8~15. The data strobes LDOS and UDQS may be used in single ended mode or paired with LDQS# and UDQS# to provide differential pair signaling to the system during both reads and writes.A control bit at EMR (1)[A10] enables or disables all complementary data strobe signals.
LDM, UDM	Input	**Data Input Mask:** Input data is masked when DM is sampled HIGH during a write cycle. LDM masks DQ0-DQ7, UDM masks DQ8-DQ15.
DQ0 - DQ15	Input / Output	**Data I/O:** The Data bus input and output data are synchronized with positive and negative edges of DQS/DQS#. The I/Os are byte-maskable during Writes.
ODT	Input	**On Die Termination:** ODT enables internal termination resistance. It is applied to each DQ, LDQS/LDQS#, UDQS/UDQS#, LDM, and UDM signal. The ODT pin is ignored if the EMR (1) is programmed to disable ODT.
V_{DD}	Supply	**Power Supply:** +1.8V ±0.1V
V_{SS}	Supply	**Ground**

V_{DDL}	Supply	**DLL Power Supply:** +1.8V ±0.1V
V_{SSDL}	Supply	**DLL Ground**
V_{DDQ}	Supply	**DQ Power:** +1.8V ±0.1V.
V_{SSQ}	Supply	**DQ Ground**
V_{REF}	Supply	**Reference Voltage for Inputs:** +0.5*V_{DDQ}
NC	-	**No Connect:** These pins should be left unconnected.

Operation Mode

Table 4 shows the truth table for the operation commands.

Table 4. Truth Table (Note (1), (2))

Command	State	CKE_{n-1}	CKE_n	DM	BA0-2	A10	A0-9, 11-12	CS#	RAS#	CAS#	WE#
BankActivate	Idle(3)	H	H	X	V	Row address		L	L	H	H
Single Bank Precharge	Any	H	H	X	V	L	X	L	L	H	L
All Banks Precharge	Any	H	H	X	X	H	X	L	L	H	L
Write	Active(3)	H	H	X	V	L	Column address (A0 – A9)	L	H	L	L
Write with AutoPrecharge	Active(3)	H	H	X	V	H		L	H	L	L
Read	Active(3)	H	H	X	V	L	Column address (A0 – A9)	L	H	L	H
Read and Autoprecharge	Active(3)	H	H	X	V	H		L	H	L	H
(Extended) Mode Register Set	Idle	H	H	X	V	OP code		L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Refresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Power Down Mode Entry	Idle	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Power Down Mode Exit	Any	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Input Mask Disable	Active	H	X	L	X	X	X	X	X	X	X
Data Input Mask Enable(4)	Active	H	X	H	X	X	X	X	X	X	X

NOTE 1: V=Valid data, X=Don't Care, L=Low level, H=High level
NOTE 2: CKEn signal is input level when commands are provided.
CKEn-1 signal is input level one clock cycle before the commands are provided.
NOTE 3: These are states of bank designated by BA signal.
NOTE 4: LDM and UDM can be enabled respectively.

Functional Description

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.
Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

● Power-up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.
The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2*V_{DDQ} and ODT [*1] at a low state (all other inputs may be undefined.) The V_{DD} voltage ramp time must be no greater than 200ms from when V_{DD} ramps from 300mV to V_{DD}min; and during the V_{DD} voltage ramp, $|V_{DD}-V_{DDQ}| \leqq 0.3V$
   - V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output, AND
   - V_{TT} is limited to 0.95 V max, AND
   - V_{REF} tracks $V_{DDQ}/2$.
   or
   - Apply V_{DD} before or at the same time as V_{DDL}.
   - Apply V_{DDL} before or at the same time as V_{DDQ}.
   - Apply V_{DDQ} before or at the same time as V_{TT} & V_{REF}.
   At least one of these two sets of conditions must be met.
2. Start clock and maintain stable condition.
3. For the minimum of 200μs after stable power and clock (CK, CK#), then apply NOP or deselect and take CKE HIGH.
4. Wait minimum of 400ns then issue precharge all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS (2) command, provide “LOW” to BA0 and BA2, “HIGH” to BA1.)
6. Issue EMRS (3) command. (To issue EMRS (3) command, provide “LOW” to BA2, “HIGH” to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "LOW" to A0, "HIGH" to BA0 and "LOW" to BA1 and BA2.)
8. Issue a Mode Register Set command for “DLL reset”.
   (To issue DLL reset command, provide "HIGH" to A8 and "LOW" to BA0-BA2)
9. Issue precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with LOW to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment).If OCD calibration is not used, EMRS OCD Default command (A9=A8=A7=HIGH) followed by EMRS OCD calibration Mode Exit command (A9=A8=A7=LOW) must be issued with other operating parameters of EMRS.
13. The DDR2 SDRAM is now ready for normal operation.

NOTE 1: To guarantee ODT off, V_{REF} must be valid and a LOW level must be applied to the ODT pin.

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, WR, and various vendor specific options to make DDR2 SDRAM useful for various applications.The default value of the mode register is not defined, therefore the mode register must be programmed during initialization for proper operation. The mode register is written by asserting LOW on CS#, RAS#, CAS#, WE#, BA0 and BA1, while controlling the state of address pins A0 - A12. The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the mode register.The mode register set command cycle time (t_{MRD}) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all bank are in the precharge state.The mode register is divided into various fields depending on functionality.

- Burst Length Field (A2, A1, A0)
  This field specifies the data length of column access and selects the Burst Length.
- Addressing Mode Select Field (A3)
  The Addressing Mode can be Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 4 and 8.
- CAS Latency Field (A6, A5, A4)
  This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field.
  $t_{CAC}(min) \leqq$ CAS Latency X t_{CK}
- Test Mode field: A7; DLL Reset Mode field: A8
  These two bits must be programmed to "00" in normal operation.
- (BA0-BA1): Bank addresses to define MRS selection.

Table 5. Mode Register Bitmap

BA2	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
																Address Field
0*2	0	0	PD	WR			DLL	TM	CAS Latency			BT	Burst Length			Mode Register

A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	BL
0	1	0	4
0	1	1	8

A12	Active power down exit time
0	Fast exit (use t_{XARD})
1	Slow exit (use t_{XARDS})

Write recovery for autoprecharge*1

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

BA1	BA0	MRS Mode
0	0	MR
0	1	EMR(1)
1	0	EMR(2)
1	1	EMR(3)

Note 1:.For DDR2-800, WR min is determined by t_{CK} (avg) max and WR max is determined by t_{CK}(avg) min. WR [cycles] = RU {t_{WR}[ns]/t_{CK}(avg)[ns]}, where RU stands for round up. The mode register must be programmed to this value.This is also used with t_{RP} to determine t_{DAL}.

NOTE 2: BA2 is reserved for future use and must be set to 0 when programming the MR.

● Extended Mode Register Set (EMRS)

- **EMR(1)**

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, ODT value selection and additive latency. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting LOW on CS#, RAS#, CAS#, WE#, BA1 and HIGH on BA0, while controlling the states of address pins A0 ~ A12. The DDR2 SDRAM should be in all bank precharge with CKE already HIGH prior to writing into the extended mode register. The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the extended mode register. Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength data-output driver. A3~A5 determine the additive latency, A2 and A6 are used for ODT value selection, A7~A9 are used for OCD control, A10 is used for DQS# disable.

- **DLL Enable/Disable**

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{AC} or t_{DQSCK} parameters.

Table 6. Extended Mode Register EMR (1) Bitmap

BA2	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0[*3]	0	1	Qoff	0[*3]	DQS#	OCD program			Rtt	Additive Latency			Rtt	D.I.C	DLL	Extended Mode Register

BA1	BA0	MRS mode
0	0	MR
0	1	EMR(1)
1	0	EMR(2)
1	1	EMR(3)

A6	A2	Rtt(NOMINAL)
0	0	ODT Disable
0	1	75Ω
1	0	150Ω
1	1	50Ω

A0	DLL Enable
0	Enable
1	Disable

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Reserved
0	1	0	Reserved
1	0	0	Reserved
1	1	1	OCD Calibration default[*1]

A1	Output Driver Impedance Control
0	Full strength
1	Reduced strength

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

A12	Qoff [*2]
0	Output buffer enabled
1	Output buffer disabled

A10	DQS#
0	Enable
1	Disable

NOTE 1: After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000.

NOTE 2: Output disabled – DQs, DQSs, DQSs#.This feature is intended to be used during I_{DD} characterization of read current.

NOTE 3: A11 and BA2 are reserved for future use and must be set to 0 when programming the MR.

- **EMR(2)**

The extended mode register (2) controls refresh related features. The default value of the extended mode register (2) is not defined, therefore the extended mode register (2) must be written after power-up for proper operation. The extended mode register(2) is written by asserting LOW on CS#, RAS#, CAS#, WE#, HIGH on BA1 and LOW on BA0, while controlling the states of address pins A0 ~ A12. The DDR2 SDRAM should be in all bank precharge with CKE already HIGH prior to writing into the extended mode register (2). The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the extended mode register (2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

Table 7. Extended Mode Register EMR(2) Bitmap

BA2	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
								↓								Address Field
0*3	1	0	0*1					SRF	0*1							Extended Mode Register(2)

A7	High Temperature Self-Refresh Rate Enable
0	Disable
1	Enable *2

NOTE 1: The rest bits in EMRS(2) are reserved for future use and all bits in EMRS(2) except A7, BA0 and BA1 must be programmed to 0 when setting the extended mode register(2) during initialization.

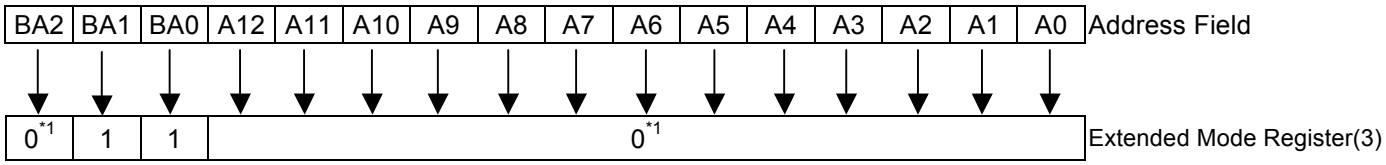
NOTE 2: Due to the migration nature, user needs to ensure the DRAM part supports higher than 85℃ Tcase temperature self-refresh entry. If the high temperature self-refresh mode is supported then controller can set the EMRS2[A7] bit to enable the self-refresh rate in case of higher than 85℃ temperature self-refresh operation.

NOTE 3: BA2 is reserved for future use and must be set to 0 when programming the MR.

- **EMR(3)**

No function is defined in extended mode register(3).The default value of the extended mode register(3) is not defined, therefore the extended mode register(3) must be programmed during initialization for proper operation.

Table 8. Extended Mode Register EMR (3) Bitmap



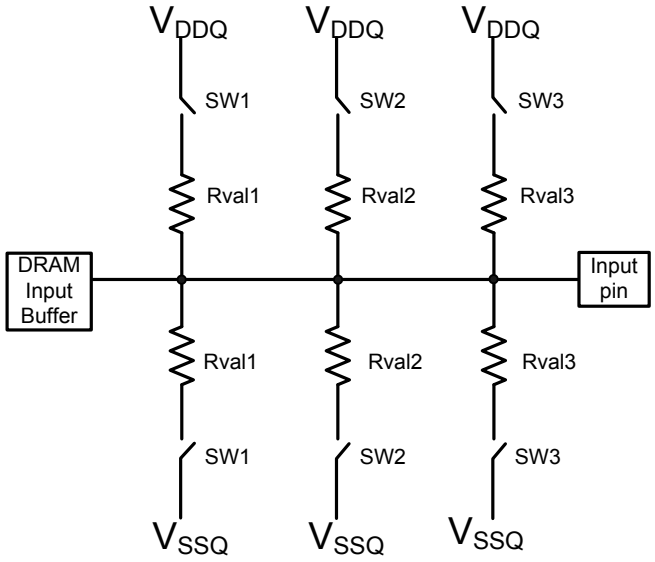
NOTE 1: All bits in EMR (3) except BA0 and BA1 are reserved for future use and must be set to 0 when programming the EMR (3).

● ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, UDQS/UDQS#, LDQS/LDQS#, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is supported for ACTIVE and STANDBY modes. It is turned off and not supported in SELF REFRESH mode.

Figure 4. Functional representation of ODT



Switch (sw1, sw2, sw3) is enabled by ODT pin.
Selection among sw1, sw2, and sw3 is determined by "Rtt (nominal)" in EMR.
Termination included on all DQs, DM, DQS, and DQS# pins

Table 9. ODT DC Electrical Characteristics

Parameter/Condition	Symbol	Min.	Nom.	Max.	Unit	Note
Rtt effective impedance value for EMRS(A6,A2)=0,1;75Ω	Rtt1(eff)	60	75	90	Ω	1
Rtt effective impedance value for EMRS(A6,A2)=1,0;150Ω	Rtt2(eff)	120	150	180	Ω	1
Rtt effective impedance value for EMRS(A6,A2)=1,1;50Ω	Rtt3(eff)	40	50	60	Ω	1
Rtt mismatch tolerance between any pull-up/pull-down pair	Rtt(mis)	-6	-	6	%	2

NOTE 1: Measurement Definition for Rtt(eff):

Apply V_{IH} (ac) and V_{IL} (ac) to test pin seperately, then measure current $I(V_{IH}(ac))$ and $I(V_{IL}(ac))$ respectively.

$$Rtt(eff)=\frac{V_{IH}(ac)-V_{IL}(ac)}{I(V_{IH}(ac))-I(V_{IL}(ac))}$$

NOTE 2: Measurement Defintion for Rtt (mis): Measure voltage (VM) at test pin (midpoint) with no load.

$$Rtt(mis)=\left(\frac{2xVM}{V_{DDQ}}-1\right)\times 100\%$$

Bank activate command

The Bank Activate command is issued by holding CAS# and WE# HIGH with CS# and RAS# LOW at the rising edge of the clock. The bank addresses BA0-BA2 are used to select the desired bank. The row addresses A0 through A12 are used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command (with or without Auto-Precharge) on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the t_{RCD}min specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure t_{RCD}min is satisfied. Additive latencies of 0, 1, 2, 3, and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined (t_{RC}). The minimum time interval between Bank Active commands is t_{RRD}

In order to ensure that 8 bank devices do not exceed the instantaneous current supplying capability of 4 bank devices, certain restrictions on operation of the 8 bank devices must be observed. There are two rules. One for restricting the number of sequential ACT commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

- 8 bank device Sequential Bank Activation Restriction : No more than 4 banks may be activated in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW}[ns] by t_{CK}[ns] or t_{CK}[ns], depending on the speed bin, and rounding up to next integer value. As an example of the rolling window, if RU{ (t_{FAW} / t_{CK}) } or RU{ (t_{FAW} / t_{CK})} is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9.
- 8 bank device Precharge All Allowance : t_{RP} for a Precharge All command for an 8 Bank device will equal to t_{RP} + 1 x t_{CK} or t_{RP} + 1 x t_{CK}, depending on the speed bin, where t_{RP} = RU{ t_{RP} / t_{CK}} and t_{RP} is the value for a single bank precharge.

Read and Write access modes

After a bank has been activated, a Read or Write cycle can be executed. This is accomplished by setting RAS# HIGH, CS# and CAS# LOW at the clock's rising edge. WE# must also be defined at this time to determine whether the access cycle is a Read operation (WE# HIGH) or a Write operation (WE# LOW). The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial Read or Write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. Any system or application incorporating random access memory products should be properly designed, tested, and qualified to ensure proper use or access of such memory products. Disproportionate, excessive, and/or repeated access to a particular address or addresses may result in reduction of product life.

Posted CAS#

Posted CAS# operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a CAS# Read or Write command to be issued immediately after the RAS bank activate command (or any time during the RAS# -CAS#-delay time, t_{RCD}, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the CAS latency (CL). Therefore if a user chooses to issue a R/W command before the t_{RCD}min, then AL (greater than 0) must be written into the EMR(1). The Write Latency (WL) is always defined as RL - 1 (Read Latency -1) where Read Latency is defined as the sum of additive latency plus CAS latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section)

Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (Write cycle), or from memory locations (Read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by the addresses A0 ~ A2 of the MRS. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS. Seamless burst Read or Write operations are supported. Interruption of a burst Read or Write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a Read or Write burst when burst length = 8 is used, see the "Burst Interruption" section of this datasheet. A Burst Stop command is not supported on DDR2 SDRAM devices.

Table 10. Burst Definition, Addressing Sequence of Sequential and Interleave Mode

Burst Length	Start Address			Sequential	Interleave
	A2	A1	A0		
4	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

● Burst read command

The Burst Read command is initiated by having CS# and CAS# LOW while holding RAS# and WE# HIGH at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the Read Latency (RL). The data strobe output (DQS) is driven LOW 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus CAS Latency (CL). The CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR SDRAMs. The AL is defined by the Extended Mode Register Set (1) (EMRS (1)).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, DQS#. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, DQS#, must be tied externally to V_{SS} through a 20 Ω to 10 KΩresistor to insure proper operation.

● Burst write operation

The Burst Write command is initiated by having CS#, CAS# and WE# LOW while holding RAS# HIGH at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a Read latency (RL) minus one and is equal to (AL + CL -1);and is the number of clocks of delay that are required from the time the Write command is registered to the clock edge associated to the first DQS strobe. A data strobe signal (DQS) should be driven LOW (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The t_{DQSS} specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles.

The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst Write to bank precharge is the write recovery time (WR). DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent.

In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at the specified AC/DC levels. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, DQS#. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, DQS#, must be tied externally to V_{SS} through a 20Ω to 10KΩ resistor to insure proper operation.

Write data mask

One Write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, Consistent with the implementation on DDR SDRAMs. It has identical timings on Write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM is not used during read cycles.

Precharge operation

The Precharge command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when CS#, RAS# and WE# are LOW and CAS# is HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA2, BA1, and BA0 are used to define which bank to precharge when the command is issued.

Table 11. Bank Selection for Precharge by address bits

A10	BA2	BA1	BA0	Precharged Bank(s)
LOW	LOW	LOW	LOW	Bank 0 only
LOW	LOW	LOW	HIGH	Bank 1 only
LOW	LOW	HIGH	LOW	Bank 2 only
LOW	LOW	HIGH	HIGH	Bank 3 only
LOW	HIGH	LOW	LOW	Bank 4 only
LOW	HIGH	LOW	HIGH	Bank 5 only
LOW	HIGH	HIGH	LOW	Bank 6 only
LOW	HIGH	HIGH	HIGH	Bank 7 only
HIGH	DON'T CARE	DON'T CARE	DON'T CARE	ALL Banks

Burst read operation followed by precharge

Minimum Read to precharge command spacing to the same bank = AL + BL/2 + max (RTP, 2) - 2 clocks. For the earliest possible precharge, the precharge command may be issued on the rising edge which "Additive latency (AL) + BL/2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS# precharge time (t_{RP}). A precharge command cannot be issued until t_{RAS} is satisfied.
The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called t_{RTP} (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command.

Burst Write operation followed by precharge

Minimum Write to Precharge command spacing to the same bank = WL + BL/2 + t_{WR}. For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge command can be issued. This delay is known as a write recovery time (t_{WR}) referenced from the completion of the burst write to the Precharge command. No Precharge command should be issued prior to the t_{WR} delay, as DDR2 SDRAM does not support any burst interrupt by a Precharge command. t_{WR} is an analog timing parameter and is not the programmed value for t_{WR} in the MRS.

Auto precharge operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the auto-precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the CAS# timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is LOW when the READ or WRITE Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is HIGH when the Read or Write Command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is CAS latency (CL) clock cycles before the end of the read burst. Auto-precharge also be implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array. This feature allows the precharge operation to be partially or completely hidden during burst Read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS# lockout circuit internally delays the Precharge operation until the array restore operation has been completed (t_{RAS} satisfied) so that the auto precharge command may be issued with any Read or Write command.

Burst read with auto precharge

If A10 is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto-Precharge operation on the rising edge which is (AL + BL/2) cycles later from the Read with AP command if t_{RAS}(min) and t_{RTP} are satisfied. If t_{RAS}(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until t_{RAS}(min) is satisfied. If t_{RTP}(min) is not satisfied at the edge, the start point of Auto-precharge operation will be delayed until t_{RTP}(min) is satisfied.

In case the internal precharge is pushed out by t_{RTP}, t_{RP} starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read with Auto-Precharge to the next Activate command becomes AL + t_{RTP} + t_{RP}. For BL = 8 the time from Read with Auto-Precharge to the next Activate command is AL + 2 + t_{RTP} + t_{RP}. Note that both parameters t_{RTP} and t_{RP} have to be rounded up to the next integer value. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously:

(1) The RAS# precharge time (t_{RP}) has been satisfied from the clock at which the Auto-Precharge begins.

(2) The RAS# cycle time (t_{RC}) from the previous bank activation has been satisfied.

Burst write with auto precharge

If A10 is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus Write recovery time (t_{WR}). The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

(1) The data-in to bank activate delay time (WR + t_{RP}) has been satisfied.

(2) The RAS# cycle time (t_{RC}) from the previous bank activation has been satisfied.

Table 12. Precharge & Auto Precharge Clariification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Note
Read	Precharge (to same Bank as Read)	AL+BL/2+max(RTP,2)-2	t_{CK}	1,2
	Precharge All	AL+BL/2+max(RTP,2)-2		
Read w/AP	Precharge (to same Bank as Read w/AP)	AL+BL/2+max(RTP,2)-2	t_{CK}	1,2
	Precharge All	AL+BL/2+max(RTP,2)-2		
Write	Precharge (to same Bank as Write)	WL+BL/2+t_{WR}	t_{CK}	2
	Precharge All	WL+BL/2+t_{WR}		
Write w/AP	Precharge (to same Bank as Write w/AP)	WL+BL/2+t_{WR}	t_{CK}	2
	Precharge All	WL+BL/2+t_{WR}		
Precharge	Precharge (to same Bank as Precharge)	1	t_{CK}	2
	Precharge All	1		
Precharge All	Precharge	1	t_{CK}	2
	Precharge All	1		

NOTE 1: RTP [cycles] =RU {t_{RTP} [ns]/t_{CK} (avg) [ns]}, where RU stands for round up.
NOTE 2: For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank.The prechrage period is satisfied after t_{RP} or t_{RP}all(=t_{RP} for 8 bank device + 1X t_{CK}) depending on the latest precharge command issued to that bank.

Refresh command

When CS#, RAS# and CAS# are held LOW and WE# HIGH at the rising edge of the clock, the chip enters the Refresh mode (REF). All banks of the DDR2 SDRAM must be precharged and idle for a minimum of the Precharge time (t_{RP}) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the Refresh command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (t_{RFC}).To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 * t_{REFI}.

Self refresh operation

The Self Refresh command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the DDR2 SDRAM retains data without external clocking. The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CS#, RAS#, CAS# and CKE# held LOW with WE# HIGH at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin LOW or using EMRS command. Once the Command is registered, CKE must be held LOW to keep the device in Self Refresh mode. The DLL is automatically disabled upon entering Self Refresh and is automatically enabled upon exiting Self Refresh. When the DDR2 SDRAM has entered Self Refresh mode all of the external signals except CKE, are "don't care". For proper Self Refresh operation all power supply pins (V_{DD}, V_{DDQ}, V_{DDL} and V_{REF}) must be at valid levels. The DRAM initiates a minimum of one refresh command internally within t_{CKE} period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the DDR2 SDRAM must remain in Self Refresh mode is t_{CKE}. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least t_{XSNR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period t_{XSRD} for proper operation except for Self Refresh re-entry. Upon exit from Self Refresh, the DDR2 SDRAM can be put back into Self Refresh mode after waiting at least t_{XSNR} period and issuing one refresh command(refresh period of t_{RFC}). NOP or Deselect commands must be registered on each positive clock edge during the Self Refresh exit interval t_{XSNR}. ODT should be turned off during t_{XSRD}. The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh mode.

Power-Down

Power-down is synchronously entered when CKE is registered LOW along with NOP or Deselect command. No read or write operation may be in progress when CKE goes LOW. These operations are any of the following: read burst or write burst and recovery. CKE is allowed to go LOW while any of other operations such as row activation, precharge or autoprecharge, mode register or extended mode register command time, or autorefresh is in progress.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are precharged, this mode is referred to as Precharge Power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as Active Power-down. For Active Power-down two different power saving modes can be selected within the MRS register, address bit A12. When A12 is set to "LOW" this mode is referred as "standard active power-down mode" and a fast power-down exit timing defined by the t_{XARD} timing parameter can be used. When A12 is set to "HIGH" this mode is referred as a power saving "LOW power active power-down mode". This mode takes longer to exit from the power-down mode and the t_{XARDS} timing parameter has to be satisfied. Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and all other input signals are "Don't Care". Power-down duration is limited by 9 times t_{REFI} of the device.

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or Deselect command). A valid, executable command can be applied with power-down exit latency, t_{XP}, t_{XARD} or t_{XARDS}, after CKE goes HIGH. Power-down exit latencies are defined in the AC spec table of this data sheet.

Asynchronous CKE LOW Event

DRAM requires CKE to be maintained "HIGH" for all valid operations as defined in this datasheet. If CKE asynchronously drops "LOW" during any valid peration DRAM is not guaranteed to preserve the contents of array. If this event occurs, memory controller must satisfy DRAM timing specification tDelay efore turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised "HIGH" again. DRAM must be fully re-initialized. DRAM is ready for normal operation after the initialization sequence.

Input clock frequency change during precharge power down

DDR2 SDRAM input clock frequency can be changed under following condition: DDR2 SDRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via EMRS after precharge power down exit. Depending on new clock frequency an additional MRS command may need to be issued to appropriately set the WR, CL etc. During DLL re-lock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

No operation command

The No Operation Command should be used in cases when the DDR2 SDRAM is in an idle or a wait state. The purpose of the No Operation Command (NOP) is to prevent the DDR2 SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when CS# is LOW with RAS#, CAS#, and WE# held HIGH at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when CS# is brought HIGH at the rising edge of the clock, the RAS#, CAS#, and WE# signals become don't cares.

Table 13. Absolute Maximum DC Ratings

Symbol	Parameter	Value	Unit	Note
V_{DD}	Voltage on V_{DD} pin relative to Vss	-1.0 ~ 2.3	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to Vss	-0.5 ~ 2.3	V	1,3
V_{DDL}	Voltage on V_{DDL} pin relative to Vss	-0.5 ~ 2.3	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.5 ~ 2.3	V	1,4
T_{STG}	Storage temperature	-55~150	°C	1,2

NOTE1: Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NOTE2: Storage temperature is the case temperature on the center/top side of the DRAM. Recommended storage temperature is not exceeding 105°C. Do not store at 150°C for more than 1000 hours.

NOTE3: When V_{DD} and V_{DDQ} and V_{DDL} are less than 500mV, Vref may be equal to or less than 300mV.

NOTE4: Voltage on any input or I/O may not exceed voltage on V_{DDQ}.

Table 14. Operating Temperature Condition

Symbol	Parameter	Value	Unit	Note
T_{OPER}	Automotive temperature	-40~105	°C	1

NOTE1: Operating temperature is the case surface temperature on center/top of the DRAM.

NOTE2: If TC exceeds 85°C, the DRAM must be refreshed externally at 2x refresh. It is required to set tREFI=3.9μs in auto refresh mode and to set '1' for EMRS (2) bit A7 in self refresh mode.

Table 15. Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{DD}	Power supply voltage	1.7	1.8	1.9	V	1
V_{DDL}	Power supply voltage for DLL	1.7	1.8	1.9	V	5
V_{DDQ}	Power supply voltage for I/O Buffer	1.7	1.8	1.9	V	1,5
V_{REF}	Input reference voltage	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	mV	2,3
V_{TT}	Termination voltage	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	4

NOTE1: There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions V_{DDQ} must be less than or equal to V_{DD}.

NOTE2: The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.

NOTE3: Peak to peak ac noise on V_{REF} may not exceed +/-2 % V_{REF} (dc).

NOTE4: V_{TT} of transmitting device must track V_{REF} of receiving device.

NOTE5: V_{DDQ} tracks with V_{DD}, V_{DDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together

Table 16. Input logic level

Symbol	Parameter	-25		Unit
		Min.	Max.	
V_{IH} (DC)	DC Input logic High Voltage	V_{REF} + 0.125	V_{DDQ} + 0.3	V
V_{IL} (DC)	DC Input Low Voltage	-0.3	V_{REF} - 0.125	V
V_{IH} (AC)	AC Input High Voltage	V_{REF} + 0.2	V_{DDQ}+V_{peak}	V
V_{IL} (AC)	AC Input Low Voltage	Vss_Q –V_{peak}	V_{REF} – 0.2	V
V_{ID} (AC)	AC Differential Voltage	0.5	V_{DDQ}	V
V_{IX} (AC)	AC Differential crosspoint Voltage	0.5 x V_{DDQ}-0.175	0.5 x V_{DDQ}+0.175	V

NOTE1: Refer to Overshoot/undershoot specification for V_{peak} value: maximum peak amplitude allowed for overshoot and undershoot.

Table 17. AC Input test conditions

Symbol	Parameter	Value	Unit	Note
V_{REF}	Input reference voltage	0.5 x V_{DDQ}	V	1
$V_{SWING(max)}$	Input signal maximum peak to peak swing	1.0	V	1
Slew Rate	Input signal minimum slew rate	1.0	V/ns	2, 3

NOTE1: Input waveform timing is referenced to the input signal crossing through the V_{IH} /$_{IL}$ (ac) level applied to the device under test.

NOTE2: The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(ac) min for rising edges and the range from V_{REF} to V_{IL} (ac) max for falling edges .

NOTE3: AC timings are referenced with input waveforms switching from V_{IL} (ac) to V_{IH} (ac) on the positive transitions and V_{IH} (ac) to V_{IL} (ac) on the negative transitions.

Table 18. Differential AC output parameters

Symbol	Parameter	Value		Unit	Note
		Min.	Max.		
$V_{ox(ac)}$	AC Differential Cross Point Voltage	0.5xV_{DDQ}-0.125	0.5xV_{DDQ}+0.125	V	1

NOTE1: The typical value of V_{OX} (ac) is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{OX} (ac) is expected to track variations in V_{DDQ}. V_{OX} (ac) indicates the voltage at which differential output signals must cross.

Table 19. AC overshoot/undershoot specification for address and control pins (A0-A12, BA0-BA2, CS#, RAS#, CAS#, WE#, CKE, ODT)

Parameter	-25	Unit
Maximum peak amplitude allowed for overshoot area	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	V
Maximum overshoot area above V_{DD}	0.66	V-ns
Maximum undershoot area below V_{SS}	0.66	V-ns

Table 20. AC overshoot/undershoot specification for clock, data, strobe, and mask pins (DQ, UDQS, LDQS, UDQS#, LDQS#, DM, CK, CK#)

Parameter	-25	Unit
Maximum peak amplitude allowed for overshoot area	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	V
Maximum overshoot area above V_{DD}	0.23	V-ns
Maximum undershoot area below V_{SS}	0.23	V-ns

Table 21. Output AC test conditions

Symbol	Parameter	Value	Unit	Note
V_{OTR}	Output timing measurement reference level	$0.5xV_{DDQ}$	V	1

NOTE1: The V_{DDQ} of the device under test is referenced.

Table 22. Output DC current drive

Symbol	Parameter	SSTL_18	Unit	Note
I_{OH}(dc)	Output minimum source DC current	-13.4	mA	1, 3, 4
I_{OL}(dc)	Output minimum sink DC current	13.4	mA	2, 3, 4

NOTE1: V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ}) /I_{OH} must be less than 21 Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.
NOTE2: V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 Ω for values of V_{OUT} between 0 V and 280 mV.
NOTE3: The dc value of V_{REF} applied to the receiving device is set to V_{TT}
NOTE4: The values of I_{OH} (dc) and I_{OL} (dc) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and VIL max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see JEDEC standard: Section 3.3 of JESD8-15A) along a 21 Ω load line to define a convenient driver current for measurement.

Table 23. Capacitance (V_{DD} = 1.8V, f = 1MHz, T_{OPER} = 25 °C)

Symbol	Parameter	DDR2-800		Unit
		Min.	Max.	
C_{IN}	Input Capacitance : Command and Address	1.0	1.75	pF
C_{CK}	Input Capacitance (CK, CK#)	1.0	2.0	pF
$C_{I/O}$	DM, DQ, DQS Input/Output Capacitance	2.5	3.5	pF
DC_{IN}	Delta Input Capacitance: Command and Address	-	0.25	pF
DC_{CK}	Delta Input Capacitance: CK, CK#	-	0.25	pF
DC_{IO}	Delta Input/Output Capacitance: DM, DQ, DQS	-	0.5	pF

NOTE: These parameters are periodically sampled and are not 100% tested.

Table 24. IDD specification parameters and test conditions

(V_{DD} = 1.8V ± 0.1V, T_{OPER} = -40~105°C)

Parameter & Test Condition		Symbol	-25	Unit
			Max.	
Operating one bank active-precharge current: t_{CK} =t_{CK} (min), t_{RC} = t_{RC} (min), t_{RAS} = t_{RAS}(min); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		I_{DD0}	72	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (min), AL = 0; t_{CK} = t_{CK} (min),t_{RC} = t_{RC} (min), t_{RAS} = t_{RAS}(min), t_{RCD} = t_{RCD} (min);CKE is HIGH, CS# is HIGH between valid commands;Address bus inputs are switching; Data pattern is same as I_{DD4W}		I_{DD1}	90	mA
Precharge power-down current: All banks idle;t_{CK} =t_{CK} (min); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		I_{DD2P}	11	mA
Precharge quiet standby current: All banks idle; t_{CK} =t_{CK} (min); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		I_{DD2Q}	22	mA
Precharge standby current: All banks idle; t_{CK} = t_{CK} (min); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		I_{DD2N}	30	mA
Active power-down current: All banks open; t_{CK} =t_{CK} (min); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	MRS(A12)=0	I_{DD3P}	28	mA
	MRS(A12)=1		20	mA
Active standby current: All banks open; t_{CK} = t_{CK}(min), t_{RAS} = t_{RAS} (max), t_{RP} = t_{RP} (min); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		I_{DD3N}	39	mA
Operating burst write current: All banks open,continuous burst writes; BL = 4, CL = CL (min), AL = 0; t_{CK}= t_{CK} (min), t_{RAS} = t_{RAS} (max), t_{RP} = t_{RP} (min); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4W}	156	mA
Operating burst read current: All banks open, continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL (min), AL = 0; t_{CK} = t_{CK} (min), t_{RAS} = t_{RAS} (max), t_{RP} = t_{RP} (min); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		I_{DD4R}	138	mA
Burst refresh current: t_{CK} = t_{CK} (min); refresh command at every t_{RFC} (min) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		I_{DD5}	120	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V;Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		I_{DD6}	18	mA
Operating bank interleave read current: All bank interleaving reads, I_{OUT}= 0mA; BL = 4, CL = CL (min), AL =t_{RCD} (min) - 1 x t_{CK} (min); t_{CK} = t_{CK} (min), t_{RC} = t_{RC} (min), t_{RRD} = t_{RRD} (min), t_{RCD} = t_{RCD} (min); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs.Data pattern is same as IDD4R		I_{DD7}	240	mA

Table 25. Electrical Characteristics and Recommended A.C. Operating Conditions

(V_{DD} = 1.8V ± 0.1V, T_{OPER} = -40~105°C)

Symbol	Parameter		-25		Unit	Specific Notes
			Min.	Max.		
$t_{CK(avg)}$	Average clock period	CL=4	3.75	8	ns	15, 33, 34
		CL=5	2.5	8	ns	15, 33, 34
		CL=6	2.5	8	ns	15, 33, 34
		CL=7	-	-	ns	15, 33, 34
$t_{CH(avg)}$	Average clock HIGH pulse width		0.48	0.52	t_{CK}	34, 35
$t_{CL(avg)}$	Average Clock LOW pulse width		0.48	0.52	t_{CK}	34, 35
WL	Write command to DQS associated clock edge		RL-1		t_{CK}	
t_{DQSS}	DQS latching rising transitions to associated clock edges		-0.25	0.25	t_{CK}	28
t_{DSS}	DQS falling edge to CK setup time		0.2	-	t_{CK}	28
t_{DSH}	DQS falling edge hold time from CK		0.2	-	t_{CK}	
t_{DQSH}	DQS input HIGH pulse width		0.35	-	t_{CK}	
t_{DQSL}	DQS input LOW pulse width		0.35	-	t_{CK}	
t_{WPRE}	Write preamble		0.35	-	t_{CK}	
t_{WPST}	Write postamble		0.4	0.6	t_{CK}	10
$t_{IS(base)}$	Address and Control input setup time		0.175	-	ns	5, 7, 9, 22, 27
$t_{IH(base)}$	Address and Control input hold time		0.25	-	ns	5, 7, 9, 23, 27
t_{IPW}	Control & Address input pulse width for each input		0.6	-	t_{CK}	
$t_{DS(base)}$	DQ & DM input setup time		0.05	-	ns	6-8, 20, 26, 29
$t_{DH(base)}$	DQ & DM input hold time		0.125	-	ns	6-8, 21, 26, 29
t_{DIPW}	DQ and DM input pulse width for each input		0.35	-	t_{CK}	
t_{AC}	DQ output access time from CK, CK#		-0.4	0.4	ns	38
t_{DQSCK}	DQS output access time from CK, CK#		-0.35	0.35	ns	38
t_{HZ}	Data-out high-impedance time from CK, CK#		-	t_{AC}(max)	ns	18, 38
$t_{LZ(DQS)}$	DQS(DQS#) low-impedance time from CK, CK#		t_{AC}(min)	t_{AC}(max)	ns	18, 38
$t_{LZ(DQ)}$	DQ low-impedance time from CK, CK#		$2t_{AC}$(min)	t_{AC}(max)	ns	18, 38
t_{DQSQ}	DQS-DQ skew for DQS and associated DQ signals		-	0.2	ns	13
t_{HP}	CK half pulse width		min (t_{CH},t_{CL})	-	ns	11, 12, 35
t_{QHS}	DQ hold skew factor		-	0.3	ns	12, 36
t_{QH}	DQ/DQS output hold time from DQS		t_{HP} -t_{QHS}	-	ns	37
t_{RPRE}	Read preamble		0.9	1.1	t_{CK}	19, 39
t_{RPST}	Read postamble		0.4	0.6	t_{CK}	19, 40
t_{RRD}	Active to active command period		10	-	ns	4, 30
t_{FAW}	Four Activate Window		45	-	ns	4, 30
t_{CCD}	CAS# to CAS# command delay		2	-	t_{CK}	
t_{WR}	Write recovery time		15	-	ns	30
t_{DAL}	Auto Power write recovery + precharge time		WR + t_{RP}	-	ns	14, 31
t_{WTR}	Internal Write to Read Command Delay		7.5	-	ns	3, 24, 30
t_{RTP}	Internal read to precharge command delay		7.5	-	ns	3, 30
t_{CKE}	CKE minimum pulse width		3	-	t_{CK}	25
t_{XSNR}	Exit self refresh to non-read command delay		t_{RFC}+10	-	ns	30
t_{XSRD}	Exit self refresh to a read command		200	-	t_{CK}	
t_{XP}	Exit precharge power down to any command		2	-	t_{CK}	
t_{XARD}	Exit active power down to read command		2	-	t_{CK}	1
t_{XARDS}	Exit active power down to read command(slow exit, lower power)		8-AL	-	t_{CK}	1, 2