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**Revision History****AS4C64M16D3A-12BCN/AS4C64M16D3A-12BIN 96 ball FBGA PACKAGE**

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Aug. 2016

## Features

- JEDEC Standard Compliant
- Power supplies:  $V_{DD}$  &  $V_{DDQ} = +1.5V \pm 0.075V$
- Operating temperature:
  - Commercial:  $0^{\circ}C$  to  $95^{\circ}C$  (TC)
  - Industrial :  $-40^{\circ}C$  to  $95^{\circ}C$  (TC)
- Supports JEDEC clock jitter specification
- Fully synchronous operation
- Fast clock rate: 800MHz
- Differential Clock, CK & CK#
- Bidirectional differential data strobe
  - DQS & DQS#
- 8 internal banks for concurrent operation
- 8n-bit prefetch architecture
- Pipelined internal architecture
- Precharge & active power down
- Programmable Mode & Extended Mode registers
- Additive Latency (AL): 0, CL-1, CL-2
- Programmable Burst lengths: 4, 8
- Burst type: Sequential / Interleave
- Output Driver Impedance Control
- 8192 refresh cycles / 64ms
  - Average refresh period
  - $7.8\mu s$  @  $-40^{\circ}C \leq TC \leq +85^{\circ}C$
  - $3.9\mu s$  @  $+85^{\circ}C < TC \leq +95^{\circ}C$
- Write Leveling
- ZQ Calibration
- Dynamic ODT (Rtt\_Nom & Rtt\_WR)
- RoHS compliant
- Auto Refresh and Self Refresh
- 96-ball 8 x 13 x 1.0mm FBGA package
  - Pb and Halogen Free

## Overview

The 1Gb Double-Data-Rate-3 DRAMs is double data rate architecture to achieve high-speed operation. It is internally configured as an eight bank DRAM.

The 1Gb chip is organized as 8Mbit x 16 I/Os x 8 bank devices. These synchronous devices achieve high speed double-data-rate transfer rates of up to 1600 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR3 DRAM key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK# falling). All I/Os are synchronized with differential DQS pair in a source synchronous fashion.

These devices operate with a single  $1.5V \pm 0.075V$  power supply and are available in BGA packages.

**Table 1. Ordering Information**

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C64M16D3A-12BCN	64M x 16	Commercial $0^{\circ}C$ to $95^{\circ}C$	800	96-ball FBGA
AS4C64M16D3A-12BIN	64M x 16	Industrial $-40^{\circ}C$ to $95^{\circ}C$	800	96-ball FBGA

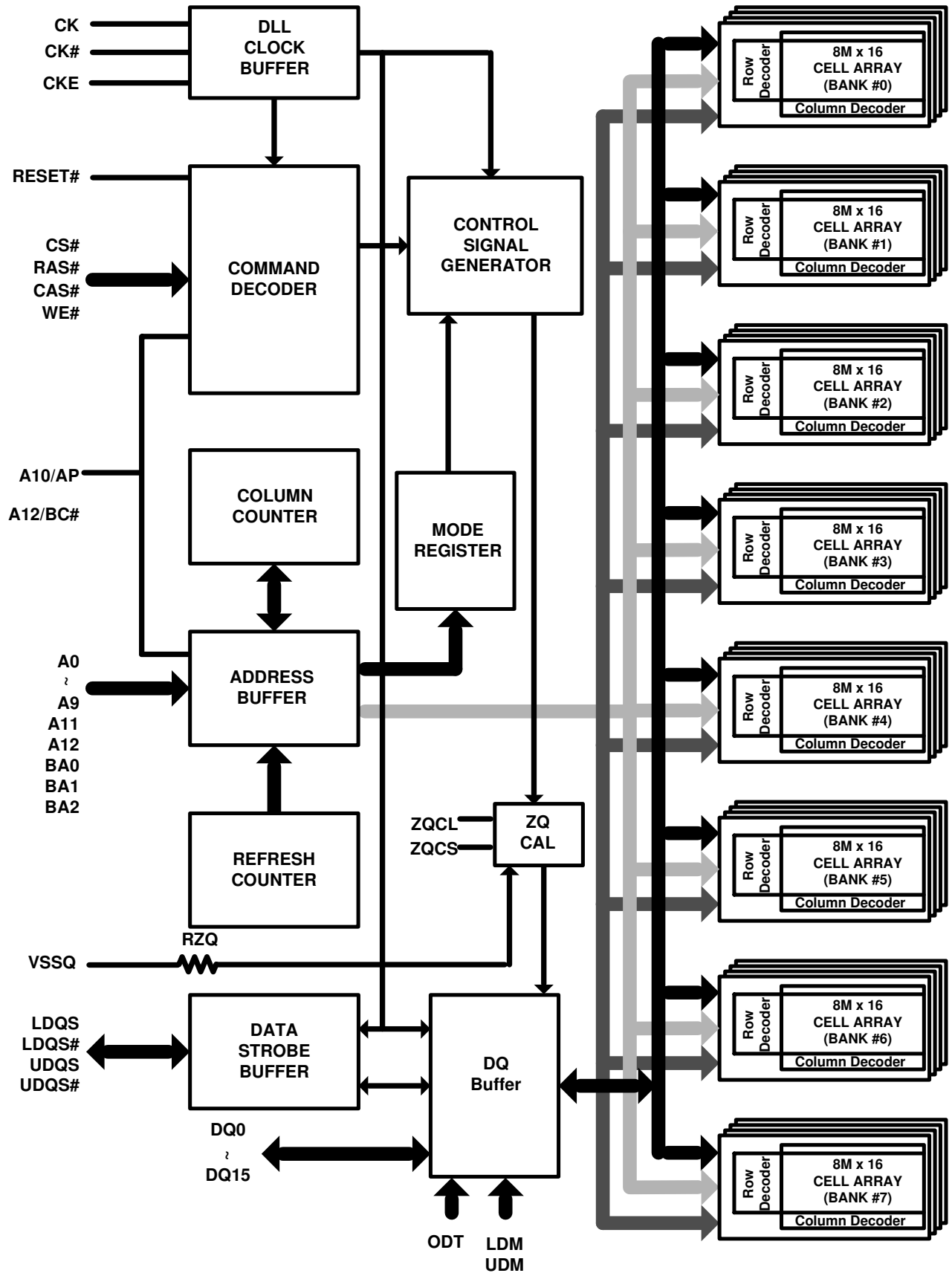
**Table 2. Speed Grade Information**

Speed Grade	Clock Frequency	CAS Latency	$t_{RCD}$ (ns)	$t_{RP}$ (ns)
DDR3-1600	800 MHz	11	13.75	13.75



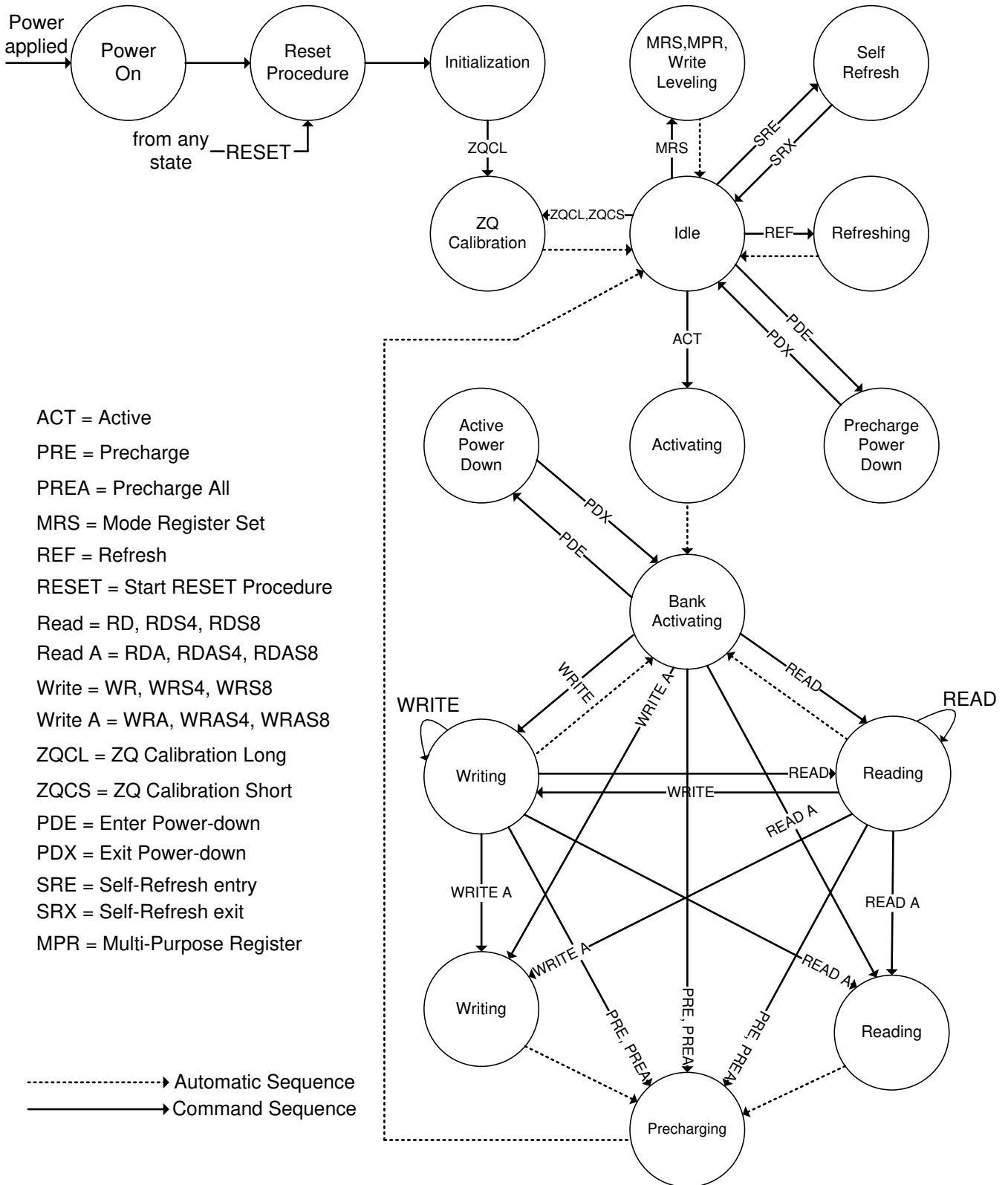
Figure 1. Ball Assignment (FBGA Top View)

	1	2	3	...	7	8	9
A	VDDQ	DQ13	DQ15		DQ12	VDDQ	VSS
B	VSSQ	VDD	VSS		UDQS#	DQ14	VSSQ
C	VDDQ	DQ11	DQ9		UDQS	DQ10	VDDQ
D	VSSQ	VDDQ	UDM		DQ8	VSSQ	VDD
E	VSS	VSSQ	DQ0		LDM	VSSQ	VDDQ
F	VDDQ	DQ2	LDQS		DQ1	DQ3	VSSQ
G	VSSQ	DQ6	LDQS#		VDD	VSS	VSSQ
H	VREFDQ	VDDQ	DQ4		DQ7	DQ5	VDDQ
J	NC	VSS	RAS#		CK	VSS	NC
K	ODT	VDD	CAS#		CK#	VDD	CKE
L	NC	CS#	WE#		A10/AP	ZQ	NC
M	VSS	BA0	BA2		NC	VREFCA	VSS
N	VDD	A3	A0		A12/BC#	BA1	VDD
P	VSS	A5	A2		A1	A4	VSS
R	VDD	A7	A9		A11	A6	VDD
T	VSS	RESET#	NC		NC	A8	VSS

**Figure 2. Block Diagram**


**Figure 3. State Diagram**

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail



**Ball Descriptions**
**Table 3. Ball Descriptions**

Symbol	Type	Description
CK, CK#	Input	<b>Differential Clock:</b> CK and CK# are driven by the system clock. All SDRAM input signals are sampled on the crossing of positive edge of CK and negative edge of CK#. Output (Read) data is referenced to the crossings of CK and CK# (both directions of crossing).
CKE	Input	<b>Clock Enable:</b> CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes LOW synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains LOW. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0-BA2	Input	<b>Bank Address:</b> BA0-BA2 define to which bank the BankActivate, Read, Write, or Bank Precharge command is being applied.
A0-A12	Input	<b>Address Inputs:</b> A0-A12 are sampled during the BankActivate command (row address A0-A12) and Read/Write command (column address A0-A9 with A10 defining Auto Precharge).
A10/AP	Input	<b>Auto-Precharge:</b> A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH).
A12/BC#	Input	<b>Burst Chop:</b> A12/BC# is sampled during Read and Write commands to determine if burst chop (on the fly) will be performed. (HIGH - no burst chop; LOW - burst chopped).
CS#	Input	<b>Chip Select:</b> CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. It is considered part of the command code.
RAS#	Input	<b>Row Address Strobe:</b> The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
CAS#	Input	<b>Column Address Strobe:</b> The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# "HIGH" or "LOW".
WE#	Input	<b>Write Enable:</b> The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
LDQS, LDQS# UDQS UDQS#	Input / Output	<b>Bidirectional Data Strobe:</b> Specifies timing for Input and Output data. Read Data Strobe is edge triggered. Write Data Strobe provides a setup and hold time for data and DQM. LDQS is for DQ0~7, UDQS is for DQ8~15. The data strobes LDOS and UDQS are paired with LDQS# and UDQS# to provide differential pair signaling to the system during both reads and writes.
LDM, UDM	Input	<b>Data Input Mask:</b> Input data is masked when DM is sampled HIGH during a write cycle. LDM masks DQ0-DQ7, UDM masks DQ8-DQ15.

DQ0 - DQ15	Input / Output	<b>Data I/O:</b> The DQ0-DQ15 input and output data are synchronized with positive and negative edges of DQS and DQS#. The I/Os are byte-maskable during Writes.
ODT	Input	<b>On Die Termination:</b> ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, DQS#. The ODT pin will be ignored if Mode-registers, MR1 and MR2, are programmed to disable RTT.
RESET#	Input	<b>Active Low Asynchronous Reset:</b> Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD
V <sub>DD</sub>	Supply	<b>Power Supply:</b> +1.5V ±0.075V
V <sub>SS</sub>	Supply	<b>Ground</b>
V <sub>DDQ</sub>	Supply	<b>DQ Power:</b> +1.5V ±0.075V.
V <sub>SSQ</sub>	Supply	<b>DQ Ground</b>
V <sub>REFCA</sub>	Supply	<b>Reference voltage for CA</b>
V <sub>REFDQ</sub>	Supply	<b>Reference voltage for DQ</b>
ZQ	Supply	<b>Reference pin for ZQ calibration.</b>
NC	-	<b>No Connect:</b> These pins should be left unconnected.



**Operation Mode Truth Table**
**Table 4. Truth Table (Note (1), (2))**

Command	State	CKE <sub>n-1</sub> <sup>(3)</sup>	CKE <sub>n</sub>	DM	BA0-2	A10/AP	A0-9, 11	A12/BC#	CS#	RAS#	CAS#	WE#
BankActivate	Idle <sup>(4)</sup>	H	H	X	V	Row address			L	L	H	H
Single Bank Precharge	Any	H	H	X	V	L	V	V	L	L	H	L
All Banks Precharge	Any	H	H	X	V	H	V	V	L	L	H	L
Write (Fixed BL8 or BC4)	Active <sup>(4)</sup>	H	H	X	V	L	V	V	L	H	L	L
Write (BC4, on the fly)	Active <sup>(4)</sup>	H	H	X	V	L	V	L	L	H	L	L
Write (BL8, on the fly)	Active <sup>(4)</sup>	H	H	X	V	L	V	H	L	H	L	L
Write with Autoprecharge (Fixed BL8 or BC4)	Active <sup>(4)</sup>	H	H	X	V	H	V	V	L	H	L	L
Write with Autoprecharge (BC4, on the fly)	Active <sup>(4)</sup>	H	H	X	V	H	V	L	L	H	L	L
Write with Autoprecharge (BL8, on the fly)	Active <sup>(4)</sup>	H	H	X	V	H	V	H	L	H	L	L
Read (Fixed BL8 or BC4)	Active <sup>(4)</sup>	H	H	X	V	L	V	V	L	H	L	H
Read (BC4, on the fly)	Active <sup>(4)</sup>	H	H	X	V	L	V	L	L	H	L	H
Read (BL8, on the fly)	Active <sup>(4)</sup>	H	H	X	V	L	V	H	L	H	L	H
Read with Autoprecharge (Fixed BL8 or BC4)	Active <sup>(4)</sup>	H	H	X	V	H	V	V	L	H	L	H
Read with Autoprecharge (BC4, on the fly)	Active <sup>(4)</sup>	H	H	X	V	H	V	L	L	H	L	H
Read with Autoprecharge (BL8, on the fly)	Active <sup>(4)</sup>	H	H	X	V	H	V	H	L	H	L	H
(Extended) Mode Register Set	Idle	H	H	X	V	OP code			L	L	L	L
No-Operation	Any	H	H	X	V	V	V	V	L	H	H	H
Device Deselect	Any	H	H	X	X	X	X	X	H	X	X	X
Refresh	Idle	H	H	X	V	V	V	V	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	V	V	V	V	L	L	L	H
SelfRefresh Exit	Idle	L	H	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H
Power Down Mode Entry	Idle	H	L	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H
Power Down Mode Exit	Any	L	H	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H
Data Input Mask Disable	Active	H	X	L	X	X	X	X	X	X	X	X
Data Input Mask Enable <sup>(5)</sup>	Active	H	X	H	X	X	X	X	X	X	X	X
ZQ Calibration Long	Idle	H	H	X	X	H	X	X	L	H	H	L
ZQ Calibration Short	Idle	H	H	X	X	L	X	X	L	H	H	L

**NOTE 1:** V=Valid data, X=Don't Care, L=Low level, H=High level

**NOTE 2:** CKEn signal is input level when commands are provided.

**NOTE 3:** CKEn-1 signal is input level one clock cycle before the commands are provided.

**NOTE 4:** These are states of bank designated by BA signal.

**NOTE 5:** LDM and UDM can be enabled respectively.

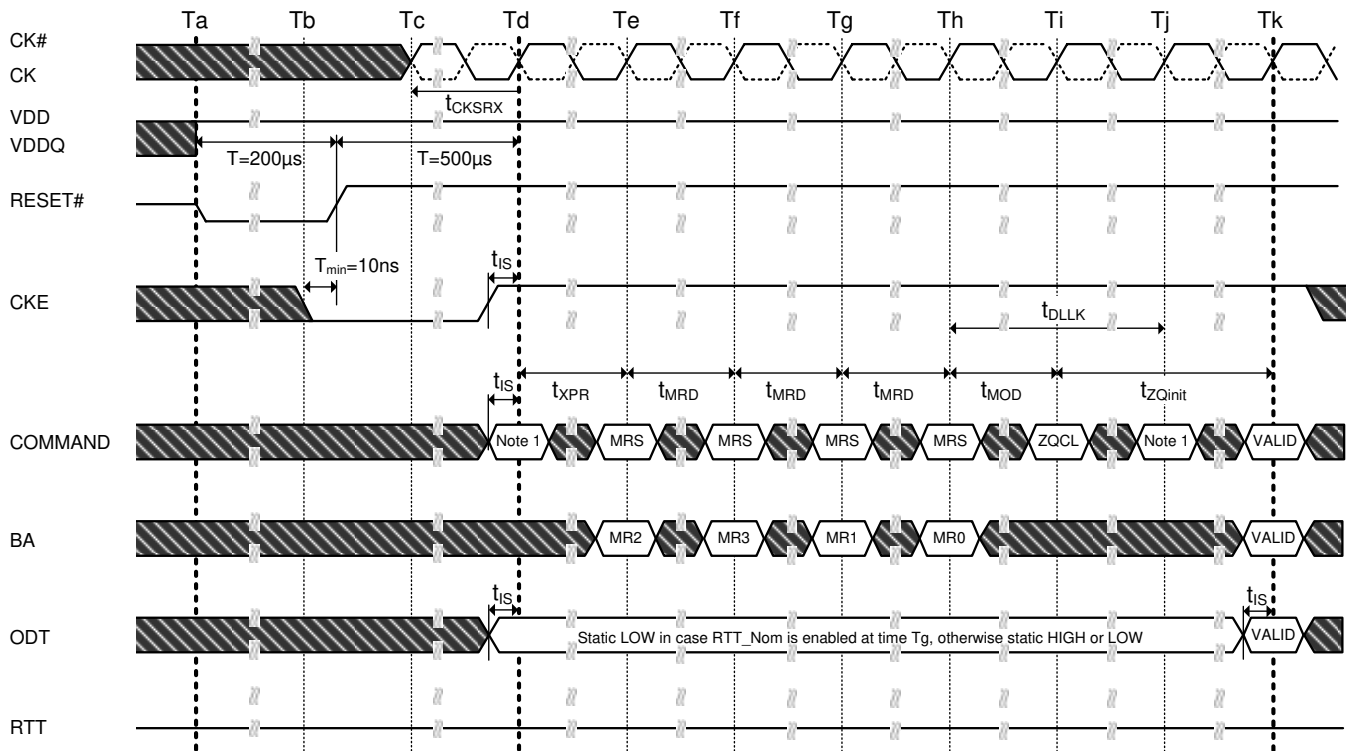
### Functional Description

The DDR3 SDRAM is a high-speed dynamic random access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation. The 8n Prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A12 select the row). The address bit registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

**Figure 4. Reset and Initialization Sequence at Power-on Ramping**



NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

▨ TIME BREAK    ▨ Don't Care

## Power-up and Initialization

The Following sequence is required for POWER UP and Initialization

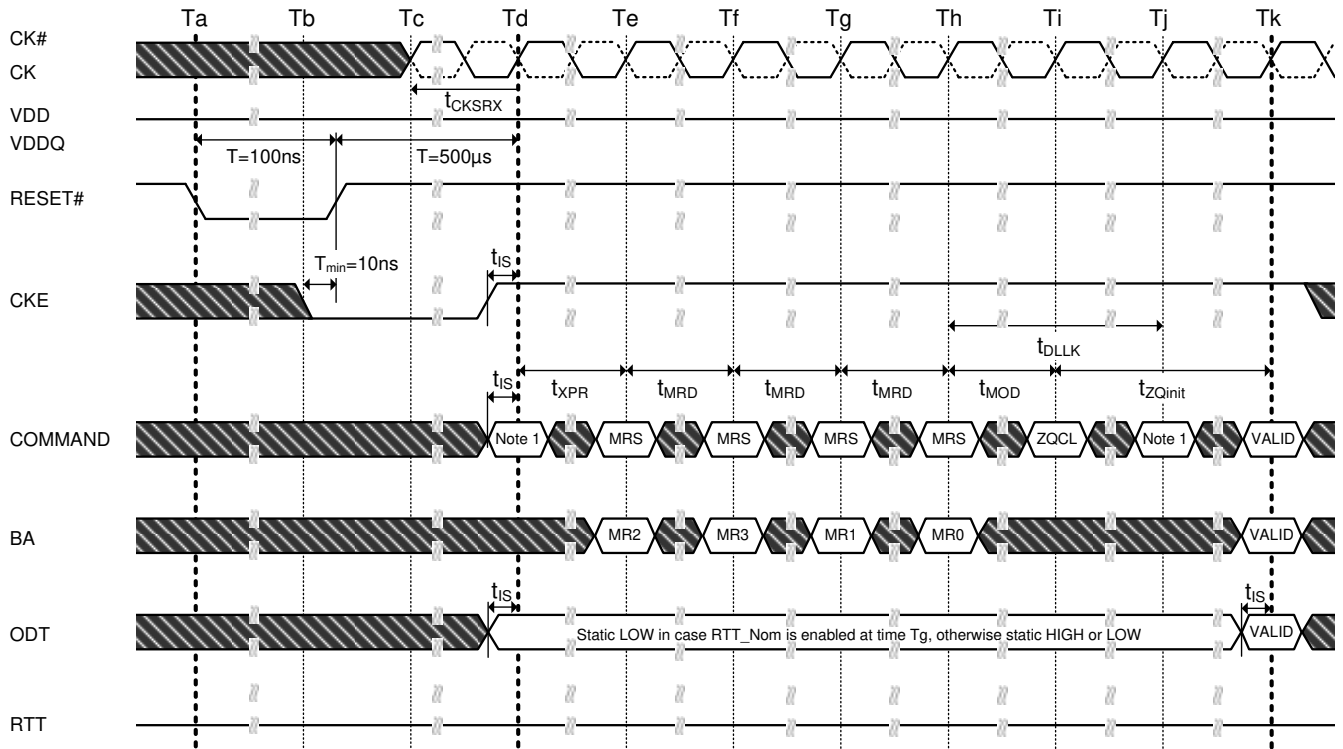
1. Apply power (RESET# is recommended to be maintained below  $0.2 \times VDD$ , all other inputs may be undefined). RESET# needs to be maintained for minimum 200us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDDmin must be no greater than 200ms; and during the ramp,  $VDD > VDDQ$  and  $(VDD - VDDQ) < 0.3$  Volts.
  - VDD and VDDQ are driven from a single power converter output, AND
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished, AND
  - Vref tracks  $VDDQ/2$ .OR
  - Apply VDD without any slope reversal before or at the same time as VDDQ.
  - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After RESET# is de-asserted, wait for another 500us until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clock (CK, CK#) need to be started and stabilized for at least 10ns or  $5t_{CK}$  (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock ( $t_{IS}$ ) must be meeting. Also a NOP or Deselect command must be registered (with  $t_{IS}$  set up time to clock) before CKE goes active. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of  $t_{DLLK}$  and  $t_{ZQinit}$ .
4. The DDR3 DRAM will keep its on-die termination in high impedance state as long as RESET# is asserted. Further, the DRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until  $t_{IS}$  before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If  $RTT\_NOM$  is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of  $t_{DLLK}$  and  $t_{ZQinit}$ .
5. After CKE being registered high, wait minimum of Reset CKE Exit time,  $t_{XPR}$ , before issuing the first MRS command to load mode register. ( $t_{XPR} = \max(t_{XS}, 5t_{CK})$ )
6. Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 and BA2)
9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command provide "High" to A8 and "Low" to BA0-BA2)
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both  $t_{DLLK}$  and  $t_{ZQinit}$  completed.
12. The DDR3 SDRAM is now ready for normal operation.

### Reset Procedure at Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below  $0.2 \cdot VDD$  anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100ns. CKE is pulled "Low" before RESET being de-asserted (min. time 10ns).
2. Follow Power-up Initialization Sequence step 2 to 11.
3. The Reset sequence is now completed. DDR3 SDRAM is ready for normal operation.

**Figure 5. Reset Procedure at Power Stable Condition**



**NOTE 1.** From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

⌘ TIME BREAK    ▨ Don't Care

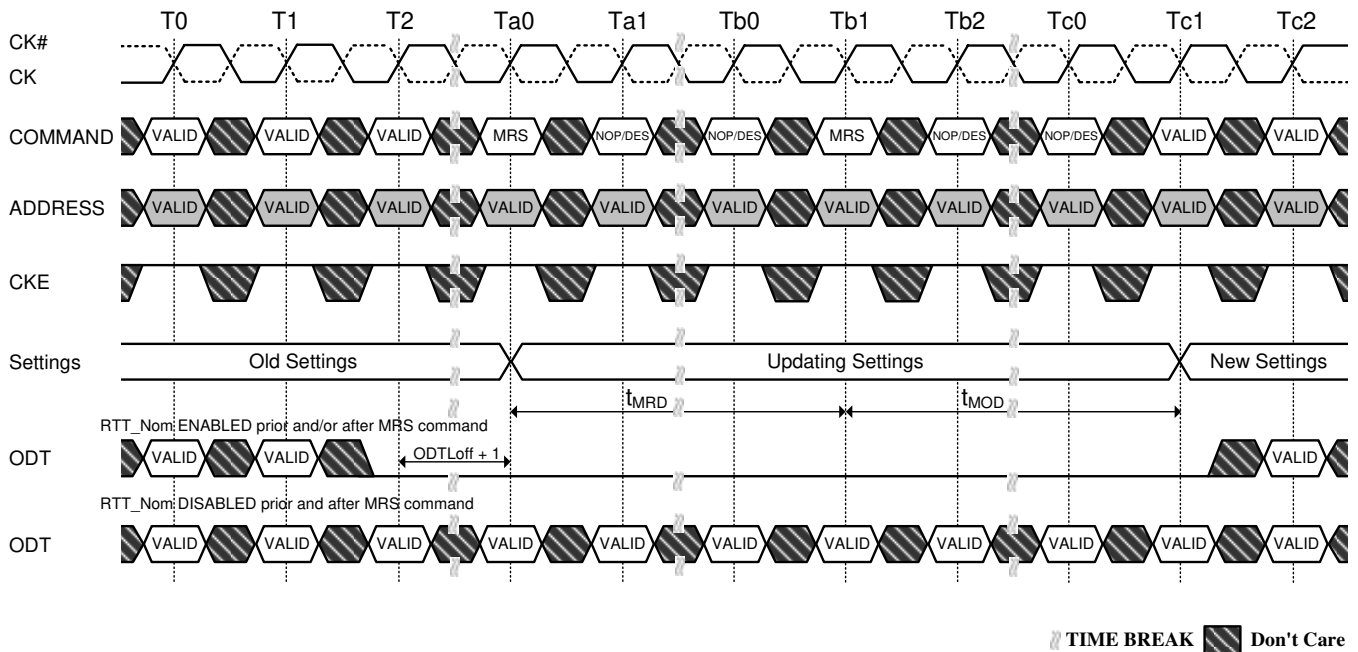
## Register Definition

### Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which mean these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time,  $t_{MRD}$  is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure of  $t_{MRD}$  timing.

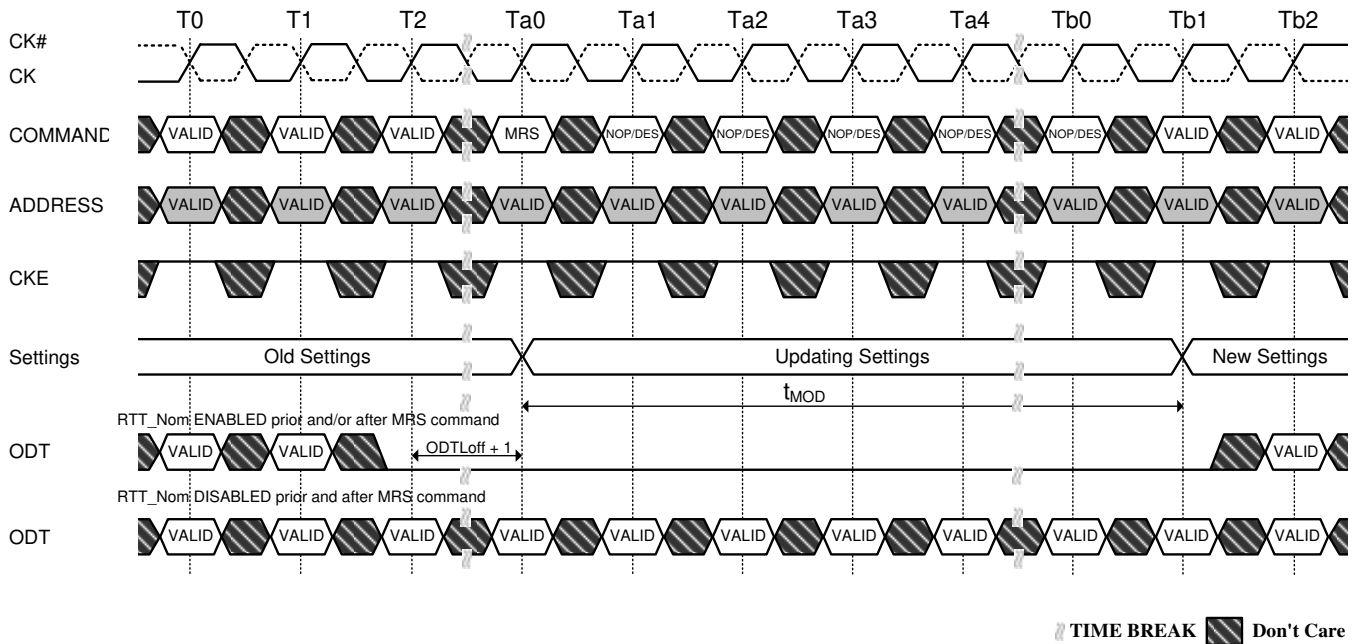
**Figure 6.  $t_{MRD}$  timing**





The MRS command to Non-MRS command delay,  $t_{MOD}$ , is required for the DRAM to update the features except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure of  $t_{MOD}$  timing.

**Figure 7.  $t_{MOD}$  timing**

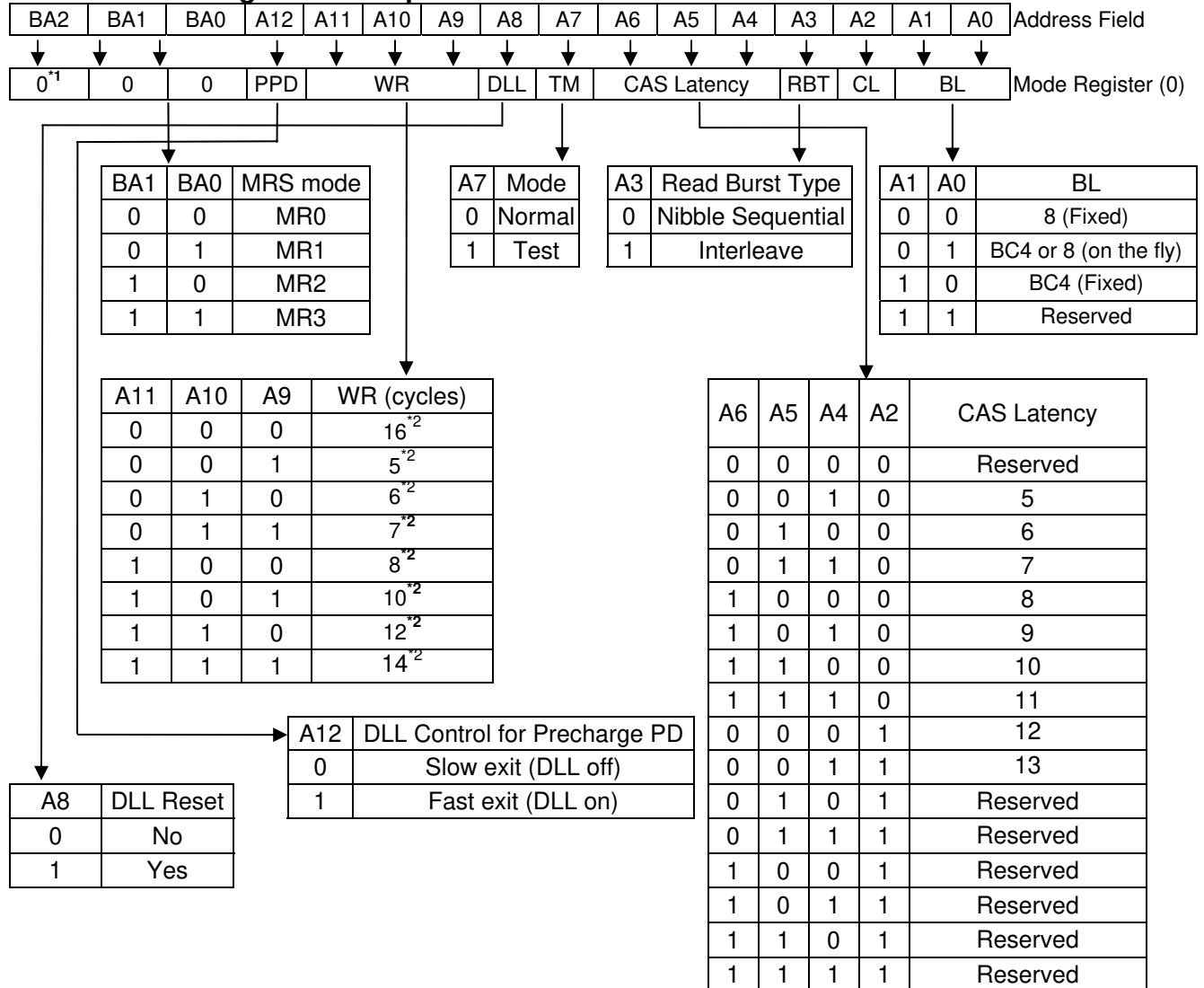


The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with  $t_{RP}$  satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

## Mode Register MR0

The mode-register MR0 stores data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR, and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 DRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to the following figure.

**Table 5. Mode Register Bitmap**



**Note 1:** BA2 and A2 are reserved for future use and must be set to 0 when programming the MR.

**Note 2:** WR (write recovery for autoprecharge) min in clock cycles is calculated by dividing tWR (ns) by tCK (ns) and rounding up to the next integer  $WR_{min} [cycles] = \text{Roundup}(tWR / tCK)$ . The value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

### - Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in the MR0 Definition as above figure. The ordering of access within a burst is determined by the burst length, burst type, and the starting column address. The burst length is defined by bits A0-A1. Burst lengths options include fix BC4, fixed BL8, and on the fly which allow BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#

**Table 6. Burst Type and Burst Order**

Burst Length	Read Write	Starting Column Address			Sequential A3=0	Interleave A3=1	Note
		A2	A1	A0			
4 Chop	Read	0	0	0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	1, 2, 3
		0	0	1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	
		0	1	0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	
		0	1	1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	
		1	0	0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	
		1	0	1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	
		1	1	0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	
		1	1	1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	
	Write	0	V	V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 2, 4, 5
		1	V	V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	
8	Read	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2
		0	0	1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0	1	0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0	1	1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1	0	1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1	1	0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		1	1	1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
	Write	V	V	V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2, 4

**Note 1:** In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

**Note 2:** 0~7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

**Note 3:** T: Output driver for data and strobcs are in high impedance.

**Note 4:** V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.

**Note 5:** X: Don't Care.

### - CAS Latency

The CAS Latency is defined by MR0 (bit A2, A4~A6) as shown in the MR0 Definition figure. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL);  $RL = AL + CL$ .

### - Test Mode

The normal operating mode is selected by MR0 (bit7=0) and all other bits set to the desired values shown in the MR0 definition figure. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM manufacturer and should not be used. No operations or functionality is guaranteed if A7=1.

### - DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Anytime the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations.)

### - Write Recovery

The programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (ns) by tCK (ns) and rounding up to the next integer: WR min [cycles] = Roundup (tWR [ns]/tCK [ns]). The WR must be programmed to be equal or larger than tWR (min).

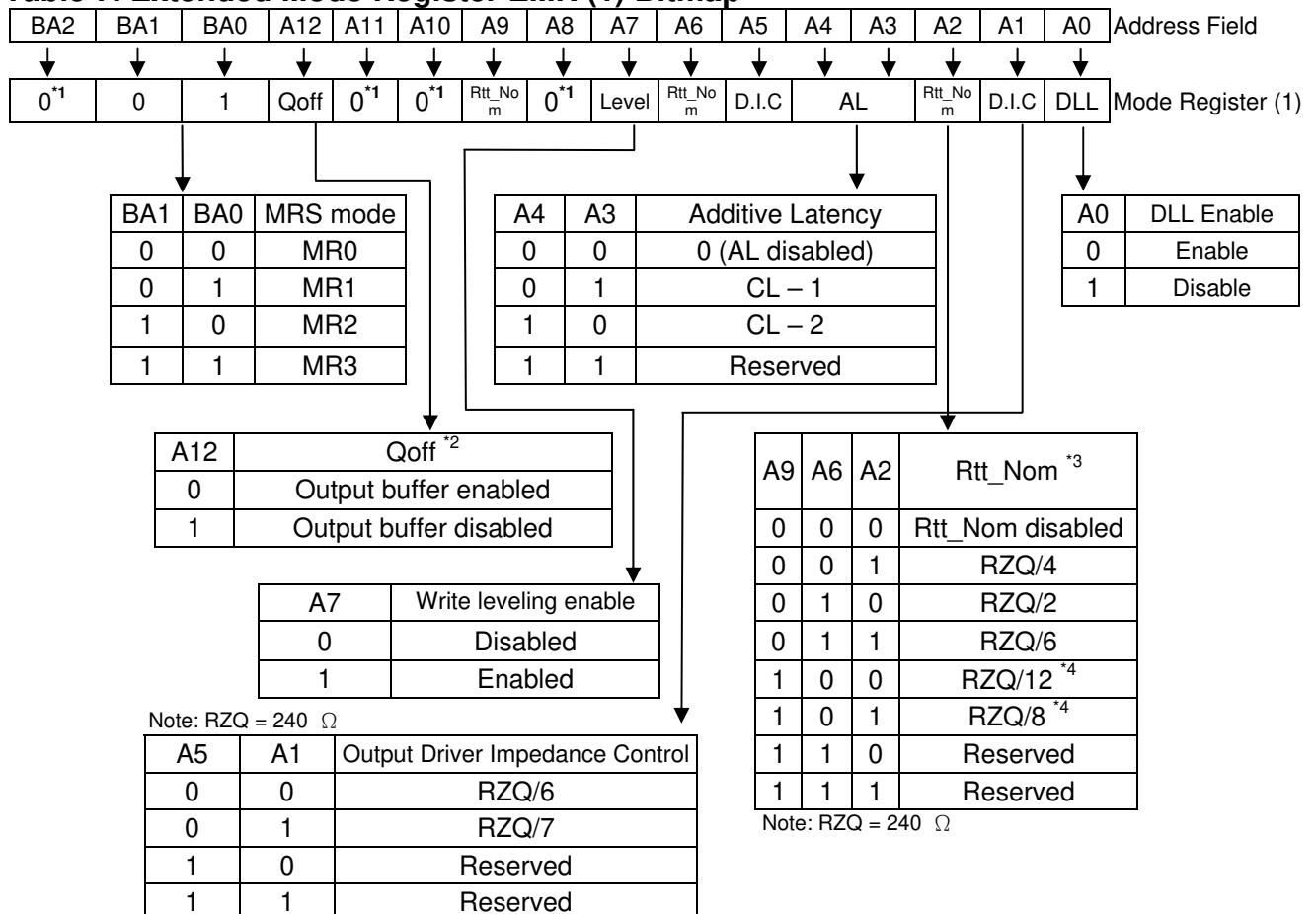
### - Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12=0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12=1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

## Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output strength, Rtt\_Nom impedance, additive latency, WRITE leveling enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to the following figure.

**Table 7. Extended Mode Register EMR (1) Bitmap**



**Note 1:** BA2 and A8, A10 ~ A11 are RFU and must be programmed to 0 during MRS.

**Note 2:** Outputs disabled - DQs, DQSs, DQS#s.

**Note 3:** In Write leveling Mode (MR1 [bit7] = 1) with MR1 [bit12] = 1, all RTT\_Nom settings are allowed; in Write Leveling Mode (MR1 [bit7] = 1) with MR1 [bit12] = 0, only RTT\_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

**Note 4:** If RTT\_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

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**- DLL Enable/Disable**

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0=0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSK, tAON, or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT\_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation are described in DLL-off Mode. The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT\_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt\_WR, MR2 {A10, A9} = {0, 0}, to disable Dynamic ODT externally

**- Output Driver Impedance Control**

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bit A1 and A5) as shown in MR1 definition figure.

**- ODT Rtt Values**

DDR3 SDRAM is capable of providing two different termination values (Rtt\_Nom and Rtt\_WR). The nominal termination value Rtt\_Nom is programmable in MR1. A separate value (Rtt\_WR) may be programmable in MR2 to enable a unique Rtt value when ODT is enabled during writes. The Rtt\_WR value can be applied during writes even when Rtt\_Nom is disabled.

**- Additive Latency (AL)**

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidth in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in MR.

**- Write leveling**

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the controller should support 'write leveling' in DDR3 SDRAM to compensate for skew.

**- Output Disable**

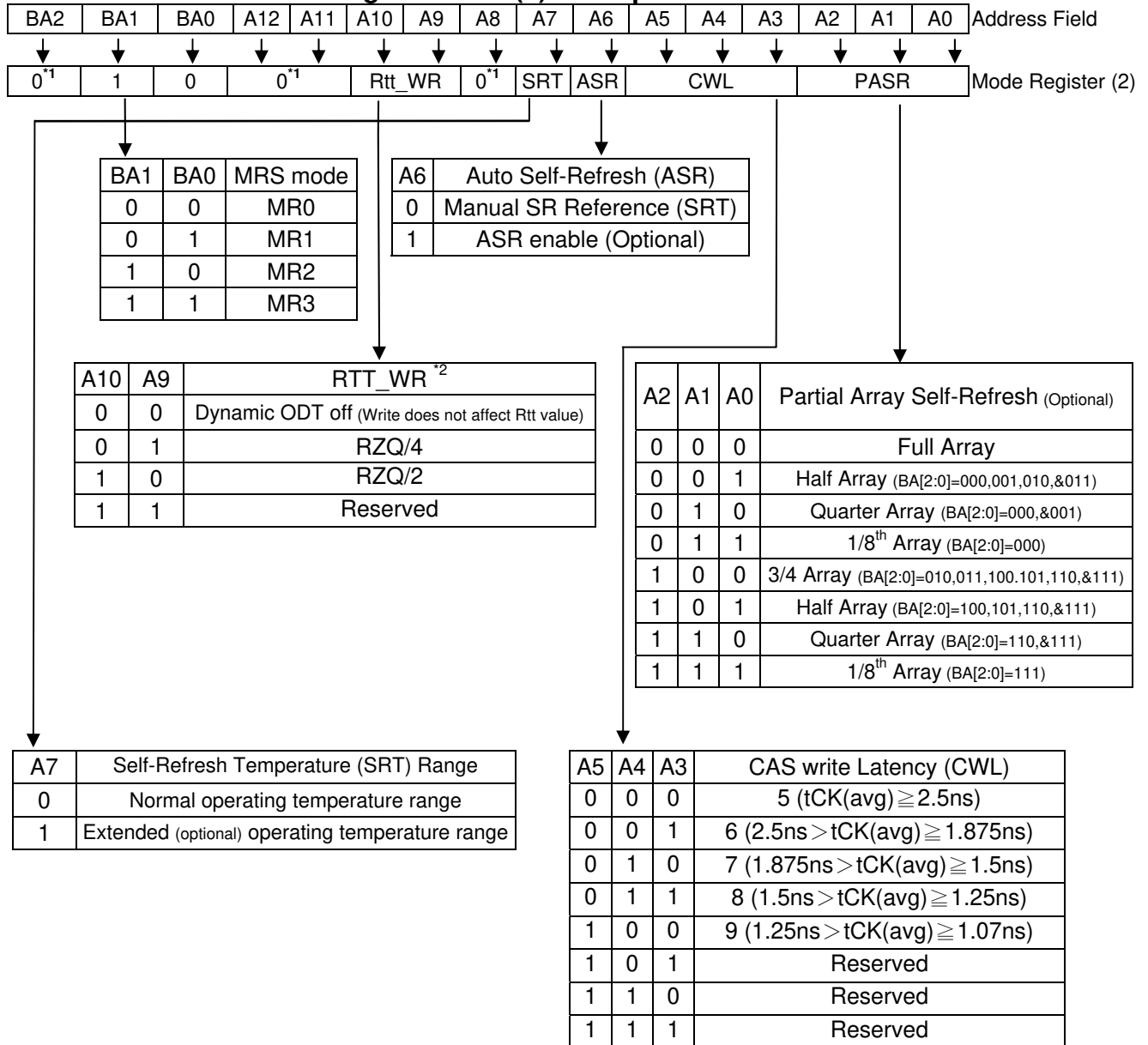
The DDR3 SDRAM outputs maybe enable/disable by MR1 (bit 12) as shown in MR1 definition. When this feature is enabled (A12=1) all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring modules power for example. For normal operation A12 should be set to '0'.



## Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt\_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

**Table 8. Extended Mode Register EMR (2) Bitmap**



**Note 1:** BA2 and A8, A11 ~ A12 are RFU and must be programmed to 0 during MRS.

**Note 2:** The Rtt\_WR value can be applied during writes even when Rtt\_Nom is disabled.  
During write leveling, Dynamic ODT is not available.

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**- Partial Array Self-Refresh (PASR)**

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

**- CAS Write Latency (CWL)**

The CAS Write Latency is defined by MR2 (bits A3-A5) shown in MR2. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 DRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL);  $WL=AL+CWL$ .

For more information on the supported CWL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins". For detailed Write operation refer to "WRITE Operation".

**- Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)**

DDR3 SDRAM must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the ASR function or program the SRT bit appropriately.

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. For more details refer to "Extended Temperature Usage". DDR3 SDRAMs must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

**- Dynamic ODT (Rtt\_WR)**

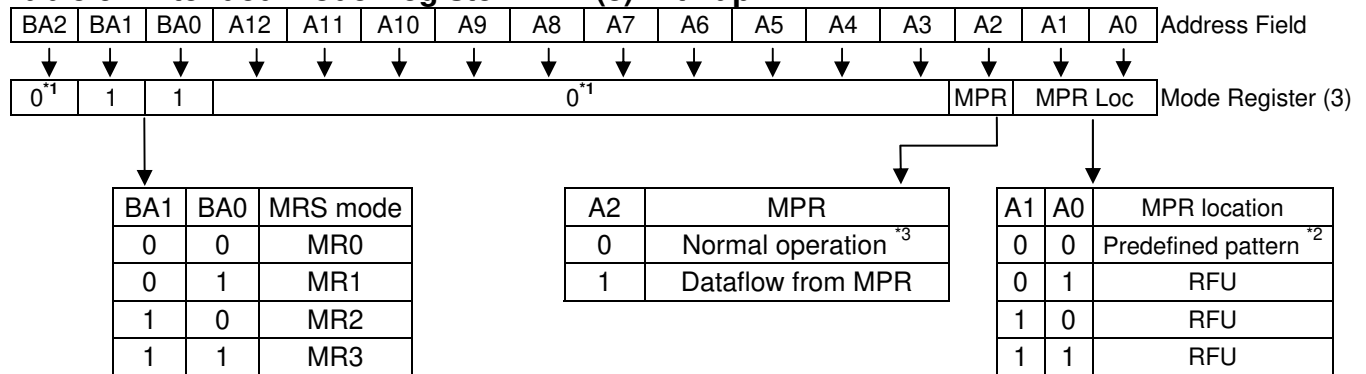
DDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings.

DDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only Rtt\_Nom is available. For details on Dynamic ODT operation, refer to "Dynamic ODT".

### Mode Register MR3

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below

**Table 9. Extended Mode Register EMR (3) Bitmap**



**Note 1:** BA2, A3 - A12 are RFU and must be programmed to 0 during MRS.

**Note 2:** The predefined pattern will be used for read synchronization.

**Note 3:** When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.

**Table 10. Absolute Maximum DC Ratings**

Symbol	Parameter	Values	Unit	Note
V <sub>DD</sub>	Voltage on VDD pin relative to Vss	-0.4 ~ 1.8	V	1,3
V <sub>VDDQ</sub>	Voltage on VDDQ pin relative to Vss	-0.4 ~ 1.8	V	1,3
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to Vss	-0.4 ~ 1.8	V	1
T <sub>STG</sub>	Storage temperature	-55 ~ 100	°C	1,2

**NOTE1:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**NOTE2:** Storage Temperature is the case surface temperature on the center/top side of the DRAM.

**NOTE3:** VDD and VDDQ must be within 300mV of each other at all times; and Vref must be not greater than 0.6VDDQ, when VDD and VDDQ are less than 500mV; Vref may be equal to or less than 300mV.

**Table 11. Temperature Range**

Symbol	Parameter	Values	Unit	Note
T <sub>OPER</sub>	Normal Operating Temperature Range	0 ~ 85	°C	1,2
	Extended Temperature Range	85 ~ 95	°C	1,3
	Industrial Temperature Range	-40 ~ 95	°C	1-4

**NOTE1:** Operating temperature is the case surface temperature on center/top of the DRAM.

**NOTE2:** The operating temperature range is the temperature where all DRAM specification will be supported.

Outside of this temperature range, even if it is still within the limit of stress condition, some deviation on portion of operating specification may be required. During operation, the DRAM case temperature must be maintained between 0-85°C under all other specification parameter. Supporting 0 - 85 °C with full JEDEC AC & DC specifications.

**NOTE3:** Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are guaranteed in this range, but the following additional apply.

- a) Refresh commands must be doubled in frequency, therefore, reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1x refresh (tREFI to 7.8us) in the Extended Temperature Range.
- b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0 and MR2 A7=1) or enable the optional Auto Self-Refresh mode (MR2 A6=1 and MR2 A7=0).

**NOTE4:** During Industrial Temperature Operation Range, the DRAM case temperature must be maintained between -40°C~95°C under all operating Conditions.

**Table 12. Recommended DC Operating Conditions**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V <sub>DD</sub>	Power supply voltage	1.425	1.5	1.575	V	1,2
V <sub>VDDQ</sub>	Power supply voltage for output	1.425	1.5	1.575	V	1,2

**NOTE1:** Under all conditions VDDQ must be less than or equal to VDD.

**NOTE2:** VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

**Table 13. Single-Ended AC and DC Input Levels for Command and Address**

Symbol	Parameter	-12		Unit	Note
		Min.	Max.		
V <sub>IH.CA(DC100)</sub>	DC input logic high	V <sub>REF+0.1</sub>	V <sub>DD</sub>	V	1,5
V <sub>IL.CA(DC100)</sub>	DC input logic low	V <sub>SS</sub>	V <sub>REF-0.1</sub>	V	1,6
V <sub>IH.CA(AC175)</sub>	AC input logic high	V <sub>REF+0.175</sub>	-	V	1,2
V <sub>IL.CA(AC175)</sub>	AC input logic low	-	V <sub>REF-0.175</sub>	V	1,2
V <sub>IH.CA(AC150)</sub>	AC input logic high	V <sub>REF+0.15</sub>	-	V	1,2
V <sub>IL.CA(AC150)</sub>	AC input logic low	-	V <sub>REF-0.15</sub>	V	1,2
V <sub>IH.CA(AC135)</sub>	AC input logic high	-	-	V	1,2
V <sub>IL.CA(AC135)</sub>	AC input logic low	-	-	V	1,2
V <sub>RefCA(DC)</sub>	Reference Voltage for ADD, CMD inputs	0.49xV <sub>DD</sub>	0.51xV <sub>DD</sub>	V	3,4

**NOTE 1:** For input only pins except RESET#. Vref = VrefCA(DC).

**NOTE 2:** See "Overshoot and Undershoot Specifications".

**NOTE 3:** The ac peak noise on VRef may not allow VRef to deviate from VRefCA(DC) by more than +/-1% VDD.

**NOTE 4:** For reference: approx. VDD/2 +/- 15 mV.

**NOTE 5:** VIH(dc) is used as a simplified symbol for VIH.CA(DC100)

**NOTE 6:** VIL(dc) is used as a simplified symbol for VIL.CA(DC100)

**NOTE 7:** VIH(ac) is used as a simplified symbol for VIH.CA(AC175), VIH.CA(AC150), VIH.CA(AC135) and VIH.CA(AC175) value is used when Vref + 0.175V is referenced, VIH.CA(AC150) value is used when Vref + 0.150V is referenced, VIH.CA(AC135) value is used when Vref + 0.135V is referenced.

**NOTE 8:** VIL(ac) is used as a simplified symbol for VIL.CA(AC175), VIL.CA(AC150), VIL.CA(AC135) and VIL.CA(AC175) value is used when Vref - 0.175V is referenced, VIL.CA(AC150) value is used when Vref - 0.150V is referenced, VIL.CA(AC135) value is used when Vref - 0.135V is referenced.

**Table 14. Single-Ended AC and DC Input Levels for DQ and DM**

Symbol	Parameter	-12		Unit	Note
		Min.	Max.		
V <sub>IH.DQ(DC100)</sub>	DC input logic high	V <sub>REF+0.1</sub>	V <sub>DD</sub>	V	1,5
V <sub>IL.DQ(DC100)</sub>	DC input logic low	V <sub>SS</sub>	V <sub>REF-0.1</sub>	V	1,6
V <sub>IH.DQ(AC150)</sub>	AC input logic high	V <sub>REF+0.15</sub>	-	V	1,2
V <sub>IL.DQ(AC150)</sub>	AC input logic low	-	V <sub>REF-0.15</sub>	V	1,2
V <sub>IH.DQ(AC135)</sub>	AC input logic high	-	-	V	1,2
V <sub>IL.DQ(AC135)</sub>	AC input logic low	-	-	V	1,2
V <sub>RefDQ(DC)</sub>	Reference Voltage for DQ, DM inputs	0.49xV <sub>DD</sub>	0.51xV <sub>DD</sub>	V	3,4

**NOTE 1:** Vref = VrefDQ(DC).

**NOTE 2:** See "Overshoot and Undershoot Specifications".

**NOTE 3:** The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD.

**NOTE 4:** For reference: approx. VDD/2 +/- 15 mV.

**NOTE 5:** VIH(dc) is used as a simplified symbol for VIH.DQ(DC100)

**NOTE 6:** VIL(dc) is used as a simplified symbol for VIL.DQ(DC100)

**NOTE 7:** VIH(ac) is used as a simplified symbol for VIH.DQ(AC150), VIH.DQ(AC135) and VIH.DQ(AC150) value is used when Vref + 0.150V is referenced, VIH.DQ(AC135) value is used when Vref + 0.135V is referenced.

**NOTE 8:** VIL(ac) is used as a simplified symbol for VIL.DQ(AC150), VIL.DQ(AC135) and VIL.DQ(AC150) value is used when Vref - 0.150V is referenced, VIL.DQ(AC135) value is used when Vref - 0.135V is referenced.



**Table 15. Differential AC and DC Input Levels**

Symbol	Parameter	-12		Unit	Note
		Min.	Max.		
V <sub>IHdiff</sub>	Differential input high	+ 0.2	Note 3	V	1
V <sub>ILdiff</sub>	Differential input logic low	Note 3	- 0.2	V	1
V <sub>IHdiff(ac)</sub>	Differential input high ac	2 x (V <sub>IH(ac)</sub> - V <sub>REF</sub> )	Notes 3	V	2
V <sub>ILdiff(ac)</sub>	Differential input low ac	Note 3	2 x (V <sub>IL(ac)</sub> - V <sub>REF</sub> )	V	2

**NOTE 1:** Used to define a differential signal slew-rate.

**NOTE 2:** For CK - CK# use V<sub>IH</sub>/V<sub>IL</sub>(ac) of ADD/CMD and V<sub>REFCA</sub>; for DQSL, DQSL#, DQSU, DQSU# use V<sub>IH</sub>/V<sub>IL</sub>(ac) of DQs and V<sub>REFDQ</sub>; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

**NOTE 3:** These values are not defined; however, the single-ended signals CK, CK#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (V<sub>IH</sub>(dc) max, V<sub>IL</sub>(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

**Table 16. Capacitance (V<sub>DD</sub> = 1.5V, f = 1MHz, T<sub>OPER</sub> = 25 °C)**

Symbol	Parameter	-12		Unit	Note
		Min.	Max.		
C <sub>IO</sub>	Input/output capacitance, (DQ, DM, DQS, DQS#)	1.4	2.3	pF	1, 2, 3
C <sub>CK</sub>	Input capacitance, CK and CK#	0.8	1.4	pF	2, 3
C <sub>DCK</sub>	Input capacitance delta, CK and CK#	0	0.15	pF	2, 3, 4
C <sub>DDQS</sub>	Input/output capacitance delta, DQS and DQS#	0	0.15	pF	2, 3, 5
C <sub>I</sub>	Input capacitance, (CTRL, ADD, CMD input-only pins)	0.75	1.3	pF	2, 3, 6
C <sub>DI_CTRL</sub>	Input capacitance delta, (All CTRL input-only pins)	-0.4	0.2	pF	2, 3, 7, 8
C <sub>DI_ADD_CMD</sub>	Input capacitance delta, (All ADD, CMD input-only pins)	-0.4	0.4	pF	2, 3, 9, 10
C <sub>DIO</sub>	Input/output capacitance delta, (DQ, DM, DQS, DQS#)	-0.5	0.3	pF	2, 3, 11
C <sub>ZQ</sub>	Input/output capacitance of ZQ pin	-	3	pF	2, 3, 12

**NOTE 1:** Although the DM pins have different functions, the loading matches DQ and DQS.

**NOTE 2:** This parameter is not subject to production test. It is verified by design and characterization. V<sub>DD</sub>=V<sub>DDQ</sub>=1.5V, V<sub>BIAS</sub>=V<sub>DD</sub>/2 and ondie termination off.

**NOTE 3:** This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.

**NOTE 4:** Absolute value of C<sub>CK</sub>-C<sub>CK#</sub>.

**NOTE 5:** Absolute value of C<sub>IO</sub>(DQS)-C<sub>IO</sub>(DQS#).

**NOTE 6:** C<sub>I</sub> applies to ODT, CS#, CKE, A0-A12, BA0-BA2, RAS#, CAS#, WE#.

**NOTE 7:** C<sub>DI\_CTRL</sub> applies to ODT, CS# and CKE.

**NOTE 8:** C<sub>DI\_CTRL</sub>=C<sub>I</sub>(CTRL)-0.5\*(C<sub>I</sub>(CK)+C<sub>I</sub>(CK#)).

**NOTE 9:** C<sub>DI\_ADD\_CMD</sub> applies to A0-A12, BA0-BA2, RAS#, CAS# and WE#.

**NOTE 10:** C<sub>DI\_ADD\_CMD</sub>=C<sub>I</sub>(ADD\_CMD) - 0.5\*(C<sub>I</sub>(CK)+C<sub>I</sub>(CK#)).

**NOTE 11:** C<sub>DIO</sub>=C<sub>IO</sub>(DQ,DM) - 0.5\*(C<sub>IO</sub>(DQS)+C<sub>IO</sub>(DQS#)).

**NOTE 12:** Maximum external load capacitance on ZQ pin: 5 pF.

**Table 17. IDD specification parameters and test conditions ( $V_{DD} = 1.5V \pm 0.075V$ ,  $T_{OPER} = -40 \sim 95 \text{ } ^\circ\text{C}$ )**

Parameter & Test Condition	Symbol	-12	Unit
		Max.	
<b>Operating One Bank Active-Precharge Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS#:</b> High between ACT and PRE; <b>Command, Address, Bank Address Inputs:</b> partially toggling; <b>Data IO:</b> MID-LEVEL; <b>DM:</b> stable at 0; <b>Bank Activity:</b> Cycling with one bank active at a time: 0,0,1,1,2,2,...; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0.	I <sub>DD0</sub>	55	mA
<b>Operating One Bank Active-Read-Precharge Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1,7</sup> ; <b>AL:</b> 0; <b>CS#:</b> High between ACT, RD and PRE; <b>Command, Address, Bank Address Inputs, Data IO:</b> partially toggling; <b>DM:</b> stable at 0; <b>Bank Activity:</b> Cycling with one bank active at a time: 0,0,1,1,2,2,...; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0.	I <sub>DD1</sub>	67	mA
<b>Precharge Standby Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS#:</b> stable at 1; <b>Command, Address, Bank Address Inputs:</b> partially toggling; <b>Data IO:</b> MID-LEVEL; <b>DM:</b> stable at 0; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0.	I <sub>DD2N</sub>	24	mA
<b>Precharge Power-Down Current Slow Exit</b> <b>CKE:</b> Low; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS#:</b> stable at 1; <b>Command, Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> MID-LEVEL; <b>DM:</b> stable at 0; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Precharge Power Down Mode:</b> Slow Exit. <sup>3</sup>	I <sub>DD2P0</sub>	11	mA
<b>Precharge Power-Down Current Fast Exit</b> <b>CKE:</b> Low; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS#:</b> stable at 1; <b>Command, Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> MID-LEVEL; <b>DM:</b> stable at 0; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Precharge Power Down Mode:</b> Fast Exit. <sup>3</sup>	I <sub>DD2P1</sub>	13	mA
<b>Precharge Quiet Standby Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS#:</b> stable at 1; <b>Command, Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> MID-LEVEL; <b>DM:</b> stable at 0; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0.	I <sub>DD2Q</sub>	19	mA
<b>Active Standby Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS#:</b> stable at 1; <b>Command, Address, Bank Address Inputs:</b> partially toggling; <b>Data IO:</b> MID-LEVEL; <b>DM:</b> stable at 0; <b>Bank Activity:</b> all banks open; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0.	I <sub>DD3N</sub>	44	mA
<b>Active Power-Down Current</b> <b>CKE:</b> Low; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS#:</b> stable at 1; <b>Command, Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> MID-LEVEL; <b>DM:</b> stable at 0; <b>Bank Activity:</b> all banks open; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0	I <sub>DD3P</sub>	26	mA
<b>Operating Burst Read Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1,7</sup> ; <b>AL:</b> 0; <b>CS#:</b> High between RD; <b>Command, Address, Bank Address Inputs:</b> partially toggling; <b>DM:</b> stable at 0; <b>Bank Activity:</b> all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0.	I <sub>DD4R</sub>	141	mA
<b>Operating Burst Write Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS#:</b> High between WR; <b>Command, Address, Bank Address Inputs:</b> partially toggling; <b>DM:</b> stable at 0; <b>Bank Activity:</b> all banks open. <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at HIGH.	I <sub>DD4W</sub>	150	mA

<b>Burst Refresh Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS#:</b> High between tREF; <b>Command, Address, Bank Address Inputs:</b> partially toggling; <b>Data IO:</b> MID-LEVEL; <b>DM:</b> stable at 0; <b>Bank Activity:</b> REF command every tRFC; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0.		I <sub>DD5B</sub>	103	mA	
<b>Self Refresh Current:</b> <b>Auto Self-Refresh (ASR):</b> Disabled <sup>4</sup> ; <b>Self-Refresh Temperature Range (SRT):</b> Normal <sup>5</sup> ; <b>CKE:</b> Low; <b>External clock:</b> Off; <b>CK and CK#:</b> LOW; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS#,</b> <b>Command, Address, Bank Address, Data IO:</b> MID-LEVEL; <b>DM:</b> stable at 0; <b>Bank Activity:</b> Self-Refresh operation; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> MID-LEVEL		T <sub>CASE</sub> : 0 - 85°C	I <sub>DD6</sub>	11	mA
		T <sub>CASE</sub> : -40 - 95°C	I <sub>DD6ET</sub>	12	mA
<b>Operating Bank Interleave Read Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>BL:</b> 8 <sup>1,7</sup> ; <b>AL:</b> CL-1; <b>CS#:</b> High between ACT and RDA; <b>Command, Address, Bank Address Inputs:</b> partially toggling; <b>DM:</b> stable at 0; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0.		I <sub>DD7</sub>	212	mA	
<b>RESET Low Current</b> <b>RESET:</b> LOW; <b>External clock:</b> Off; <b>CK and CK#:</b> LOW; <b>CKE:</b> FLOATING; <b>CS#, Command, Address, Bank Address, Data IO:</b> FLOATING; <b>ODT Signal:</b> FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.		I <sub>DD8</sub>	11	mA	

**NOTE 1:** Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

**NOTE 2:** Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT\_Nom enable: set MR1 A[9,6,2] = 011B; RTT\_Wr enable: set MR2 A[10,9] = 10B

**NOTE 3:** Pecharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit

**NOTE 4:** Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

**NOTE 5:** Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range

**NOTE 6:** Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device

**NOTE 7:** Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B