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# AS5030

## 8-Bit Programmable High Speed Magnetic Rotary Encoder

## 1 General Description

The AS5030 is a contactless magnetic rotary encoder for accurate angular measurement over a full turn of 360°.
It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip is required.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 8 bit = 256 positions per revolution. This digital data is available as a serial bit stream and as a PWM signal.

In addition to the angle information, the strength of the magnetic field is also available as a 6-bit code.

Data transmission can be configured for 1-wire (PWM), 2-wires (CLK, DIO) or 3-wires (CLK, DIO, CS).

A software programmable (OTP) zero position simplifies assembly as the zero position of the magnet does not need to be mechanically aligned.

A Power Down Mode together with fast startup- and measurement cycles allows for very low average power consumption and makes the AS5030 also suitable for battery operated equipment.

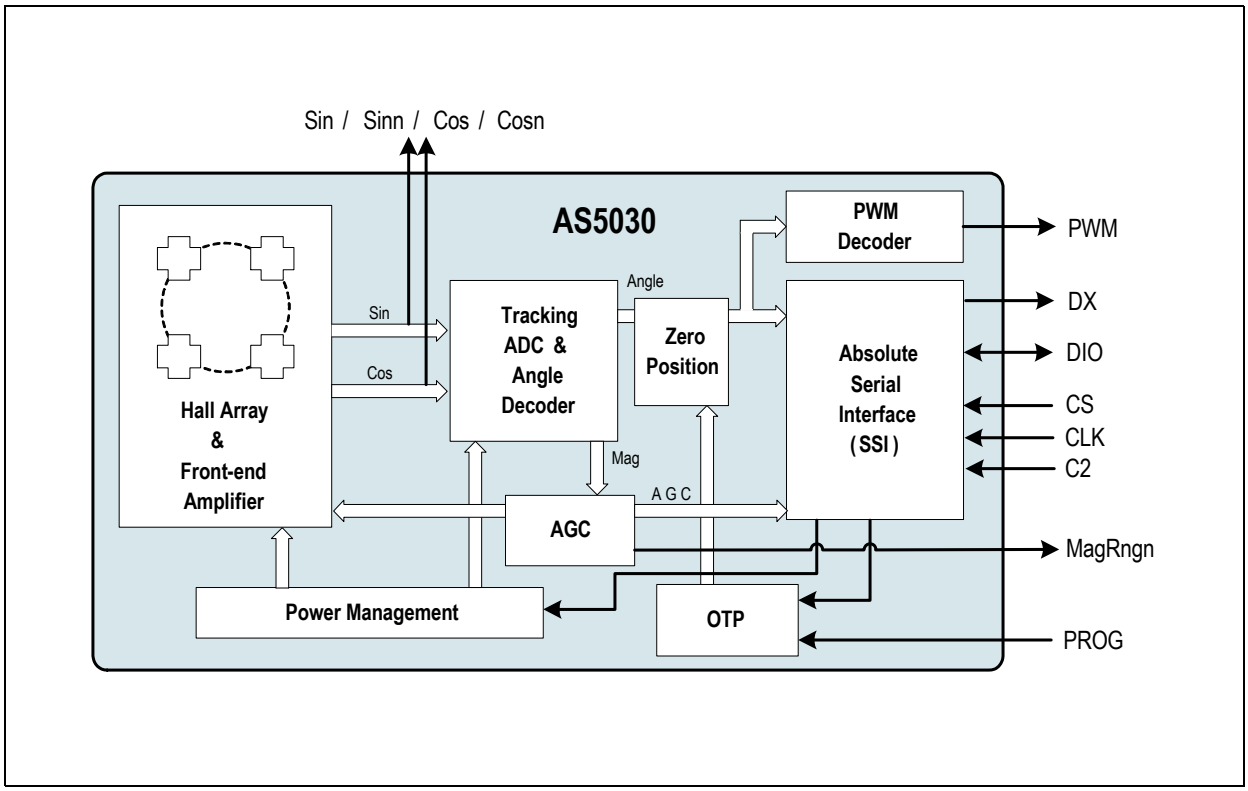
## 2 Key Features

- 360° contactless angular position encoding
- Two digital 8-bit absolute outputs:
  - Serial interface
  - Pulse width modulated (PWM) output
- User programmable zero position
- Direct measurement of magnetic field strength allows exact determination of vertical magnet distance
- Serial read-out of multiple interconnected AS5030 devices using daisy chain mode
- Wide magnetic field input range: 20 ~ 80mT
- Wide temperature range: -40°C to +125°C
- Small Pb-free package: TSSOP 16

## 3 Applications

The AS5030 is suitable for Contactless rotary position sensing, Rotary switches (human machine interface), AC/DC motor position control, Robotics and Encoder for battery operated equipment.

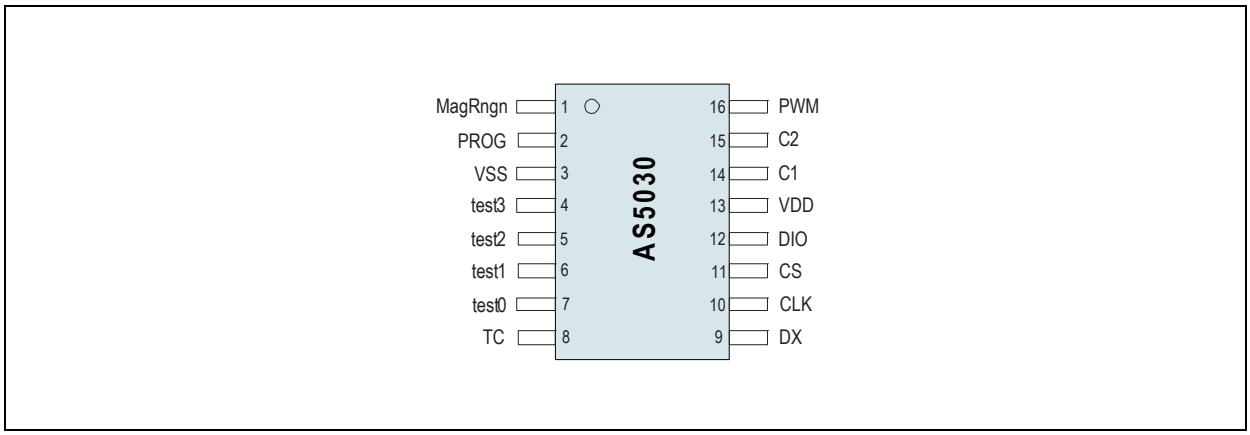
*Figure 1. AS5030 Block Diagram*



## Contents

# 4 Pin Assignments

*Figure 2. Pin Assignments (Top View)*




## 4.1 Pin Descriptions

*Table 1. Pin Descriptions*

| Pin Number | Pin Name | Pin Type | Description |
|---|---|---|---|
| 1 | MagRngn | Digital output / tri-state | Push-Pull output. Is 'HIGH' when the magnetic field strength is too weak, e.g. due to missing magnet |
| 2 | PROG | Supply pin | Programming voltage input. Must be left open in normal operation. Maximum load = 20pF (except during programming) |
| 3 | VSS | | Supply ground |
| 4 | T3_SINn | - | This pin is used for factory testing. For normal operation it must be left unconnected. Inverse SIN (Sinn) output in SIN/COS output mode |
| 5 | T2_SIN | - | This pin is used for factory testing. For normal operation it must be left unconnected. SIN output in SIN/COS mode |
| 6 | T1_COSn | - | This pin is used for factory testing. For normal operation it must be left unconnected. Inverse COS (Cosn) output in SIN/COS mode |
| 7 | T0_COS | - | This pin is used for factory testing. For normal operation it must be left unconnected. COS output in SIN/COS mode |
| 8 | TC | - | Test pin. Connect to VSS or leave unconnected |
| 9 | DX | Digital output | Digital output for 2-wire operation and Daisy Chain mode |
| 10 | CLK | Digital input / Schmitt-Trigger | Clock Input of Synchronous Serial Interface; Schmitt-Trigger input |
| 11 | CS | | Chip Select for serial data transmission, active high; Schmitt-Trigger input, external pull-down resistor (~50kΩ) required in read-only mode |
| 12 | DIO | Bi-directional digital pin | Data output / command input for digital serial interface |
| 13 | VDD | Supply pin | Positive supply voltage, 4.5V to 5.5V |
| 14 | C1 | Digital input (standard CMOS; no pull-up or pull-down) | Configuration input: Connect to VSS for normal operation, connect to VDD to enable SIN-COS outputs. This pin is scanned at power-on-reset and at wake-up from one of the Ultra-low Power Modes |
| 15 | C2 | | Configuration input: Connect to VSS for 3-wire operation, connect to VDD for 2-wire operation. This pin is scanned at power-on-reset and at wake-up from one of the Ultra-low Power Modes |
| 16 | PWM | Digital output | Pulse Width Modulation output, 2µs pulse width per step (2µs ~ 512µs) |

# 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Table 2. Absolute Maximum Ratings*

| Symbol | Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|---|
| **Electrical Parameters** | | | | | |
| $V_{DD}$ | Supply voltage | -0.3 | 7 | V | Except during OTP programming |
| $V_{IN}$ | Input pin voltage | VSS - 0.5 | VDD + 0.5 | V | |
| $I_{scr}$ | Input current (latch-up immunity) | -100 | 100 | mA | Norm: Jedec 78 |
| **Electrostatic Discharge** | | | | | |
| ESD | Electrostatic Discharge | ±2 | | kV | Norm: MIL 883 E method 3015 |
| $\Theta_{JA}$ | Package thermal resistance | | 137 | °C/W | Still Air / Single Layer PCB |
| | | | 89 | °C/W | Still Air / Multilayer PCB |
| **Temperature Ranges and Storage Conditions** | | | | | |
| $T_{strg}$ | Storage temperature | -55 | +150 | °C | Min -67ºF; Max +257ºF |
| $T_{BODY}$ | Body temperature | | 260 | °C | The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn). |
| | Humidity non-condensing | 5 | 85 | % | |
| MSL | Moisture Sensitive Level | 3 | | | Represents a maximum floor time of 168h |

# 6 Electrical Characteristics

*TAMB = -40°C to +125°C, VDD5V = 4.5V ~ 5.5V, all voltages referenced to VSS, unless otherwise noted.*

## 6.1 Operating Conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VDD | Positive supply voltage | | 4.5 | | 5.5 | V |
| IDD | Operating current | No load on outputs. Minimum AGC (strong magnetic field) | | 14 | 18 | mA |
| | | No load on outputs. Maximum AGC (weak or no magnetic field) | | 18 | 22 | |
| $I_{off}$ | Power-down current | Low Power Mode | | 1400 | 2000 | µA |
| | | Ultra-low Power Mode | | 30 | 120 | |
| TAMB | Ambient temperature | -40°F ~ +257°F | -40 | | 125 | °C |

## 6.2 System Parameters

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| N | Resolution | | | 8 | | bit |
| | | | | 1.406 | | ° |
| $T_{PwrUp}$ | Power up time | Startup from zero; AGC not regulated | | | 1000 | µs |
| | | Startup from zero until regulated AGC | | | 3300 | |
| | | Startup from Power Down Mode | | | 500 | |
| | | Startup from Low Power Mode Setting 1: no hysteresis, no reset | | | 46 | |
| | | Setting 2: hysteresis and reset | | | 1500 | |
| $t_{da}$ | Propagation delay | Analog signal path; over full temperature range | | 15 | 17 | µs |
| $t_{dd}$ | Tracking rate | step rate of tracking ADC; 1 step = 1.406° | 0.85 | 1.15 | 1.45 | µs |
| $t_{delay}$ | Signal processing delay | Total signal processing delay, analog + digital ($t_{da}$ + $t_{dd}$) | | 16.15 | 18.45 | µs |
| T | Analog filter time constant | Internal low-pass filter | 4.1 | 6.6 | 12.5 | µs |
| $INL_{cm}$ | Accuracy | centered magnet | -2 | | 2 | ° |
| | | within horizontal displacement radius (see Magnet Specifications on page 7) | -3 | | 3 | |
| TN | Transition noise | rms (1 sigma) | | | 0.235 | ° |
| $POR_r$ | Power-on-reset levels | VDD rising | 3.5 | | 4.5 | V |
| $POR_f$ | | VDD falling | 3.0 | | 4.5 | V |
| Hyst | | Hysteresis \| $POR_r$ - $POR_f$ \| | | 500 | | mV |

## 6.3 Magnet Specifications

Recommended magnet: NdFeB 35H BR = 12.000 Gauss, Ø6mm x 2.5mm

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| MD | Magnet diameter | Diametrically magnetized | | 6 | | mm |
| MT | Magnet thickness | | | 2.5 | | mm |
| $B_i$ | Magnetic input range | At chip surface, on a radius of 1mm | 20 | | 80 | mT |
| $v_i$ | Magnet rotation speed | To maintain locked state | | | 30.000 | rpm |
| $B_{max}$ | Magnetic field high detection | TAMB=25°C, AGC @ lower limit, 1 sigma = 2.5mT | | 52 | | mT |
| $B_{min}$ | Magnetic field low detection | TAMB=25°C, AGC @ upper limit, 1 sigma = 1.5mT | | 23 | | |
| | Hall array radius | Over x/y chip center | | 1 | | mm |
| | Vertical distance of magnet | Recommended distance; operation outside this range is possible, accuracy may be reduced | 0.5 | 1 | 1.8 | mm |
| | Horizontal magnet displacement radius | From diagonal package center | | | 0.25 | mm |
| | | From diagonal IC center | | | 0.5 | |
| $tk_M$ | Recommended magnet material and temperature drift | NdFeB Material | | -0.12 | | %/K |
| | | SmCo Material | | -0.035 | | |

## 6.4 Magnetic Field Alarm Limits

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $AGC_{FF}$ | Magnetic field too low alarm limit | AGC = $FF_H$ untrimmed, 25°C, 1sigma | 20.3 | | 23.6 | mT |
| $AGC_0$ | Magnetic field too high alarm limit | AGC = $0_H$ untrimmed, 25°C, 1sigma | 44.5 | | 52.2 | mT |
| | Magnetic field alarm limit trim range | (see Hall Element Sensitivity Options on page 7) | 100 | | 121 | % |
| | Temperature coefficient of alarm ranges | Sensitivity increases with temperature which partly compensates the temperature coefficient of the magnet | | 0.052 | | %/K |

## 6.5 Hall Element Sensitivity Options

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| sens | Hall element sensitivity setting | sens = 00 (default); low sensitivity (see 18-bit OTP Write Commands on page 25) | | 100 | | % |
| | | sens = 01 | | 106 | | |
| | | sens = 10 | | 113 | | |
| | | sens = 11 (high sensitivity) | | 121 | | |

## 6.6 Programming Parameters

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{PROG}$ | Programming voltage | Static voltage at pin PROG | 8.0 | | 8.5 | V |
| $I_{PROG}$ | Programming current | | | | 100 | mA |
| $Tamb_{PROG}$ | Programming ambient temperature | During programming | 0 | | 85 | °C |
| $t_{PROG}$ | Programming time | Timing is internally generated | 2 | | 4 | µs |
| $V_{R,prog}$ | Analog readback voltage | During Analog Readback mode at pin PROG | | | 0.5 | V |
| $V_{R,unprog}$ | | | 2.2 | | 3.5 | |

## 6.7 DC Characteristics of Digital Inputs and Outputs

***CMOS Inputs:*** CLK, CS, DIO, C1, C2

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High level input voltage | | 0.7*VDD | | | V |
| $V_{IL}$ | Low level input voltage | | | | 0.3*VDD | V |
| $I_{LEAK}$ | Input leakage current | | | | 1 | µA |

***CMOS Outputs:*** DIO, MagRngn, PWM, DX

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High level output voltage | Source current <4mA | VDD-0.5 | | | V |
| $V_{OH}$ | Low level output voltage | Sink current <4mA | | | 0.4 | V |
| $C_L$ | Capacitive load | | | | 35 | pF |

***CMOS Tristate Output:*** DIO

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $IO_Z$ | Tristate leakage current | CS = low | | | 1 | µA |

## 6.8 8-bit PWM Output

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $N_{PWM}$ | PWM resolution | | | 8 | | bit |
| | | | | 2 | | µs/step |
| $PW_{MIN}$ | PWM pulse width | Angle = 0° ($00_H$) | 1.66 | 2.26 | 2.85 | µs |
| $PW_{MAX}$ | PWM pulse width | Angle = 358.6° ($FF_H$) | 427 | 578 | 731 | µs |
| $PW_P$ | PWM period | Over full temperature range[1] | 428 | 581 | 734 | µs |
| $f_{PWM}$ | PWM frequency | 1 / PWM period | | 1.72 | | kHz |
| Hyst | Digital hysteresis[2] | At change of rotation direction | | 1 | | bit |

1. The tolerance of the absolute PWM pulse width and frequency can be eliminated by using the duty cycle $t_{ON}/(t_{ON}+t_{OFF})$ for angle measurement(see 1-Wire PWM Connection on page 16).
2. Hysteresis may be temporarily disabled by software(see 16-bit Write Command on page 24).

## 6.9 Serial 8-bit Output

***3-wire Interface.***

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{CLK}$ | Clock frequency | Normal operation | | | 6 | MHz |
| $t_{CLK}$ | | | 166.6 | | | ns |
| $f_{clk,P}$ | Clock frequency | During OTP programming | 250 | | 500 | kHz |

***2-wire Interface.***

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{CLK}$ | Clock frequency | Normal operation | 0.1 | | 6 | MHz |
| $t_{CLK}$ | | | 166.6 | | 10,000 | ns |
| $f_{clk,P}$ | Clock frequency | During OTP programming | 250 | | 500 | kHz |
| $t_{TO}$ | Synchronization timeout | Rising edge of CLK to internally generated chip select on pin DX | 16.6 | 27 | 34.3 | ms |
| Hyst | Digital hysteresis[1] | At change of rotation direction | | 1 | | bit |

1. Hysteresis may be temporarily disabled by software.

## 6.10 General Data Transmission Timings

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| t0 | Rising CLK to CS | | CLK/2 +0 | | CLK/2 +50 | ns |
| t1 | Chip select to positive edge of CLK | | 50 | | | ns |
| t2 | Chip select to drive bus externally | | 0 | | | ns |
| t3 | Setup time command bit data valid to positive edge of CLK | | 50 | | | ns |
| t4 | Hold time command bit data valid after positive edge of CLK | | 15 | | | ns |
| t5 | Float time positive edge of CLK for last command bit to bus float | | | | CLK/2 +0 | ns |
| t6 | Bus driving time positive edge of CLK for last command bit to bus drive | | CLK/2 +0 | | | ns |
| t7 | Setup time data bit data valid to positive edge of CLK | | CLK/2 +0 | | CLK/2 +30 | ns |
| t8 | Hold time data bit data valid after positive edge of CLK | | CLK/2 +0 | | | ns |
| t9 | Hold time chip select positive edge CLK to negative edge of chip select | | CLK/2 +50 | | | ns |
| t10 | Bus floating time negative edge of chip select to float bus | | | | 50 | ns |
| t11 | Hold time data bit @ write access data valid to positive edge of CLK | | 50 | | | ns |
| t12 | Hold time data bit @ write access data valid after positive edge of CLK | | 15 | | | ns |
| t13 | Bus floating time negative edge of chip select to float bus | | | | 50 | ns |
| $t_{TO}$ | Timeout period in 2-wire mode (from rising edge of CLK) | | 20 | | 24 | µs |

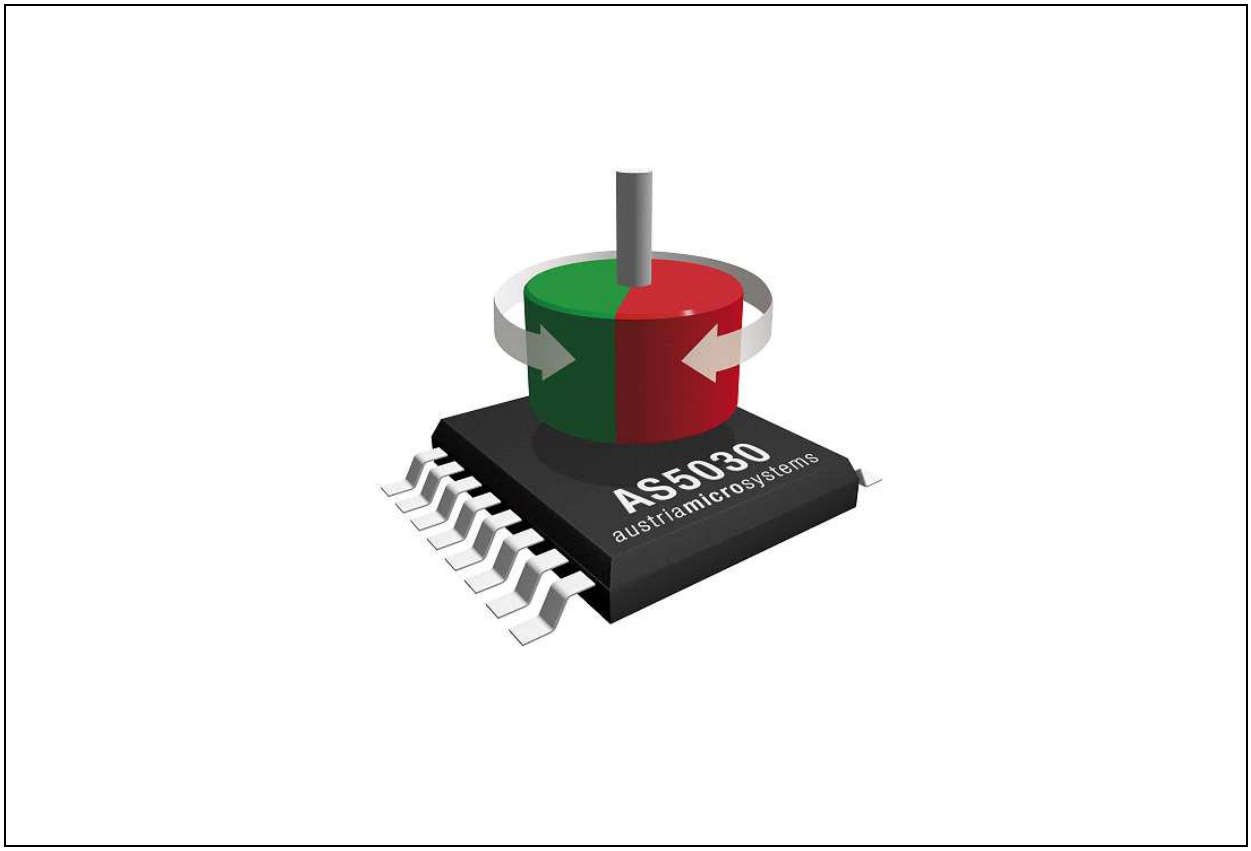
See Figure 5 for the corresponding timing diagram.

# 7 Detailed Description

The benefits of AS5030 are as follows:

- Complete system-on-chip, no calibration required
- Flexible system solution provides absolute serial and PWM output
- Ideal for applications in harsh environments due to magnetic sensing principle
- High reliability due to non-contact sensing
- Robust system, tolerant to horizontal misalignment, airgap variations, temperature variations and external magnetic fields

*Figure 3. Typical Arrangement of AS5030 and Magnet*




## 7.1 Connecting the AS5030

The following examples show various ways to connect the AS5030 to an external controller:

## 7.2 Serial 3-Wire R/W Connection

In this mode, the AS5030 is connected to the external controller via three signals:

Chip Select (CS), Clock (CLK) inputs and bi-directional DIO (Data In/Out) output.

The controller sends commands over the DIO pin at the beginning of each data transmission sequence, such as reading the angle or putting the AS5030 in and out of the reduced power modes.
A pull-down resistor is not required.

C1 and C2 are hardware configuration inputs. C1 must always be connected to VSS, C2 selects 3-wire mode (C2 = low) or 2-wire mode (C2 = high)

*Figure 4. SSI Read/Write Serial Data Transmission*

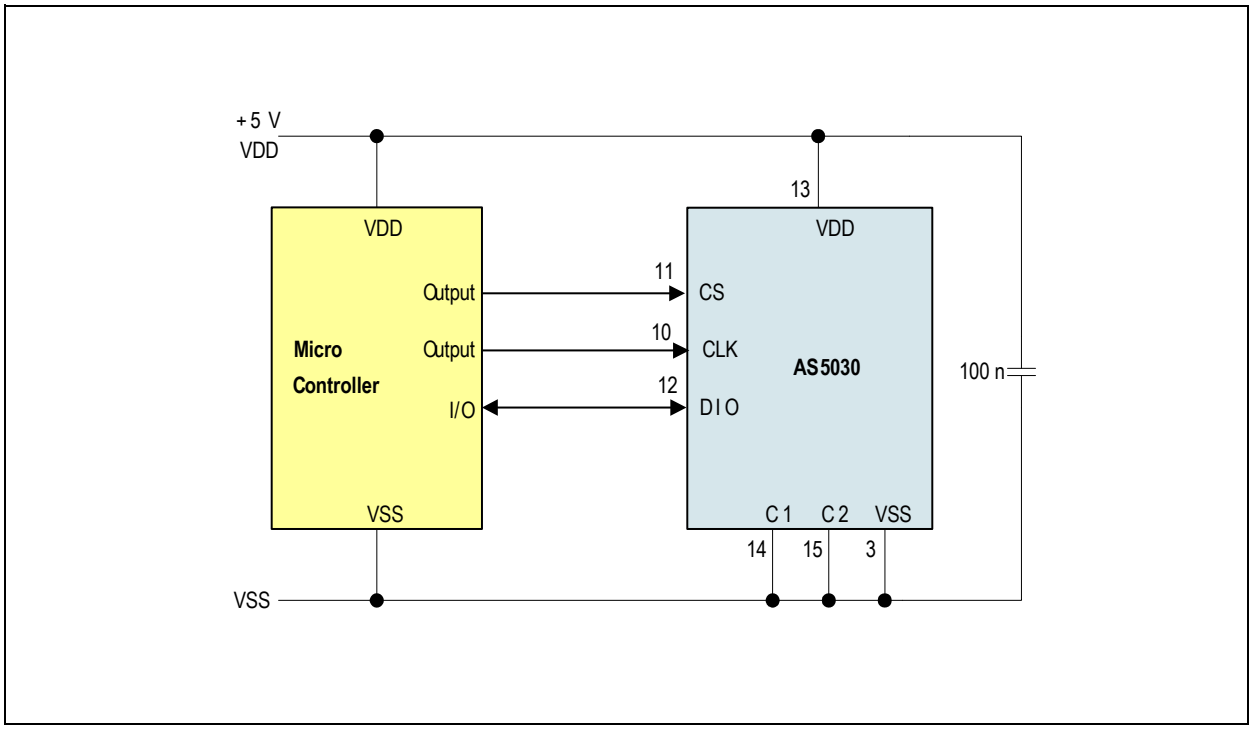



*Figure 5. Timing Diagram in 3-wire SSI R/W Mode*

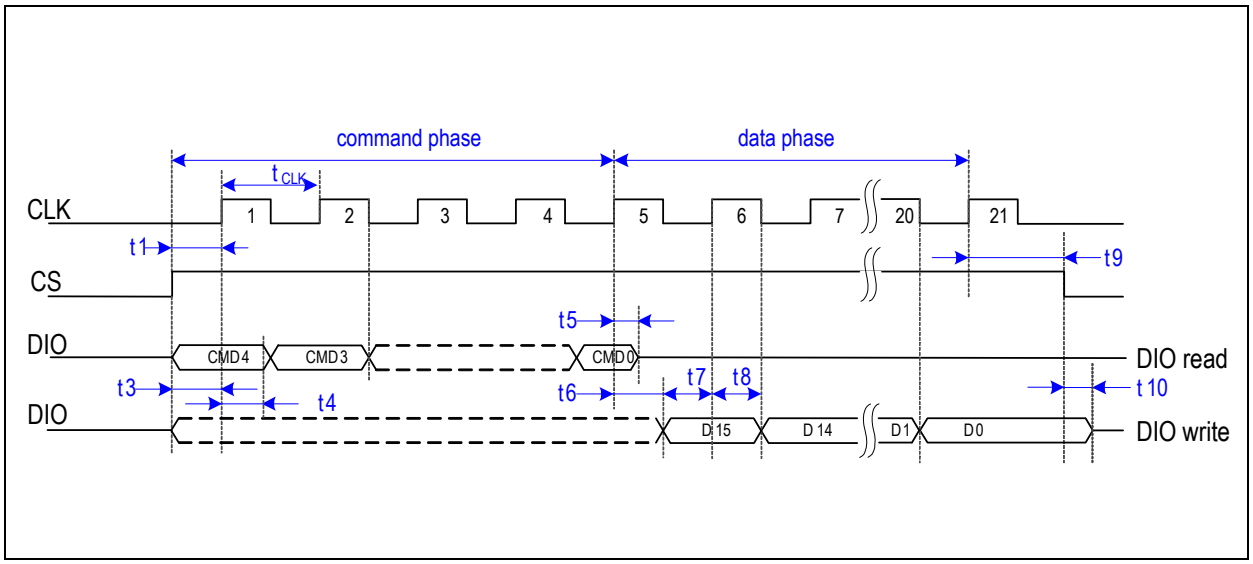



*Table 3. Serial Bit Sequence (16-bit read/write)*

| Write Command | | | | | Read / Write Data | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C4 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

## 7.3 Serial 3-Wire Read-only Connection

If the AS5030 is only used to provide the angular data (no power down or OTP access) this simplified connection is possible. The Chip Select (CS) and Clock (CLK) connection is the same as in the R/W mode, but only a digital input pin (not an I/O pin) is required for the DIO connection. As the first 5 bits of the data transmission are command bits sent to the AS5030, both the microcontroller and the AS5030 are configured as digital inputs during this phase. Therefore, a pull-down resistor must be added to make sure that the AS5030 reads “00000” as the first 5 bits which sets the Read_Angle command.

All further application examples are shown in R/W mode, however read-only mode is also possible, unless otherwise noted.

*Figure 6. SSI Read-only Serial Data Transmission*

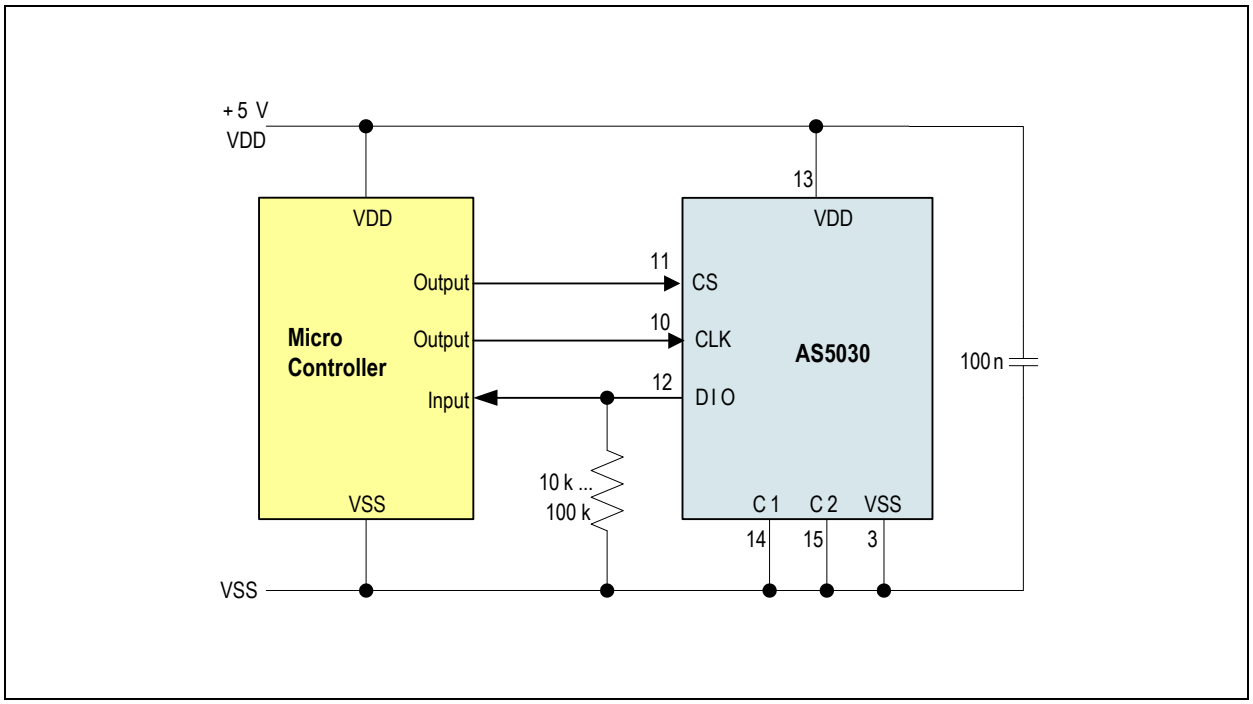



*Figure 7. Timing Diagram in 2-wire and 3-wire SSI Mode*

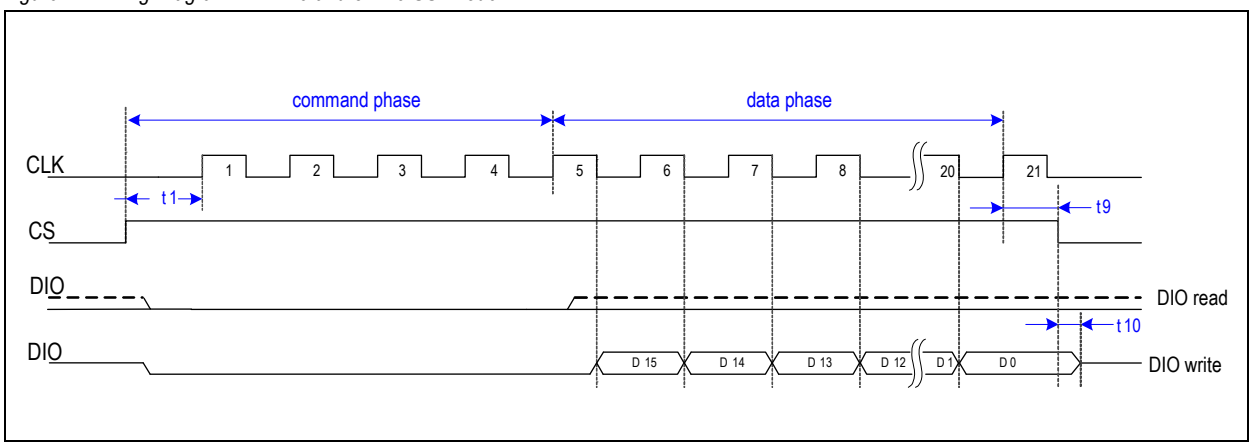



*Table 4. Serial Bit Sequence (16-bit read/write)*

| Read | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | 0 | C2 | lock | AGC | | | | | | Angle | | | | | | | |
| | | | | | | | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

## 7.4 Serial 2-Wire Connection (R/W Mode)

By connecting the configuration input C2 to VDD, the AS5030 is configured to 2-wire data transmission mode.

Only Clock (CLK) and Data (DIO) signals are required. A Chip Select (CS) signal is automatically generated by the DX output, when a time-out of CLK occurs (typ. 20µs).

**Note:** Read-only mode is also possible in this configuration.

*Figure 8. SSI R/W Mode 2-wire Data Transmission*

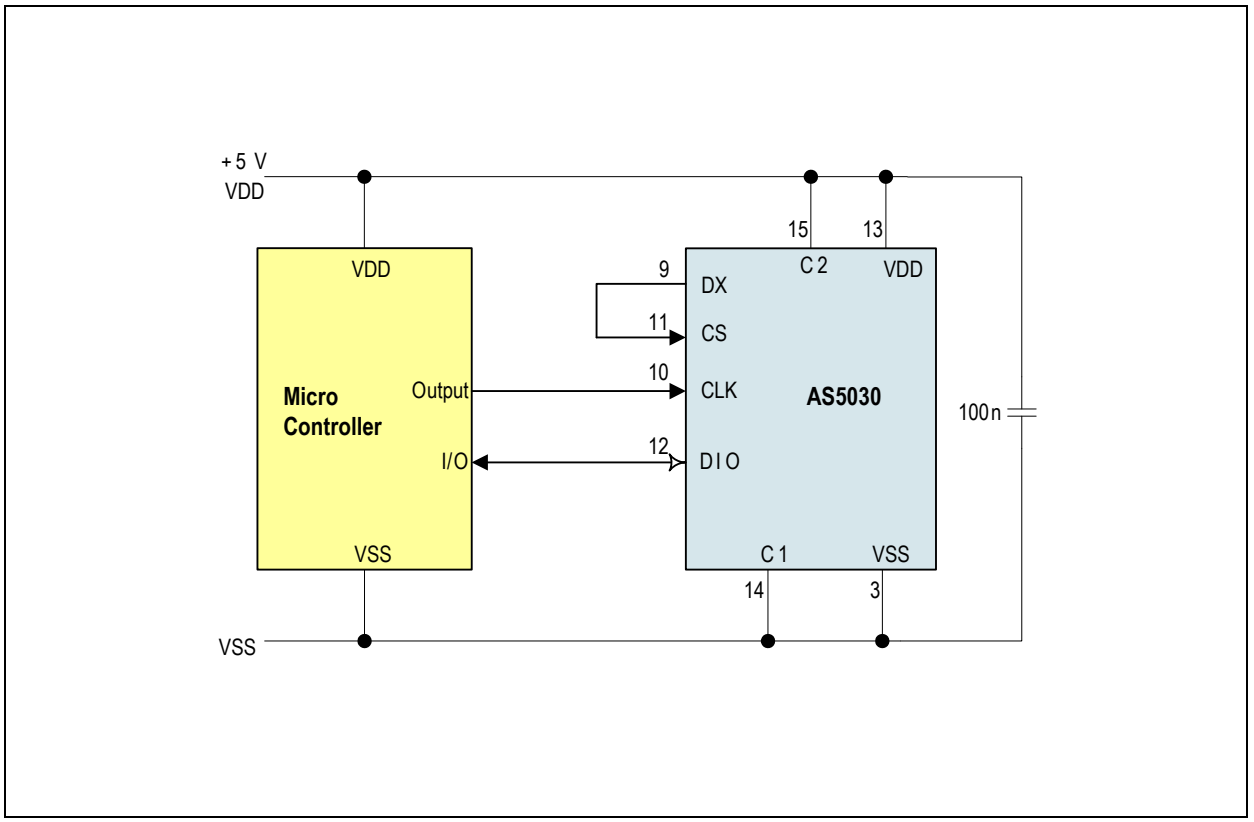
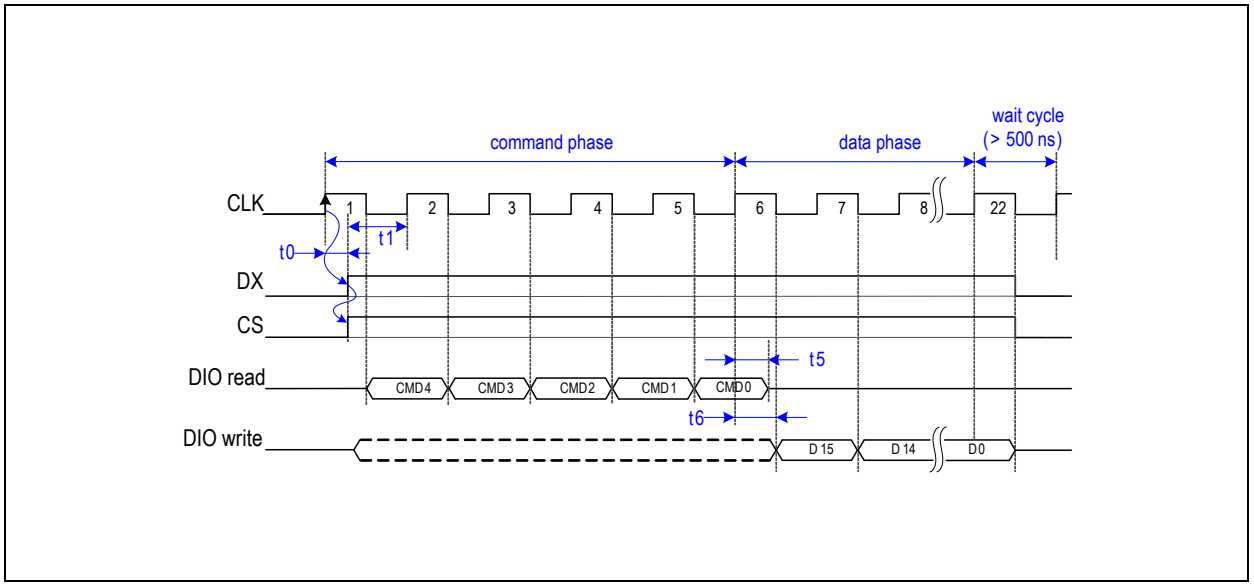



*Figure 9. Timing Diagram in 2-wire SSI Mode*



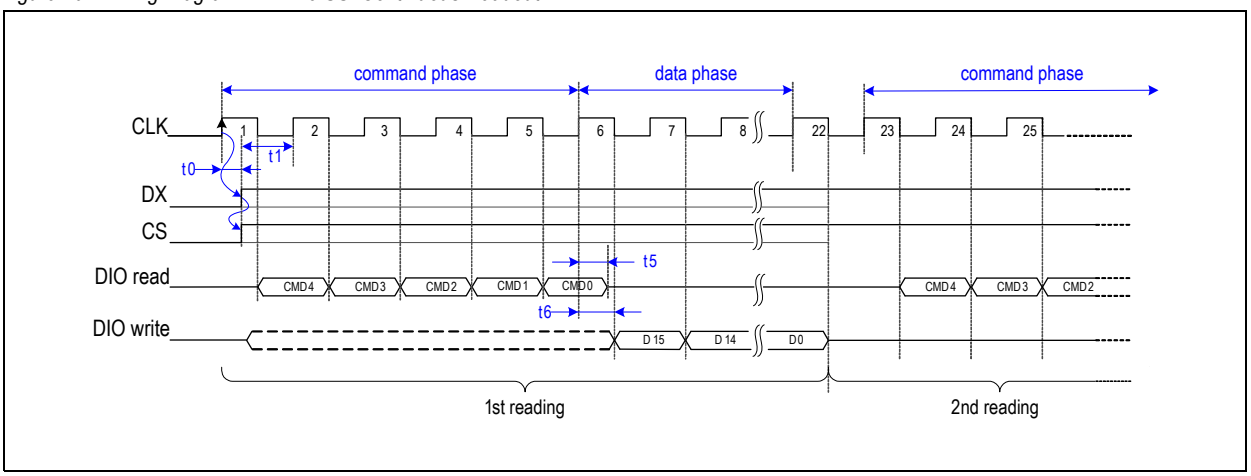
## 7.5 Serial 2-Wire Continuous Readout

The termination of each readout sequence by a timeout of CLK after the 22nd clock pulse as described in Serial 2-Wire Connection (R/W Mode) is the safest method to ensure synchronization, as each timeout of CLK resets the serial interface.

However, it is not mandatory to apply a timeout of CLK and consequently synchronization after each reading. It is also possible to read several consecutive angle values without synchronization by simply continuing the CLK pulses without timeout after the 22nd clock. The 23rd clock is equal to the 1st clock of the next measurement, etc.

This is the fastest way to read multiple angle values, as there is no timeout period between the readings. It is still possible to synchronize the serial data transmission by a timeout of CLK after a given number of readouts (e.g. synchronize after every 5th reading, etc.)

*Figure 10. Timing Diagram in 2-wire SSI Continuous Readout*




## 7.6 Serial 2-Wire Differential SSI Connection

With the addition of a RS-422 / RS-485 transceiver, a fully differential data transmission, according to the 21-bit SSI interface standard is possible. To be compatible with this standard, the CLK signal must be inverted. This is done by reversing the Data+ and Data- lines of the transceivers.

**Note:** This type of transmission is read-only.

*Figure 11. 2-wire SSI Read-only Mode*

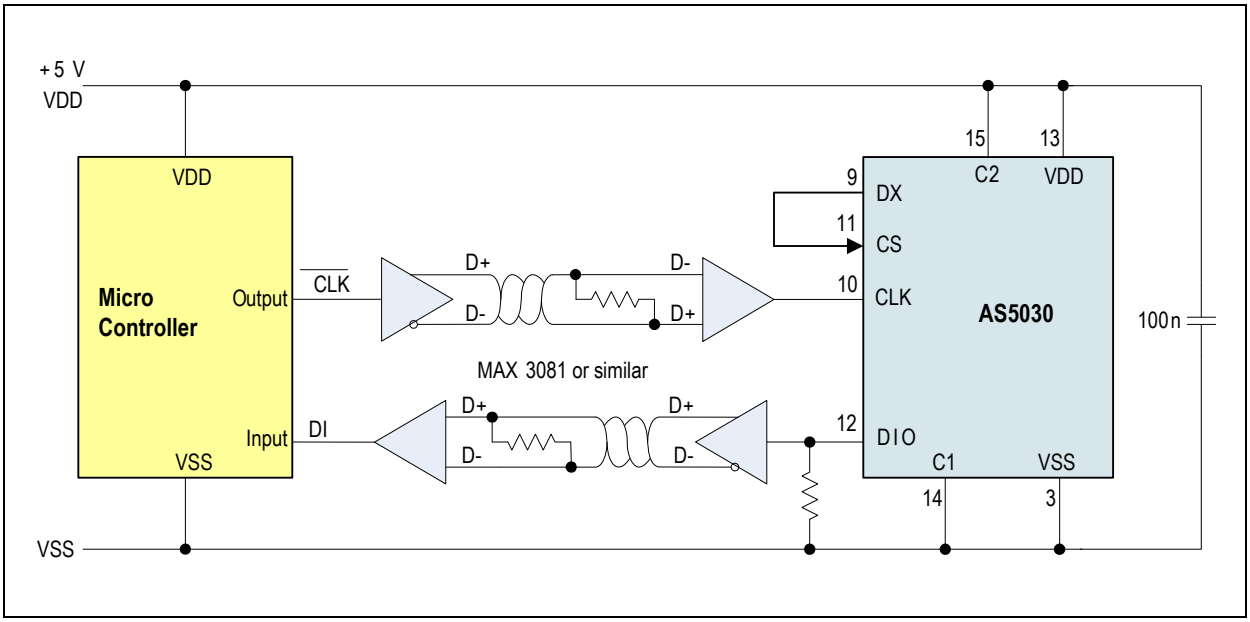


*Figure 12. Timing Diagram in 2-wire Read only Mode (differential transmission)*

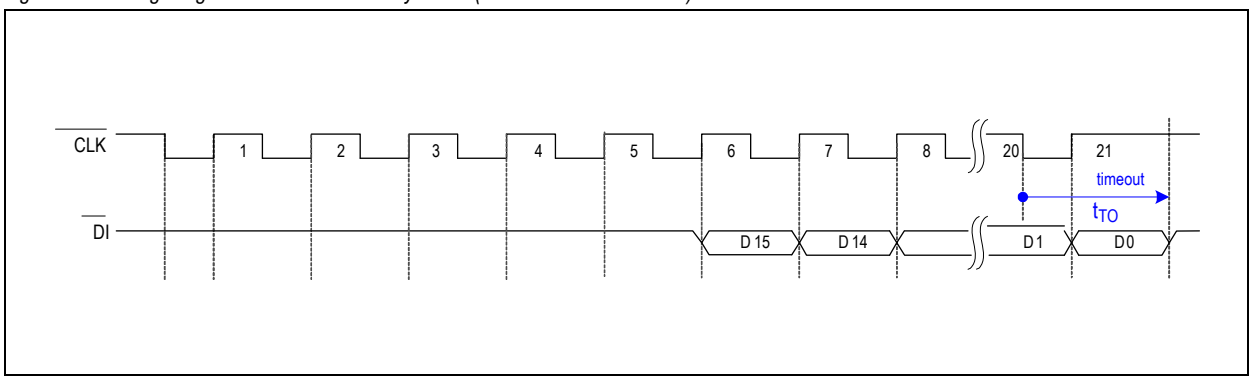



*Table 5. SSI Read-only Serial Bit Sequence (21bit read)*

| Read | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D20** | **D19** | **D18** | **D17** | **D16** | **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 0 | 0 | 0 | 0 | 0 | C2 | lock | AGC | | | | | | Angle | | | | | | | |
| | | | | | | | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

## 7.7 1-Wire PWM Connection

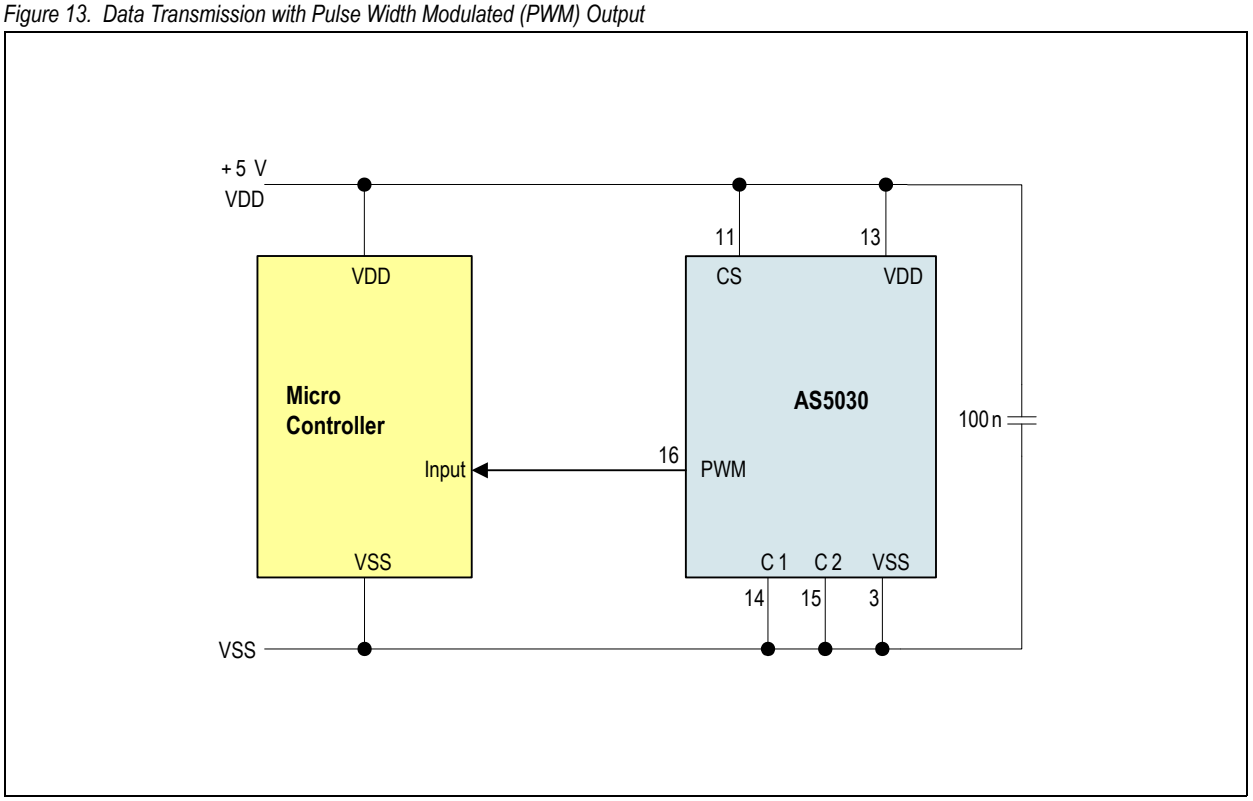
This configuration uses the least number of wires: only one line (PWM) is used for data, leaving the total number of connection to three, including the supply lines. This type of configuration is especially useful for remote sensors.

Ultra-low Power Mode is not possible in this configuration, as there is no bi-directional data transmission.

If the AS5030 angular data is invalid, the PWM output will remain at low state. Pins that are not shown may be left open.

Note that the PWM output is invalid when the AGC is disabled.

*Figure 13. Data Transmission with Pulse Width Modulated (PWM) Output*



The minimum PWM pulse width $t_{ON}$ (PWM = high) is 1 LSB @ 0° (Angle reading = $00_H$).

1LSB = nom. 2.26µs.

The PWM pulse width increases with 1LSB per step. At the maximum angle 358.6° (Angle reading = $FF_H$), the pulse width $t_{ON}$ (PWM = high) is 256 LSB and the pause width $t_{OFF}$ (PWM = low) is 1 LSB.

This leads to a total period ($t_{ON}$ + $t_{OFF}$) of 257LSB.

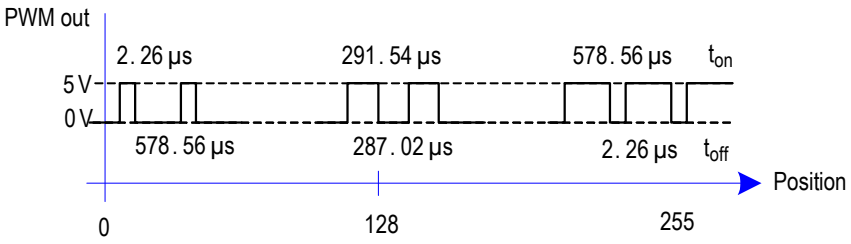



*Table 6. SSI Read-only Serial Bit Sequence (21-bit read)*

| Position | Angle | High | t_high | Low | t_low | Duty-Cycle |
|---|---|---|---|---|---|---|
| 0 | 0° | 1 | 2.26µs | 256 | 578.56µs | 0.39% |
| 127 | 178.59 | 128 | 287.02µs | 129 | 291.54µs | 49.4% |
| 128 | 180° | 129 | 291.54µs | 128 | 287.02µs | 50.2% |
| 255 | 358.59° | 256 | 578.56µs | 1 | 2.26µs | 99.6% |

This means that the PWM pulse width is (position + 1) LSB, where position is 0….255.

The tolerance of the absolute pulse width and -frequency can be eliminated by calculating the angle with the duty cycle rather than with the absolute pulse width:

*(EQ 1)*

$$angle[8-bit] = \left(257 \frac{t_{ON}}{t_{ON} + t_{OFF}}\right) - 1$$

results in an 8-bit value from $00_H$ to $FF_H$,

*(EQ 2)*

$$angle[°] = \frac{360}{256}\left[\left(257 \frac{t_{ON}}{t_{ON} + t_{OFF}}\right) - 1\right]$$

results in a degree value from 0° ~ 358.6°

**Note:** The absolute frequency tolerance is eliminated by dividing $t_{ON}$ by ($t_{ON}$+$T_{OFF}$), as the change of the absolute timing effects both $T_{ON}$ and $T_{OFF}$ in the same way.

## 7.8 Analog Output

This configuration is similar to the PWM connection (only three lines including supply are required). With the addition of a low-pass filter at the PWM output, this configuration produces an analog voltage that is proportional to the angle.

This filter can be either passive (as shown) or active. The lower the bandwidth of the filter, the less ripple of the analog output can be achieved.

If the AS5030 angular data is invalid, the PWM output will remain at low state and thus the analog output will be 0V. Pins that are not shown may be left open.

**Note:** The PWM output is invalid when the AGC is disabled.

*Figure 14. Data Transmission with Pulse Width Modulated (PWM) Output*

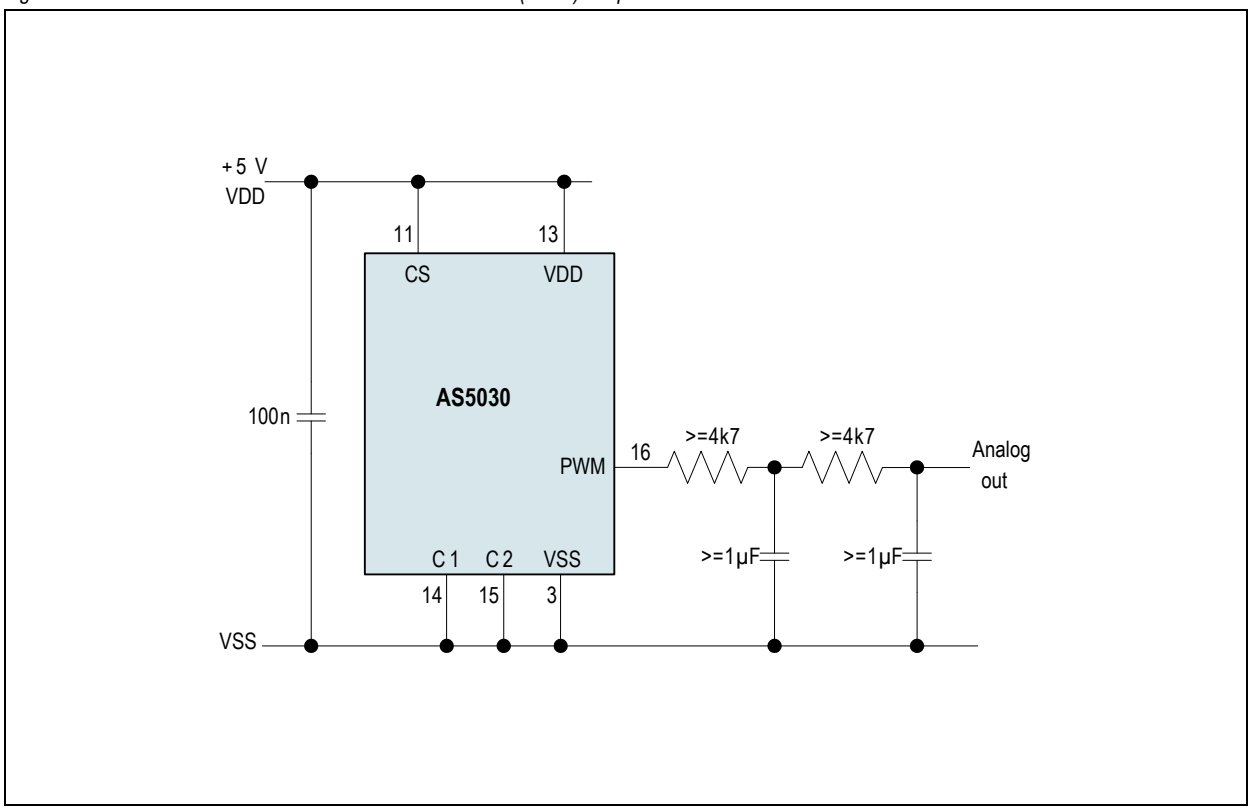
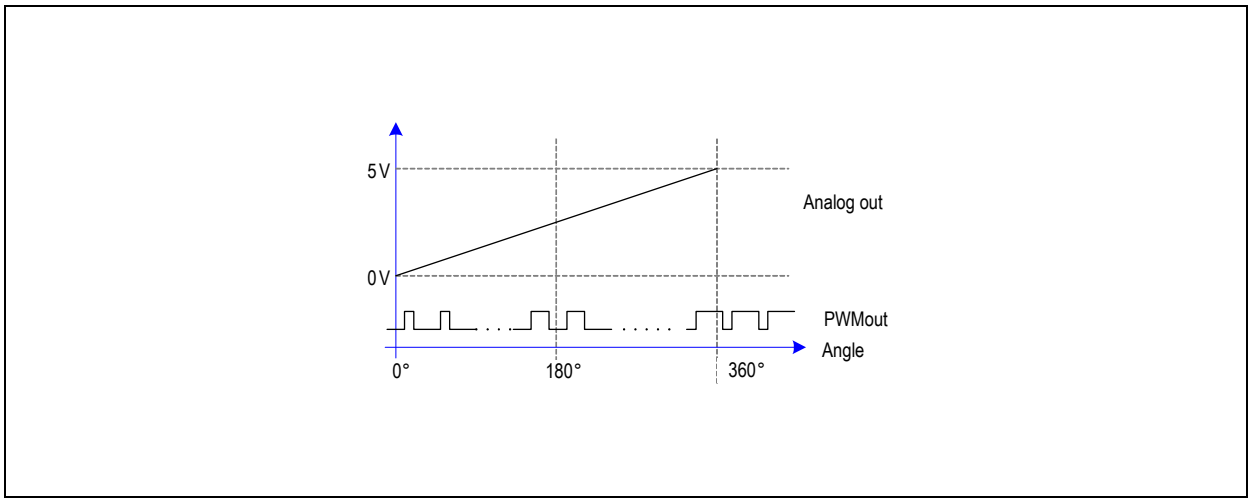



*Figure 15. Relation of PWM/Analog Output With Angle*



## 7.9 Analog Sin/Cos Outputs with External Interpolator

By connecting C1 to VDD, the AS5030 provides analog Sine and Cosine outputs (Sin, Cos) of the Hall array front-end for test purposes. These outputs allow the user to perform the angle calculation by an external ADC + µC, e.g. to compute the angle with a high resolution.

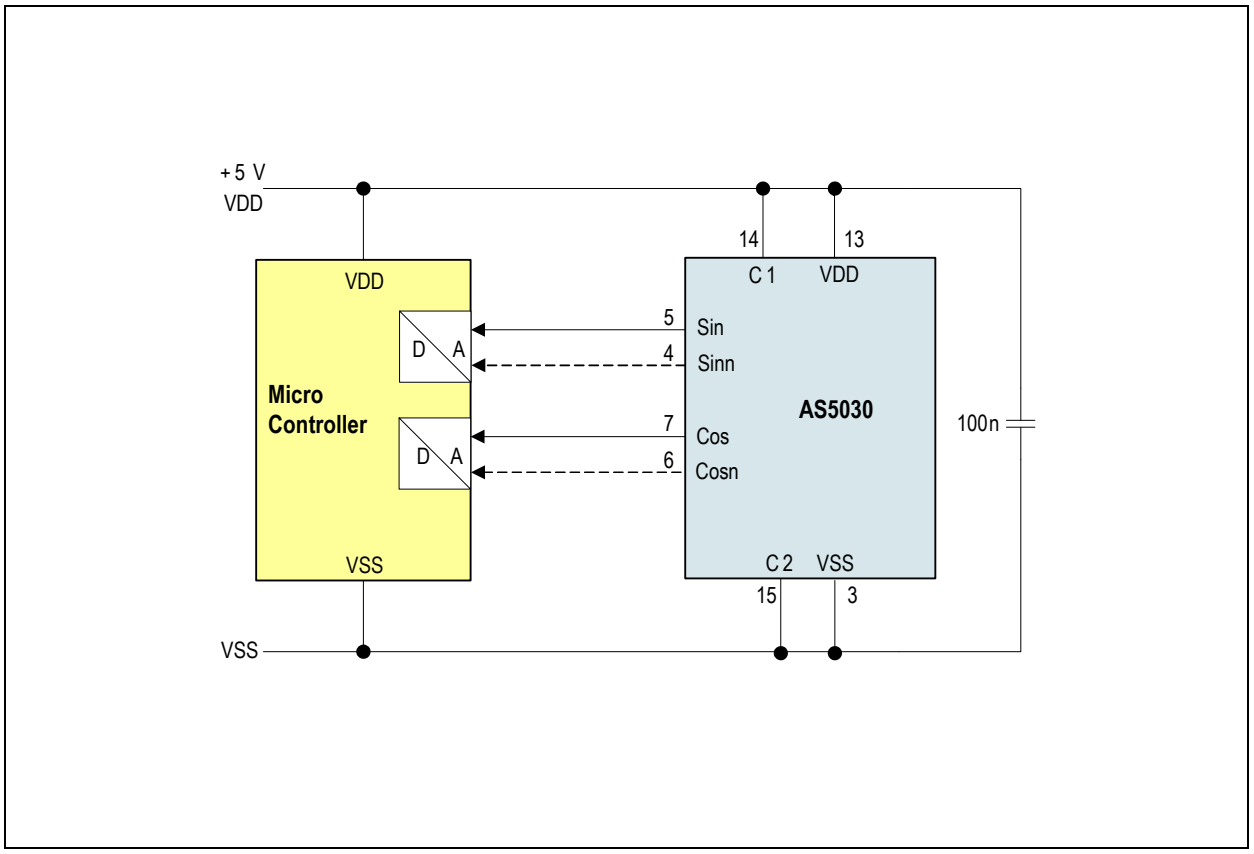
In addition, the inverted Sine and Cosine signals (Sinn, Cosn; see dotted lines) are available for differential signal transmission.

The input resistance of the receiving amplifier or ADC should be greater than 100kΩ. The signal lines should be kept as short as possible, longer lines should be shielded in order to achieve best noise performance.

The SIN / COS / SINn / COSn signals are amplitude controlled to ~1.3Vp (differential) by the internal AGC controller. The DC bias voltage is 2.25V.

If the SIN(n)- and COS(n)- outputs cannot be sampled simultaneously, it is recommended to disable the automatic gain control as the signal amplitudes may be changing between two readings of the external ADC. This may lead to less accurate results.

*Figure 16. Sine and Cosine Outputs for External Angle Calculation*



## 7.10 3-Wire Daisy Chain Mode

The Daisy Chain mode allows connection of more than one AS5030 to the same controller interface. Independent of the number of connected devices, the interface to the controller remains the same with only three signals: CSn, CLK and DO. In Daisy Chain mode, the data from the second and subsequent devices is appended to the data of the first device.

The 100nF buffer cap at the supply (shown only for the last device) is recommended for all devices.

The total number of serial bits is: n*21, where n is the number of connected devices: e.g. for 2 devices, the serial bit stream is 42bits. For three devices it is 63 bits.

*Figure 17. Connection of Devices in 3-wire Daisy Chain Mode*

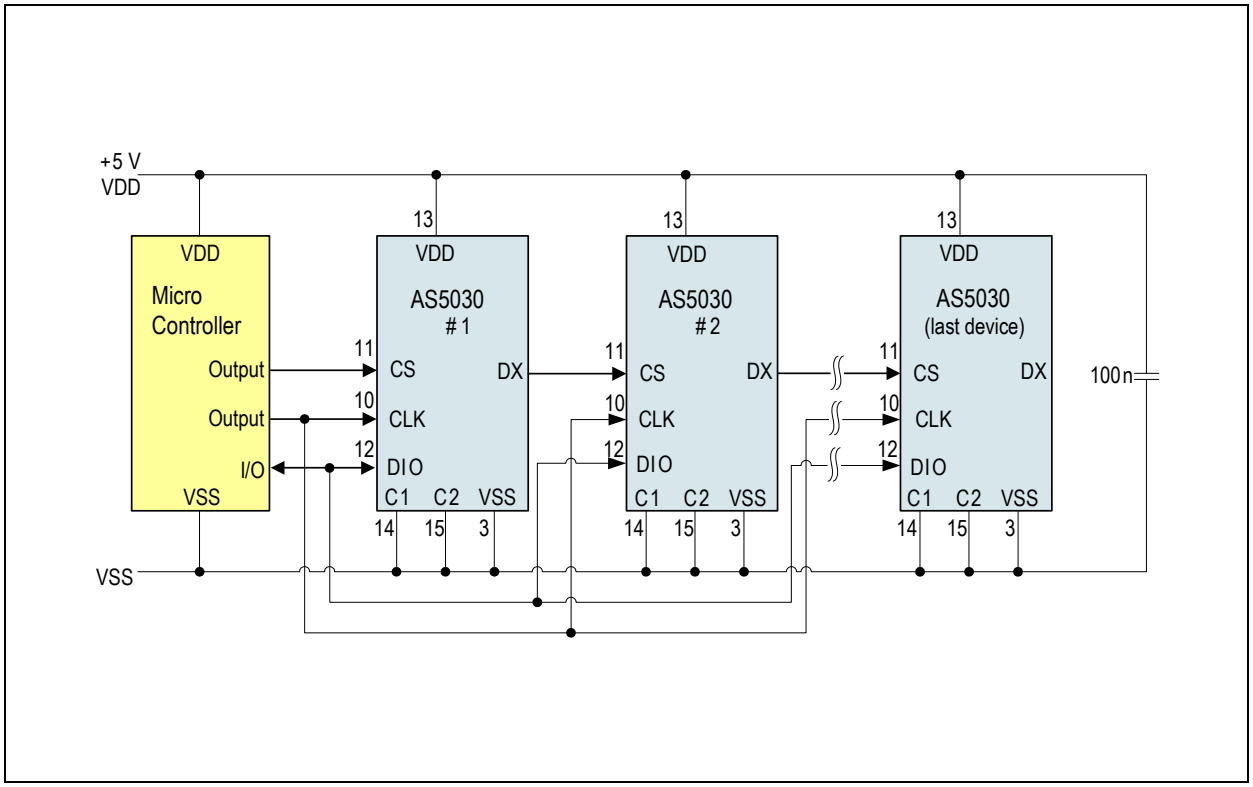
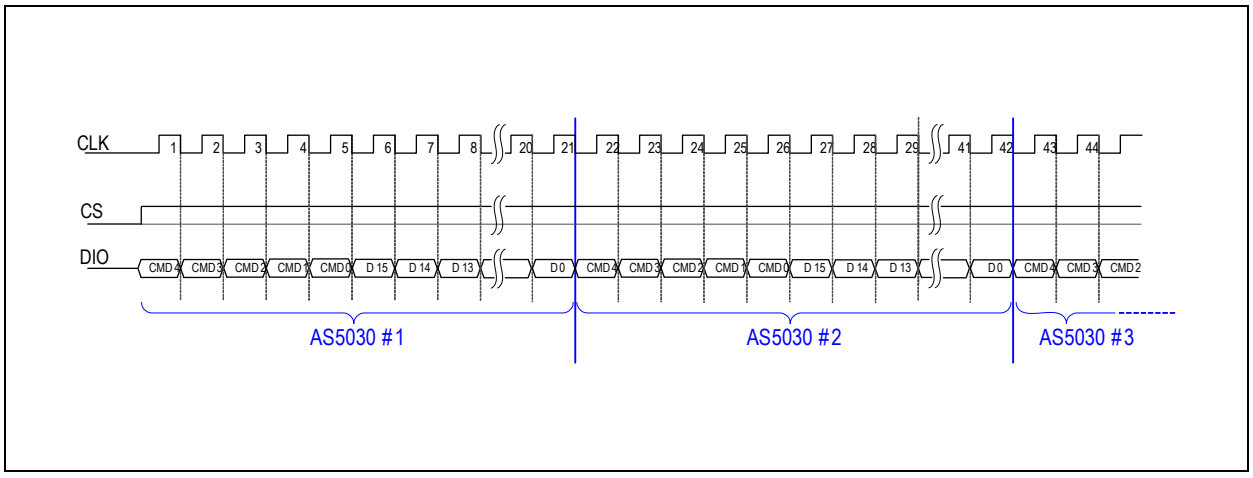



*Figure 18. Timing Diagram in 3-wire Daisy Chain Mode*



## 7.11 2-Wire Daisy Chain Mode

The AS5030 can also be connected in 2-wire Daisy Chain mode, requiring only two signals (Clock and Data) for any given number of daisy-chained devices. Note that the connection of all devices except the last device is the same as for the 3-wire connection (see Figure 17). The last device must have pin C2 (#15) set to 'high' and feeds the DX signal to CS of the first device.

Again, each device should be buffered with a 100nF cap (shown only for the last device).

The total number of serial bits is: n*21, where n is the number of connected devices. Note that this configuration requires one extra clock (#1) to initiate the generation of the CS signal for the first device. After reading the last device, the communication must be reset back to the first device by introducing a timeout of CLK (no rising edge for >24µs)

*Figure 19. 2-wire Daisy Chain Mode*

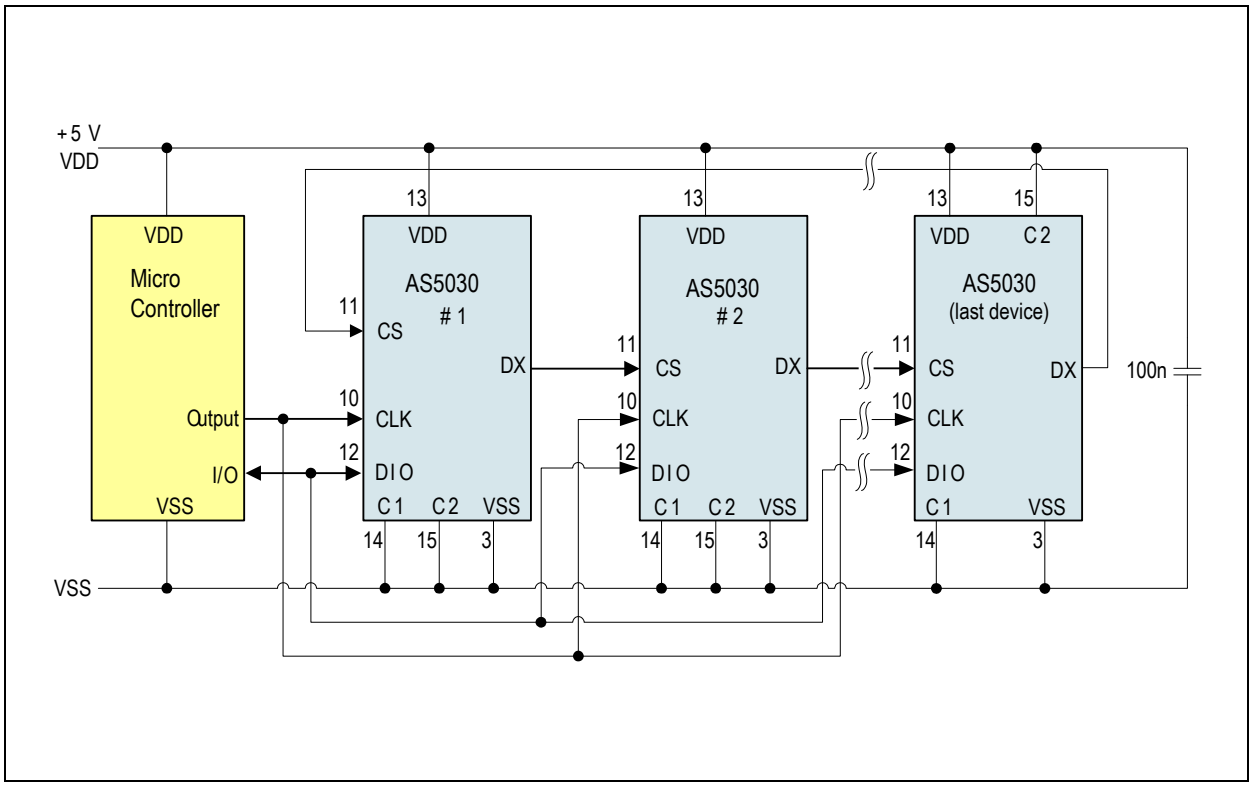
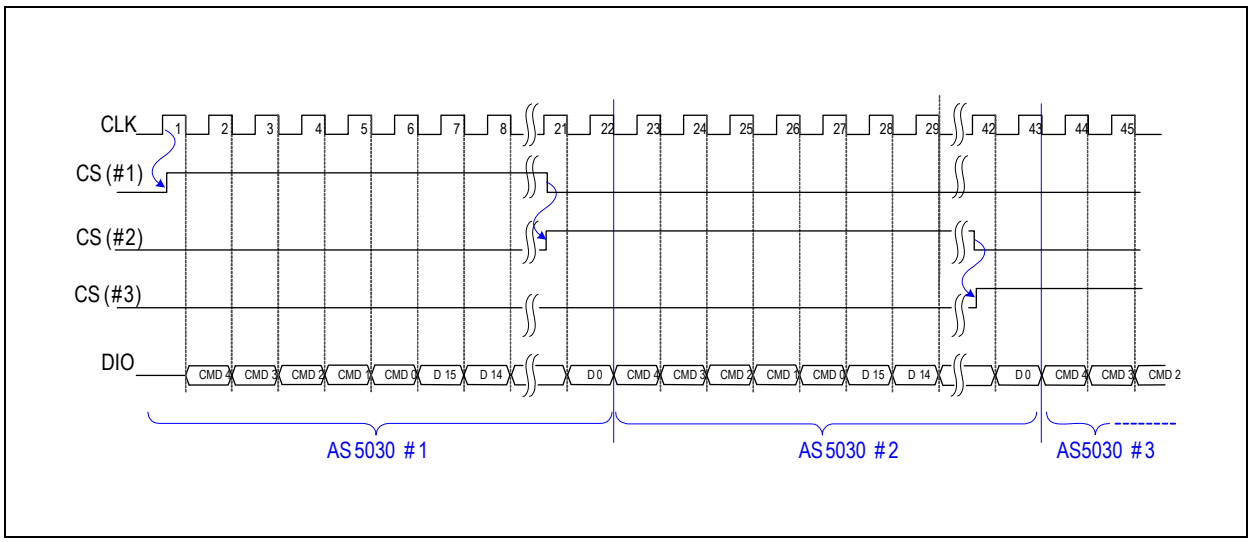



*Figure 20. Timing Diagram in 2-wire Daisy Chain Mode*



# 8 Application Information

***AS5030 Parameter and Features List.***

| Parameter | Description |
|---|---|
| Supply voltage | 5V ± 10% |
| Supply current | Low Power Mode, non-operational: typ. 1.4mA<br>Ultra-low Power Mode, non-operational: typ. 30µA<br>Normal operating mode: typ. 14mA. |
| Absolute output; Serial Interface | 21-bit Synchronous Serial Interface (SSI): 5 command bits, 2 data valid bits, 6 data bits for magnetic field strength, 8 data bits for angle.<br>Configurable for 2-wire (Clock, Data) or 3-wire (Chip Select, Clock, Data) operation<br>Daisy Chain mode for reading multiple encoders through a 2- or 3-wire interface.<br>Zero Position Programming (OTP) |
| SSI clock rate | ≤ 6 MHz data clock rate, 250 ~ 500kHz during programming |
| 2-wire readout mode | DIO and CLK signals. 0.1 ~ 6MHz clock rate. Synchronization through time-out of CLK signal. |
| Power down modes | Activated and deactivated by software commands.<br>Low Power Mode: power down current = 1.4mA typ.; power up time <150µs<br>Ultra-low Power Mode: power down current = 30µA typ.; power up time <500µs |
| Digital input cells | CLK, CS = Schmitt trigger inputs |
| SIN-COS mode | Sine, inverse Sine, Cosine and inverse Cosine outputs. 360° per period. |
| Maximum speed | 30.000 rpm with locked ADC |
| Resolution and accuracy | Resolution = 8-bit (1.406°)<br>Accuracy ≤ ± 2° with centered magnet |
| Transition noise | 0.24°rms (1 sigma) |
| PWM output | 2.26µs / Step, PWM will be permanently low when angular data is not valid (e.g. during startup). |
| Digital output current | 4mA @ VDD = 5V (PWM, DIO, DX, MagRngn outputs) |
| OTP programming mode | Through serial interface with static programming voltage on pin #2 (PROG)<br>16-bit OTP programming register. OTP user programming options:<br>Angular zero position: 8 bit<br>Hall element sensitivity: 2 bit |
| Magnetic field range | Trimmable in four steps with OTP programming (sensitivity)<br>maximum/minimum ratio ~ 2.5:1. Field range window = 20 ~ 80mT<br>(e.g. maximum sensitivity range = 20 ~ 48mT, minimum sensitivity range = 32 ~ 80mT |
| Non-valid-range indication | By hardware: MagRngn pin indicates locked condition of ADC<br>By software: LOCK1&2 status bits indicate locked condition of ADC |
| Start-up timings | Start-up time after shutdown < 2ms<br>Start-up time after power-down from Ultra-low Power Mode: < 500µs<br>Start-up time after power-down from Low Power Mode: < 150µs |
| ESD protection | ± 2kV |
| Operating temperature | -40°C ~ +125°C |

## 8.1 AS5030 Programming

The AS5030 has an integrated 18-Bit OTP ROM for configuration purposes.

### 8.1.1 OTP Programming Options

The OTP programming options can be set permanently by programming or temporarily by overwriting. Both methods are carried out over the serial interface, but with different commands (WRITE OTP, PROG OTP).

**Note:** During the 18bit OTP programming, each bit needs 4 clock pulses to be validated.

- **Zero Position Programming**
  This programming option allows the user to program any rotation angle of the magnet as the new zero position. This useful feature simplifies the assembly process as the magnet does not need to be mechanically adjusted to the electrical zero position. It can be assembled in any rotation angle and later matched to the mechanical zero position by zero position programming.
  The 8-bit user programmable zero position can be applied both temporarily (command WRITE OTP, $\#1F_H$) or permanently (command PROG OTP, $\#19_H$)
- **Magnetic Field Optimization**
  This programming option allows the user to match the vertical distance of the magnet with the optimum magnetic field range of the AS5030 by setting the sensitivity level.
  The 2-bit user programmable sensitivity setting can be applied both temporarily (command WRITE OTP, $\#1F_H$) or permanently (command PROG OTP, $\#19_H$)

### 8.1.2 Reduced Power Mode Programming Options

These temporary programming options are also carried out over the serial interface.

- **Low Power Mode**
  Low Power Mode is a power saving mode with fast start-up. In Low Power Mode, all internal digital registers are frozen and the power consumption is reduced to max. 1.5mA. The serial interface remains active. Start-up from this mode to normal operation can be accomplished within 150µs. This mode is recommended for applications, where low power, but fast start-up and short reading cycle intervals are required.
- **Ultra-low Power Mode**
  Ultra-low Power Mode is a power saving mode with even reduced power-down current consumption. In this mode, all chip functions are frozen and the power consumption is reduced to max. 50µA. The serial interface remains active. Start-up from this mode to normal operation can be accomplished within 500µs. This mode is recommended for applications, where very low average power consumption is required, e.g. for battery operated equipment. For example, in a cycled operation with 10 readings per second, the average power consumption of the AS5030 can be reduced to only 120µA.

## 8.2 AS5030 Read / Write Commands

Data transmission with the AS5030 is handled over the 2-wire or 3-wire interface. The transmission protocol begins with sending a 5-bit command to the AS5030, followed by reading or writing 16 or 18 bits of data:

### 8.2.1 16-bit Read Command

| Command | Bin | Hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RD ANGLE | 00000 | 00 | C2 | lock | AGC 5:0 | | | | | | Angle 7:0 | | | | | | | |

**C2** displays status of hardware pin C2 (pin #15)

**Lock** indicates that the AGC is locked. Data is invalid when this bit is 0

**AGC** 6-bit AGC register. Indicates the strength of the magnet (e.g. for push-button applications)

$000000_b$ indicates a strong magnetic field
$111111_b$ indicates a weak magnetic field
ideally, the vertical distance of the magnet should be chosen such that the AGC value is in the middle (around 100000b)

**Angle** 8-bit Angle value; represents the rotation angle of the magnet. One step = 360°/256 = 1.4°

### 8.2.2 16-bit Write Command

These settings are temporary; they cannot be programmed permanently. The settings will be lost when the power supply is removed.

| Command | Bin | Hex | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EN PROG | 10000 | 10 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| SET PWR MODE | 10001 | 11 | ULP/ LPn | PSM | 0 | | | | | | | | | | | | | |
| DIS HYST | 10011 | 13 | HYS | 0 | | | | | | | | | | | | | | |
| DIS AGC | 10101 | 15 | 0 | 0 | 0 | 0 | 0 | rst | 0 | 0 | 0 | AGC 5:0 | | | | | | FA |

**EN PROG** command must be sent with a fixed 16-bit code ($8CAE_H$) to enable subsequent OTP access.

**ULP/LP**n selects the Ultra-low Power Mode, when bit PSM is set: 0 = Low Power Mode, 1 = Ultra-low Power Mode

**PSM** enables power saving modes: 0 = normal operation, 1 = reduced power mode selected by bit ULP/LPn

**HYS** disables the hysteresis of the digital serial and PWM outputs:
0 (default) = 1-bit hysteresis, 1 = no hysteresis

**DIS AGC** disables the automatic gain control. The AGC will be frozen to a gain setting written in bits AGC 5:0 (D6:D1), bit FA must be set.

**rst** General Reset: 0 = normal operation, 1 = perform general reset (required after return from reduced power modes)

**FA** Freeze AGC; 0 = normal operation, 1= freeze AGC with the values stored in bits AGC 5:0. The PWM output will be invalid when bit FA is set.

### 8.2.3 18-bit OTP Read Commands

**Note:** To prohibit unintentional access to the OTP register, OTP PROG/write access is only enabled after the EN PROG command has been sent. OTP access is locked again by sending a RD ANGLE or SET PWR MODE command.

EN PROG need not to be sent before a READ OTP.

During the 18bit OTP read/write transfer, each bit needs 4 clock pulses to be validated.

| Command | Bin | Hex | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| READ OTP | 01111 | 0F | reserved for factory settings | | | | | | | | sens 1:0 | | zero position 7:0 | | | | | | | |
| ANALOG OTP RD | 01001 | 09 | reserved for factory settings | | | | | | | | sens 1:0 | | zero position 7:0 | | | | | | | |

**READ OTP** reads the contents of the OTP register in digital form. The reserved area may contain any value

**ANALOG OTP RD** reads the contents of the OTP register as an analog voltage at pin PROG

**sens** reads the sensitivity setting of the Hall elements: 00 = low sensitivity, 11 = high sensitivity

**zero position** reads the programmed zero position; the actual angle of the magnet which is displayed as 000

### 8.2.4 18-bit OTP Write Commands

During the 18bit OTP read/write transfer, each bit needs 4 clock pulses to be validated.

| Command | Bin | Hex | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WRITE OTP | 11111 | 1F | copy factory settings obtained from READ OTP command | | | | | | | | sens 1:0 | | zero position 7:0 | | | | | | | |
| PROG OTP | 11001 | 19 | 00000000 reserved for factory settings, | | | | | | | | sens 1:0 | | zero position 7:0 | | | | | | | |

**WRITE OTP:** non-permanent ("soft write") modification of the OTP register. To set the reserved factory settings area properly, a preceding READ OTP command must be made to receive the correct setting for bits D17:D10. The WRITE OTP command must then set these bits in exactly the same way. Improper setting of the factory settings by a WRITE OTP command may cause malfunction of the chip. The OTP register, including the factory settings can be restored to default by a power-up cycle.
For non-permanent writing, a programming voltage at pin PROG (#2) is not required. EN_PROG must be sent before WRITE_OTP to enable OTP.

**PROG OTP:** permanent modification of the OTP register. An unprogrammed OTP bit contains a '0, programmed bits are 1's. It is possible to program the OTP in several sequences. However, only a 0 can be programmed to 1. Once programmed, an OTP bit cannot be set back to 0. For subsequent programming, bits that are already programmed should be set to 0 to avoid double programming.
During permanent programming, the factory settings D17:D10 should always be set to zero to avoid modification of the factory settings. Modifying the factory settings may cause irreversible malfunction of the chip.
For permanent programming, a static programming voltage of 8.0-8.5V must be applied at pin PROG (#2). EN_PROG must be sent before PROG_OTP to enable OTP.

**sens** sets the sensitivity setting of the Hall elements:
00: gain factor = 1.65 (low sensitivity)
01: gain factor = 1.75
10: gain factor = 1.86
11: gain factor = 2.00 (high sensitivity)
**zero position** sets the user programmable zero position; the actual angle of the magnet which is displayed as 000

*Figure 21. Timing Diagram in OTP 18-bit Read/Write Mode*