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AS5043

Programmable 360° Magnetic Angle Encoder with Absolute SSI and Analog Outputs

General Description

The AS5043 is a contactless magnetic angle encoder for accurate measurement up to 360°.

It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device.

The AS5043 provides a digital 10-bit as well as a programmable analog output that is directly proportional to the angle of a magnet, rotating over the chip.

The analog output can be configured in many ways, including user programmable angular range, adjustable output voltage range, voltage or current output, etc...

An internal voltage regulator allows operation of the AS5043 from 3.3V or 5.0V supplies.

Ordering Information and *Content Guide* appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5043, Programmable 360° Magnetic Angle Encoder with Absolute SSI and Analog Outputs are listed below:

Figure 1:
Added Value of Using AS5043

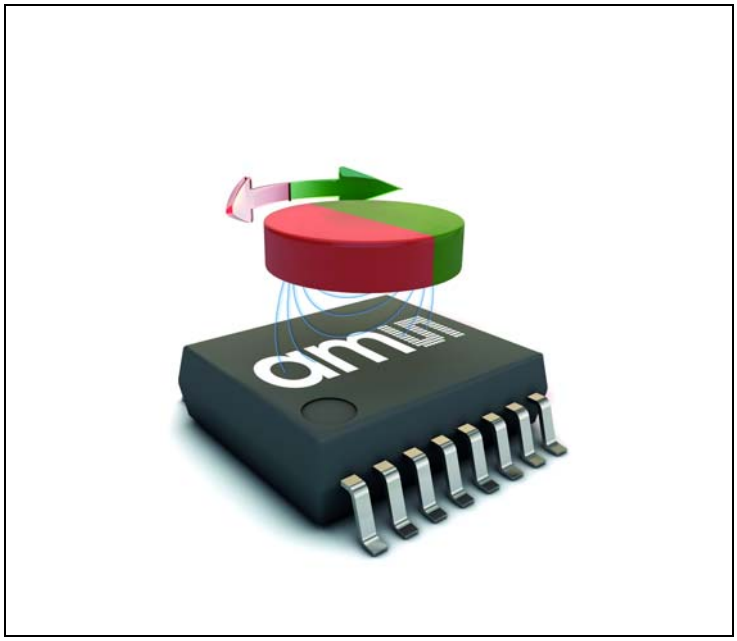
Benefits	Features
• Highest reliability and durability	• Contactless high resolution rotational position encoding over a full turn of 360 degrees
• Simple programming	• Simple user-programmable zero position
• Multiple interfaces	• Serial communication interface (SSI) • Programmable 10-bit analog output
• Ideal for robotic and motor applications	• Input mode for optimizing noise vs. speed
• Failure diagnostics	• Failure detection mode for magnet placement monitoring and loss of power supply
• Easy setup	• Serial read-out of multiple interconnected AS5043 devices using Daisy Chain mode
• Small form factor	• SSOP 16 (5.3mm x 6.2mm)
• Robust environmental tolerance	• Wide temperature range: -40°C to 125°C

Applications

AS5043, Programmable 360° Magnetic Angle Encoder with Absolute SSI and Analog Outputs is ideal for applications with an angular travel range from a few degrees up to a full turn of 360°, such as:

- Industrial applications:
  - Contactless rotary position sensing
  - Robotics
  - Valve controls
- Automotive applications:
  - Throttle position sensors
  - Gas/brake pedal position sensing
  - Headlight position control
- Front panel rotary switches
- Replacement of potentiometers

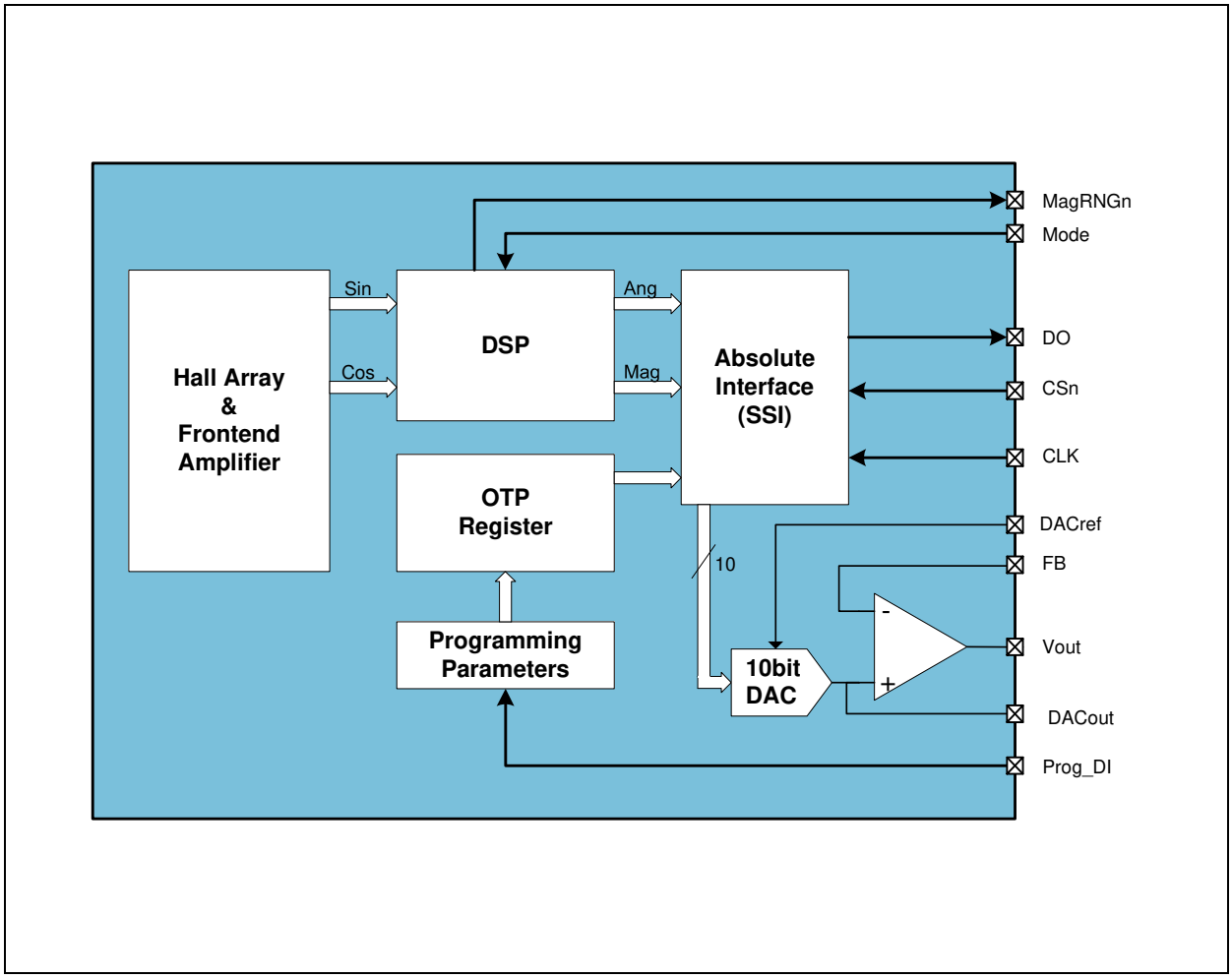
Figure 2:
Typical Arrangement of AS5043 and Magnet



Block Diagram

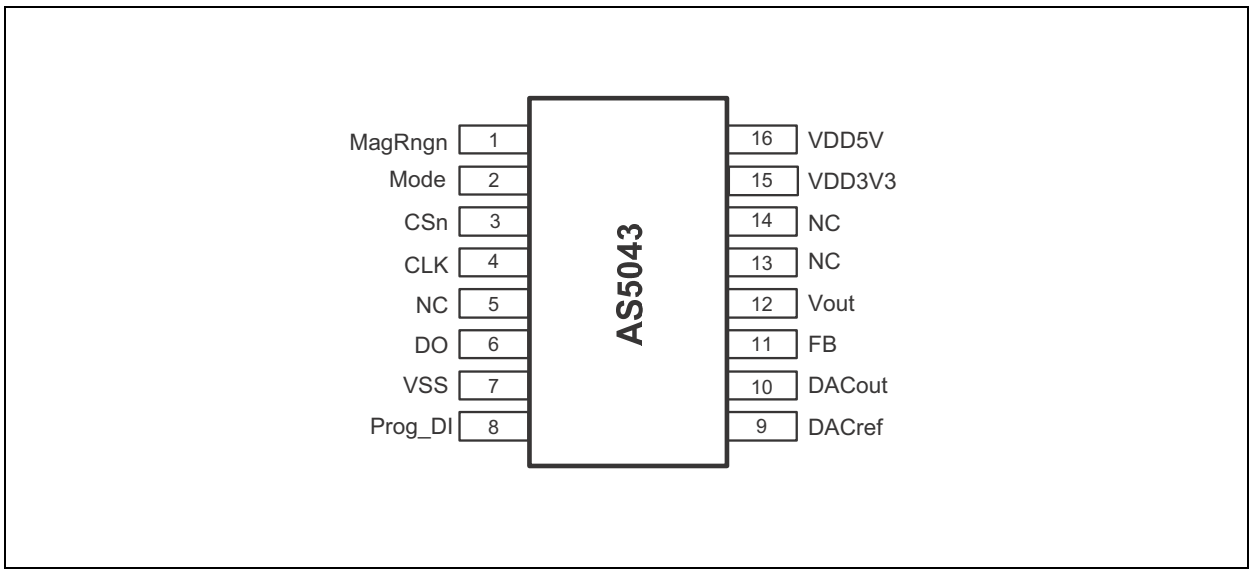
The functional blocks of this device are shown below:

Figure 3:
AS5043 Block Diagram



Pin Assignment

Figure 4:
AS5043 Pin Configuration SSOP16



Package = SSOP16 (16 lead Shrink Small Outline Package)

Figure 5:
Pin Description SSOP16

Pin	Symbol	Type	Description
1	MagRngn	DO_OD	Magnet Field **Mag**nitude **R**a**NG**e warning; active low, indicates that the magnetic field strength is outside of the recommended limits.
2	Mode	DI_PD, ST	**Mode** input. Select between low noise (low, connect to VSS) and high speed (high, connect to VDD5V) mode at power up. Internal pull-down resistor.
3	CSn	DI_PU, ST	**C**hip **S**elect, active low; Schmitt-Trigger input, internal pull-up resistor (~50kΩ)
4	CLK	DI,ST	**Cl**oc**k** Input of Synchronous Serial Interface; Schmitt-Trigger input
5	NC	-	Must be left unconnected
6	DO	DO_T	**D**ata **O**utput of Synchronous Serial Interface
7	VSS	S	Negative Supply Voltage (GND)
8	Prog_DI	DI_PD	OTP **Prog**ramming Input and Data Input for Daisy Chain mode. Internal pull-down resistor (~74kΩ). Should be connected to VSS if programming is not used
9	DACref	AI	**DAC Ref**erence voltage input for external reference
10	DACout	AO	**DAC out**put (unbuffered, Ri ~8kΩ)
11	FB	AI	**F**eed**b**ack, OPAMP inverting input

Pin	Symbol	Type	Description
12	Vout	AO	OPAMP **out**put
13	NC	-	Must be left unconnected
14	NC	-	Must be left unconnected
15	VDD3V3	S	3V-Regulator Output for internal core, regulated from VDD5V.Connect to VDD5V for 3V supply voltage. Do not load externally.
16	VDD5V	S	Positive Supply Voltage, 3.0 to 5.5 V

Abbreviations for Pin Types in Figure 5:

DO_OD : Digital output open drain

DI_PD : Digital input pull-down

DI_PU : Digital input pull-up

S : Supply pin

DO_T : Digital output /tri-state

ST : Schmitt-Trigger input

AI : Analog input

AO : Analog output

D1 : Digital input

Pin Description

Pins 7, **15** and **16** are supply pins, pins **5**, **13** and **14** are for internal use and must be left open.

Pin 1 is the magnetic field strength indicator, **MagRNGn**. It is an open-drain output that is pulled to VSS when the magnetic field is out of the recommended range (45mT to 75mT). The chip will still continue to operate, but with reduced performance, when the magnetic field is out of range. When this pin is low, the analog output at pins #10 and #12 will be 0V to indicate the out-of-range condition.

Pin 2 MODE allows switching between filtered (slow) and unfiltered (fast mode). This pin must be tied to VSS or VDD5V, and must not be switched after power up.

Pin 3 Chip Select (**CSn**; active low) selects a device for serial data transmission over the SSI interface. A “logic high” at CSn forces output DO to digital tri-state.

Pin 4 CLK is the clock input for serial data transmission over the SSI interface.

Pin 6 DO (Data Out) is the serial data output during data transmission over the SSI interface.

Pin 8 PROG_DI is used to program the different operation modes, as well as the zero-position in the OTP register.

This pin is also used as a digital input to shift serial data through the device in Daisy Chain Mode.

Pin 9 DACref is the external voltage reference input for the Digital-to-Analog Converter (DAC). If selected, the analog output voltage on pin 12 (V_{out}) will be ratiometric to the voltage on this pin.

Pin10 DACout is the unbuffered output of the DAC. This pin may be used to connect an external OPAMP, etc. to the DAC.

Pin 11 FB (**F**eedback) is the inverting input of the OPAMP buffer stage.

Access to this pin allows various OPAMP configurations.

Pin 12 Vout is the analog output pin. The analog output is a DC voltage, ratiometric to VDD5V (3.0 – 5.5V) or an external voltage source and proportional to the angle.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
VDD5V	DC supply voltage at pin VDD5V	-0.3	7	V	Pin VDD5V
VDD3V3			5	V	Pin VDD3V3
V_{in}	Input pin voltage	-0.3	VDD5V +0.3	V	Pins MagRngn, Mode, CSn, CLK, DO, DACout, FB, Vout
		-0.3	5		Pin DACref
		-0.3	7.5		Pin PROG_DI
I_{scr}	Input current (latchup immunity)	-100	100	mA	JEDEC 78
ESD	Electrostatic discharge	±2		kV	MIL 883 E method 3015
T_{strg}	Storage temperature	-55	125	°C	Min – 67°F; Max 257°F
T_{Body}	Body temperature		260	°C	t=20s to 40s, IPC/JEDEC J-Std-020C Lead finish 100% Sn “matte tin”
RH_{NC}	Relative humidity (non condensing)	5	85	%	
MSL	Moisture sensitivity level	3			Maximum floor life time of 168h

Electrical Characteristics

Operating Conditions

Figure 7:
Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{amb}	Ambient temperature	-40		125	°C	-40°F to 257°F
I_{supp}	Supply current		16	21	mA	
VDD5V	Supply voltage at pin VDD5V	4.5	5.0	5.5	V	5V operation
VDD3V3	Voltage regulator output voltage at pin VDD3V3	3.0	3.3	3.6	V	
VDD5V	Supply voltage at pin VDD5V	3.0	3.3	3.6	V	3.3V operation (pins VDD5V and VDD3V3 connected)
VDD3V3	Supply voltage at pin VDD3V3	3.0	3.3	3.6	V	

DC Characteristics for Digital Inputs and Outputs

CMOS Schmitt-Trigger Inputs: CLK, CSn (Internal Pull-Up), Mode (Internal Pull-Down)

(operating conditions: T_{amb} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation) VDD5V = 4.5V to 5.5V (5V operation) unless otherwise noted)

Figure 8:
CMOS Schmitt-Trigger Inputs: CLK, CSn (CSn = Internal Pull-Up), Mode (Internal Pull-Down)

Symbol	Parameter	Min	Max	Unit	Note
V_{IH}	High level input voltage	0.7 * VDD5V		V	Normal operation
V_{IL}	Low level input voltage		0.3 * VDD5V	V	
V_{Ion}-V_{Ioff}	Schmitt Trigger hysteresis	1		V	
I_{LEAK}	Input leakage current	-1	1	µA	Pin CLK, VDD5V = 5.0V
I_{iL}	Pull-up low level input current	-30	-100	µA	Pin CSn, VDD5V= 5.0V
I_{iH}	Pull-down high level input current	30	100	µA	Pin Mode, VDD5V= 5.0V

CMOS Input: Program Input (Prog)

(operating conditions: T_{amb} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation) VDD5V = 4.5V to 5.5V (5V operation) unless otherwise noted)

Figure 9:
CMOS Input: Program Input (Prog)

Symbol	Parameter	Min	Max	Unit	Note
V_{IH}	High level input voltage	0.7 * VDD5V	5	V	
V_{PROG}	High level input voltage	See Programming Conditions		V	During programming
V_{IL}	Low level input voltage		0.3 * VDD5V	V	
I_{iL}	Pull-down high level input current		100	µA	VDD5V: 5.5V

CMOS Output Open Drain: MagRngn

(operating conditions: T_{amb} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation) VDD5V = 4.5V to 5.5V (5V operation) unless otherwise noted).

Figure 10:
CMOS Output Open Drain: MagRngn

Symbol	Parameter	Min	Max	Unit	Note
V_{OL}	Low level output voltage		VSS+0.4	V	
I_O	Output current		4 2	mA	VDD5V: 4.5V VDD5V: 3V
I_{OZ}	Open drain leakage current		1	µA	

Tristate CMOS Output: DO

(operating conditions: T_{amb} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation) VDD5V = 4.5V to 5.5V (5V operation) unless otherwise noted).

Figure 11:
Tristate CMOS Output: DO

Symbol	Parameter	Min	Max	Unit	Note
V_{OH}	High level output voltage	VDD5V-0.5		V	
V_{OL}	Low level output voltage		VSS+0.4	V	
I_O	Output current		4 2	mA	VDD5V: 4.5V VDD5V: 3V
I_{OZ}	Tri-state leakage current		1	µA	

Digital-to-Analog Converter

Figure 12:
Digital-to-Analog Converter

Symbol	Parameter	Min	Typ	Max	Unit	Note	OTP Setting
	Resolution		10		bit		
V_{OUTM1}	Output range	0		Vref	V	0% …100% V_{ref} (default)	ClampMdEn = 0 (default)
V_{OUTM2}		0.10 *Vref		0.90 *Vref	V	10% …90% V_{ref}	ClampMdEn = 1
$R_{Out,DAC}$	Output resistance			8	kΩ	Unbuffered Pin DACout (#10)	
V_{ref}	DAC reference voltage (DAC full scale range)	0.2		VDD3V3 - 0.2	V	DAC reference = external: Pin: DACref (#9)	RefExt EN = 1
				VDD5V / 2	V	DAC reference = internal	RefExtEn = 0 (default)
INL_{DAC}	Integral non-linearity			±1.5	LSB	Non-Linearity of DAC and OPAMP; -40°C to 125°C, for all analog modes: 1LSB = Vref / 1024	
DNL_{DAC}	Differential non-linearity			±0.5	LSB		
Hyst	Analog output hysteresis			1	LSB	All analog modes	
				2	LSB	At 360°-0° transition, 360° mode only	OR1,OR0 = 00 (default)

OPAMP Output Stage

Figure 13:
OPAMP Output Stage

Symbol	Parameter	Min	Typ	Max	Unit	Note
VDD5V	Power Supply Range	3.0		5.5	V	
CL	Parallel Load Capacitance			100	pF	
RL	Parallel Load Resistance	4.7			kΩ	3.3V operation
A0	Open Loop Gain	92	130	144	dB	
VosOP	Offset Voltage RTI	-5		5	mV	3 sigma
VoutL	Output Range Low			0.05 * VDD5V	V	Linear range of analog output
VoutH	Output Range High	0.95 * VDD5V			V	
Isink	Current capability sink	4.8		50	mA	Permanent short circuit current: V_{out} to VDD5V
Isource	Current capability source	4.6		66	mA	Permanent short circuit current: V_{out} to VSS
V_{noise}	Output noise	160	220	490	µVrms	Over full temperature range; BW= 1Hz …10MHz, Gain = 2x
Gain	OPAMP gain (non-inverting)		2			Internal; OTP: FB_int EN = 1
		1		4		External OTP: FB_int EN = 0 (default) With external resistors, pins Vout [#12] and FB [#11]: see Figure 33

Magnetic Input Specification

(operating conditions: T_{amb} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation) VDD5V = 4.5V to 5.5V (5V operation) unless otherwise noted).

Two-pole cylindrical diametrically magnetized source:

Figure 14:
Magnetic Input Specification

Symbol	Parameter	Min	Typ	Max	Unit	Note
d_{mag}	Diameter	4	6		mm	Recommended magnet: Ø 6mm x 2.5mm for cylindrical magnets
t_{mag}	Thickness	2.5			mm	
B_{pk}	Magnetic input field amplitude	45		75	mT	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm
B_{off}	Magnetic offset			± 10	mT	Constant magnetic stray field
	Field non-linearity			5	%	Including offset gradient
f_{mag_abs}	Input frequency (rotational speed of magnet)			10	Hz	Absolute mode: 600 rpm @ readout of 1024 positions (see Figure 48)
f_{mag_inc}				166	Hz	Incremental mode: no missing pulses at rotational speeds of up to 10,000 rpm (see Figure 48)
Disp	Displacement radius			0.25	mm	Max. offset between defined device center and magnet axis
	Recommended magnet material and temperature drift		-0.12		%/K	NdFeB (Neodymium Iron Boron)
			-0.035			SmCo (Samarium Cobalt)

Electrical System Specifications

(operating conditions: T_{amb} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation) VDD5V = 4.5V to 5.5V (5V operation) unless otherwise noted).

Figure 15:
Electrical System Specifications

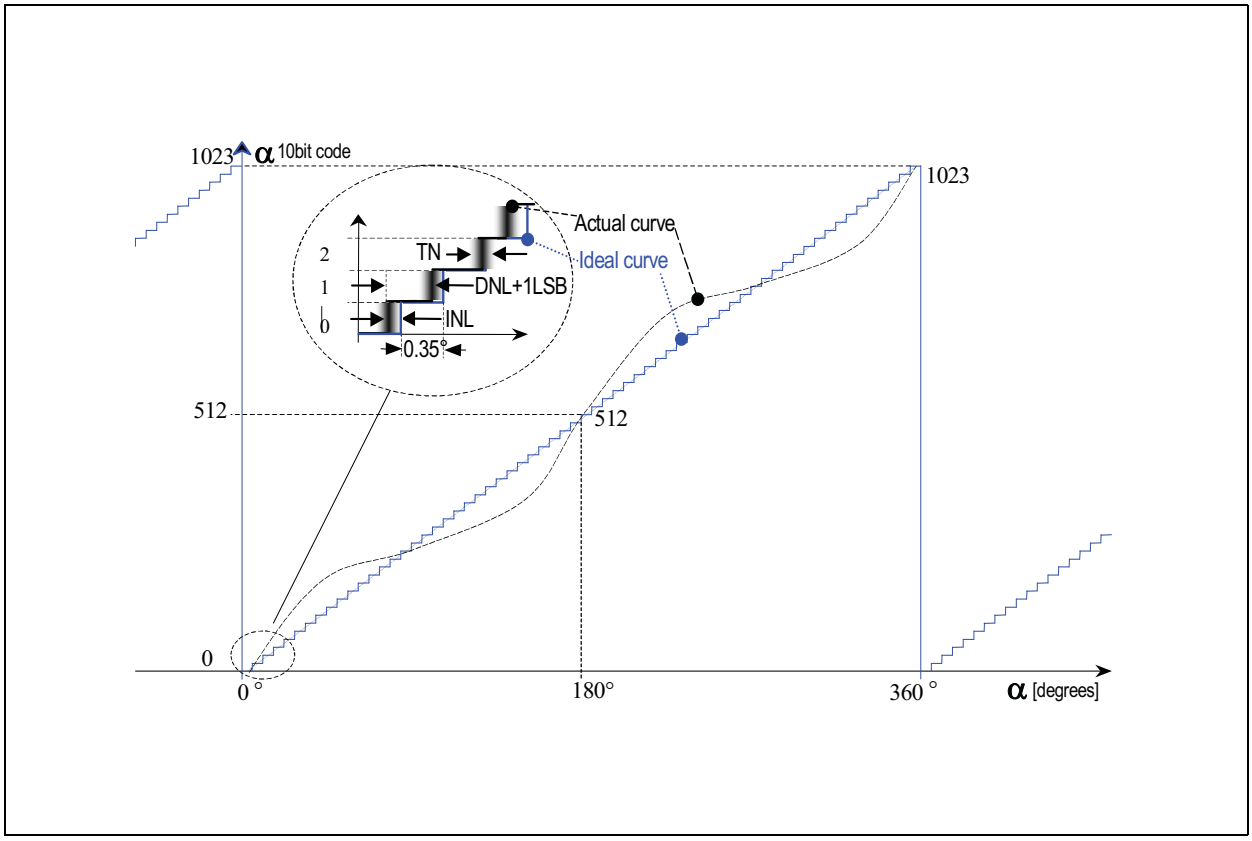
Symbol	Parameter	Min	Typ	Max	Unit	Note
RES	Resolution (1)			10	bit	0.352 deg
INL_{opt}	Integral non-linearity (optimum)(1)			± 0.5	deg	Maximum error with respect to the best line fit. Verified at optimum magnet placement, T_{amb} =25 °C.
INL_{temp}	Integral non-linearity (optimum) (1)			± 0.9	deg	Maximum error with respect to the best line fit. Verified at optimum magnet placement, T_{amb} = -40°C to 125°C
INL	Integral non-linearity (1)			± 1.4	deg	Best line fit = (Err_{max} – Err_{min}) / 2 Over displacement tolerance with 6mm diameter magnet, T_{amb} = -40°C to 125°C
DNL	Differential non-linearity (1)			±0.176	deg	10bit, no missing codes
TN	Transition noise (1)			0.06	deg RMS	1 sigma, fast mode (pin MODE = 1)
				0.03		1 sigma, slow mode (pin MODE=0 or open)
V_{on}	Power-ON reset threshold ON voltage; 300mV typ. hysteresis	1.37	2.2	2.9	V	DC supply voltage 3.3V (VDD3V3)
V_{off}	Power-ON reset threshold OFF voltage; 300mV typ. hysteresis	1.08	1.9	2.6	V	DC supply voltage 3.3V (VDD3V3)
t_{PwrUp}	Power-up time, Until offset compensation finished, OCF = 1, Angular Data valid			20	ms	Fast mode (pin MODE=1)
				80		Slow mode (pin MODE=0 or open)
t_{delay}	System propagation delay absolute output : delay of ADC and DSP			96	µs	Fast mode (pin MODE=1)
				384		Slow mode (pin MODE=0 or open)

Symbol	Parameter	Min	Typ	Max	Unit	Note
$f_{S, mode\ 0}$	Internal sampling rate for absolute output	2.48	2.61	2.74	kHz	T_{amb} = 25°C, slow mode (pin MODE = 0 or open)
		2.35	2.61	2.87		T_{amb} = -40°C to 125°C, slow mode (pin MODE = 0 or open)
$f_{S, mode\ 1}$	Internal sampling rate for absolute output	9.90	10.42	10.94	kHz	T_{amb} = 25°C, fast mode (pin MODE = 1)
		9.38	10.42	11.46		T_{amb} = -40°C to 125°C, fast mode (pin MODE = 1)
CLK	Read-out frequency	>0		1	MHz	Max. clock frequency to read out serial data

Note(s) and/or Footnote(s):

1. Digital interface

Figure 16:
Integral and Differential Non-Linearity Example (exaggerated curve)



Integral Non-Linearity (INL) is the maximum deviation between actual position and indicated position.

Differential Non-Linearity (DNL) is the maximum deviation of the step length from one position to the next.

Transition Noise (TN) is the repeatability of an indicated position.

Timing Characteristics

Synchronous Serial Interface (SSI)

(operating conditions: T_{amb} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation) VDD5V = 4.5V to 5.5V (5V operation) unless otherwise noted).

Figure 17:
Synchronous Serial Interface (SSI)

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_{DO} active	Data output activated (logic high)			100	ns	Time between falling edge of CSn and data output activated
$t_{CLK\ FE}$	First data shifted to output register	500			ns	Time between falling edge of CSn and first falling edge of CLK
$T_{CLK\ /\ 2}$	Start of data output	500			ns	Rising edge of CLK shifts out one bit at a time
$t_{DO\ valid}$	Data output valid			413	ns	Time between rising edge of CLK and data output valid
$t_{DO\ tristate}$	Data output tristate			100	ns	After the last bit DO changes back to “tristate”
t_{CSn}	Pulse width of CSn	500			ns	CSn = high; To initiate read-out of next angular position
f_{CLK}	Read-out frequency	>0		1	MHz	Clock frequency to read out serial data

Programming Conditions

(operating conditions: T_{amb} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation) VDD5V = 4.5V to 5.5V (5V operation) unless otherwise noted).

Figure 18:
Programming Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
$t_{Prog\ enable}$	Programming enable time	2			µs	Time between rising edge at Prog pin and rising edge of CSn
$t_{Data\ in}$	Write data start	2			µs	
$t_{Data\ in\ valid}$	Write data valid	250			ns	Write data at the rising edge of CLK_{PROG}
$t_{Load\ PROG}$	Load programming data	3			µs	
t_{PrgR}	Rise time of V_{PROG} before CLK_{PROG}	0			µs	
t_{PrgH}	Hold time of V_{PROG} after CLK_{PROG}	0		5	µs	
CLK_{PROG}	Write data – programming CLK_{PROG}			250	kHz	
t_{PROG}	CLK pulse width	1.8	2	2.2	µs	During programming; 16 clock cycles
$t_{PROG\ finished}$	Hold time of V_{PROG} after programming	2			µs	Programmed data is available after next power-on
V_{PROG}	Programming voltage	7.3	7.4	7.5	V	Must be switched OFF after zapping
$V_{ProgOff}$	Programming voltage OFF level	0		1	V	Line must be discharged to this level
I_{PROG}	Programming current			130	mA	During programming
CLK_{Aread}	Analog read CLK			100	kHz	Analog readback mode
$V_{programmed}$	Programmed Zener voltage (log.1)			100	mV	V_{Ref}-V_{PROG} during analog readback mode (see Analog Readback Mode)
$V_{unprogrammed}$	Unprogrammed Zener voltage (log. 0)	1			V	

Functional Description

The AS5043 is manufactured in a CMOS standard process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip.

The integrated Hall elements are placed in a circle around the center of the device and deliver a voltage representation of the magnetic field perpendicular to the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5043 provides accurate high-resolution absolute angular position information. For this purpose a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals.

The DSP is also used indicate movements of the magnet towards or away from the chip and to indicate, when the magnetic field is outside of the recommended range (status bits = MagInc, MagDec; hardware pin = MagRngn).

A small low cost diametrically magnetized (two-pole) standard magnet, centered over the chip, is used as the input device.

The AS5043 senses the orientation of the magnetic field and calculates a 10-bit binary code. This code can be accessed via a Synchronous Serial Interface (SSI). In addition, the absolute angular representation is converted to an analog signal, ratiometric to the supply voltage.

The analog output can be configured in many ways, such as 360°/180°/90° or 45° angular range, external or internal DAC reference voltage, 0-100%*VDD or 10-90% *VDD analog output range, external or internal amplifier gain setting.

The various output modes as well as a user programmable zero position can be programmed in an OTP register. As long as no programming voltage is applied to pin PROG, the new setting may be overwritten at any time and will be reset to default when power is cycled. To make the setting permanent, the OTP register must be programmed by applying a programming voltage.

The AS5043 is tolerant to magnet misalignment and unwanted external magnetic fields due to differential measurement technique and Hall sensor conditioning circuitry.

It is also tolerant to airgap and temperature variations due to Sin-/Cos- signal evaluation.

3.3V / 5V Operation

The AS5043 operates either at 3.3V ±10% or at 5V ±10%. This is made possible by an internal 3.3V Low-Dropout (LDO) Voltage regulator. The core supply voltage is always taken from the LDO output, as the internal blocks are always operating at 3.3V.

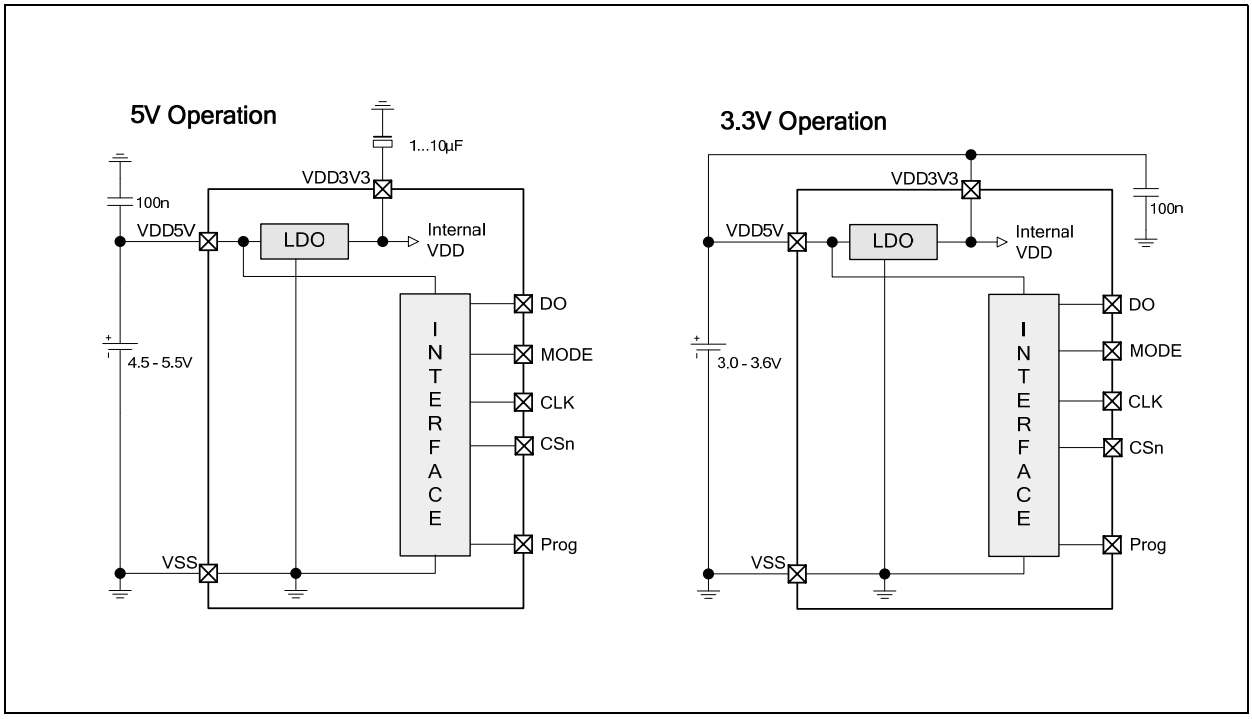
For 3.3V operation, the LDO must be bypassed by connecting VDD3V3 with VDD5V (see Figure 19).

For 5V operation, the 5V supply is connected to pin VDD5V, while VDD3V3 (LDO output) must be buffered by a 1 to10µF capacitor, which should be placed close to the supply pin.

The VDD3V3 output is intended for internal use only. It should not be loaded with an external load.

The voltage levels of the digital interface I/O's correspond to the voltage at pin VDD5V, as the I/O buffers are supplied from this pin (see Figure 19).

Figure 19:
Connections for 5V / 3.3V Supply Voltages



A buffer capacitor of 100nF is recommended in both cases close to pin VDD5V. Note that pin VDD3V3 must always be buffered by a capacitor. It must not be left floating, as this may cause an instable internal 3.3V supply voltage which may lead to larger than normal jitter of the measured angle.

10-Bit Absolute Synchronous Serial Interface (SSI)

The serial data transmission timing is outlined in Figure 21: if CSn changes to logic low, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out sequence will be initiated. After a minimum time $t_{CLK\ FE}$, data is latched into the output shift register with the first falling edge of CLK.

Each subsequent rising CLK edge shifts out one bit of data.The serial word contains 16 bits, the first 10 bits are the angular information D[9:0], the subsequent 6 bits contain system information, about the validity of data such as OCF, COF, LIN, Parity and Magnetic Field status (increase / decrease / out of range).
A subsequent measurement is initiated by a logic "high" pulse at CSn with a minimum duration of t_{CSn}. Data transmission may be terminated at any time by pulling CSn = high.

Serial Data Contents

D9:D0 absolute angular position data (MSB is clocked out first).

OCF (**O**ffset **C**ompensation **F**inished), logic high indicates that the Offset Compensation Algorithm has finished and data is valid.

COF (**C**ORDIC **O**verflow), logic high indicates an out of range error in the CORDIC part. When this bit is set, the data at D9:D0 is invalid. The absolute output maintains the last valid angular value. This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

LIN (**L**inearity Alarm), logic high indicates that the input field generates a critical output linearity. When this bit is set, the data at D9:D0 may still be used, but may contain invalid data. This warning may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

Data D9:D0 is valid, when the status bits have the following configurations:

Figure 20:
Status Bit Outputs

OCF	COF	LIN	Mag INC	Mag DEC	Parity
1	0	0	0	0	Even checksum of bits 1:15
			0	1	
			1	0	

MagInc, (**M**agnitude **I**ncrease) becomes HIGH, when the magnet is pushed towards the IC, thus the magnetic field strength is increasing.

MagDec, (**M**agnitude **D**ecrease) becomes HIGH, when the magnet is pulled away from the IC, thus the magnetic field strength is decreasing.

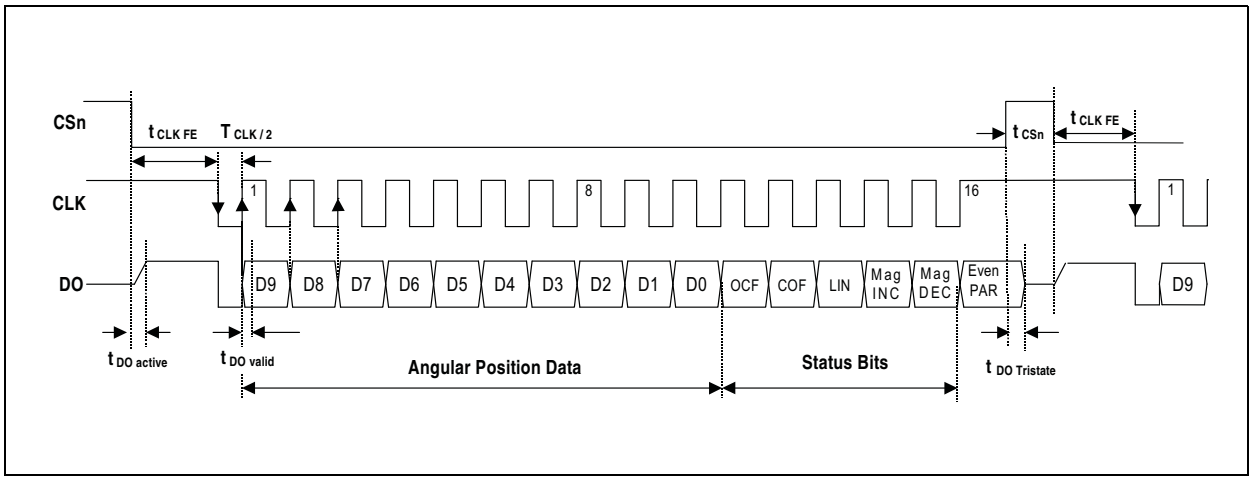
Both signals HIGH indicate a magnetic field that is out of the allowed range (see Figure 22).

Note(s): Pin 1 (MagRngn) is a combination of MagInc and MagDec. It is active low via an open drain output and requires an external pull-up resistor. If the magnetic field is in range, this output is turned OFF. (logic "high").

Even Parity bit for transmission error detection of bits 1 …15 (D9 …D0, OCF, COF, LIN, MagInc, MagDec)

The absolute angular output is always set to a resolution of 10 bit / 360°. Placing the magnet above the chip, angular values increase in clockwise direction by default.

Figure 21:
Synchronous Serial Interface with Absolute Angular Position Data



Z-Axis Range Indication (Push Button Feature, Red/Yellow/Green Indicator)

The AS5043 provides several options of detecting movement and distance of the magnet in the vertical (Z-) direction. Signal indicators MagINC, MagDEC and LIN are available as status bits in the serial data stream, while MagRngn is an open-drain output that indicates an out-of range status (On in YELLOW or RED range). Additionally, the analog output provides a safety feature in the form that it will be turned OFF when the magnetic field is too strong or too weak (RED range). The serial data is always available, the red/yellow/green status is indicated by the status bits as shown below:

Figure 22:
Magnetic Field Strength Indicators

SSI Status Bits			Hardware Pins		Description
Mag INC	Mag DEC	LIN	Mag Rngn	Analog Output	
0	0	0	OFF	Enabled	No distance change Magnetic Input Field OK (GREEN range, ~45mT … 75mT)
0	1	0	OFF	Enabled	Distance increase, GREEN range; Pull-function. This state is dynamic and only active while the magnet is moving away from the chip.
1	0	0	OFF	Enabled	Distance decrease, GREEN range; Push- function. This state is dynamic and only active while the magnet is moving towards the chip.
1	1	0	ON	Enabled	YELLOW Range: Magnetic field is ~ 25mT …45mT or ~75mT …135mT. The AS5043 may still be operated in this range, but with slightly reduced accuracy.
1	1	1	ON	Disabled	RED Range: Magnetic field is ~<25mT or >~135mT. The analog output will be turned OFF in this range by default. It can be enabled permanently by OTP programming (see Diagnostic Output Mode). It is still possible to use the absolute serial interface in the red range, but not recommended.

Mode Input Pin

The absolute angular position is sampled at a rate of 10.4kHz (t=96µs) in fast mode and at a rate of 2.6kHz (t=384µs) in slow mode.
These modes are selected by pin MODE (#2) during the power up of the AS5043. This pin activates or deactivates an internal filter, which is used to reduce the digital jitter and consequently the analog output noise.
Activating the filter by pulling Mode = LOW reduces the transition noise to <0.03° rms. At the same time, the sampling rate is reduced to 2.6kHz and the signal propagation delay is increased to 384µs. This mode is recommended for high precision, low speed and ≤360° applications.
Deactivating the filter by setting Mode = HIGH increases the sampling rate to 10.4kHz and reduces the signal propagation delay to 96µs. The transition noise will increase to <0.06° rms. This mode is recommended for higher speed and full scale= 360° applications.

Switching the MODE pin affects the following parameters:

Figure 23:
Mode Pin Settings

Parameter	Slow Mode (Pin MODE = 0)	Fast Mode (Pin MODE = 1)
Sampling rate	2.61 kHz (383µs)	10.42 kHz (95.9µs)
Transition noise (1 sigma)	≤ 0.03° rms	≤ 0.06° rms
Propagation delay	384µs	96µs
Startup time	20ms	80ms

The MODE pin should be set at power-up. A change of the mode during operation is not allowed.

Daisy Chain Mode

The Daisy Chain mode allows connection of several AS5043's in series, while still keeping just one digital input for data transfer (see "Data IN" in Figure 24 below). This mode is accomplished by connecting the data output (DO; pin 9) to the data input (Prog; pin 8) of the subsequent device. An RC filter must be implemented between each PROG pin of device n and DO pin of device n+1, to prevent the encoders to enter the alignment mode, in case of ESD discharge, long cables, or not conform signal levels or shape. Using the values R=100R and C=1nF allow a max. CLK frequency of 1MHz on the whole chain. The serial data of all connected devices is read from the DO pin of the first device in the chain. The length of the serial bit stream increases with every connected device, it is

n * (16+1) bits:

e.g. 34 bit for two devices, 51 bit for three devices, etc…

The last data bit of the first device (Parity) is followed by a dummy bit and the first data bit of the second device (D9), etc… (see Figure 25).

Figure 24:
Daisy Chain Hardware Configuration

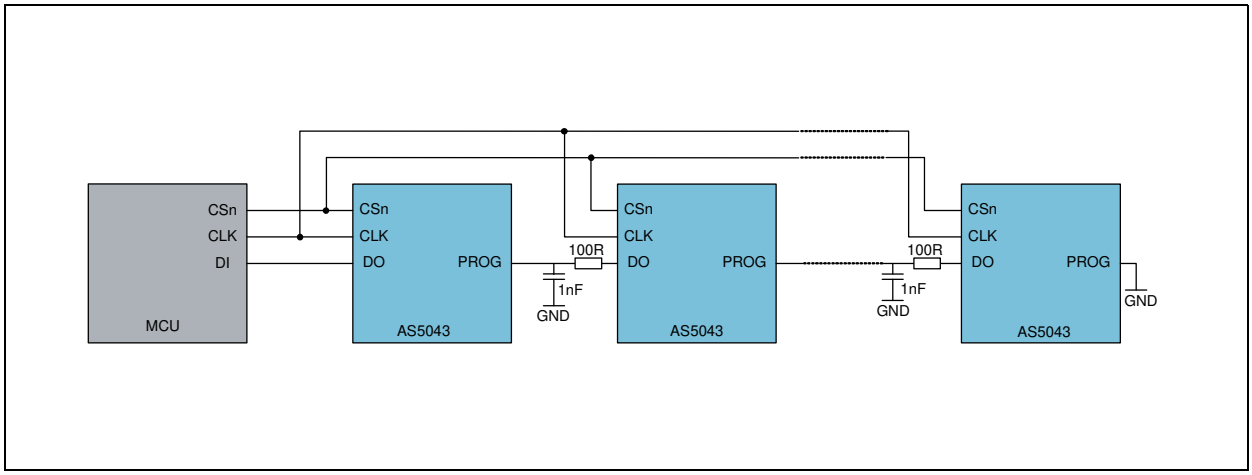
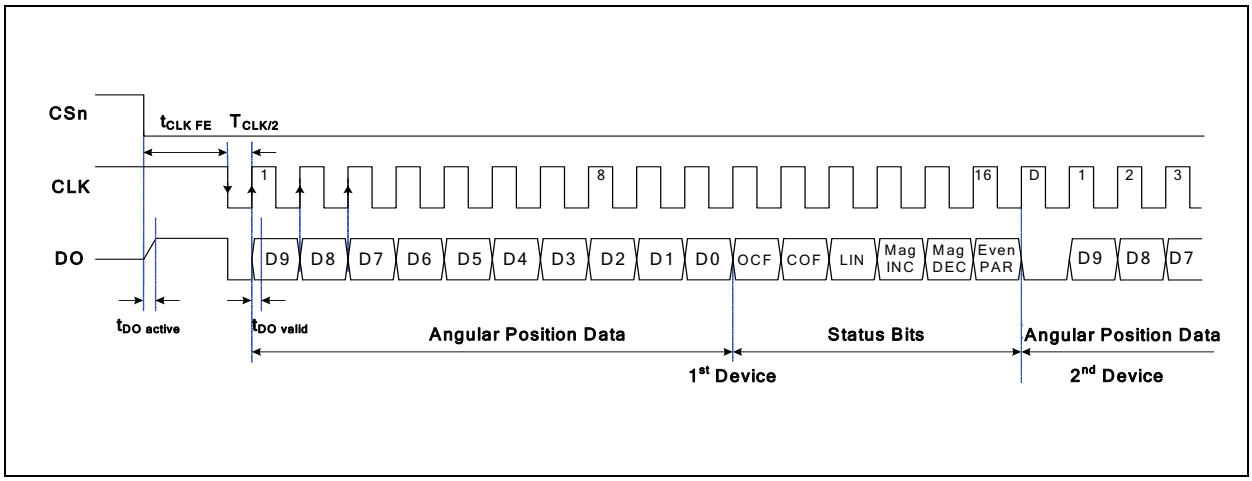


Figure 25:
Daisy Chain Data Transfer Timing Diagram



Analog Output

The analog output V_{out} provides an analog voltage that is proportional to the angle of the rotating magnet and ratiometric to the supply voltage VDD5V (max.5.5V). It can source or sink currents up to ±1mA in normal operation (up to 66mA short circuit current).
The analog output block consists of a digital angular range selector, a 10-bit Digital-to-Analog converter and an OPAMP buffer stage (see Figure 33).
The digital range selector allows a preselection of the angular range for 360°,180°,90° or 45° (see Figure 38). Fine-tuning of the angular range can be accomplished by adjusting the gain of the OPAMP buffer stage.
The reference voltage for the Digital-to-Analog converter (DAC) can be taken internally from VDD5V / 2. In this mode, the output voltage is ratiometric to the supply voltage.
Alternatively, an external DAC reference can be applied at pin DACref (#9). In this mode, the analog output is ratiometric to the external reference voltage.
An ON-chip diagnostic feature turns the analog output OFF in case of an error (broken supply or magnetic field out of range; see Figure 22).
The DAC output can be accessed directly at pin #10 DACout.
The addition of an OPAMP to the DAC output allows a variety of user configurable options, such as variable output voltage ranges and variable output voltage versus angle response. By adding an external transistor, the analog voltage output can be buffered to allow output currents up to hundred milliamperes or more.
Furthermore, the OPAMP can be configured as constant current source.

As an OTP option, the DAC can be configured to 2 different output ranges:
a) 0 to 100% V_{DACref}. The reference point may be either taken from VDD5V/2 or from the external DACref input. The 0%… 100% range allows easy replacement of potentiometers. Due to the nature of rail-to-rail outputs, the linearity will degrade at output voltages that are close to the supply rails.
b) 10%… 90% V_{DACref}. This range allows better linearity, as the OPAMP is not driven to the rails. Furthermore, this mode allows failure detection, when the analog output voltage is outside of the normal operating range of 10%… 90%VDD, as in the case of broken supply or when the magnetic field is out of range and the analog output is turned OFF.

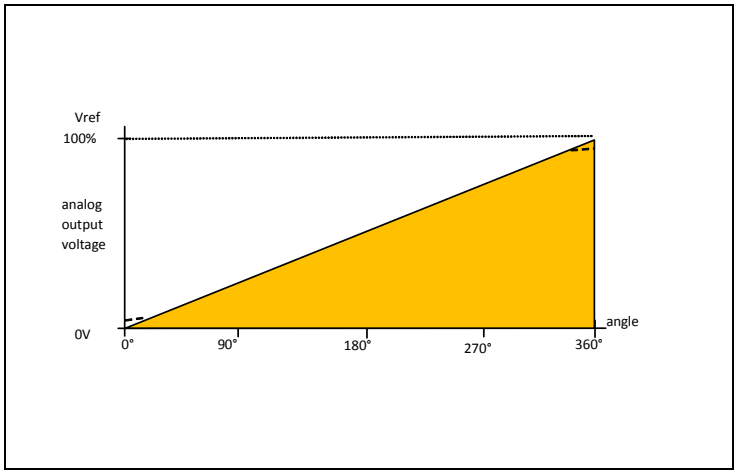
Analog Output Voltage Modes

The Analog output voltage modes are programmable by OTP. Depending on the application, the analog output can be selected as rail-to-rail output or as clamped output with 10%-90% VDD5V.
The output is ratiometric to the supply voltage (VDD5V), which can range from 3.0V to 5.5V. If the DAC reference is switched to an external reference (pin DACref), the output is ratiometric to the external reference.

Full Scale Mode

This output mode provides a ratiometric DAC output of (0% to 100%)x Vref[1], amplified by the OPAMP stage (default =internal 2x gain, see Figure 33)

Figure 26:
Analog Output, Full Scale Mode (shown for 360°mode)



Note(s):

- In real case the output does not reach 100% Vref, because of saturation effects of the OPAMP output driver transistors. Figure 26 describes a linear output voltage from rail to rail (0V to VDD) over 360°.
- See Figure 38 for further angular range programming options.