AS5045B

12-Bit Programmable Magnetic Position Sensor

General Description

The AS5045B is a contactless magnetic position sensor for accurate angular measurement over a full turn of 360 degrees.

It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip, is required. The magnet can be placed above or below the IC.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 0.0879º = 4096 positions per revolution. This digital data is available as a serial bit stream and as a PWM signal.

An internal voltage regulator allows the AS5045B to operate at either 3.3V or 5V supplies.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5045B, 12-Bit Programmable Magnetic Position Sensor are listed below:

Figure 1:
Added Value of Using AS5045B

Benefits	Features
• Highest reliability and durability	• Contactless high resolution rotational position encoding over a full turn of 360 degrees
• Simple programming	• Simple user-programmable zero position and settings
• Multiple interfaces	• Serial communication interface (SSI) • 10-bit pulse width modulated (PWM) output • Quadrature A/B and Index output signal
• Ideal for motor applications	• Rational speeds up to 30,000 rpm
• Failure diagnostics	• Failure detection mode for magnet placement monitoring and loss of power supply
• Easy setup	• Serial read-out of multiple interconnected AS5045B devices using Daisy Chain mode
• Great flexibility at a huge application area	• Detects movement of magnet in Z-axis (Red-Yellow-Green indicator)
• Small form factor	• SSOP 16 (5.3mm x 6.2mm)
• Robust environmental tolerance	• Wide temperature range: -40°C to 125°C

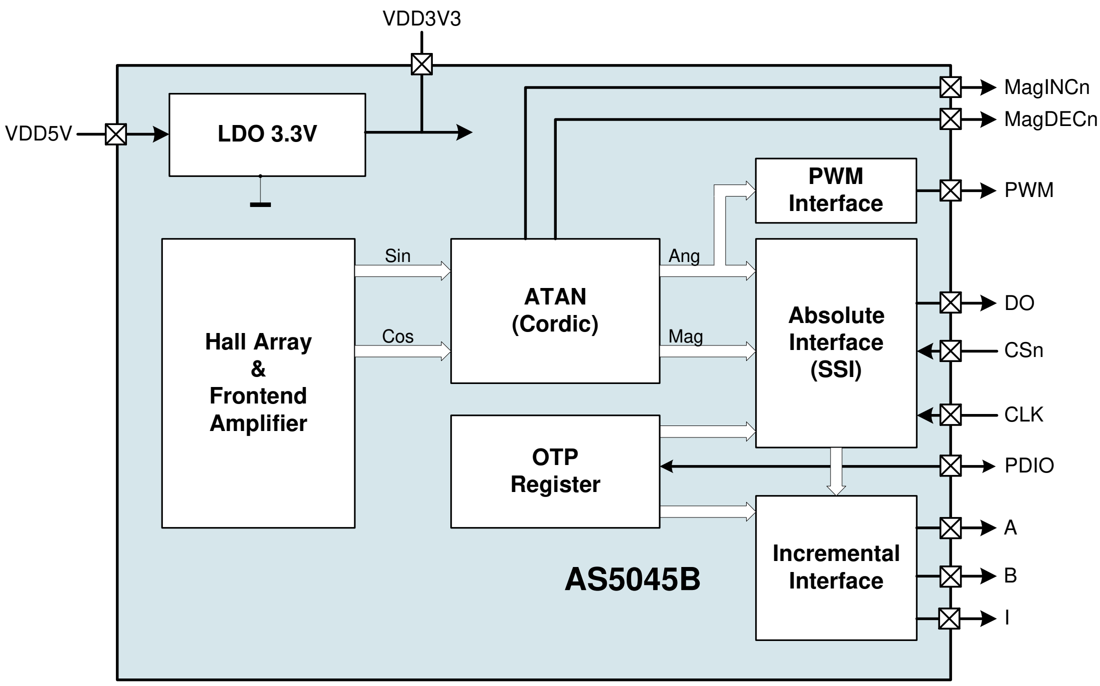
Applications

The device is ideal for industrial applications like automatic or elevator doors, robotics, motor control and optical encoder replacement.

Block Diagram

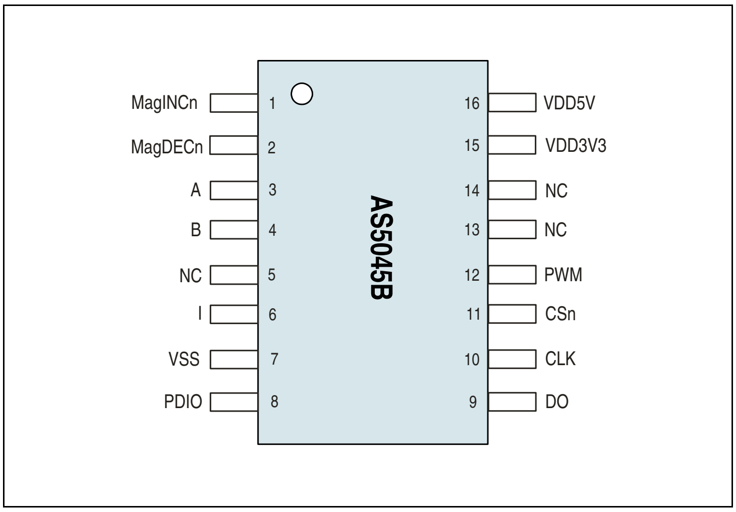
The functional blocks of this device are shown below:

Figure 2:
Block Diagram Rotary Position Sensor IC



Pin Assignment

Figure 3:
Pin Diagram (Top View)



The following SSOP16 shows the description of each pin of the standard SSOP16 package (Shrink Small Outline Package, 16 leads, body size: 5.3mm x 6.2mmm; see Figure 3.

Figure 4:
Pin Description

Pin Name	Pin Number	Pin Type	Description
MagINCn	1	Digital output open drain	**Magnet Field Magnitude Increase.** Active low. Indicates a distance reduction between the magnet and the device surface. (see Figure 14)
MagDECn	2		**Magnet Field Magnitude Decrease.** Active low. Indicates a distance increase between the device and the magnet. (see Figure 14)
A	3	Digital output	Quadrature output A (1024 Pulses)
B	4		Quadrature output B (1024 Pulses)
NC	5	-	Must be left unconnected
I	6	Digital output	Index signal for the quadrature output.
VSS	7	Supply pin	Negative supply voltage (GND)
PDIO	8	Digital input pull-down	**OTP Programming Input and Data Input for Daisy Chain Mode.** Pin has an internal pull-down resistor (74kΩ). Connect this pin to VSS if programming is not required.
DO	9	Digital output/ tri-state	**Data Output** of Synchronous Serial Interface

Pin Name	Pin Number	Pin Type	Description
CLK	10	Digital input, Schmitt-Trigger input	**Clock Input** of Synchronous Serial Interface; Schmitt-Trigger input
CSn	11	Digital input pull-down, Schmitt-Trigger input	**Chip Select.** Active low. Schmitt-Trigger input, internal pull-up resistor (50kΩ)
PWM	12	Digital output	Pulse Width Modulation
NC	13	-	Must be left unconnected
NC	14	-	Must be left unconnected
VDD3V3	15	Supply pin	3V-Regulator output, internally regulated from VDD5V. Connect to VDD5V for 3V supply voltage. Do not load externally.
VDD5V	16	Supply pin	Positive supply voltage, 3.0V to 5.5V

Pin 1 and 2 are the magnetic field change indicators, MagINCn and MagDECn (magnetic field strength increase or decrease through variation of the distance between the magnet and the device). These outputs can be used to detect the valid magnetic field range. Furthermore those indicators can also be used for contactless push-button functionality.

Pin 3 and 4 are used for incremental angle information in 12-bit quadrature signal format. Additional sync mode and sine/cosine mode are used with Pin3 and Pin4.

Pin 6 Index output used for incremental angle information. (Zero position reference).

Pins 7, 15, and 16 are supply pins, pins 5, 13, and 14 are for internal use and must not be connected.

Pin 8 (PDIO) is used to program the zero-position into the OTP (see page 26). This pin is also used as digital input to shift serial data through the device in daisy chain configuration, (see page 17).

Pin 11 Chip Select (CSn; active low) selects a device within a network of AS5045Bs and initiates serial data transfer. A logic high at CSn puts the data output pin (DO) to tri-state and terminates serial data transfer. This pin is also used for alignment mode (see Alignment Mode) and programming mode (see Programming the AS5045B).

Pin 12 allows a single wire output of the 12-bit absolute position value. The value is encoded into a pulse width modulated signal with 1µs pulse width per step (1µs to 4096µs over a full turn). By using an external low pass filter, the digital PWM signal is converted into an analog voltage, e.g. for making a direct replacement of potentiometers possible.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
DC supply voltage at pin VDD5V	-0.3	7	V	
DC supply voltage at pin VDD3V3		5	V	
Input pin voltage	-0.3	VDD5V +0.3	V	Except VDD3V3
Input current (latchup immunity)	-100	100	mA	EIA/JESD78 Class II Level A
Electrostatic Discharge				
Electrostatic discharge	± 2		kV	JESD22-A114E
Temperature Ranges and Storage Conditions				
Storage temperature	-55	150	ºC	Min -67ºF; Max 302ºF
Package body temperature		260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Relative humidity non-condensing	5	85	%	
Moisture sensitivity level (MSL)	3			Represents a maximum floor time of 168h

Electrical Characteristics

T_{AMB} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation) VDD5V = 4.5V to 5.5V (5V operation), unless otherwise noted.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Operating Conditions						
T_{AMB}	Ambient temperature	-40°F to 257°F	-40		125	°C
I_{supp}	Supply current			16	21	mA
VDD5V	Supply voltage at pin VDD5V	5V operation	4.5	5.0	5.5	V
VDD3V3	Voltage regulator output voltage at pin VDD3V3		3.0	3.3	3.6	
VDD5V	Supply voltage at pin VDD5V	3.3V operation (pin VDD5V and VDD3V3 connected)	3.0	3.3	3.6	V
VDD3V3	Supply voltage at pin VDD3V3		3.0	3.3	3.6	
V_{ON}	Power-on reset thresholds On voltage; 300mV typ. hysteresis	DC supply voltage 3.3V (VDD3V3)	1,37	2.2	2.9	V
V_{off}	Power-on reset thresholds Off voltage; 300mV typ. hysteresis		1.08	1.9	2.6	
Programming Conditions						
V_{PROG}	Programming voltage	Voltage applied during programming	3.3		3.6	V
$V_{ProgOff}$	Programming voltage off level	Line must be discharged to this level	0		1	V
I_{PROG}	Programming current	Current during programming			100	mA
$R_{programmed}$	Programmed fuse resistance (log 1)	10µA max. current @ 100mV	10k		∞	Ω
$R_{unprogrammed}$	Unprogrammed fuse resistance (log 0)	2mA max. current @ 100mV	50		100	Ω

Symbol	Parameter	Condition	Min	Typ	Max	Units
DC Characteristics CMOS Schmitt-Trigger Inputs: CLK, CSn (CSn = Internal Pull-Up)						
V_{IH}	High level input voltage	Normal operation	0.7 * VDD5V			V
V_{IL}	Low level input voltage				0.3 * VDD5V	V
V_{Ion}- V_{Ioff}	Schmitt trigger hysteresis		1			V
I_{LEAK}	Input leakage current	CLK only	-1		1	µA
I_{iL}	Pull-up low level input current	CSn only, VDD5V: 5.0V	-30		-100	µA
DC Characteristics CMOS / Program Input: PDIO						
V_{IH}	High level input voltage		0.7 * VDD5V		VDD5V	V
V_{PROG} (1)	High level input voltage	During programming	3.3		3.6	V
V_{IL}	Low level input voltage				0.3 * VDD5V	V
I_{IH}	High level input current	VDD5V: 5.5V	30		100	µA
DC Characteristics CMOS Output Open Drain: MagINCn, MagDECn						
I_{OZ}	Open drain leakage current				1	µA
V_{OL}	Low level output voltage				VSS + 0.4	V
I_O	Output current	VDD5V: 4.5V			4	mA
		VDD5V: 3V			2	mA
DC Characteristics CMOS Output: PWM						
V_{OH}	High level output voltage		VDD5V – 0.5			V
V_{OL}	Low level output voltage				VSS +0.4	V
I_O	Output current	VDD5V: 4.5V			4	mA
		VDD5V: 3V			2	mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
DC Characteristics CMOS Output: A, B, Index						
V_{OH}	High level output voltage		VDD5V – 0.5			V
V_{OL}	Low level output voltage				VSS +0.4	V
I_O	Output current	VDD5V: 4.5V			4	mA
		VDD5V: 3V			2	
DC Characteristics Tri-state CMOS Output: DO						
V_{OH}	High level output voltage		VDD5V – 0.5			V
V_{OL}	Low level output voltage				VSS +0.4	V
I_O	Output current	VDD5V: 4.5V			4	mA
		VDD5V: 3V			2	
I_{OZ}	Tri-state leakage current				1	µA

Note(s):

1. Either with 3.3V or 5V supply.

Magnetic Input Specification

T_{AMB} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation) VDD5V = 4.5V to 5.5V (5V operation) unless otherwise noted.

Two-pole cylindrical diametrically magnetized source:

Figure 7:
Magnetic Input Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
d_{mag}	Diameter	Recommended magnet: Ø 6mm x 2.5mm for cylindrical magnets	4	6		mm
t_{mag}	Thickness		2.5			mm
B_{pk}	Magnetic input field amplitude	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm	45		75	mT
B_{off}	Magnetic offset	Constant magnetic stray field			± 10	mT
f_{mag_abs}	Input frequency (rotational speed of magnet)	153 rpm @ 4096 positions/rev			2.54	Hz
Disp	Displacement radius	Max. offset between defined device center and magnet axis (see Figure 32)			0.25	mm
Ecc	Eccentricity	Eccentricity of magnet center to rotational axis			100	µm
	Recommended magnet material and temperature drift	NdFeB (Neodymium Iron Boron)		-0.12		%/K
		SmCo (Samarium Cobalt)		-0.035		

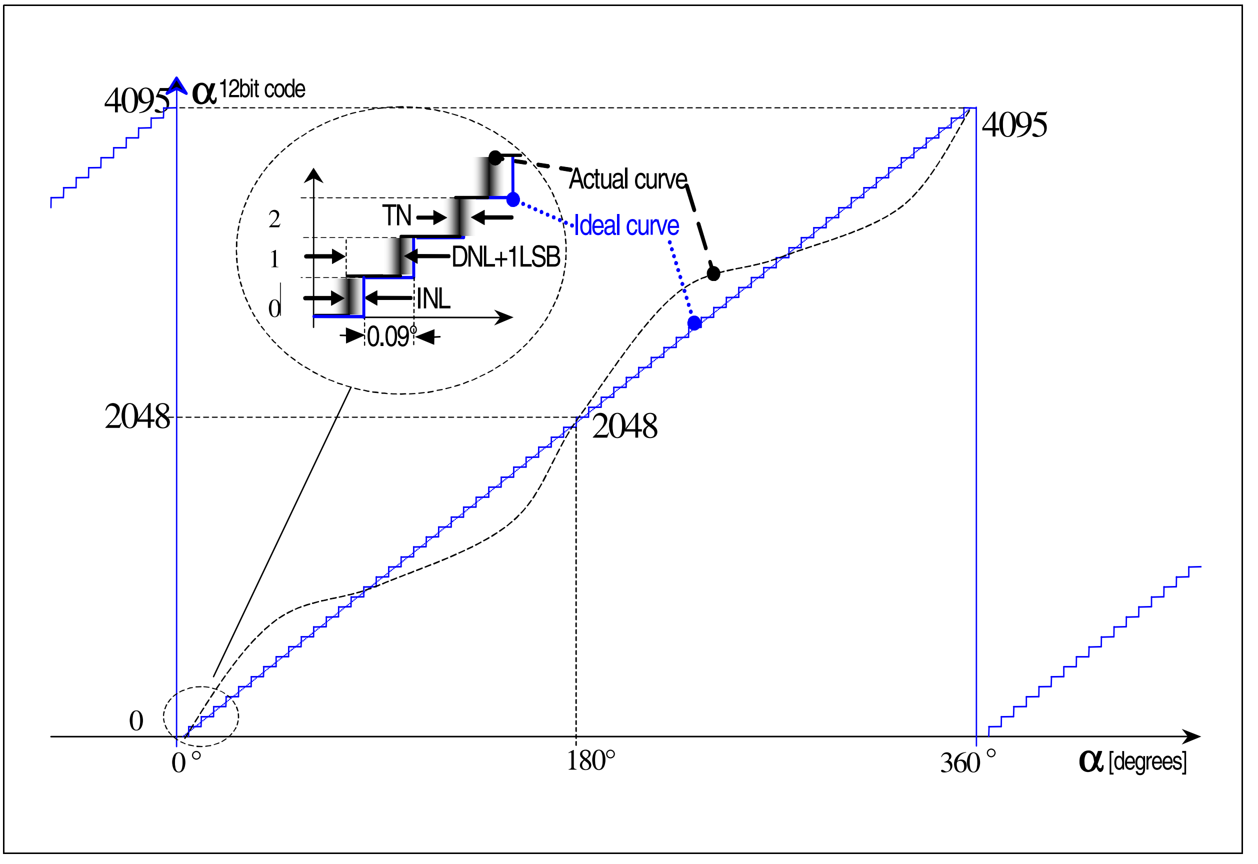
System Specifications

T_{AMB} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation)
VDD5V = 4.5V to 5.5V (5V operation) unless otherwise noted.

Figure 8:
Input Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
RES	Resolution	0.088 deg			12	bit
INL_{opt}	Integral non-linearity (optimum)	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{AMB} =25 °C.			± 0.5	deg
INL_{temp}	Integral non-linearity (optimum)	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{AMB} = -40°C to 125°C			± 0.9	deg
INL	Integral non-linearity	Best line fit = (Err_{max} – Err_{min}) / 2 Over displacement tolerance with 6mm diameter magnet, without calibration, T_{AMB} = -40°C to 125°C			± 1.4	deg
DNL	Differential non-linearity	12-bit, no missing codes			± 0.044	deg
TN	Transition noise	1 sigma			0.06	deg RMS
t_{PwrUp}	Power-up time	Until status bit OCF = 1			20	ms
t_{delay}	System propagation delay absolute output : delay of ADC, DSP and absolute interface				96	µs
$t_{delayINC}$	System propagation delay incremental output				192	µs
f_S	Internal sampling rate for absolute output		9.38	10.42	11.46	kHz
CLK/SEL	Read-out frequency	Max. clock frequency to read out serial data			1	MHz

Figure 9:
Integral and Differential Non-Linearity Example



Integral Non-Linearity (INL) is the maximum deviation between actual position and indicated position.

Differential Non-Linearity (DNL) is the maximum deviation of the step length from one position to the next.

Transition Noise (TN) is the repeatability of an indicated position.

Timing Characteristics

T_{AMB} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation) VDD5V = 4.5V to 5.5V (5V operation) unless otherwise noted.

Figure 10:
Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Synchronous Serial Interface (SSI)						
$t_{DOactive}$	Data output activated (logic high)	Time between falling edge of CSn and data output activated			100	ns
t_{CLKFE}	First data shifted to output register	Time between falling edge of CSn and first falling edge of CLK	500			ns
$T_{CLK/2}$	Start of data output	Rising edge of CLK shifts out one bit at a time	500			ns
$t_{DOvalid}$	Data output valid	Time between rising edge of CLK and data output valid			413	ns
$t_{DOtristate}$	Data output tri-state	After the last bit DO changes back to “tri-state”			100	ns
t_{CSn}	Pulse width of CSn	CSn =high; To initiate read-out of next angular position	500			ns
f_{CLK}	Read-out frequency	Clock frequency to read out serial data	>0		1	MHz
Pulse Width Modulation Output						
f_{PWM}	PWM frequency	Signal period = 4098µs ±10% at T_{AMB} = -40ºC to 125ºC	220	244	268	Hz
PW_{MIN}	Minimum pulse width	Position 0d; angle 0 degree	0.90	1	1.10	µs
PW_{MAX}	Maximum pulse width	Position 4098d; angle 359.91 degrees	3686	4096	4506	µs
Programming Conditions						
t_{PROG}	Programming time per bit	Time to prog. a single fuse bit	10		20	µs
t_{CHARGE}	Refresh time per bit	Time to charge the cap after t_{PROG}	1			µs
f_{LOAD}	LOAD frequency	Data can be loaded at n x 2µs			500	kHz
f_{READ}	READ frequency	Read the data from the latch			2.5	MHz
f_{WRITE}	WRITE frequency	Write the data to the latch			2.5	MHz

Detailed Description

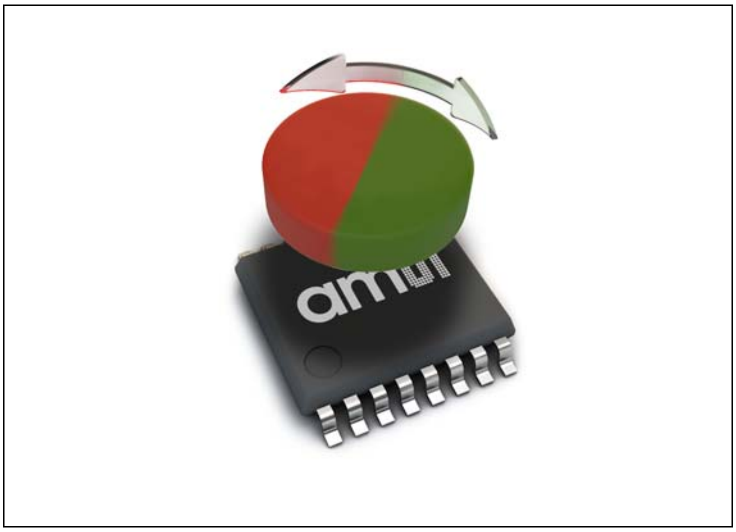
The AS5045B is manufactured in a CMOS standard process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip. The integrated Hall elements are placed around the center of the device and deliver a voltage representation of the magnetic field at the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5045B provides accurate high-resolution absolute angular position information. For this purpose a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals.

The DSP is also used to provide digital information at the outputs MagINCn and MagDECn that indicate movements of the used magnet towards or away from the device's surface. A small low cost diametrically magnetized (two-pole) standard magnet provides the angular position information (see Figure 31).

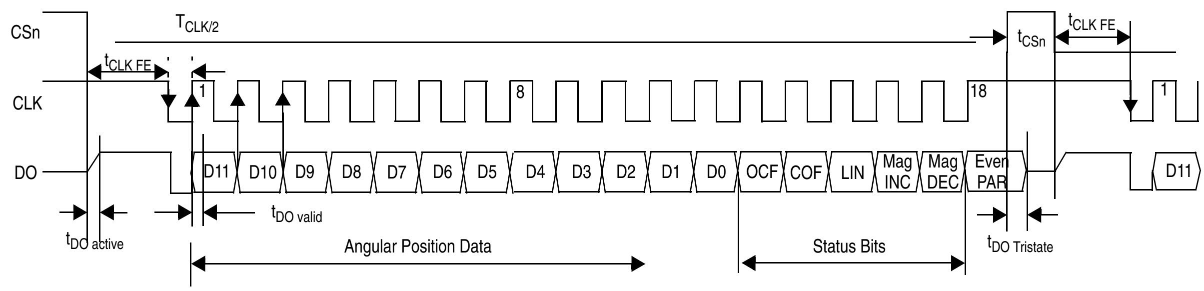
The AS5045B senses the orientation of the magnetic field and calculates a 12-bit binary code. This code can be accessed via a Synchronous Serial Interface (SSI). In addition, an absolute angular representation is given by a Pulse Width Modulated signal at pin 12 (PWM). This PWM signal output also allows the generation of a direct proportional analog voltage, by using an external Low-Pass-Filter. The AS5045B is tolerant to magnet misalignment and magnetic stray fields due to differential measurement technique and Hall sensor conditioning circuitry.

Figure 11:
Typical Arrangement of AS5045B and Magnet



Synchronous Serial Interface (SSI)

Figure 12:
Synchronous Serial Interface with Absolute Angular Position Data



If CSn changes to logic low, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out will be initiated.

- After a minimum time $t_{CLK\ FE}$, data is latched into the output shift register with the first falling edge of CLK.
- Each subsequent rising CLK edge shifts out one bit of data.
- The serial word contains 18 bits, the first 12 bits are the angular information D[11:0], the subsequent 6 bits contain system information, about the validity of data such as OCF, COF, LIN, Parity and Magnetic Field status (increase/decrease).
- A subsequent measurement is initiated by a “high” pulse at CSn with a minimum duration of t_{CSn}.

Data Content

D11:D0 absolute angular position data (MSB is clocked out first)

OCF (Offset Compensation Finished), logic high indicates the finished Offset Compensation Algorithm

COF (CORDIC Overflow), logic high indicates an out of range error in the CORDIC part. When this bit is set, the data at D11:D0 is invalid. The absolute output maintains the last valid angular value.

This alarm can be resolved by bringing the magnet within the X-Y-Z tolerance limits.

LIN (Linearity Alarm), logic high indicates that the input field generates a critical output linearity.
When this bit is set, the data at D11:D0 can still be used, but can contain invalid data. This warning can be resolved by bringing the magnet within the X-Y-Z tolerance limits.

Even Parity bit for transmission error detection of bits 1 to 17 (D11 to D0, OCF, COF, LIN, MagINC, MagDEC)

Placing the magnet above the chip, angular values increase in clockwise direction by default.

Data D11:D0 is valid, when the status bits have the following configurations:

Figure 13:
Status Bit Outputs

OCF	COF	LIN	Mag INC	Mag DEC	Parity
1	0	0	0	0	Even checksum of bits 1:15
			0	1	
			1	0	
			1	1	

Note(s):

1. MagInc=MagDec=1 is only recommended in YELLOW mode (see Figure 14).

Z-Axis Range Indication (Push Button Feature, Red/Yellow/Green Indicator). The AS5045B provides several options of detecting movement and distance of the magnet in the Z-direction. Signal indicators MagINCn and MagDECn are available both as hardware pins (pins #1 and 2) and as status bits in the serial data stream (see Figure 12).

In the default state, the status bits MagINC, MagDec and pins MagINCn, MagDECn have the following function.

Figure 14:
Magnetic Field Strength Red-Yellow-Green Indicator

Status Bits			Hardware Pins		OTP: Mag CompEn = 1 (Red-Yellow-Green)
Mac INC	Mag DEC	LIN	Mac INCn	Mag DECn	Description
0	0	0	Off	Off	No distance change Magnetic input field OK (GREEN range, ~45mT to 75mT)
1	1	0	On	Off	YELLOW range: magnetic field is ~ 25mT to 45mT or ~75mT to 135mT. The AS5045B can still be operated in this range, but with slightly reduced accuracy.
1	1	1	On	On	RED range: magnetic field is ~<25mT or >~135mT. It is still possible to operate the AS5045B in the red range, but not recommended.
All other combinations			n/a	n/a	Not available

Note(s):

1. Pin 1 (MagINCn) and pin 2 (MagDECn) are active low via open drain output and require an external pull-up resistor. If the magnetic field is in range, both outputs are turned off.

The two pins can also be combined with a single pull-up resistor. In this case, the signal is high when the magnetic field is in range. It is low in all other cases (see Figure 14).

Incremental Mode

The AS5045B has an internal interpolator block. This function is used if the input magnetic field is to fast and a code position is missing. In this case an interpolation is done.

With the OTP bits OutputMd0 and OutputMd1 a specific mode can be selected. For the available pre-programmed incremental versions (10-bit and 12-bit), these bits are set during test at ams. These settings are permanent and can not be recovered.

A change of the incremental mode (WRITE command) during operation could cause problems. A power-on-reset in between is recommended.

Figure 15:
Incremental Mode_Table

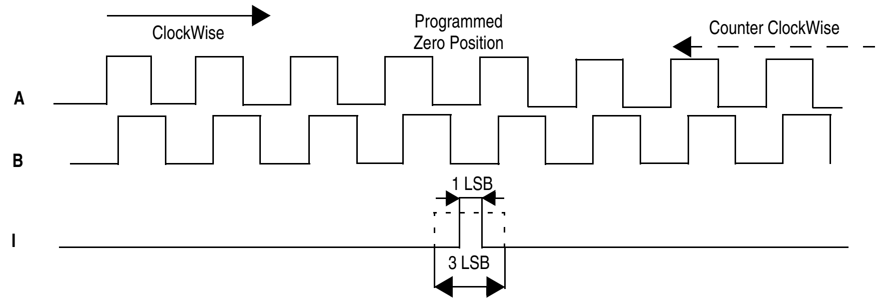
<table>
<tr><th>Mode</th><th>Description</th><th>Output Md1</th><th>Output Md0</th><th>Resolution</th><th>Dtest1_A and DTest2_B Pulses</th><th>Index Width</th></tr>
<tr><td>Default mode</td><td>AS5145 function DTEST1_A and DTEST2_B are not used. The Mode_Index pin is used for selection of the decimation rate (low speed/high speed).</td><td>0</td><td>0</td><td></td><td></td><td></td></tr>
<tr><td>10-bit Incremental mode (low DNL)</td><td rowspan="2">DTEST1_A and DTEST2_B are used as A and B signal. In this mode the Mode_Index Pin is switched from input to output and will be the Index Pin. The decimation rate is set to 64 (fast mode) and cannot be changed from external.</td><td>0</td><td>1</td><td>10</td><td>256</td><td rowspan="2">1/3 LSB</td></tr>
<tr><td>12-bit Incremental mode (high DNL)</td><td>1</td><td>0</td><td>12</td><td>1024</td></tr>
<tr><td>Sync mode</td><td>In this mode a control signal is switched to DTEST1_A and DTEST2_B.</td><td>1</td><td>1</td><td></td><td></td><td></td></tr>
</table>

Incremental Power-Up Lock Option

After power-up, the incremental outputs can optionally be locked or unlocked, depending on the status of the CSn pin:

- CSn = low at power-up: CSn has an internal pull-up resistor and must be externally pulled low ($R_{ext} \leq 5k\Omega$). If Csn is low at power-up, the incremental outputs (A, B, Index) will be high until the internal offset compensation is finished. This unique state (A=B=Index = high) can be used as an indicator for the external controller to shorten the waiting time at power-up. Instead of waiting for the specified maximum power up-time (0), the controller can start requesting data from the AS5045B as soon as the state (A=B=Index = high) is cleared.
- CSn = high or open at power-up: In this mode, the incremental outputs (A, B, Index) will remain at logic high state, until CSn goes low or a low pulse is applied at CSn. This mode allows intentional disabling of the incremental outputs until, for example the system microcontroller is ready to receive data.

Figure 16:
Incremental Output



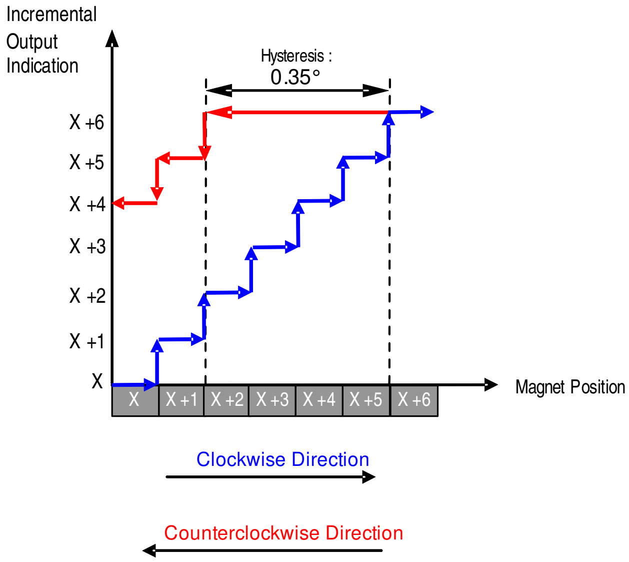
The hysteresis trimming is done at the final test (factory trimming) and set to 4 LSB, related to a 12-bit number.

Incremental Output Hysteresis

To avoid flickering incremental outputs at a stationary magnet position, a hysteresis is introduced. In case of a rotational direction change, the incremental outputs have a hysteresis of 4 LSB. Regardless of the programmed incremental resolution, the hysteresis of 4 LSB always corresponds to the highest resolution of 12-bit. In absolute terms, the hysteresis is set to 0.35 degrees for all resolutions. For constant rotational directions, every magnet position change is indicated at the incremental outputs (see Figure 17). For example, if the magnet turns clockwise from position "x+3" to "x+4", the incremental output would also indicate this position accordingly.

A change of the magnet's rotational direction back to position "x+3" means that the incremental output still remains unchanged for the duration of 4 LSB, until position "x+2"is reached. Following this direction, the incremental outputs will again be updated with every change of the magnet position.

Figure 17:
Hysteresis Window for Incremental Outputs



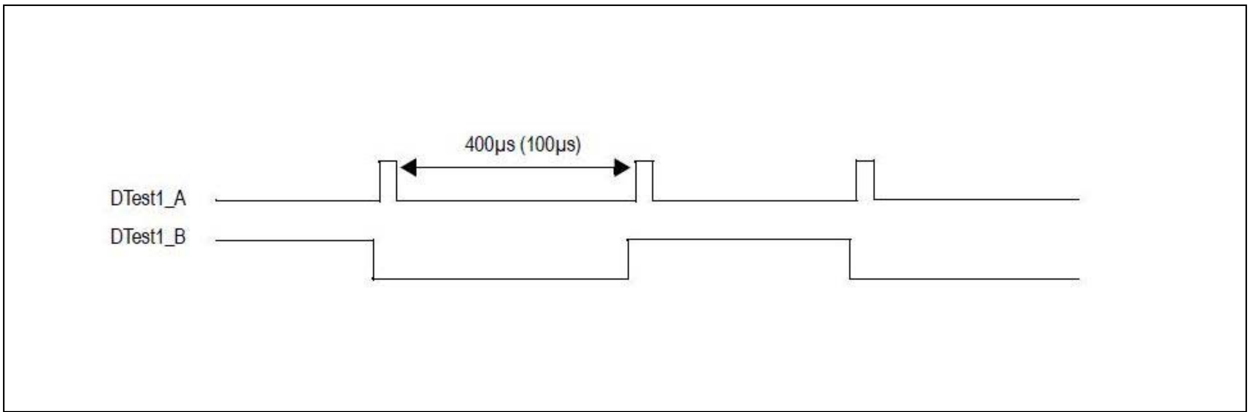
Incremental Output Validity

During power on the incremental output is kept stable high until the offset compensation is finished and the CSn is low (internal Pull Up) the first time. In quadrature mode A = B = Index = high indicates an invalid output. If the interpolator recognizes a difference larger than 128 steps between two samples it holds the last valid state. The interpolator synchronizes up again with the next valid difference. This avoids undefined output burst, e.g. if no magnet is present.

Sync Mode

This mode is used to synchronize the external electronic with the AS5045B. In this mode two signals are provided at the pins DTEST1_A and DTEST2_B. By setting Bit 48 in the OTP register, the Sync Mode will be activated.

Figure 18:
Dtest1_A and DTest2_B



Every rising edge at DTEST1_A indicates that new data in the device is available. With this signal it is possible to trigger an external customer Microcontroller (interrupt) and start the SSI readout. DTEST2_B indicates the phase of available data.

Sine/Cosine Mode

This mode can be enabled by setting the OTP Factory-bit FS2. If this mode is activated the 16 bit sine and 16 bit cosine digital data of both channels will be switched out. Due to the high resolution of 16 bits of the data stream an accurate calculation can be done externally. In this mode the open drain outputs of DTEST1_A and DTEST2_B are switched to push-pull mode. At pin MagDECn the clock impulse, at pin MagINCn the Enable pulse will be switched out. The pin PWM indicates, which phase of signal is being presented. The mode is not available in the default mode.

Daisy Chain Mode

The daisy chain mode allows connection of several AS5045Bs in series, while still keeping just one digital input for data transfer (see "Data IN" in Figure 19). This mode is accomplished by connecting the data output (DO; pin 9) to the data input (PDIO; pin 8) of the subsequent device. The serial data of all connected devices is read from the DO pin of the first device in the chain. The length of the serial bit stream increases with every connected device, it is n * (18+1) bits: n= number of devices. e.g. 38 bit for two devices, 57 bit for three devices, etc.

The last data bit of the first device (Parity) is followed by a dummy bit and the first data bit of the second device (D11), etc. (see Figure 20).

Figure 19:
Daisy Chain Hardware Configuration

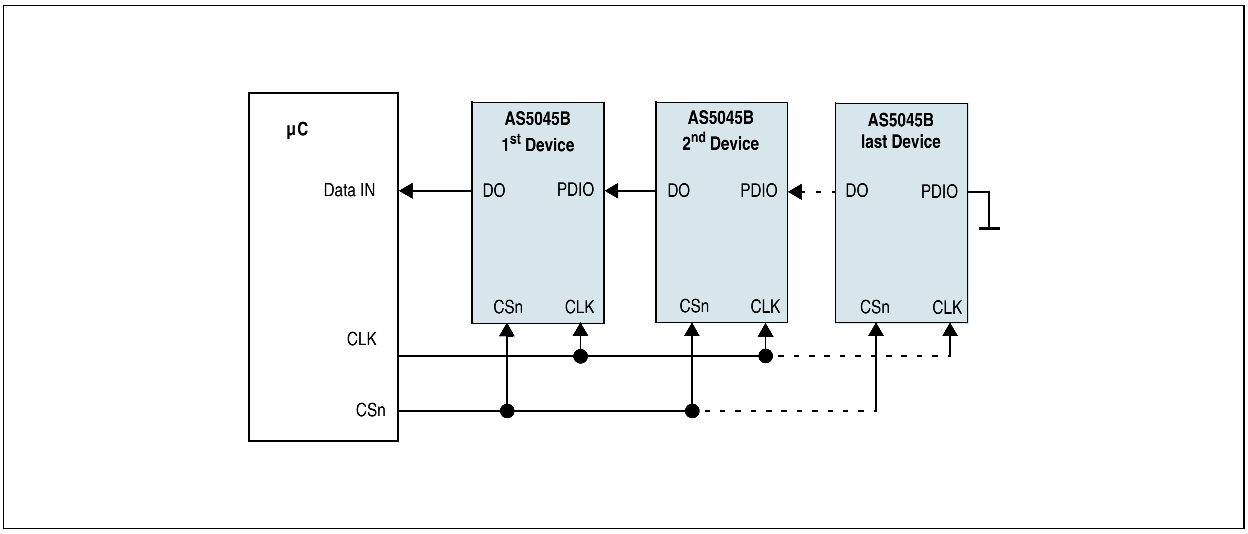
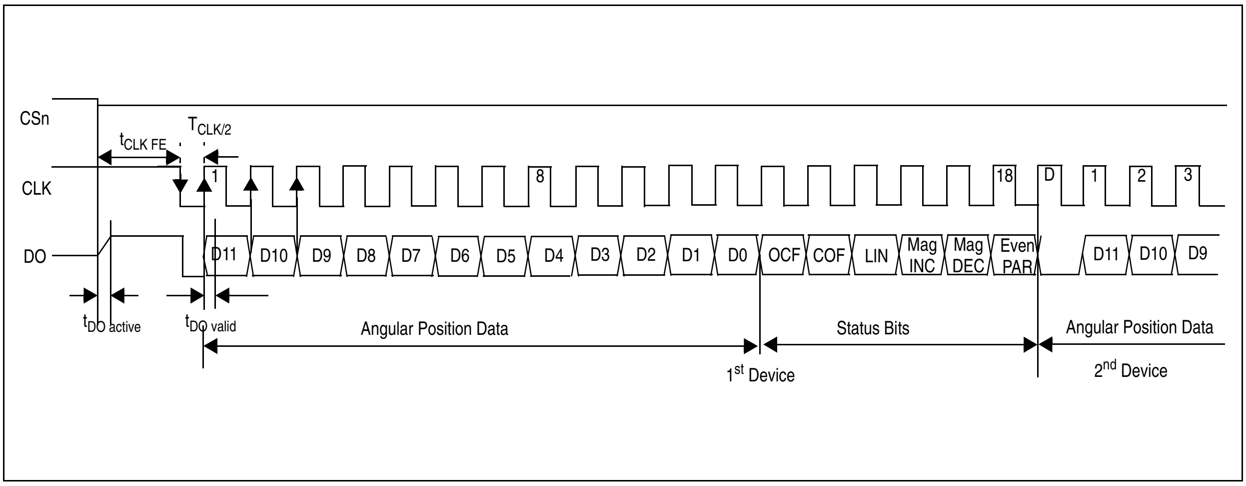


Figure 20:
Daisy Chain Mode Data Transfer



Pulse Width Modulation (PWM) Output

The AS5045B provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle. For angle position 0 to 4094

(EQ1) $$Position = \frac{t_{on} \cdot 4098}{(t_{on} + t_{off})} - 1$$

Examples:

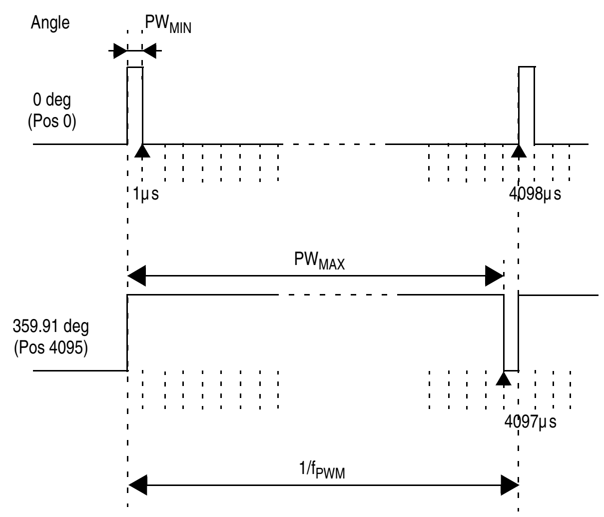
1. An angle position of 180° will generate a pulse width ton = 2049µs and a pause toff of 2049 µs resulting in Position = 2048 after the calculation:
   2049 * 4098 / (2049 + 2049) -1 = 2048
2. An angle position of 359.8° will generate a pulse width ton = 4095µs and a pause toff of 3 µs resulting in Position = 4094 after the calculation:
   4095 * 4098 / (4095 + 3) -1 = 4094

Exception:

1. An angle position of 359.9° will generate a pulse width ton = 4097µs and a pause toff of 1 µs resulting in Position = 4096 after the calculation:
   4097 * 4098 / (4097 + 1) -1 = 4096

The PWM frequency is internally trimmed to an accuracy of ±5% (±10% over full temperature range). This tolerance can be cancelled by measuring the complete duty cycle as shown above.

Figure 21:
PWM Output Signal



Changing the PWM Frequency

The PWM frequency of the AS5045B can be divided by two by setting a bit (PWMhalfEN) in the OTP register (see Programming the AS5045B). With PWMhalfEN = 0 the PWM timing is as shown in Figure 22.

Figure 22:
PWM Signal Parameters (Default Mode)

Symbol	Parameter	Typ	Unit	Note
f_{PWM}	PWM frequency	244	Hz	Signal period: 4097µs
PW_{MIN}	MIN pulse width	1	µs	• Position 0d • Angle 0 deg
PW_{MAX}	MAX pulse width	4097	µs	• Position 4095d • Angle 359.91 deg

When PWMhalfEN = 1, the PWM timing is as shown in Figure 23.

Figure 23:
PWM Signal Parameters with Half Frequency (OTP Option)

Symbol	Parameter	Typ	Unit	Note
f_{PWM}	PWM frequency	122	Hz	Signal period: 8194µs
PW_{MIN}	MIN pulse width	2	µs	• Position 0d • Angle 0 deg
PW_{MAX}	MAX pulse width	8194	µs	• Position 4095d • Angle 359.91 deg

Analog Output

An analog output can be generated by averaging the PWM signal, using an external active or passive low pass filter. The analog output voltage is proportional to the angle: 0°= 0V; 360° = VDD5V.

Using this method, the AS5045B can be used as direct replacement of potentiometers.

Figure 24:
Simple 2nd Order Passive RC Low Pass Filter

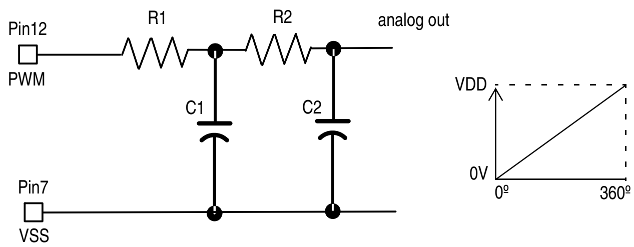


Figure 21 shows an example of a simple passive low pass filter to generate the analog output.

(EQ2) $R1, R2 \geq 10k\Omega \qquad C1, C2 \geq 2.2\mu F / 6V$

R1 should be greater than or equal to 4k7 to avoid loading of the PWM output. Larger values of Rx and Cx will provide better filtering and less ripple, but will also slow down the response time.

Application Information

The benefits of AS5045B are as follows:

- Complete system-on-chip
- Flexible system solution provides absolute and PWM outputs simultaneously
- Ideal for applications in harsh environments due to contactless position sensing
- No calibration required
- No temperature compensation necessary

Programming the AS5045B

After power-on, programming the AS5045B is enabled with the rising edge of CSn with PDIO = high and CLK = low.

The AS5045B programming is a one-time-programming (OTP) method, based on poly silicon fuses. The advantage of this method is that a programming voltage of only 3.3V to 3.6V is required for programming (either with 3.3V or 5V supply).

The OTP consists of 52 bits, of which 21 bits are available for user programming. The remaining 31 bits contain factory settings and a unique chip identifier (Chip-ID).

A single OTP cell can be programmed only once. Per default, the cell is “0”; a programmed cell will contain a “1”. While it is not possible to reset a programmed bit from “1” to “0”, multiple OTP writes are possible, as long as only unprogrammed “0”-bits are programmed to “1”.

Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command at any time. This setting will be cleared and overwritten with the hard programmed OTP settings at each power-up sequence or by a LOAD operation. Use **application note AN514X_10** to get more information about the programming options.

The OTP memory can be accessed in the following ways:

- **Load Operation:** The Load operation reads the OTP fuses and loads the contents into the OTP register. A Load operation is automatically executed after each power-on-reset.
- **Write Operation:** The Write operation allows a temporary modification of the OTP register. It does not program the OTP. This operation can be invoked multiple times and will remain set while the chip is supplied with power and while the OTP register is not modified with another Write or Load operation.