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AS5047P

14-Bit On-Axis Magnetic Rotary Position Sensor with 12-Bit Decimal and Binary Incremental Pulse Count for 28krpm High Speed Capability

General Description

The AS5047P is a high-resolution rotary position sensor for high speed (up to 28krpm) angle measurement over a full 360 degree range. This new position sensor is equipped with revolutionary integrated dynamic angle error compensation (DAEC™) with almost 0 latency and offers a robust design that suppresses the influence of any homogenous external stray magnetic field.

A standard 4-wire SPI serial interface allows a host microcontroller to read 14-bit absolute angle position data from the AS5047P and to program non-volatile settings without a dedicated programmer.

Incremental movements are indicated on a set of ABI signals with a maximum resolution of 4000 steps /1000 pulses per revolution in decimal mode and 4096 steps /1024 pulses per revolution in binary mode. The resolution of the ABI signal is programmable and can be reduced to 100 steps per revolution, or 25 pulses per revolution.

Brushless DC (BLDC) motors are controlled through a standard UVW commutation interface with a programmable number of pole pairs from 1 to 7. The absolute angle position is also provided as PWM-encoded output signal.

The AS5047P is available as a single die in a compact 14-pin TSSOP package.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5047P, 14-Bit On-Axis Magnetic Rotary Position Sensor with 12-Bit Decimal and Binary Incremental Pulse Count for 28krpm High Speed Capability are listed below:

Figure 1:
Added Value of Using the AS5047P

Benefits	Features
• High speed application	• Up to 28krpm
• Easy to use – saving costs on DSP	• DAEC™ Dynamic angle error compensation
• Good resolution for motor and position control	• 14-bit core resolution

Benefits	Features
• Simple optical encoder replacement	• ABI programmable decimal and binary pulse-count: 1000,500,400,300,200,100, 50,25,1024,512,256 ppr
• No programmer needed (via SPI command)	• Zero position, configuration programmable
• Versatile choice of the interface	• Independent output interfaces: SPI, ABI, UVW, PWM
• Lower system costs (no shielding)	• Immune to external stray field

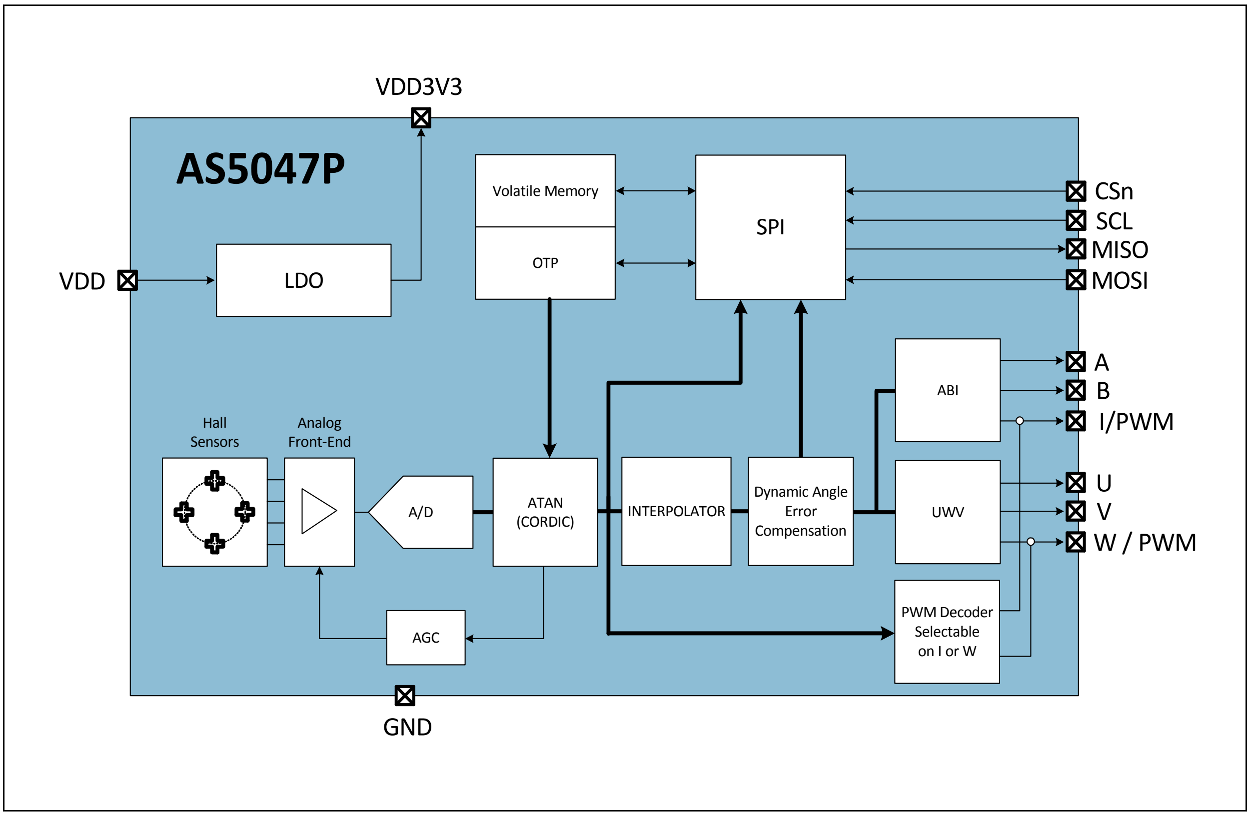
Applications

The AS5047P is ideally suited to support BLDC motor commutation for the most challenging industrial applications such as factory automation, building automation, robotics, PMSM (permanent magnet synchronous motor) and stepper motors closed loop regulation, as well as optical encoder replacement.

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS5047P Block Diagram



Pin Assignment

Figure 3:
TSSOP-14 Pin Assignment

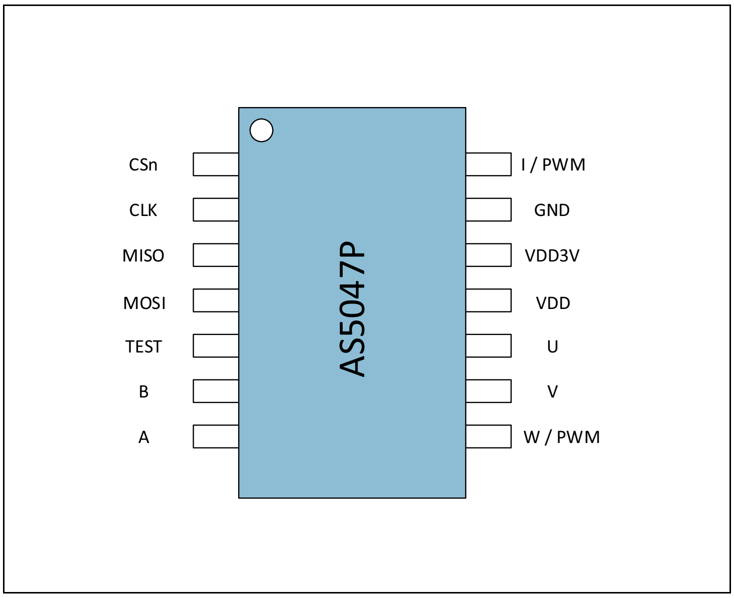


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	CSn	Digital input	SPI chip select (active low)
2	CLK	Digital input	SPI clock
3	MISO	Digital output	SPI master data input, slave output
4	MOSI	Digital input	SPI master data output, slave input
5	Test		Test pin (connect to ground)
6	B	Digital output	Incremental signal B
7	A	Digital output	Incremental signal A

Pin Number	Pin Name	Pin Type	Description
8	W/PWM	Digital output	Commutation signal W or PWM
9	V	Digital output	Commutation signal V
10	U	Digital output	Commutation signal U
11	VDD	Power supply	5V power supply voltage for on-chip regulator
12	VDD3V3	Power supply	3.3V on-chip low-dropout (LDO) output. Requires an external decoupling capacitor (1uF)
13	GND	Power supply	Ground
14	I	Digital output	Incremental signal I (index) or PWM

Note(s) and/or Footnote(s):

1. Floating state of a digital input is not allowed.
2. If SPI is not used, a Pull up resistor on CSn is required.
3. If SPI is not used, a Pull down resistor on CLK and MOSI is required.
4. If SPI is not used, the pins MISO can be left open.
5. If ABI, UVW or PWM is not used, the pins can be left open.

Absolute Maximum Ratings

Stresses beyond those listed parameters under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Parameters regarding normal operation of the sensor are listed in section Electrical Characteristics.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
VDD5	DC supply voltage at VDD pin	-0.3	7.0	V	
VDD3	DC supply voltage at VDD3V3 pin	-0.3	5.0	V	
V_{SS}	DC supply voltage at GND pin	-0.3	0.3	V	
V_{in}	Input pin voltage		VDD+0.3	V	
I_{scr}	Input current (latch-up immunity)	-100	100	mA	AEC-Q100-004
ESD	Electrostatic discharge	±2		kV	AEC-Q100-002
P_t	Total power dissipation (all supplies and outputs)		150	mW	
Ta5V0	Ambient temperature 5V0	-40	125	°C	In the 5.0V power supply mode only
Ta3V3	Ambient temperature 3V3	-40	125	°C	In the 3.3V power supply mode if NOISESET = 0
TaProg	Programming temperature	5	45	°C	Programming @ room temperature (25°C ± 20°C)
T_{strg}	Storage temperature	-55	150	°C	
T_{body}	Package body temperature		260	°C	IPC/JEDEC J-STD-020
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	3			Represents a maximum floor lifetime of 168h

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD	Positive supply voltage	5.0V operation mode	4.5	5.0	5.5	V
VDD3V3	Positive supply voltage	3.3V operation mode; only from -40 to 125°C	3.0	3.3	3.6	V
VDD_Burn	Positive supply voltage	Supply voltage required for programming in 3.3V operation	3.3		3.5	V
V_{REG}	Regulated Voltage	Voltage at VDD3V3 pin if VDD ≠ VDD3V3	3.2	3.4	3.6	V
I_{DD}	Supply current				15	mA
V_{IH}	High-level input voltage		0.7×VDD			V
V_{IL}	Low-level input voltage				0.3×VDD	V
V_{OH}	High-level output voltage		VDD-0.5			V
V_{OL}	Low-level output voltage				V_{SS}+0.4	V
I_Out	Current on digital output (ABI, UVW)				1	mA
I_Out_MISO	Current on digital output MISO				4	mA
C_L	Capacitive load on digital output				50	pf

Magnetic Characteristics

Figure 7:
Magnetic Specifications

Symbol	Parameter	Conditions	Min	Max	Unit
Bz	Orthogonal magnetic field strength, normal operating mode	Required orthogonal component of the magnetic field strength measured at the die's surface along a circle of 1.1mm	35	70	mT

Note(s) and/or Footnote(s):

1. it is possible to operate the AS5047P below 35mT with reduced noise performance.

System Characteristics

Figure 8:
System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Core resolution			14		bit
RES_ABI	Resolution of the ABI interface	Programmable with register setting (ABIRES)	100		4096	Steps per revolution
INL_{OPT} @ 25°C	Non-linearity, optimum placement of the magnet				±0.8	degree
$INL_{OPT+TEMP}$	Non-linearity optimum placement of the magnet over the full Temperature Range				±1	degree
$INL_{DIS+TEMP}$	Non-linearity @ displacement of magnet and temperature -40°C to 150°C	Assuming N35H Magnet (D=8mm, H=3mm) 500µm displacement in x and y z-distance @ 2000µm			±1.2	degree
ONL	RMS output noise (1 sigma). Not tested, guaranteed by design.	Orthogonal component for the magnetic field within the specified range (Bz), NOISESET = 0			0.068	degree
ON_PWM	RMS output noise (1 sigma) on PWM interface	Orthogonal component for the magnetic field within the specified range (Bz)			0.068	degree
t_{delay}	System propagation delay –core	Reading angle via SPI	90		110	µs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{delay_DAEC}	System propagation delay after dynamic angle error correction.	At ABI and UVW interfaces	1.5		1.9	µs
t_{sampl}	Sampling rate	Refresh rate at SPI	202	222	247	ns
DAE_{1700}	Dynamic angle error	At 1700 RPM constant speed			0.02	degree
DAE_{max}	Dynamic angle error	At 14500 RPM constant speed			0.18	degree
DAE_{acc}	Dynamic angle error at constant acceleration (25krad/s^2)	25k radians/s^2 constant acceleration			0.175	degree
MS	Maximum speed				28000	RPM

Reference magnet: N35H, 8mm diameter; 3mm thickness.

Timing Characteristics

Figure 9:
Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pon}	Power-on time	Time frame between VDD > VDDmin and first valid angular value. Not tested, guaranteed by design			10	ms

Detailed Description

The AS5047P is a Hall-effect magnetic sensor using a CMOS lateral technology. The lateral Hall sensors convert the magnetic field component perpendicular to the surface of the chip into a voltage.

The signals from the Hall sensors are amplified and filtered by the analog front-end (AFE) before being converted by the analog-to-digital converter (ADC). The output of the ADC is processed by the hardwired CORDIC (coordinate rotating digital computer) block to compute the angle and magnitude of the magnetic vector. The intensity of the magnetic field (magnitude) is used by the automatic gain control (AGC) to adjust the amplification level for compensation of the temperature and magnetic field variations.

The internal 14-bit resolution is available by readout register via the SPI interface. The resolution on the ABI output can be programmed from 4096 to 100 steps per revolution.

The Dynamic Angle Error Compensation block corrects the calculated angle regarding latency, by using a linear prediction calculation algorithm. At constant rotation speed the latency time is internally compensated by the AS5047P, reducing the dynamic angle error at the SPI, ABI and UVW outputs. The AS5047P allows to switch OFF the UVW output interface to display the absolute angle as PWM-encoded signal on the pin W.

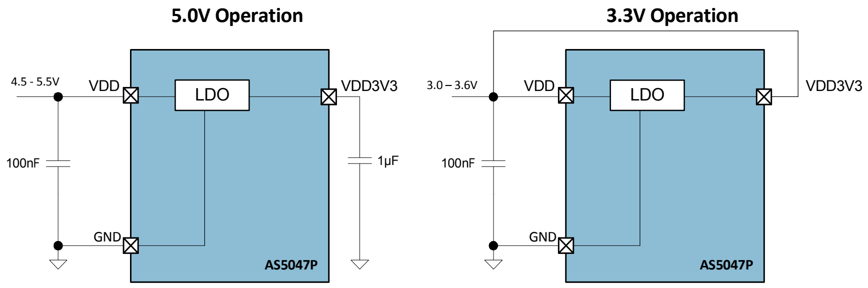
At higher speeds, the interpolator fills in missing ABI pulses and generates the UVW signals with no loss of resolution. The non-volatile settings in the AS5047P can be programmed through the SPI interface without any dedicated programmer. The AS5047P is built for high speed application up to 28krpm.

Power Management

The AS5047P can be either powered from a 5.0V supply using the on-chip low-dropout regulator or from a 3.3V voltage supply. The LDO regulator is not intended to power any other loads, and it needs a 1 µF capacitor to ground located close to the chip for decoupling as shown in Figure 10.

In 3.3V operation, VDD and VREG must be tied together.

Figure 10:
5.0V and 3.3V Power Supply Options



After applying power to the chip, the power-on time (t_{pon}) must elapse before the AS5047P provides the first valid data.

Dynamic Angle Error Compensation

The AS5047P uses 4 integrated Hall sensors which produce a voltage proportional to the orthogonal component of the magnetic field to the die. These voltage signals are amplified, filtered, and converted into the digital domain to allow the CORDIC digital block to calculate the angle of the magnetic vector. The propagation of these signals through the analog front-end and digital back-end generates a fixed delay between the time of measurement and the availability of the measured angle at the outputs. This latency generates a dynamic angle error represented by the product of the angular speed (ω)and the system propagation delay (t_{delay}):

$$DAE = \omega \times t_{delay}$$

The dynamic angle compensation block calculates the current magnet rotation speed (ω) and multiplies it with the system propagation delay (t_{delay}) to determine the correction angle to reduce this error. At constant speed, the residual system propagation delay is t_{delay_DAEC}.

The angle represented on the PWM interface is not compensated by the Dynamic Angle Error Compensation algorithm. It is also possible to disable the Dynamic Angle Error Compensation with the setting DAECDIS. Disabling the Dynamic Angle Error Compensation gives a noise benefit of 0.016 degree rms.This setting can be advantageous for low speed (under 100rpm) respectively static positioning applications.

SPI Interface (slave)

The SPI interface is used by a host microcontroller (master) to read or write the volatile memory as well as to program the non-volatile OTP registers. The AS5047P SPI only supports slave operation mode. It communicates at clock rates up to 10 MHz.

The AS5047P SPI uses mode=1 (CPOL=0, CPHA=1) to exchange data. As shown in Figure 11, a data transfer starts with the falling edge of CSn (SCL is low). The AS5047P samples MOSI data on the falling edge of SCL. SPI commands are executed at the end of the frame (rising edge of CSn). The bit order is MSB first. Data is protected by parity.

SPI Timing

The AS5047P SPI timing is shown in Figure 11.

Figure 11:
SPI Timing Diagram

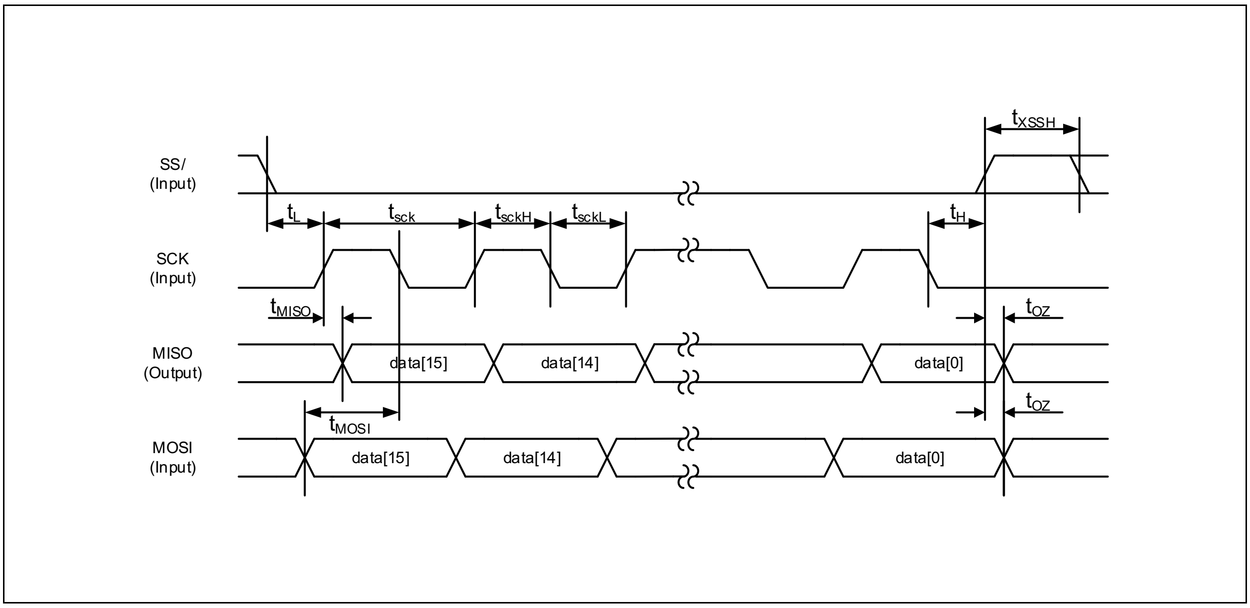


Figure 12:
SPI Timing

Parameter	Description	Min	Max	Units
t_L	Time between CSn falling edge and CLK rising edge	350		ns
t_{clk}	Serial clock period	100		ns
t_{clkL}	Low period of serial clock	50		ns
t_{clkH}	High period of serial clock	50		ns
t_H	Time between last falling edge of CLK and rising edge of CSn	tclk / 2		ns
t_{CSn}	High time of CSn between two transmissions	350		ns
t_{MOSI}	Data input valid to falling clock edge	20		ns
t_{MISO}	CLK edge to data output valid		51	ns
t_{OZ}	Release bus time after CS rising edge.		10	ns

SPI Transaction

An SPI transaction consists of a 16-bit command frame followed by a 16-bit data frame. Figure 13 shows the structure of the command frame.

Figure 13:
SPI Command Frame

Bit	Name	Description
15	PARC	Parity bit (even) calculated on the lower 15 bits of command frame
14	R/W	0: Write 1: Read
13:0	ADDR	Address to read or write

To increase the reliability of communication over the SPI, an even parity bit PARC must be generated and sent. A wrong setting of the parity bit causes an parity bit error which is shown the PARERR bit in the error flag register. The parity bit is calculated from the lower 15 bits of the command frame. The 16-bit command consists of a register address and read/write bit which indicates if the transaction is a read or write and the parity bit.

Figure 14 shows the read data frame.

Figure 14:
SPI Read Data Frame

Bit	Name	Description
15	PARD	Parity bit (even) calculated on the lower 15 bits
14	EF	0: No command frame error occurred 1: Error occurred
13:0	DATA	Data

The parity bit PARD is calculated by the AS5047D of the lower 15 bits of data frame. If an error occurred in the previous SPI command frame, the EF bit is set high. The SPI read is sampled on the rising edge of CSn and the data is transmitted on MISO with the next read command, as shown in Figure 15.

Figure 15:
SPI Read

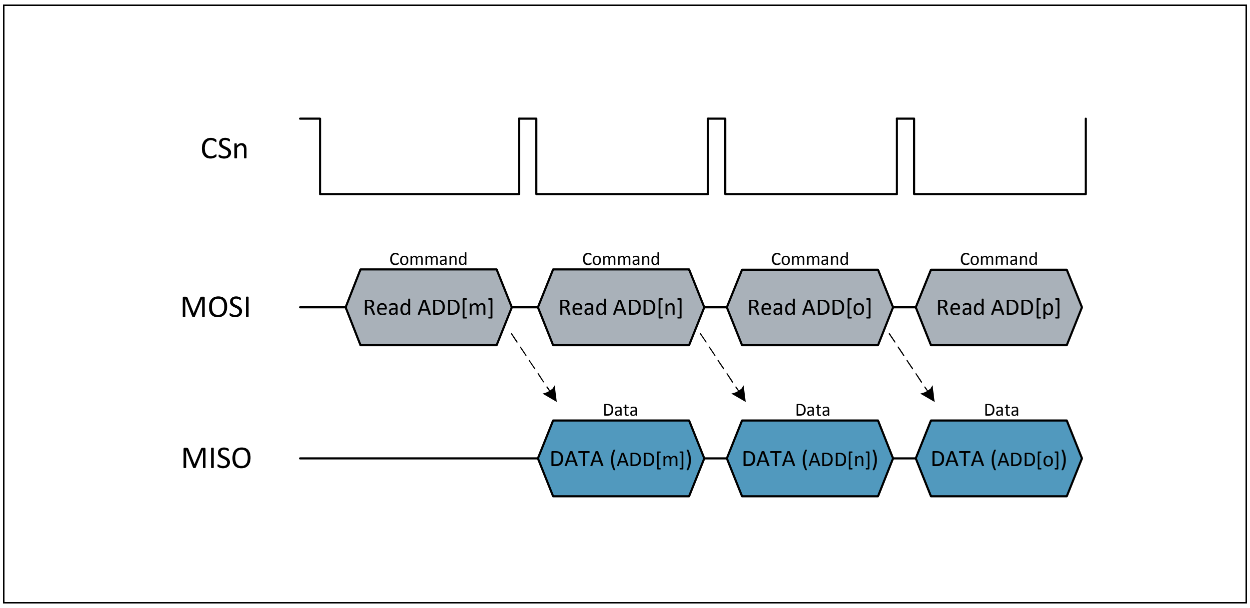


Figure 16:
SPI Write Data Frame

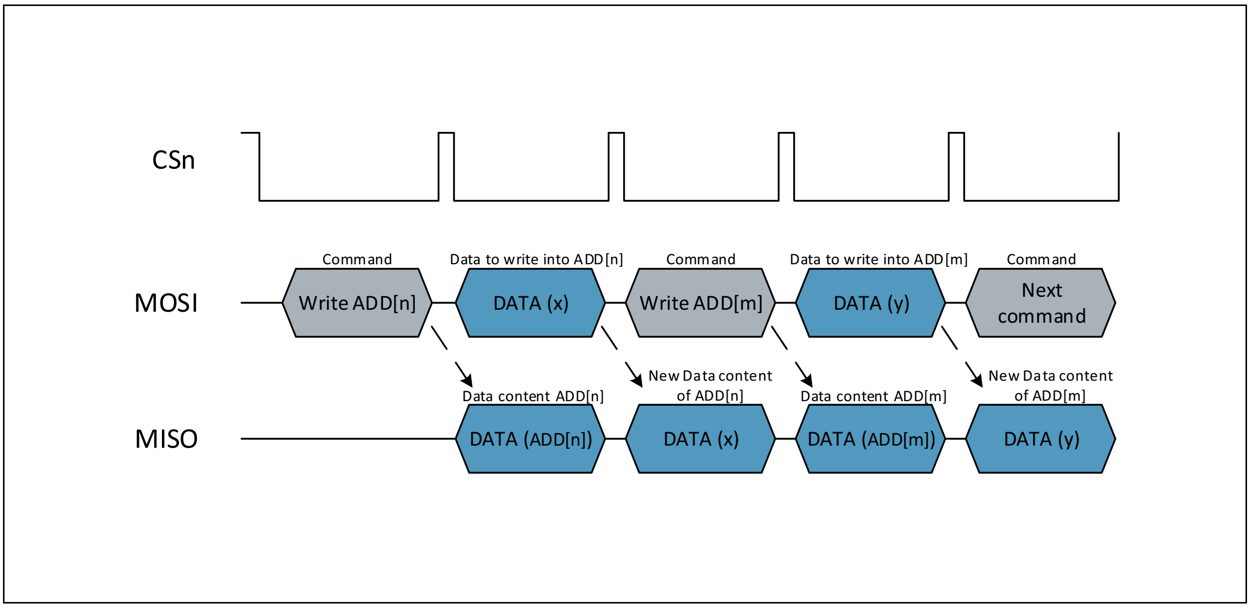
Bit	Name	Description
15	PARD	Parity bit (even)
14	0	Always low
13:0	DATA	Data

The parity bit PARD must be calculated from the 16-bit data.

In an SPI write transaction, the write command frame is followed by a write data frame at MOSI. The write data frame consists of the new content of register which address is in the command frame.

During the new content is transmitted on MOSI by the write data frame, the old content is send on MISO. At the next command on MOSI the actual content of the register is transmitted on MISO, as shown in Figure 17.

Figure 17:
SPI Write Transaction



Volatile Registers

The volatile registers are shown in Figure 18. Each register has a 14-bit address.

Figure 18:
Volatile Register Table

Address	Name	Default	Description
0x0000	NOP	0x0000	No operation
0x0001	ERRFL	0x0000	Error register
0x0003	PROG	0x0000	Programming register
0x3FFC	DIAAGC	0x0180	Diagnostic and AGC
0x3FFD	MAG	0x0000	CORDIC magnitude
0x3FFE	ANGLEUNC	0x0000	Measured angle without dynamic angle error compensation
0x3FFF	ANGLECOM	0x0000	Measured angle with dynamic angle error compensation

Reading the NOP register is equivalent to a nop (no operation) instruction for the AS5047P.

Figure 19:
ERRFL (0x0001)

Name	Read/Write	Bit Position	Description
PARERR	R	2	Parity error
INVCOMM	R	1	Invalid command error: set to 1 by reading or writing an invalid register address
FRERR	R	0	Framing error: is set to 1 when a non-compliant SPI frame is detected

Reading the ERRFL register automatically clears its contents (ERRFL=0x0000).

Figure 20:
PROG (0x0003)

Name	Read/Write	Bit Position	Description
PROGVER	R/W	6	Program verify: must be set to 1 for verifying the correctness of the OTP programming
PROGOTP	R/W	3	Start OTP programming cycle
OTPREF	R/W	2	Refreshes the non-volatile memory content with the OTP programmed content
PROGEN	R/W	0	Program OTP enable: enables programming the entire OTP memory

The PROG register is used for programming the OTP memory. (See programming the zero position.)

Figure 21:
DIAAGC (0x3FFC)

Name	Read/Write	Bit Position	Description
MAGL	R	11	Diagnostics: Magnetic field strength too low; AGC=0xFF
MAGH	R	10	Diagnostics: Magnetic field strength too high; AGC=0x00
COF	R	9	Diagnostics: CORDIC overflow
LF	R	8	Diagnostics: Offset compensation LF=0:internal offset loops not ready regulated LF=1:internal offset loop finished
AGC	R	7:0	Automatic gain control value

Figure 22:
MAG (0x3FFD)

Name	Read/Write	Bit Position	Description
CMAG	R	13:0	CORDIC magnitude information

Figure 23:
ANGLE (0x3FFE)

Name	Read/Write	Bit Position	Description
CORDICANG	R	13:0	Angle information without dynamic angle error compensation

Figure 24:
ANGLECOM (0x3FFF)

Name	Read/Write	Bit Position	Description
DAECANG	R	13:0	Angle information with dynamic angle error compensation

Non-Volatile Registers (OTP)

The OTP (One-Time Programmable) memory is used to store the absolute zero position of the sensor and the customer settings permanently in the sensor IC.

SPI write/read access is possible several times for all non-volatile registers (soft write). Soft written register content will be lost after a hardware reset.

The programming itself can be done just once. Therefore the content of the non-volatile registers is stored permanently in the sensor. The register content is still present after a hardware reset and cannot be overwritten.

For a correct function of the sensor the OTP programming is not required. If no configuration or programming is done, the non-volatile registers are in default state 0x0000h..

Figure 25:
Non-Volatile Register Table

Address	Name	Default	Description
0x0016	ZPOSM	0x0000	Zero position MSB
0x0017	ZPOSL	0x0000	Zero position LSB /MAG diagnostic
0x0018	SETTINGS1	0x0001	Custom setting register 1
0x0019	SETTINGS2	0x0000	Custom setting register 2

Figure 26:
ZPOSM (0x0016)

Name	Read/Write/Program	Bit Position	Description
ZPOSM	R/W/P	7:0	8 most significant bits of the zero position

Figure 27:
ZPOSL (0x0017)

Name	Read/Write/Program	Bit Position	Description
ZPOSL	R/W/P	5:0	6 least significant bits of the zero position
comp_l_error_en	R/W/P	6	This bit enables the contribution of MAGH (Magnetic field strength too high) to the error flag
comp_h_error_en	R/W/P	7	This bit enables the contribution of MAGL (Magnetic field strength too low) to the error flag

Figure 28:
SETTINGS1 (0x0018)

Name	Read/Write/Program	Bit Position	Description
Factory Setting	R	0	Pre-Programmed to 1
NOISESET	R/W/P	1	Noise setting
DIR	R/W/P	2	Rotation direction
UVW_ABI	R/W/P	3	Defines the PWM Output (0 = ABI is operating, W is used as PWM 1 = UVW is operating, I is used as PWM)
DAECDIS	R/W/P	4	Disable Dynamic Angle Error Compensation (0 = DAE compensation ON, 1 = DAE compensation OFF)
ABIBIN	R/W/P	5	ABI decimal or binary selection of the ABI pulses per revolution
Dataselect	R/W/P	6	This bit defines which data can be read form address 16383dec (3FFFhex). 0->DAECANG 1->CORDICANG
PWMon	R/W/P	7	Enables PWM (setting of UVW_ABI Bit necessary)

Figure 29:
SETTINGS2 (0x0019)

Name	Read/Write/Program	Bit Position	Description
UVWPP	R/W/P	2:0	UVW number of pole pairs (000 = 1, 001 = 2, 010 = 3, 011 = 4, 100 = 5, 101 = 6, 110 = 7, 111 = 7)
HYS	R/W/P	4:3	Hysteresis setting
ABIRES	R/W/P	7:5	Resolution of ABI

ABI Incremental Interface

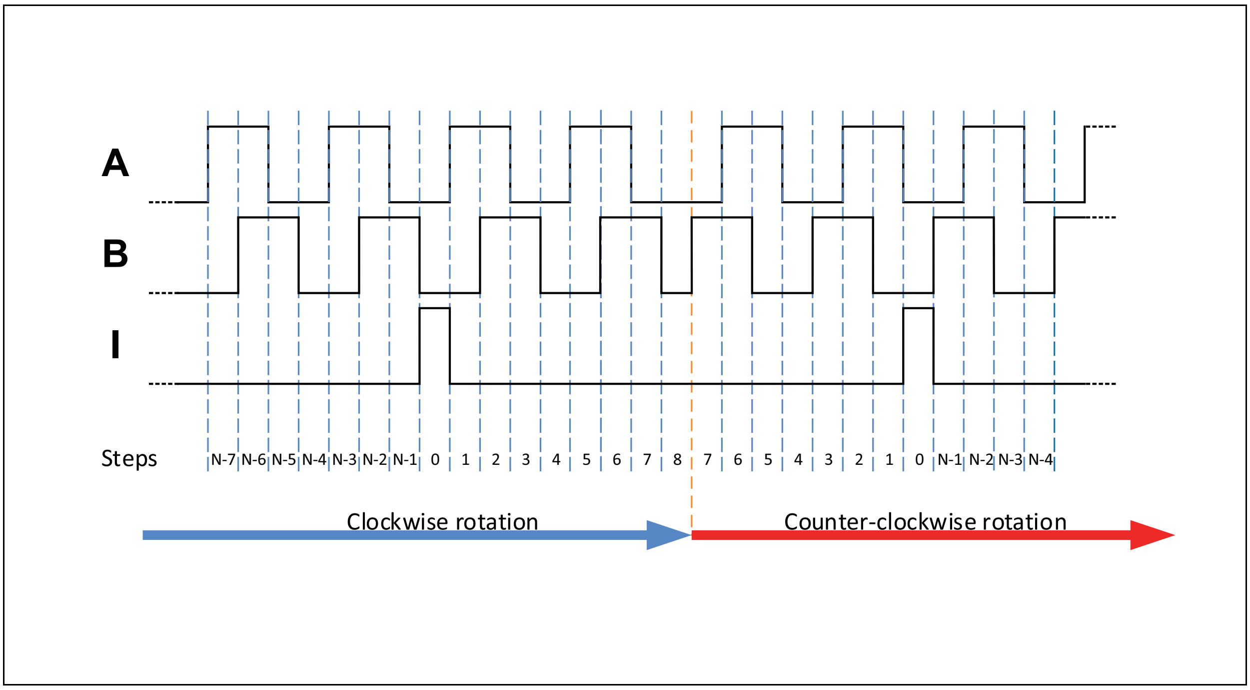
The AS5047P can send the angle position to the host microcontroller through an incremental interface. This interface is available simultaneously with the other interfaces. By default, the incremental interface is set to work at the highest resolution 4096 step per revolution, or 1024 pulses per revolution (ppr). It is possible to select between a decimal and binary pulses per revolution, respectively with the bit ABIBIN and select the pulses per revolution with the bit ABIRES as shown in Figure 30.

Figure 30:
ABI Resolution Setting

ABIRES	ABIBIN	Steps Per Revolution	Pulses Per Revolution
000	0	4000	1000
001	0	2000	500
010	0	1600	400
011	0	1200	300
100	0	800	200
101	0	400	100
110	0	200	50
111	0	100	25
000	1	4096	1024
001	1	2048	512
010	1	1024	256

The phase shift between the signals A and B indicates the rotation direction: e.g. DIR-Bit = 0, clockwise (A leads, B follows) or counterclockwise (B leads, A follows). During the start-up time, after power ON to the chip, all three ABI signals are high.

Figure 31:
ABI Signals at 11-Bit Resolution



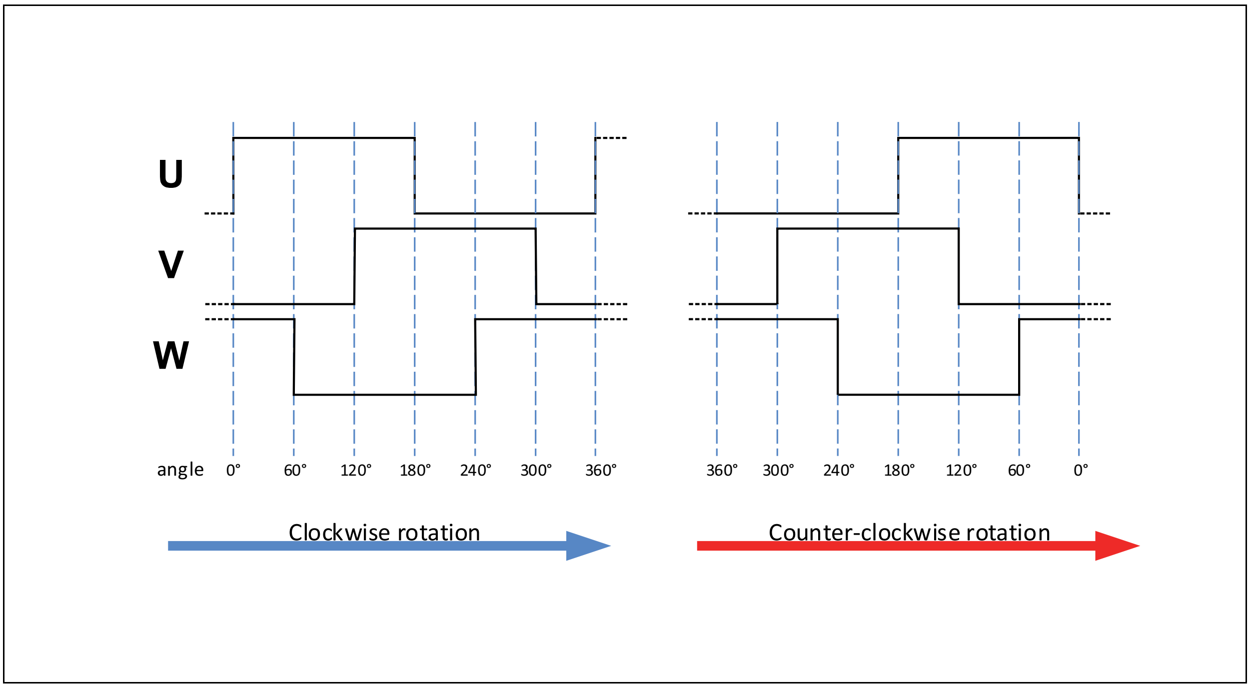
The Figure 31 shows the ABI signal flow if the magnet rotates in clockwise direction and counter-clockwise direction (DIR=0). The rotation direction of the magnet is defined as clockwise (DIR=0) when the view is from the topside of AS5047D. With the bit DIR, it is possible to invert the rotation direction.

UVW Commutation Interface

The AS5047P can emulate the UVW signals generated by the three discrete Hall switches commonly used in BLDC motors. The UVWPP field in the SETTINGS register selects the number of pole pairs of the motor (from 1 to 7 pole pairs). The UVW signals are generated with 14-bit resolution.

During the start-up time, after power ON of the chip, the UVW signals are low.

Figure 32:
UVW Signals



The Figure 32 shows the UVW signal flow if the magnet rotates in clockwise direction and counter-clockwise direction (DIR=0). The rotation direction of the magnet is defined as clockwise (DIR=0) when the view is from the topside of AS5047D. With the bit DIR, it is possible to invert the rotation direction.

PWM

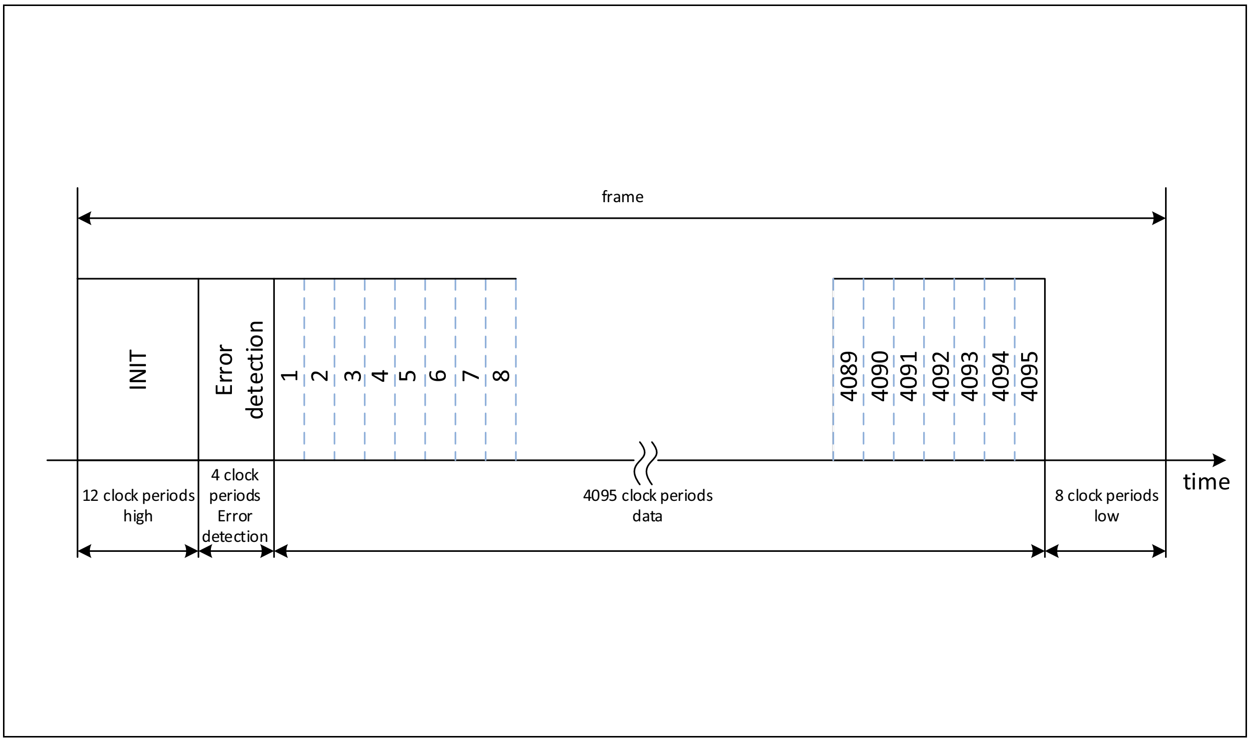
The PWM can be enabled with the bit setting PWMon. The PWM encoded signal is displayed on the pin W or the pin I. The bit setting UVW_ABI defines which output is used as PWM.The PWM output consists of a frame of 4119 PWM clock periods, as shown in Figure 33. The PWM frame has the following sections:

- 12 PWM Clocks for INIT
- 4 PWM Clocks for Error detection
- 4095 PWM clock periods of data
- 8 PWM clock periods low

The angle is represented in the data part of the frame with a 12-bit resolution. One PWM clock period represents 0.088 degree and has a typical duration of 444 ns.

If the embedded diagnostic of the AS5047P detects any error the PWM interface displays only 12 clock periods high (0.3% duty-cycle). Respectively the 4 clocks for error detection are forced to low.

Figure 33:
Pulse Width Modulation Encoded Signal



Hysteresis

The hysteresis can be programmed in the HYS bits if the SETTINGS2 register and depends on the chosen resolution of the incremental interface (ABIRES), as shown in the Figure 34.

Figure 34:
Hysteresis Settings

HYS	Hysteresis Related to 11 Bit ABI Resolution
00	3
01	2
10	1
11	0

Automatic Gain Control (AGC) and CORDIC Magnitude

The AS5047P uses AGC to compensate for variations in the magnetic field strength due to changes of temperature, air gap between the chip and the magnet, and demagnetization of the magnet. The automatic gain control value can be read in the AGC field of the DIAAGC register. Within the specified input magnetic field strength (Bz), the Automatic Gain Control works in a closed loop and keeps the CORDIC magnitude value (MAG) constant. Below the minimum input magnetic field strength, the CORDIC magnitude decreases and the MAGL bit is set.

Diagnostic Features

The AS5047P supports embedded self-diagnostics.

MAGH: magnetic field strength too high, set if AGC = 0x00. This indicates the non-linearity error may be increased.

MAGL: magnetic field strength too low, set if AGC = 0xFF. This indicates the output noise of the measured angle may be increased.

COF: CORDIC overflow. This indicates the measured angle is not reliable.

LF: offset compensation completed. At power-up, an internal offset compensation procedure is started, and this bit is set when the procedure is completed.

OCF Error / COF Error

In case of an OCF or COF error, all outputs are changing into a safe state:

SPI Output: Information in the DIAAGC (0x3FFC) register. The angle information is still valid.

PWM Output: PWM Clock Period 13 - 16 of the first 16 PWM Clock Periods = low. Additional there is no angle information valid (all 4096 clock periods = low)

ABI Output: The state of ABI is frozen to ABI = 111

UVW Output: The state of UVW is frozen to UVW = 000

MAGH Error / MAGL Error

Default diagnostic setting for MAGH error /MAGL error:

In case of a MAGH error or MAGL error, there is no safe state on the PWM,ABI or UVW outputs if comp_h_error_en is 0 and comp_l_error_en is 0.

The error flags can be read out with the DIAAGC (0x3FFC) register.

Enhanced diagnosis setting for MAGH error / MAGL error:

In case of a MAGH error or MAGL error, the PWM,ABI or UVW outputs are going into a safe state if comp_h_error_en is 1 and comp_l_error_en is 1. The device is operating with the performance as explained.

SPI Output: Information in the DIAAGC (0x3FFC) register. The angle information is still valid, if the MAGH or MAGL error flag is on.

PWM Output: PWM Clock Period 13 - 16 of the first 16 PWM Clock

Periods = low. Additional there is no angle information valid (all

4096 clock periods = low)

ABI Output: The state of ABI is frozen to ABI = 111

UVW Output: The state of UVW is frozen to UVW = 000

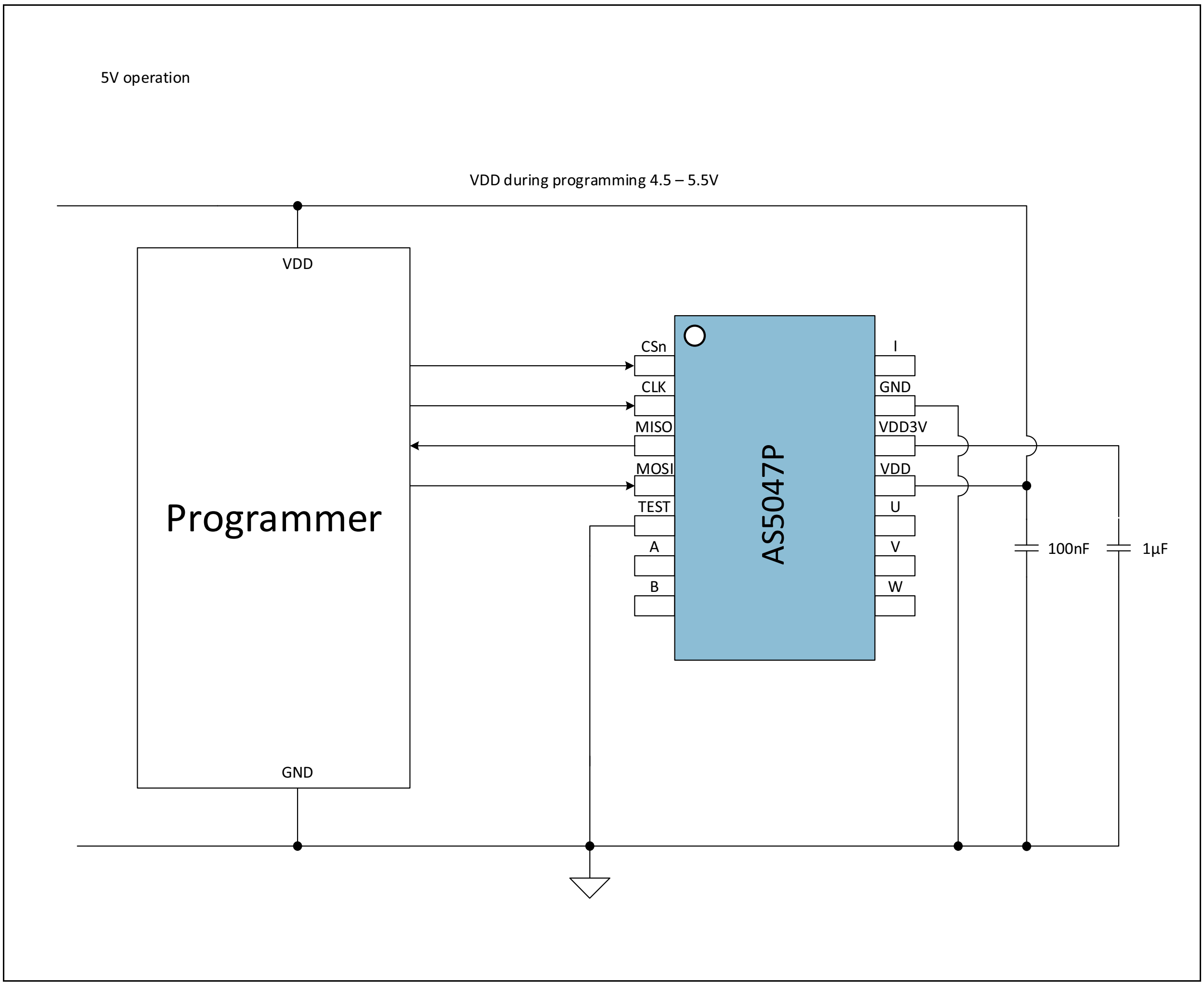
Important: When comp_(h/l)_error_en is enabled a marginal magnetic field input can cause toggling of MAGH or MAGL which will lead to toggling of the ABI/UVW outputs between operational mode and failure mode.

Application Information

Burn and Verification of the OTP Memory

Step-by-step procedure to permanently program the non-volatile memory (OTP):

Figure 35:
Minimum Programming Diagram for the AS5047P in 5 V Operation



Note(s) and/or Footnote(s):

1. In terms of EMC and for remote application, additional circuits are necessary.