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AS5132

360 Step (8.5 bit) Programmable High Speed Magnetic Position Sensor

General Description

The AS5132 is a contactless magnetic position sensor for accurate angular measurement over a full turn of 360 degrees. It is a system-on-chip, combining integrated Hall elements, analog frontend and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip is required.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 8.5 bit = 360 positions per revolution. This digital data is available as serial output over the interface and as a pulse width modulated (PWM) signal.

An additional U,V,W output can be used for a block commutation for a brushless DC motor. An incremental signal is available as an option.

In addition to the angle information, the strength of the magnetic field is also available as a 5-bit code.

A one time programmable (OTP) memory is used for permanent zero angle position programming. The magnet does not need to be aligned mechanically.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5132, 360 Step (8.5 bit) Programmable High Speed Magnetic Position Sensor are listed below:

Figure 1:
Added Value of Using AS5132

Benefits	Features
• Complete system-on-chip, no calibration required	• 360º contactless angular position sensing
• Multiple data output formats	• Serial synchronous interface • Pulse width modulated output (PWM) • Incremental output formats

Benefits	Features
• Ideal for applications in harsh environments due to magnetic sensing principle	• High reliability due to non-contact sensing
• Robust system, tolerant to horizontal misalignment, airgap variations, temperature variations and external magnetic stray fields	• Wide magnetic field input range: 20 – 80 mT (typical) • Wide temperature range: -40ºC to 150ºC • Fully automotive qualified to AEC-Q100, grade 0

Applications

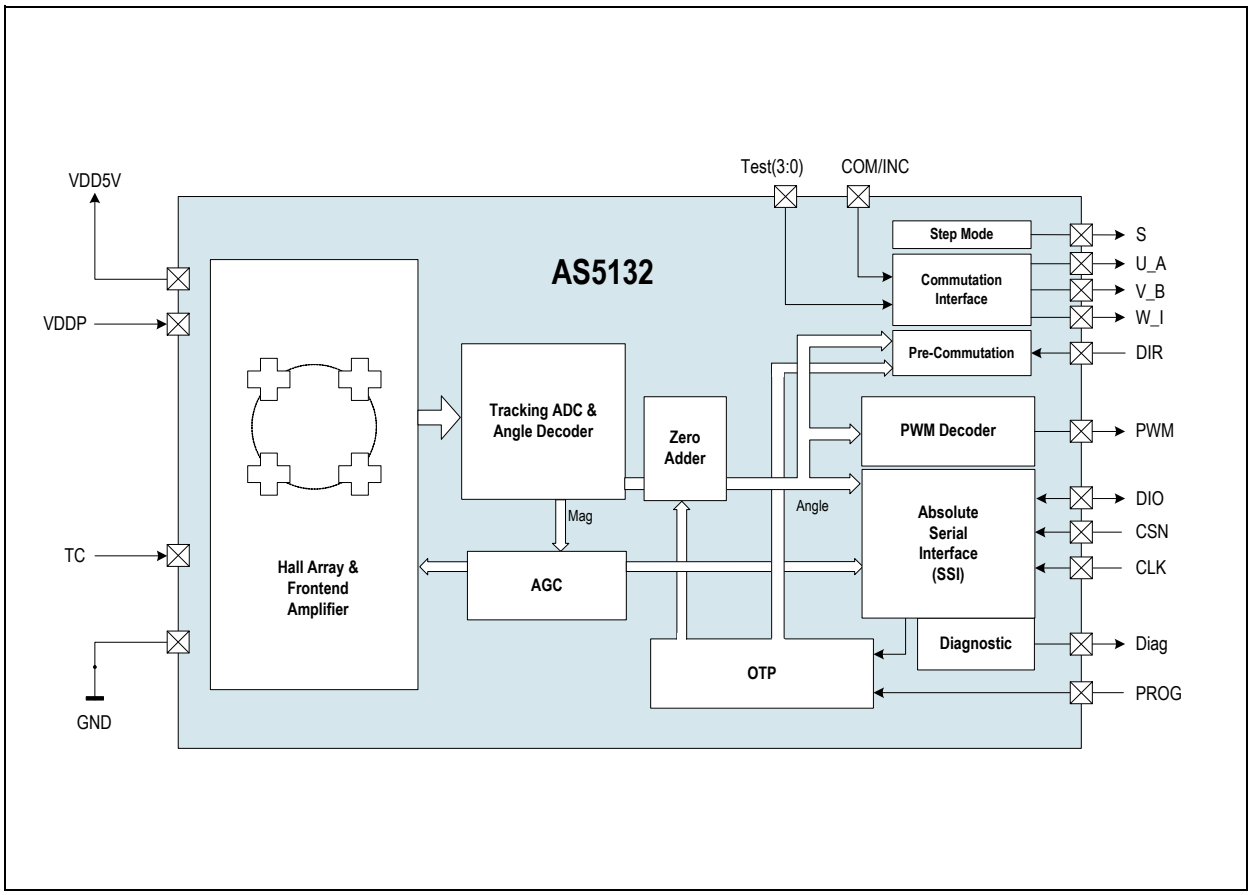
The AS5132 is suitable for:

- Contactless rotary position sensing
- Rotary switches (human machine interface)
- AC/DC motor position control
- Brushless DC motor position control

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS5132 Block Diagram



Pin Assignment

The AS5132 pin assignments are described below.

Figure 3:
Pin Diagram

Pin Assignments (Top View):
Package drawing is not to scale.

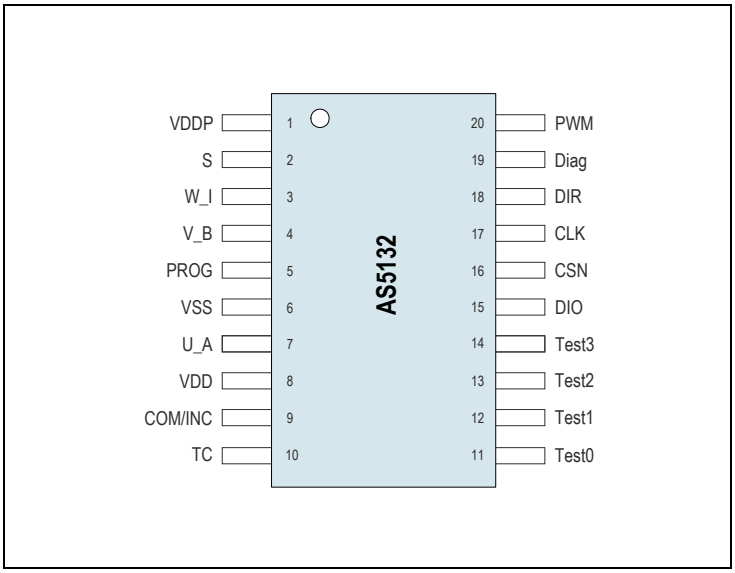


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	VDDP	Supply	Supply voltage for the selected pins (1)
2	S	Digital output	Step output (8mA, VDDP)
3	W_I		Commutation output or incremental output
4	V_B		
5	PROG	Analog Input / Output	Programming voltage input. Do not connect this pin to VSS. Connectivity for programming see Figure 24
6	VSS	Supply	Supply ground
7	U_A	Digital output	Commutation output or incremental output
8	VDD	Supply	Positive supply voltage
9	COM / INC	Digital input / Schmitt-Trigger	Selection of the output mode. This pin is also used for external clock mode (VDDP)
10	TC	Analog input	Test pin. Connect to VSS in application

Pin Number	Pin Name	Pin Type	Description
11	Test0	Analog input /output	Test pin, selection of output format for incremental or step mode
12	Test1		
13	Test2		
14	Test3		
15	DIO	Bi-directional digital	Data I/O for serial interface (VDDP)
16	CSN	Digital input / Schmitt-Trigger	Chip select input (active low) (VDDP) (connected to a pull-up resistor if not used in application)
17	CLK		Clock input for serial interface (VDDP)
18	DIR		Input signal for the pre-commutation at start-up (VDDP)
19	Diag	Digital output / Open Drain	Diagnostic output (open drain)
20	PWM	Digital output	PWM output (8mA, VDDP)

Note(s):

1. VDDP can be customized to the voltage levels of the peripheral circuitry to economize voltage level drivers.
2. Typ. CSN Pull_up resistor of 10kOhm necessary. Floating state of a digital input is not allowed.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD}	Supply voltage	-0.3	7	V	Except during OTP programming
VDDP	DC supply voltage	0.3	7	V	Cannot be higher than VDD+0.3
V_{IN}	Input pin voltage	VSS-0.5	VDD	V	
I_{scr}	Input current (latch up immunity)	-100	100	mA	Norm: EIA/JESD78 Class II Level A
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge	±2		kV	Norm: JESD22-A114E
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-55	150	°C	
T_{body}	Body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
RH_{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level	3			Represents a maximum floor time of 168h

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) method.

T_{AMB} = -40ºC to 150ºC, VDD = 4.5V to 5.5V, all voltages referenced to VSS, unless otherwise noted.

Operating Conditions

Figure 6:
Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Positive supply voltage		4.4		5.5	V
VDDP	Positive supply voltage periphery		3.0		5.5	V
IDD	Operating current	No load on outputs. Supply current can be reduced by using stronger magnets.		15	22	mA

System Parameters

Figure 7:
System Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
N	Resolution			8.5		Bit
				1		Deg
T_{PwrUp}	Power up time				≤ 4100	µs
t_s	Tracking rate	Step rate of tracking ADC; 1 step = 1º			5.2	µs/step
INL_{cm}	Accuracy	Centered magnet	-2		2	Deg
		Within horizontal displacement radius	-3		3	
t_{delay}	Propagation delay	Internal signal processing time			22	µs
TN	Transition noise	peak-peak			1.41	Deg

Magnet Specifications

Figure 8:
Magnet Specifications

Symbol	Parameter	Conditions	Min	Max	Units
B_Z	Magnetic input range	At die surface	20	80	mT
V_i	Magnet rotation speed	To maintain locked state (1)		72,900	rpm

Note(s):

1. Maximum rotation speed is dependent on the internal time reference.
   Maximum value is calculated with lowest sequence over all operating conditions.

Programming Parameters

Figure 9:
Programming Parameters

Symbol	Parameter	Conditions	Min	Max	Units
V_{PROG}	Programming voltage	Static voltage at pin PROG	8	8.5	V
I_{PROG}	Programming current	During programming		100	mA
$Tamb_{PROG}$	Programming ambient temperature		0	85	°C
t_{PROG}	Programming time		2	4	µs
$V_{R,prog}$	Analog readback voltage	During analog readback mode at pin PROG		0.5	V
$V_{R,unprog}$			2	3.5	

DC Characteristics of Digital Inputs

Figure 10:
CMOS Inputs COM/INC, CSN, CLK, DIO, DIR

Symbol	Parameter	Min	Max	Units	Note
V_{IH}	High level input voltage	0.7*VDDP	VDDP	V	COM/INC refer to VDD
V_{IL}	Low level input voltage	0	0.3*VDDP	V	
I_{LEAK}	Input leakage current		1	µA	

DC Characteristics of Digital Outputs

Figure 11:
CMOS Outputs S, U_A, V_B, W_I, PWM, DIO

Symbol	Parameter	Min	Max	Units	Note
V_{OH}	High level output voltage	VDDP-0.5	VDDP	V	PWM and S have 8mA output load, DIO has 4mA output load.
		VDD-0.5	VDD		U_A, V_B, W_I have 4mA output load.
V_{OL}	Low level output voltage	0	VSS+0.4	V	PWM and S have 8mA output load, DIO, U_A, V_B, W_I has 4mA output load.
CL	Capacitive load		35	pF	

Timing Characteristics

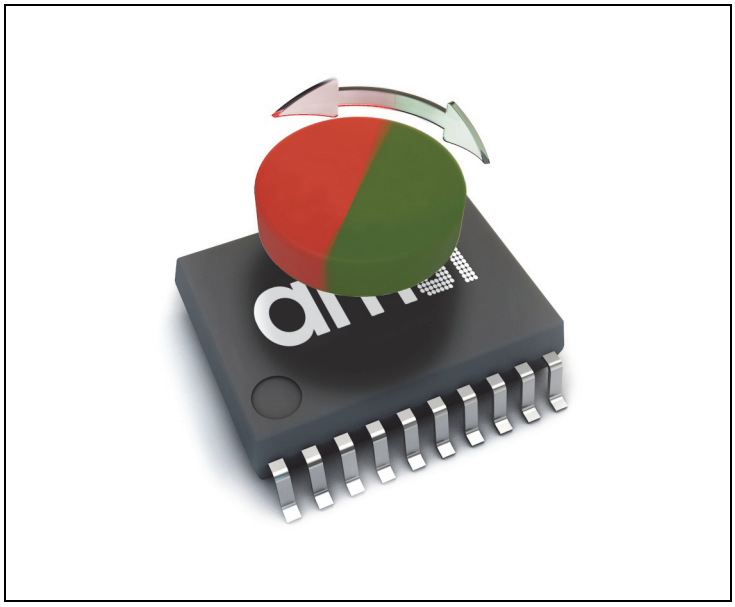
Figure 12:
Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units
f_{CLK}	Clock frequency normal operation		5	6	MHz
f_{CLKP}	Clock frequency during OTP programming	200		650	kHz
t_1	CSn to positive edge of CLK	150			ns
t_2	CSn to drive bus externally	0			ns
t_3	Setup time command bit (data valid to positive edge of CLK)	50			ns
t_4	Hold time command bit (data valid after positive edge of CLK)	15			ns
t_5	Float time (positive edge of CLK for last command bit to bus float)			$0.5 * 1/f_{CLK}$	ns
t_6	Bus driving time (positive edge of CLK for last command bit to bus drive)	$0.5 * 1/f_{CLK}$			ns
t_7	Data valid time (positive edge of CLK to bus valid)	$0.5 * 1/f_{CLK}$		$0.5 * 1/f_{CLK} + 50$	ns
t_8	Hold time data bit (data valid after positive edge of CLK)	$0.5 * 1/f_{CLK}$			ns

Symbol	Parameter	Min	Typ	Max	Units
t_9	Hold time CSn (positive edge of last CLK to negative edge of CSn)	0.5 *1/f_{CLK}			ns
t_{10}	Bus floating time (positive edge of CSn to float bus)			50	ns
t_{11}	Setup time data bit @ write access (data valid to positive edge of CLK)	50			ns
t_{12}	Hold time data bit @ write access (data valid after positive edge of CLK)	15			ns
t_{13}	Bus floating time (positive edge of CSn to float bus)			50	ns
t_{14}	CSn high time	2			µs

Detailed Description

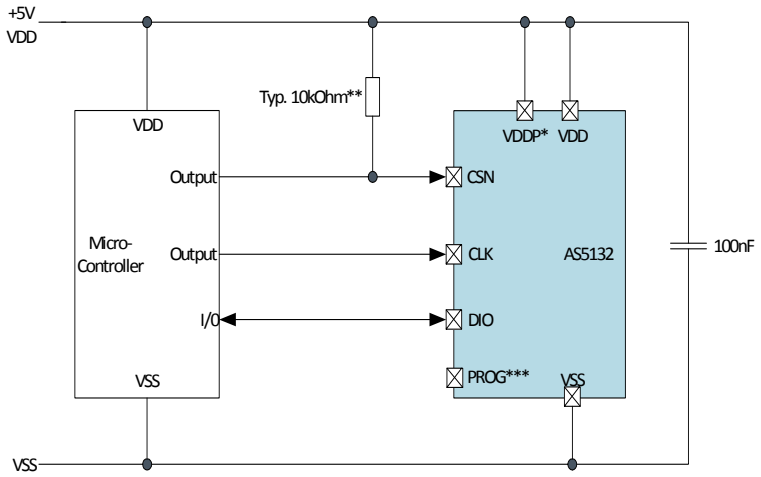
Figure 13:
Typical Arrangement of AS5132 and Magnet



Synchronous Serial Interface (SSI)

The absolute angle data can be read out over the synchronous serial interface using the pins **CSN**, **DIO** and **CLK**. It is a bidirectional interface therefore a read or write access is possible. The organization of the protocol is byte wise and starts with the command byte followed by the data information.

Figure 14:
Read / Write Serial Data Transmission



* DIO output pin is connected internally to the VDDP voltage domain. VDD and VDDP can be separately connected too.
** Recommend pull-up resistor (typ. 10kOhm)
***Depending on the use case:
- Application use case (connection to VDD or leave unconnected. Capacitive load during operation and startup not allowed)
- Programming use case (see Figure 24)

Figure 14 shows the connection of the AS5132 to a micro controller. Depending on the command byte are different access types possible. In normal mode the number of clocks is equal the number of data bits.

Figure 15:
Data Organization of the SSI Protocol 16-Bit Data

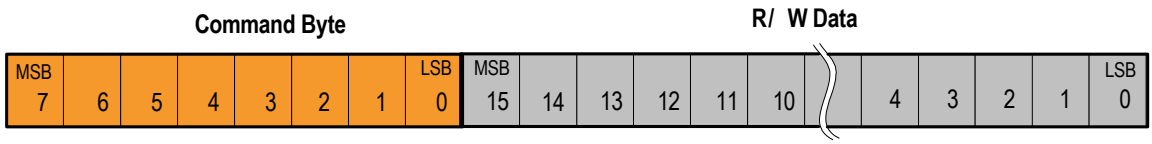
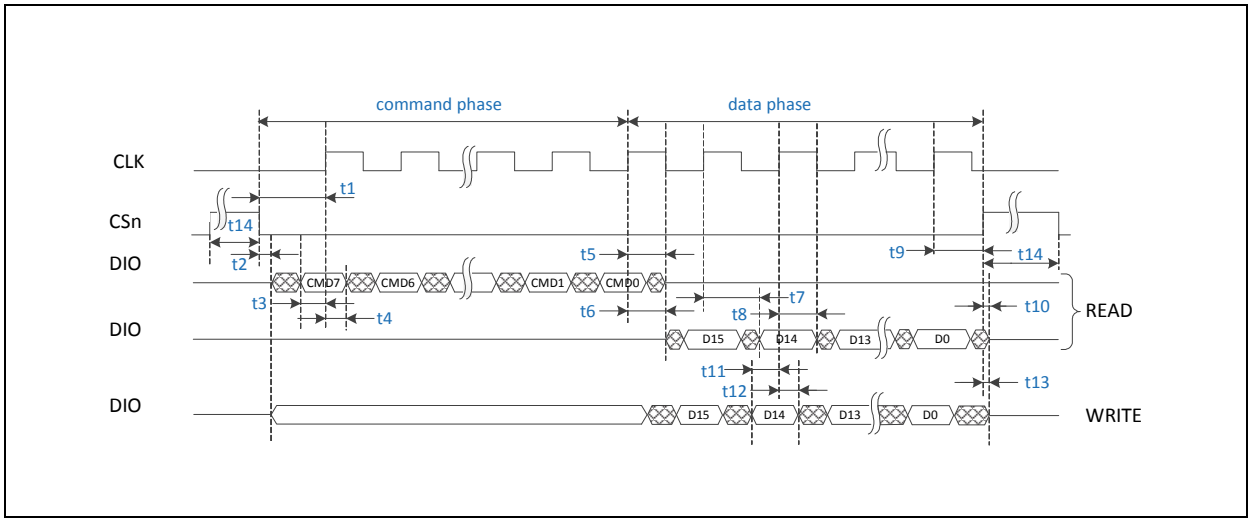


Figure 15 shows the organization of the data. The first section is used to setup the operating mode and the address. During write mode the micro controller drives the data line and generates in addition the CSN and CLK signal. Figure 16 shows SSI Read and write operations in normal mode.

Figure 16:
SSI Normal Read and Write Mode



The first 8 command data bits are written by the microcontroller. After the command data the device takes over the **DIO** line and writes the data information. A high impedance phase must be considered before the device drives the output line.

Commands of the SSI in Normal Mode

Figure 17:
Read/Write Interface Commands in Normal Mode

Command Name	Command Data	Access Mode	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
WRITE CONFIG	0001_0111	write		GEN RST	Hyst Dis	PRE_COM_DYN<5:0>						MTC2	MTC1					
SET MT COUNTER	0001_0100	write	MT - COUNTER <8:0>															
EN PROG	1000_0100	write	0	1	1	0	0	1	0	1	0	1	1	1	0	0	0	0
RD MT COUNTER	0000_0100	read	MT - COUNTER <8:0>									EZ ERR						P
RD_ANGLE	0000_0000	read	ANGLE <8:0>									LOCK ADC	AGC <5:1>					P

Note(s):

1. Gray bits can be ignored by the user.

GEN RST: A HI generates a reset of the AS5132. GEN RST must be set to LO after reset.

Hyst_Dis: Hysteresis disable.

PRE_COM_DYN <5:0>: Absolute dynamic pre-commutation value. Depending on the setup of the pole pairs, a mechanical angle offset can be adjusted. The range is 0 to 63 mechanical degrees (LSBs).

MT-COUNTER <8:0>: The multiturn counter can be set or read over the interface.

EN PROG: This command with the data content enables the access to the OTP register in extended mode. OTP Programming mode is only possible in extended mode with special connection Figure 24 on page 18.

EZ ERR: Indicates a wrong operation of the OTP memory after programming at room temperature.This bit is not intended for OTP diagnostic in the application over life time. This bit lose also validity over a time.

ANGLE <8:0>: Absolute angle information with angular true resolution (360 steps).

LOCK ADC: Indicates a locked ADC. An angle value is only valid in case of a locked ADC. During sleep mode is the LOCK ADC bit LO.

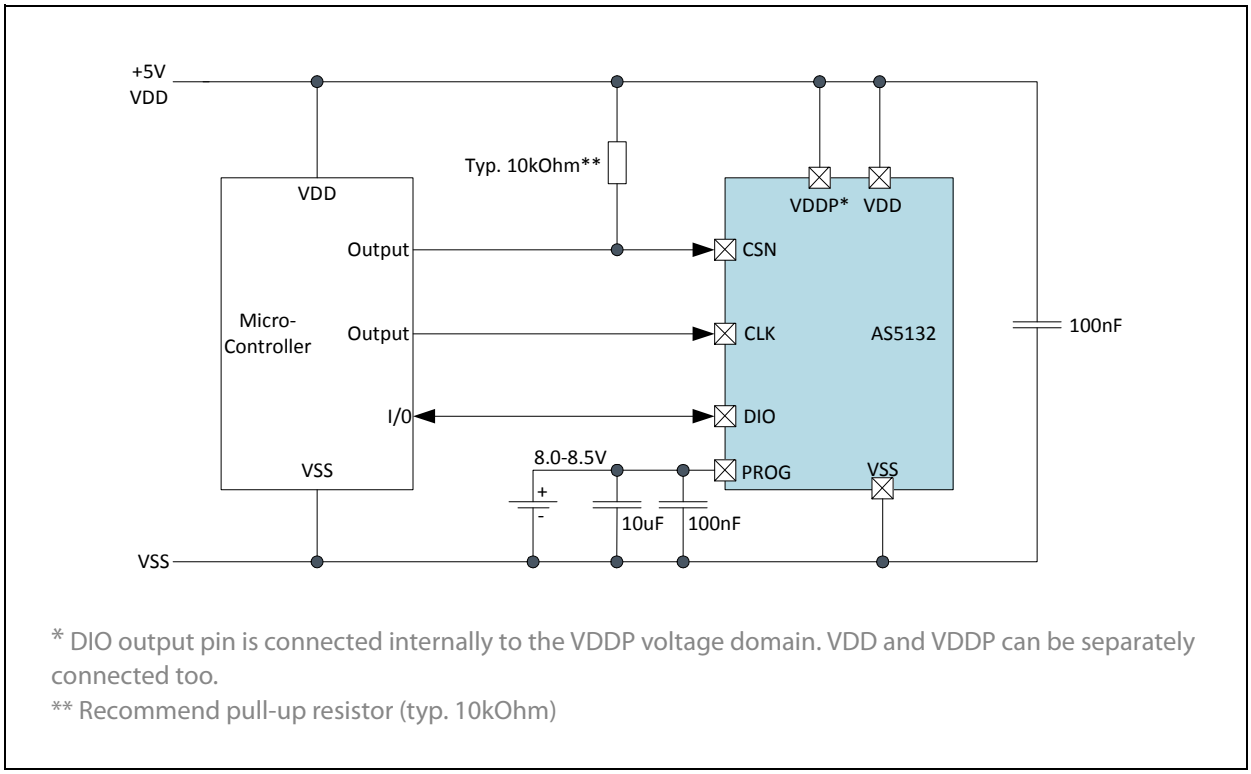
AGC <5:1>: Automatic gain control value indicates the magnetic field strength.

P: Parity information of the 15 data bits. Odd parity.

Extended Synchronous Serial Interface Mode

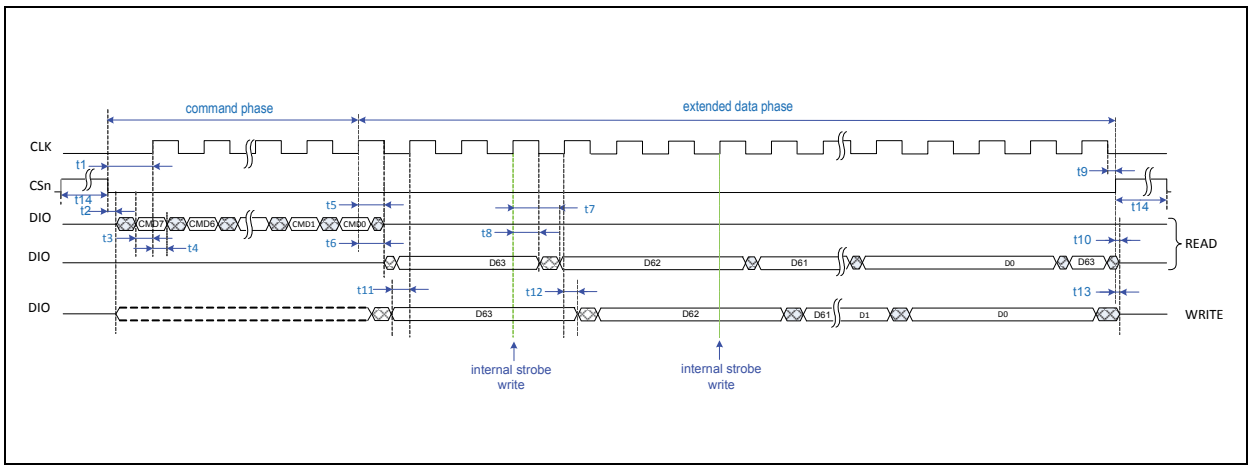
The absolute angle data can be read out over the synchronous serial interface using the pins **CSN**, **DIO** and **CLK**. It is a bidirectional interface therefore a read or write access is possible. The organization of the protocol is byte wise and starts with the command byte followed by the data information.

Figure 18:
Connectivity During Programming in Extended Mode



* DIO output pin is connected internally to the VDDP voltage domain. VDD and VDDP can be separately connected too.
** Recommend pull-up resistor (typ. 10kOhm)

Figure 19:
SSI Extended Read and Write Mode



In extended mode the digital interface requires four clocks per data bit. During this time the device is able to handle internal signals for special access.

Figure 20:
Read/Write Interface Commands in Extended Mode

Command Name	Command Data	Access Mode	MSB 63	...	17	16	15	14	13	12	11	10	9	8	...	LSB 0
WRITE OTP	0001_1111	ext. write	TST<46:0>			SENSITIVITY <1:0>		ext. CLK EN	PRE_COM_STAT <1:0>		UVW <2:0>			ZERO ANGLE <8:0>		
PROG OTP	0001_1001	ext. write	TST<46:0>			SENSITIVITY <1:0>		ext. CLK EN	PRE_COM_STAT <1:0>		UVW <2:0>			ZERO ANGLE <8:0>		
READ OTP	0000_1111	ext. write	TST<46:0>			SENSITIVITY <1:0>		ext. CLK EN	PRE_COM_STAT <1:0>		UVW <2:0>			ZERO ANGLE <8:0>		
READ ANA	0000_1001	ext. read	TST<46:0>			SENSITIVITY <1:0>		ext. CLK EN	PRE_COM_STAT <1:0>		UVW <2:0>			ZERO ANGLE <8:0>		

Note(s):

1. TST is pre-programed by ams AG and used for test purpose.

Programming Parameters

ZERO ANGLE <8:0>: Zero position value. This value is permanent added to the internal absolute position. Use range 0 to 359.

UVW <2:0>: Setup of the number of pole pairs. In the step mode configuration, the bit UVW<2> is used to invert the step mode output signal.

Figure 21:
Possible Settings for UVW Outputs

UVW <2:0>			Number of Pole Pairs
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	6
1	1	1	6

SENSITIVITY <1:0>: Setup of the amplification within the internal signal path. The sensitivity adjustment can be used to center the AGC value at default conditions.

Figure 22:
Setup of the Sensitivity

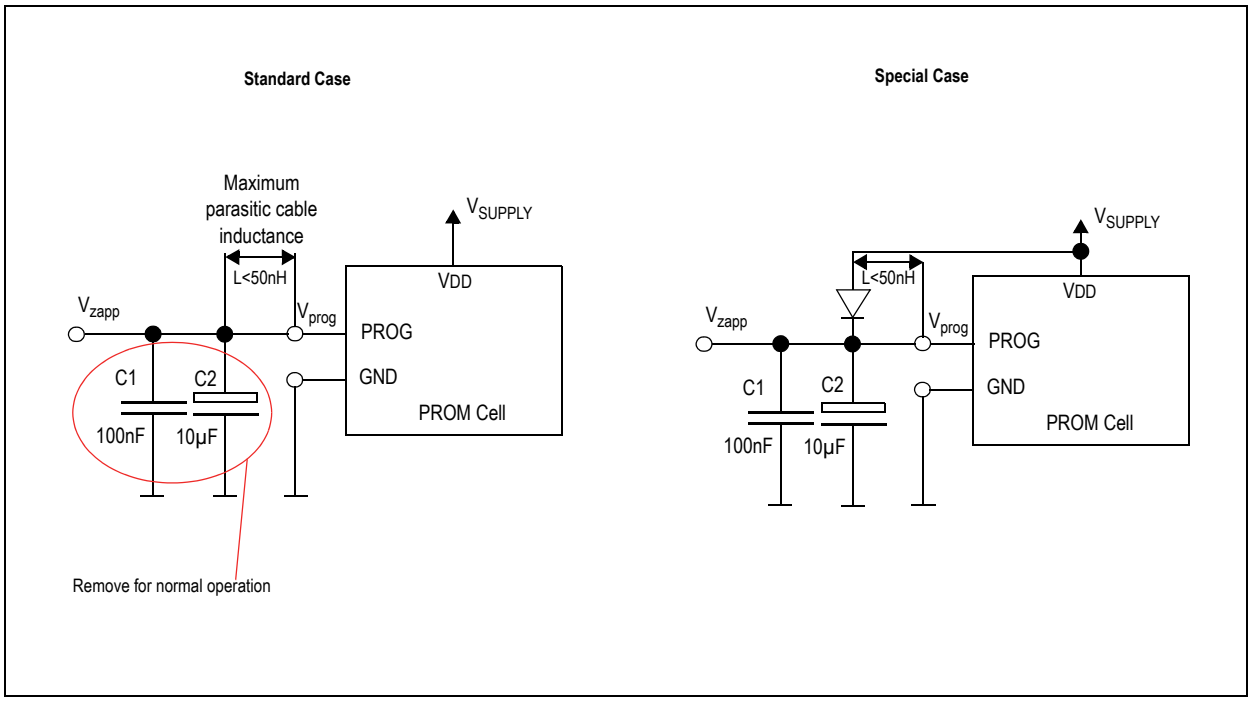
SENSITIVITY <1:0>		Sensitivity Setting		
		Min	Typ	Max
0	0	1.6	1.65	1.75
0	1	1.79	1.88	1.98
1	0	2.01	2.11	2.22
1	1	2.23	2.35	2.47

Figure 23:
Setup Parameters for the Static Pre-Commutation

PRE_COM_STAT <1:0>		Static Pre-commutation Value in Mechanical Degrees
0	0	0
0	1	2
1	0	4
1	1	8

Ext. CLK EN: Enables the external CLK mode for the PWM output. The external CLK mode is only possible in commutation mode. The state of the pin COM/INC is not considered in this case for mode selection.

Figure 24:
OTP Programming Connection



The maximum capacitive load at PROG in normal operation should be less than 20pF. However, during programming the capacitors C1+C2 are needed to buffer the programming voltage during current spikes, but they must be removed for normal operation. To overcome this contradiction, the recommendation is to add a diode (4148 or similar) between PROG and V_{DD} as shown in Figure 24 (special case setup), if the capacitors can not be removed at final assembly.
Due to D1, the capacitors C1+C2 are loaded with V_{DD}-0.7V at startup, hence not influencing the readout of the internal OTP registers. During programming the OTP, the diode ensures that no current is flowing from PROG (8V to 8.5V) to VDD (5V).
In the standard case (see Figure 24), the verification of a correct OTP readout must be done by analog readback. The special case setup provides the analog readback of the OTP as well.
As long as the PROG pin is accessible it is recommended to use standard setup. In case the PROG pin is not accessible at final assembly, the special setup is recommended.

Programming Verification

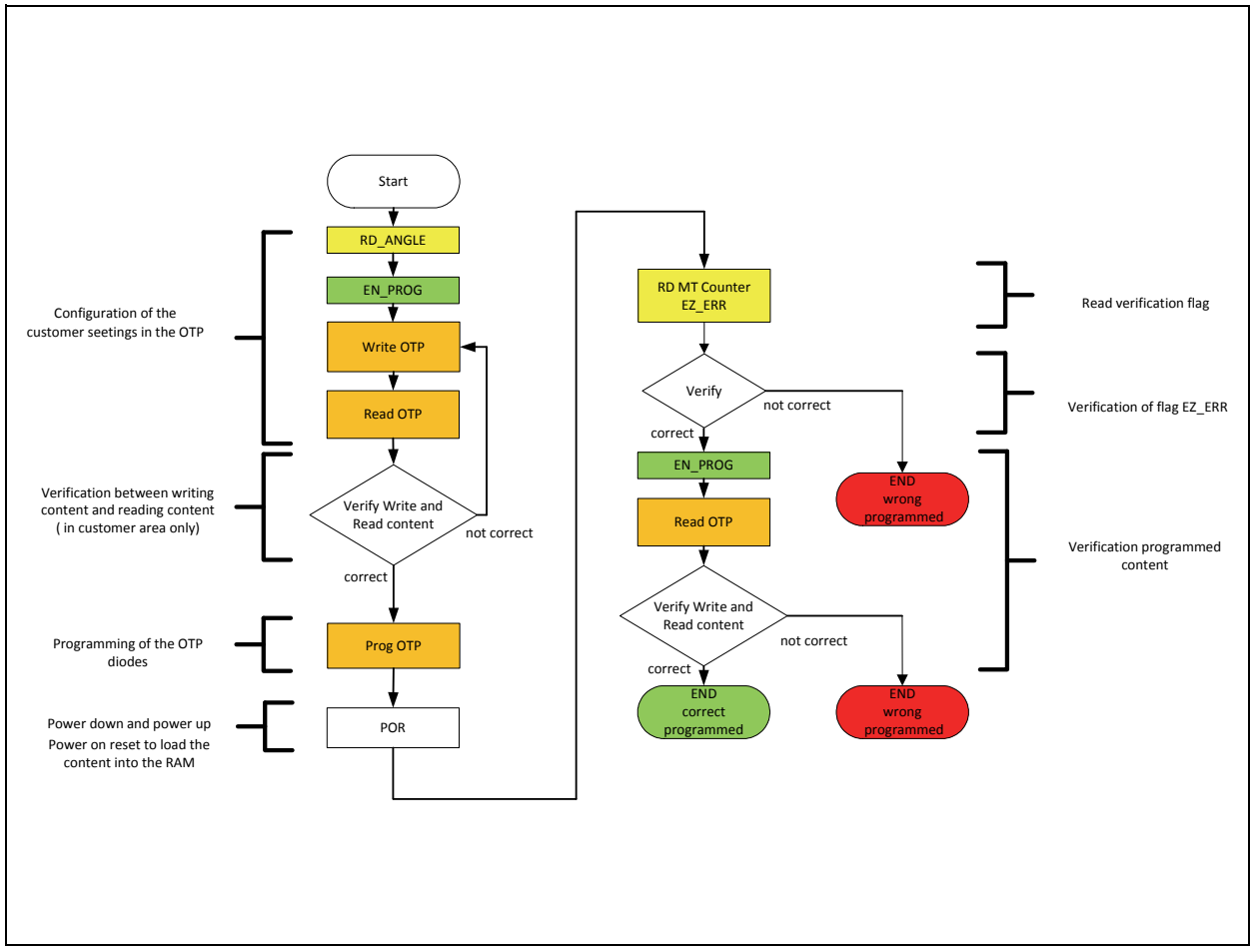
The verification of the OTP programming is mandatory using following methods:

Digital Verification: Checking the EZ ERR bit (0 = OK, 1 = error)

- Restricted to temperature range: 25 °C ± 20 °C
- Right after the programming (max. 1 hour with same conditions 25°C ± 20 °C)

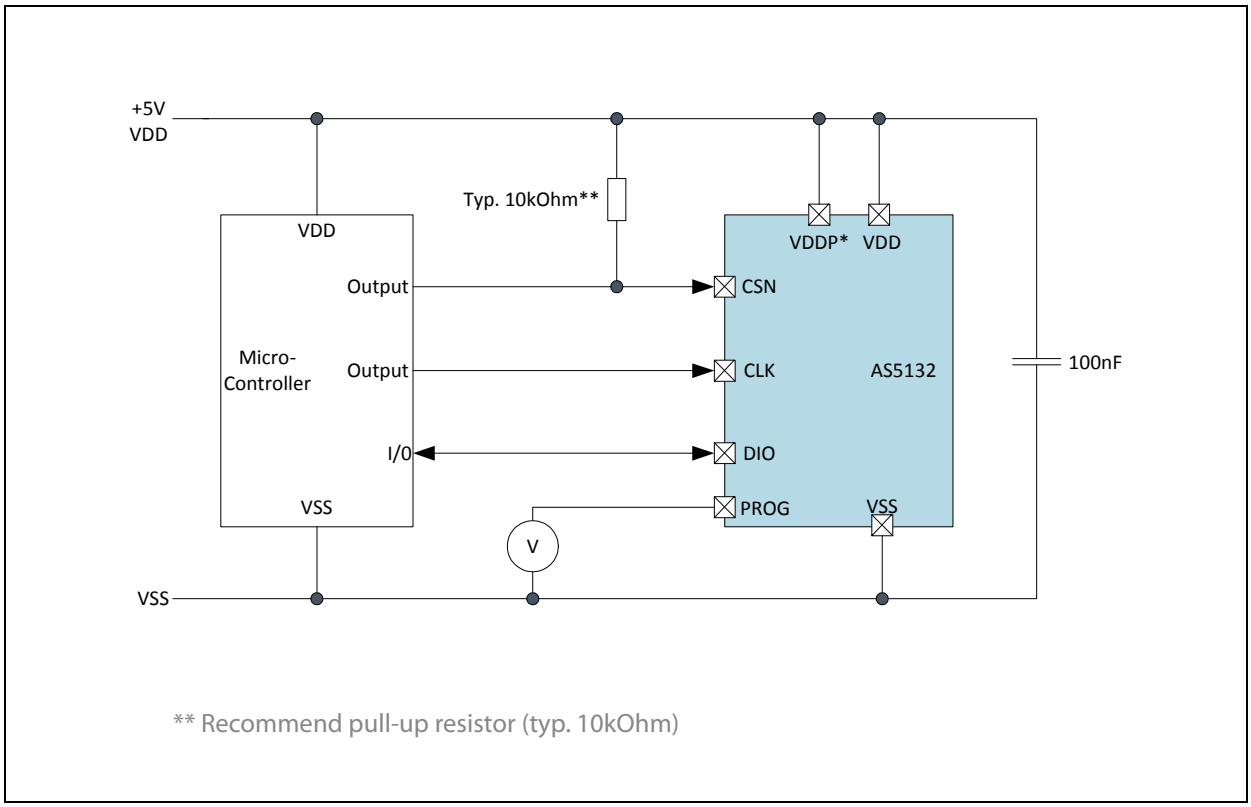
Figure 25 shows the correct digital verification flow. The EZ_ERR bit is valid only after a power on reset. This bit becomes invalid after a OTP write or read access.

Figure 25:
Programming & Digital Verification Flow



Analog Verification: By switching into Extended Mode and sending a READ ANA command, the pin PROG becomes an output sending an analog voltage with each clock representing a sequence of the bits in the OTP register (starting with D61). A voltage of <500mV indicates a correctly programmed bit ("1") while a voltage level between 2V and 3.5V indicates a correctly unprogrammed bit ("0"). Any voltage level in between indicates incorrect programming.

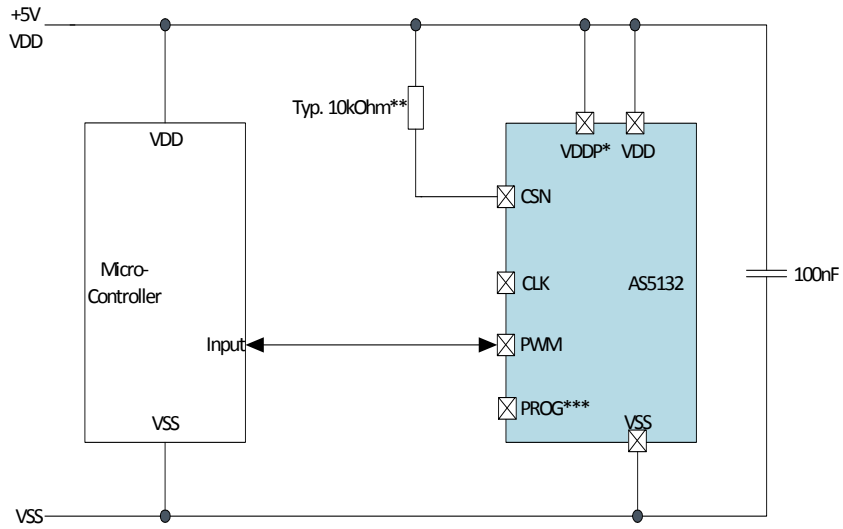
Figure 26:
Analog OTP Verification



Pulse Width Modulation (PWM) Output

The AS5132 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the absolute angle position. Figure 29 shows the output format. In case of an internal error the high pulse contains 12 steps. An error can be easily identified by the external microcontroller. The zero degree angle position is build with 16 steps (12 + 4) high and 359 steps low followed by 8 exit steps.

Figure 27:
PWM Output



*PWM output pin is connected internally to the VDDP voltage domain. VDD and VDDP can be separately connected

** Recommended pull-up (typ. 10kOhm). Floating state of a digital input in an application is not allowed

***Depending on the use case:

- Application use case (connection to VDD or leave unconnected. Capacitive load during operation and startup not allowed)
- Programming use case (see Figure 24)

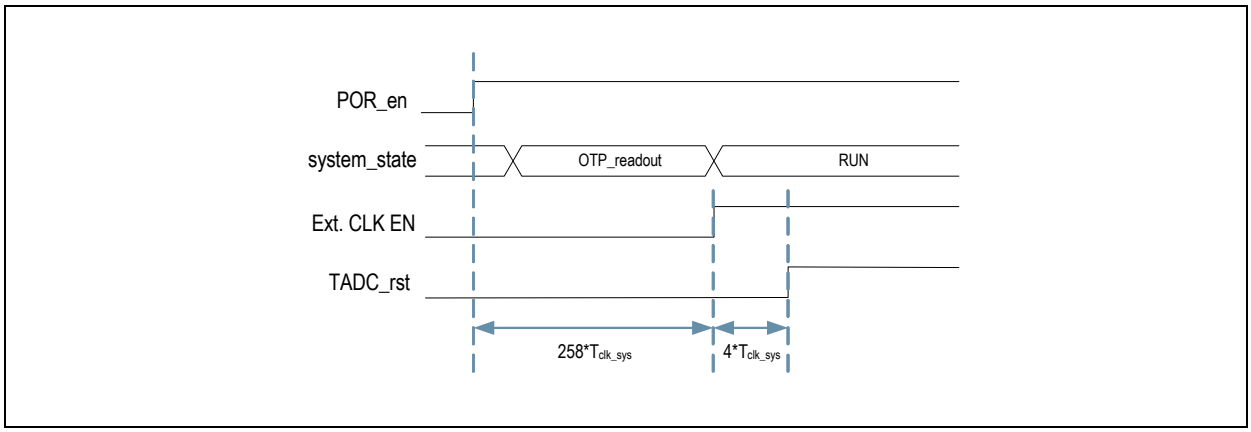
PWM External Clock

The PWM period depends on the setting of the OTP bit **Ext. CLK EN**. By default the internal clock source is used as a reference. An external clock can be connected to the pin COM/INC.

In case Ext. CLK EN is set, the output-mode which is determined by the states of {COM/INC, Test3, Test2, Test1, Test0} Figure 31 on page 23 during start-up is overwritten and U,V,W commutation mode signals are activated.

After internal power on reset (POR_en), the OTP is read out. When the Ext. CLK EN is programmed successfully, the COM/INC pin is used as external clock for the PWM block. After 4 clock cycles of Ext. CLK EN, the reset of TADC (TADC_rst) and the PWM block is released.

Figure 28:
Start-Up Procedure



The reset for the PWM block is synchronized to the external PWM clock. This ensures a save reset also in case the external clock on COM/INC is already running during start-up.

Figure 29:
PWM Output Signal

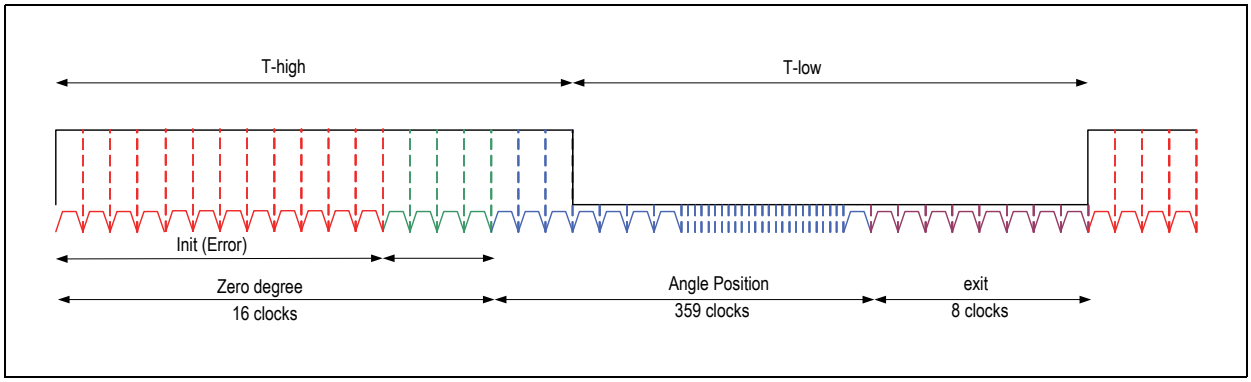


Figure 30:
PWM Timing with Internal and External CLK Source

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{PWMint}	PWM Period internal	600	750	900	µs	Internal clock source
T_{PWMext}	PWM Period external	383 / CLK_{PWM}			µs	External clock provided over COM / INC pin
CLK_{PWM}	Clock external mode	0		766	kHz	

Incremental Outputs

Two different incremental output modes are possible. Quadrature A/B mode and selectable Step Mode can be selected by the pins **TEST0**, **TEST1**, **TEST2**, **TEST3** and **COM / INC**.

Figure 31:
Configuration of the Incremental Output Modes

COM / INC	TEST3	TEST2	TEST1	TEST0	Output Mode	Pin Assignment
1	0	0	0	0	Quadrature A/B/I Mode 90 pulses per channel	A → U_A B → V_B I → W_I '0' → S
1	0	0	0	1	Stepmode 24 pulses and Index width 2	'0' → U_A '0' → V_B '0' → W_I S_24_2 → S
1	0	0	1	0	Stepmode 60 pulses and Index width 2	'0' → U_A '0' → V_B '0' → W_I S_60_2 → S
1	0	0	1	1	Stepmode 90 pulses and Index width 2	'0' → U_A '0' → V_B '0' → W_I S_90_2 → S
1	0	1	0	0	Stepmode 180 pulses and Index width 2	'0' → U_A '0' → V_B '0' → W_I S_180_2 → S
0	0	0	0	0	U,V,W Commutation Mode (OTP setting)	U → U_A V → V_B W → W_I '0' → S

Note(s):

1. The pin setting COM / INC has priority. In case of a low state the device is exclusively in the commutation mode. Not specified states of TEST3, TEST2, TEST1 and TEST0 in incremental mode will enable the quadrature A/B/I mode. This configuration is only read once at startup. It is not recommended to change the state during operation.

Quadrature A/B Output

Figure 32:
Incremental Output of the AS5132

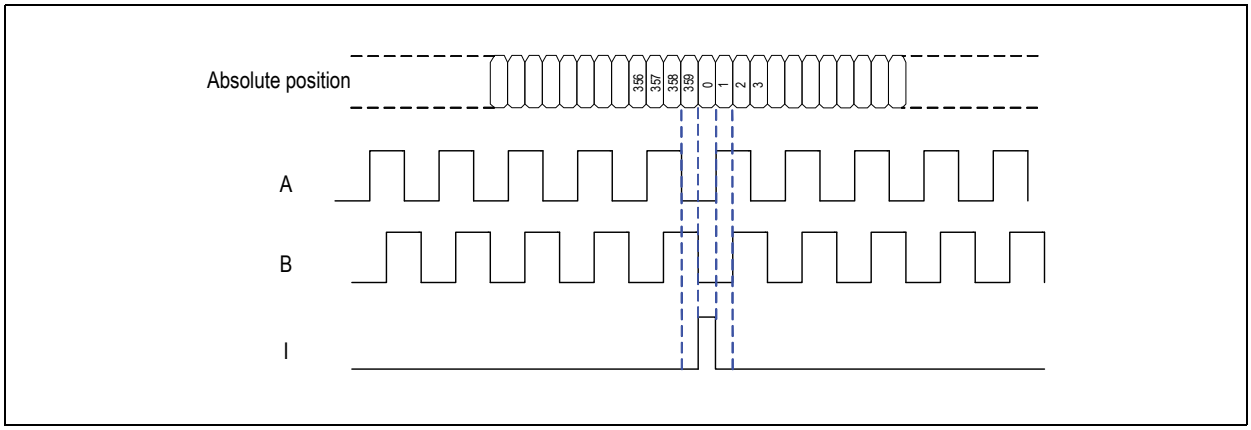


Figure 32 shows the two-channel quadrature output. The index position is mapped to the absolute mechanical zero position. The phase shift between channel A and B indicates the direction of the magnet movement. Channel A leads channel B at a clockwise rotation of the magnet (top view) by 90 electrical degrees. Channel B leads channel A at a counter-clockwise rotation.

Step Output Mode

Step Output mode provides a specific combination of the **A** incremental signal and the index signal **I**. The number of pulse can be configured with the input pattern of the test input pins.

Figure 33:
Step Mode of the AS5132 with Different Number of Pulses