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AS5145/AS5145-I10/AS5145-I12

DataSheet

12-Bit Programmable Magnetic Rotary Encoder

1 General Description

The AS5145 is a contact less magnetic rotary encoder for accurate angular measurement over a full turn of 360 degrees.
It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip, is required. The magnet may be placed above or below the IC.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 0.0879º = 4096 positions per revolution. This digital data is available as a serial bit stream and as a PWM signal.

An internal voltage regulator allows the AS5145 to operate at either 3.3V or 5V supplies.

Figure 1. Arrangement of AS5145 and Magnet

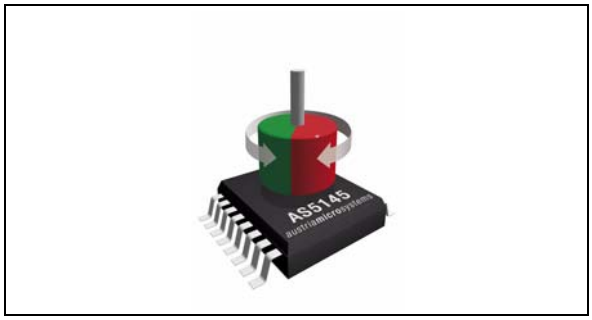


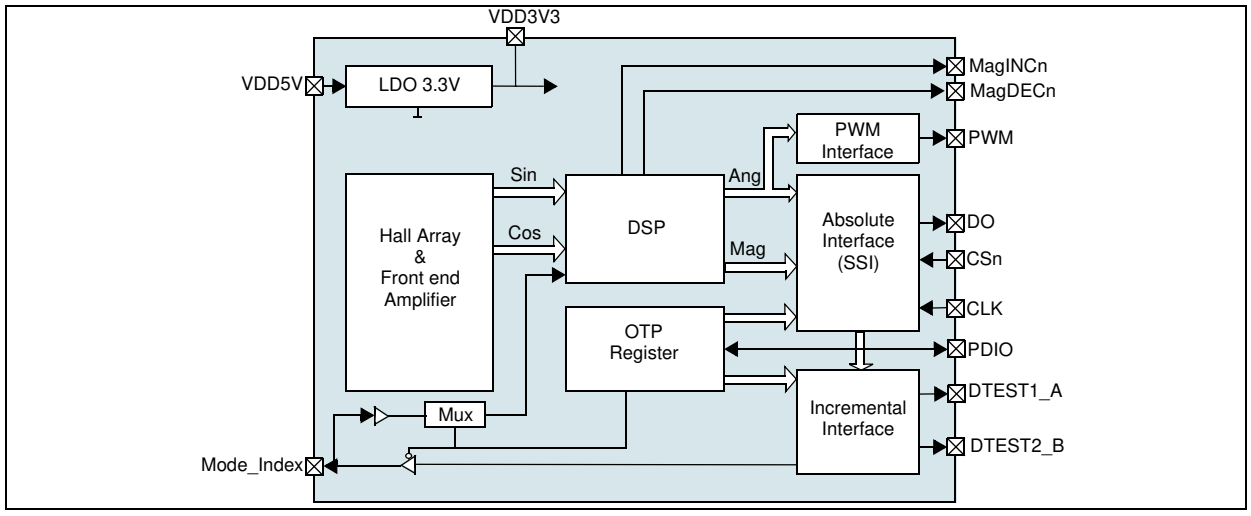
Figure 2. Block Diagram

2 Key Features

- Contact less high resolution rotational position encoding over a full turn of 360 degrees
- Two digital 12 bit absolute outputs:
  - Serial interface
  - Pulse width modulated (PWM) output
- Three incremental outputs
- Quadrature A/B (10 or 12-bit) and Index output signal (pre-programmed versions available AS5145-I10/AS5145-I12)
- User programmable zero position
- Failure detection mode for magnet placement, monitoring, and loss of power supply
- Red-Yellow-Green indicators display placement of magnet in Z-axis
- Serial read-out of multiple interconnected AS5145 devices using Daisy Chain mode
- Tolerant to magnet misalignment and gap variations
- Wide temperature range: - 40ºC to +150ºC
- Fully automotive qualified to AEC-Q100, grade 0
- Small Pb-free package: SSOP 16 (5.3mm x 6.2mm)

3 Applications

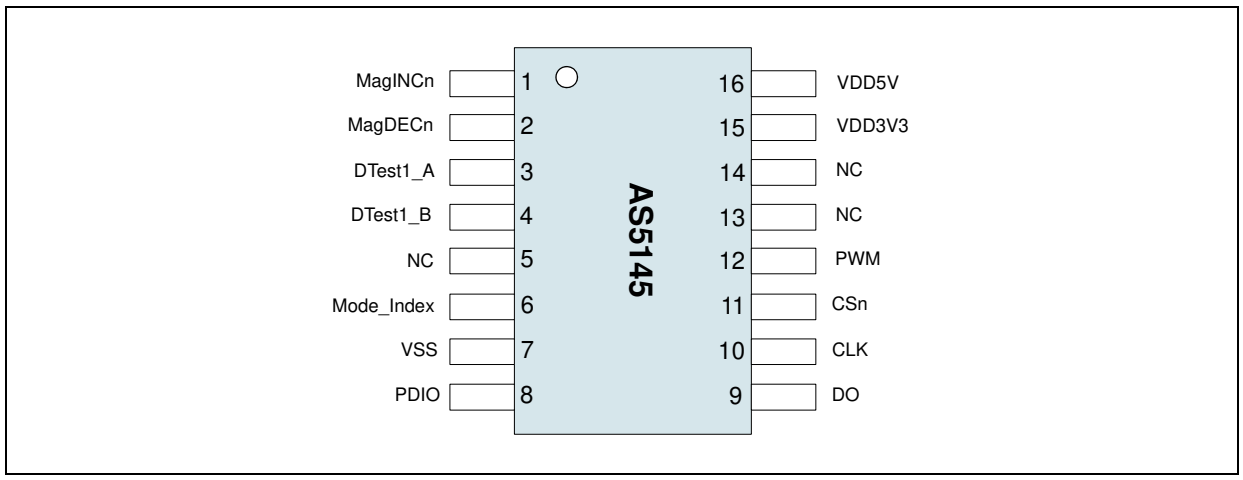
The device is ideal for industrial applications like contactless rotary position sensing and robotics; automotive applications like steering wheel position sensing, transmission gearbox encoder, head light position control, torque sensing, valve position sensing and replacement of high end potentiometers.



Contents

4 Pin Assignments

Figure 3. Pin Assignments (Top View)



Pin Description

The following SSOP16 shows the description of each pin of the standard SSOP16 package (Shrink Small Outline Package, 16 leads, body size: 5.3mm x 6.2mmm; (see Figure 3).

Table 1. Pin Description

Pin Number	Pin Name	Description
1	MagINCn	Magnet Field **Mag**nitude **INC**rease; active low, indicates a distance reduction between the magnet and the device surface. (see Table 9)
2	MagDECn	Magnet Field **Mag**nitude **DEC**rease; active low, indicates a distance increase between the device and the magnet. (see Table 9)
3	DTest1_A	Test output in default mode
4	DTest2_B	Test output in default mode
5	NC	Must be left unconnected
6	Mode_Index	Select between slow (open, low: VSS) and fast (high) mode. Internal pull-down resistor (~10kΩ).
7	VSS	Negative Supply Voltage (GND)
8	PDIO	OTP Programming Input and Data Input for Daisy Chain mode. Internal pull-down resistor (~74kΩ). Connect to VSS if not used
9	DO	**D**ata **O**utput of Synchronous Serial Interface
10	CLK	**Cl**o**ck** Input of Synchronous Serial Interface; Schmitt-Trigger input
11	CSn	**C**hip **S**elect, active low; Schmitt-Trigger input, internal pull-up resistor (~50kΩ)
12	PWM	**P**ulse **W**idth **M**odulation of approximately. 244Hz; 1µs/step (opt. 122Hz; 2µs/step)
13	NC	Must be left unconnected
14	NC	Must be left unconnected

Table 1. Pin Description

Pin Number	Pin Name	Description
15	VDD3V3	3V-Regulator Output, internally regulated from VDD5V. Connect to VDD5V for 3V supply voltage. Do not load externally.
16	VDD5V	Positive Supply Voltage, 3.0 to 5.5 V

Pin 1 and 2 are the magnetic field change indicators, MagINCn and MagDECn (magnetic field strength increase or decrease through variation of the distance between the magnet and the device). These outputs can be used to detect the valid magnetic field range. Furthermore those indicators can also be used for contact-less push-button functionality.

Pin 3 and 4 are multi function pins for sync mode, sin/cosine mode and incremental mode.

Pin 6 Mode_Index allows switching between filtered (slow) and unfiltered (fast mode). In incremental mode, the pin changes from input to output and provides the index pulse information. A change of the Mode during operation is not allowed. The setup must be constant during power up and during operation.

Pins 7, 15, and 16 are supply pins, pins 5, 13, and 14 are for internal use and must not be connected.

Pin 8 (PDIO) is used to program the zero-position into the OTP(see page 20). This pin is also used as digital input to shift serial data through the device in Daisy Chain configuration, (see page 15).

Pin 11 Chip Select (CSn; active low) selects a device within a network of AS5145 encoders and initiates serial data transfer. A logic high at CSn puts the data output pin (DO) to tri-state and terminates serial data transfer. This pin is also used for alignment mode (see Alignment Mode on page 23) and programming mode (see Programming the AS5145 on page 20).

Pin 12 allows a single wire output of the 12-bit absolute position value. The value is encoded into a pulse width modulated signal with 1µs pulse width per step (1µs to 4096µs over a full turn). By using an external low pass filter, the digital PWM signal is converted into an analog voltage, e.g. for making a direct replacement of potentiometers possible.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
DC supply voltage at pin VDD5V	-0.3	7	V	
DC supply voltage at pin VDD3V3		5	V	
Input pin voltage	-0.3	VDD5V +0.3	V	Except VDD3V3
Input current (latchup immunity)	-100	100	mA	Norm: EIA/JESD78 Class II Level A
Electrostatic discharge		± 2	kV	Norm: JESD22-A114E
Storage temperature	-55	125	ºC	Min – 67ºF; Max +257ºF
Package Body temperature		260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	

6 Electrical Characteristics

TAMB = -40 to +150ºC, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted.

Table 3. Electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating Conditions						
TAMB	Ambient temperature		-40		+150	ºC
I_{supp}	Supply current			16	21	mA
VDD5V	Supply voltage at pin VDD5V	5V Operation	4.5	5.0	5.5	V
VDD3V3	Voltage regulator output voltage at pin VDD3V3		3.0	3.3	3.6	
VDD5V	Supply voltage at pin VDD5V	3.3V Operation (pin VDD5V and VDD3V3 connected)	3.0	3.3	3.6	V
VDD3V3	Supply voltage at pin VDD3V3		3.0	3.3	3.6	
VON	Power-on reset thresholds On voltage; 300mV typ. hysteresis	DC supply voltage 3.3V (VDD3V3)	1,37	2.2	2.9	V
V_{off}	Power-on reset thresholds Off voltage; 300mV typ. hysteresis		1.08	1.9	2.6	
Programming Conditions						
V_{PROG}	Programming voltage	Voltage applied during programming	3.3		3.6	V
$V_{ProgOff}$	Programming voltage off level	Line must be discharged to this level	0		1	V
IPROG	Programming current	Current during programming			100	mA
$R_{programmed}$	Programmed fuse resistance (log 1)	10µA max. current @ 100mV	100k		∞	Ω
$R_{unprogrammed}$	Unprogrammed fuse resistance (log 0)	2mA max. current @ 100mV	50		100	Ω
DC Characteristics CMOS Schmitt-Trigger Inputs: CLK, CSn. (CSn = Internal Pull-up)						
VIH	High level input voltage	Normal operation	0.7 * VDD5V			V
VIL	Low level input voltage				0.3 * VDD5V	V
V_{Ion-} V_{Ioff}	Schmitt Trigger hysteresis		1			V
ILEAK	Input leakage current	CLK only	-1		1	µA
I_{iL}	Pull-up low level input current	CSn only, VDD5V: 5.0V	-30		-100	
DC Characteristics CMOS / Program Input: PDIO						
VIH	High level input voltage		0.7 * VDD5V		VDD5V	V
V_{PROG}[1]	High level input voltage	During programming	3.3		3.6	V
VIL	Low level input voltage				0.3 * VDD5V	V
I_{iL}	High level input current	VDD5V: 5.5V	30		100	µA
DC Characteristics CMOS Output Open Drain: MagINCn, MagDECn						
I_{OZ}	Open drain leakage current				1	µA
VOL	Low level output voltage				VSS + 0.4	V

Table 3. Electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_O	Output current	$V_{DD}5V$: 4.5V			4	mA
		$V_{DD}5V$: 3V			2	
DC Characteristics CMOS Output: PWM						
V_{OH}	High level output voltage		$V_{DD}5V$ – 0.5			V
V_{OL}	Low level output voltage			VSS +0.4		V
I_O	Output current	$V_{DD}5V$: 4.5V		4		mA
		$V_{DD}5V$: 3V		2		
DC Characteristics CMOS Output: A, B, Index						
V_{OH}	High level output voltage		$V_{DD}5V$ – 0.5			V
V_{OL}	Low level output voltage			VSS +0.4		V
I_O	Output current	$V_{DD}5V$: 4.5V		4		mA
		$V_{DD}5V$: 3V		2		
DC Characteristics Tri-state CMOS Output: DO						
V_{OH}	High level output voltage		$V_{DD}5V$ – 0.5			V
V_{OL}	Low level output voltage			VSS +0.4		V
I_O	Output current	$V_{DD}5V$: 4.5V		4		mA
		$V_{DD}5V$: 3V		2		
I_{OZ}	Tri-state leakage current			1		µA

1. Either with 3.3V or 5V supply.

Magnetic Input Specification

operating conditions: T_{AMB} = -40 to +150°C, $V_{DD}5V$ = 3.0 to 3.6V (3V operation) $V_{DD}5V$ = 4.5 to 5.5V (5V operation) unless otherwise noted.

Two-pole cylindrical diametrically magnetized source:

Table 4. Magnetic Input Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
d_{mag}	Diameter	Recommended magnet: Ø 6mm x 2.5mm for cylindrical magnets	4	6		mm
t_{mag}	Thickness		2.5			mm
B_{pk}	Magnetic input field amplitude	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm	45		75	mT
B_{off}	Magnetic offset	Constant magnetic stray field			± 10	mT
	Field non-linearity	Including offset gradient			5	%

Table 4. Magnetic Input Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{mag_abs}	Input frequency (rotational speed of magnet)	153 rpm @ 4096 positions/rev; fast mode			2.54	Hz
		38 rpm @ 4096 positions/rev; slow mode			0.63	
Disp	Displacement radius	Max. offset between defined device center and magnet axis (see Figure 18)			0.25	mm
Ecc	Eccentricity	Eccentricity of magnet center to rotational axis			100	µm
	Recommended magnet material and temperature drift	NdFeB (Neodymium Iron Boron)		-0.12		%/K
		SmCo (Samarium Cobalt)		-0.035		

System Specifications

operating conditions: TAMB = -40 to +150°C, VDD5V = 3.0 to 3.6V (3V operation) VDD5V = 4.5 to 5.5V (5V operation) unless otherwise noted.

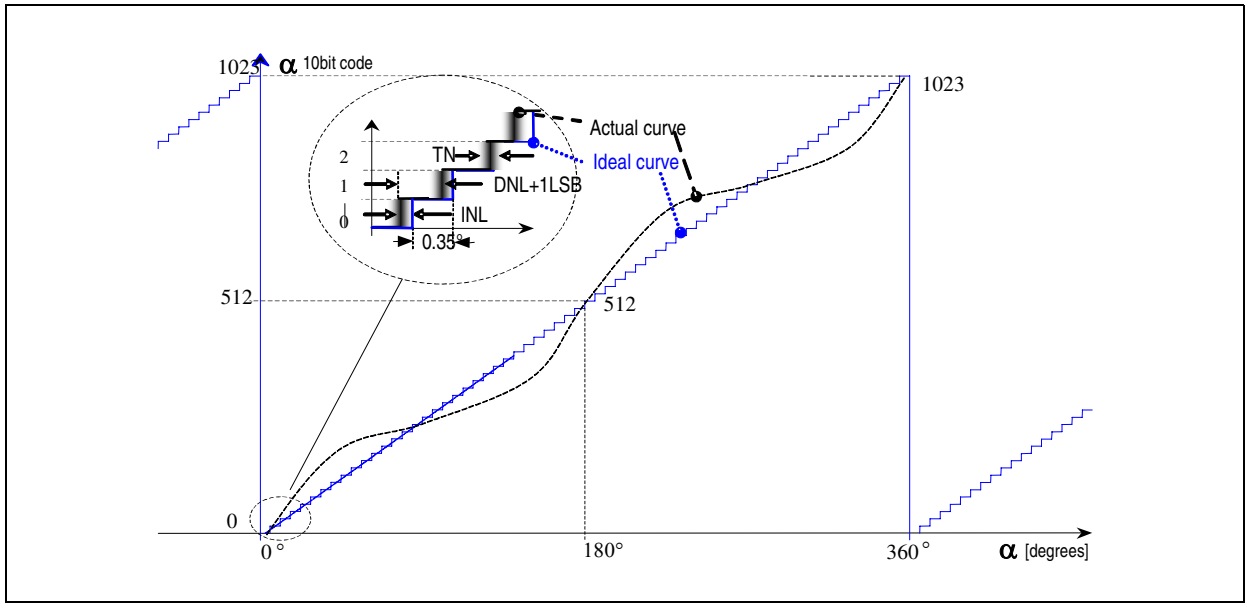
Table 5. Input Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
RES	Resolution	0.088 deg			12	bit
INL_{opt}	Integral non-linearity (optimum)	Maximum error with respect to the best line fit. Centered magnet without calibration, TAMB =25 ºC.			± 0.5	deg
INL_{temp}	Integral non-linearity (optimum)	Maximum error with respect to the best line fit. Centered magnet without calibration, TAMB = -40 to +150ºC			± 0.9	deg
INL	Integral non-linearity	Best line fit = (Err_{max} – Err_{min}) / 2 Over displacement tolerance with 6mm diameter magnet, without calibration, TAMB = -40 to +150ºC			± 1.4	deg
DNL	Differential non-linearity	12bit, no missing codes			± 0.044	deg
TN	Transition noise	1 sigma, fast mode (MODE = 1)			0.06	Deg RMS
		1 sigma, slow mode (MODE = 0 or open)			0.03	
t_{PwrUp}	Power-up time	Fast mode (Mode = 1); Until status bit OCF = 1			20	ms
		Slow mode (Mode = 0 or open); Until OCF = 1			80	
t_{delay}	System propagation delay absolute output : delay of ADC, DSP and absolute interface	Fast mode (MODE = 1)			96	µs
		Slow mode (MODE = 0 or open)			384	
f_S	Internal sampling rate for absolute output:	TAMB = 25ºC, slow mode (MODE=0 or open)	2.48	2.61	2.74	kHz
		TAMB = -40 to +150ºC, slow mode (MODE=0 or open)	2.35	2.61	2.87	

Table 5. Input Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_S	Internal sampling rate for absolute output	T_{AMB} = 25ºC, fast mode (MODE = 1)	9.90	10.42	10.94	kHz
		T_{AMB} = -40 to +150ºC, fast mode (MODE=1)	9.38	10.42	11.46	
CLK/ SEL	Read-out frequency	Max. clock frequency to read out serial data			1	MHz

Figure 4. Integral and Differential Non-Linearity Example



Integral Non-Linearity (INL) is the maximum deviation between actual position and indicated position.

Differential Non-Linearity (DNL) is the maximum deviation of the step length from one position to the next. Transition Noise (TN) is the repeatability of an indicated position.

7 Timing Characteristics

T_{AMB} = -40 to +150 ºC, $V_{DD}5V$ = 3.0 to 3.6V (3V operation) $V_{DD}5V$ = 4.5 to 5.5V (5V operation), unless otherwise noted.

Table 6. Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Synchronous Serial Interface (SSI)						
$t_{DOactive}$	Data output activated (logic high)	Time between falling edge of CSn and data output activated			100	ns
t_{CLKFE}	First data shifted to output register	Time between falling edge of CSn and first falling edge of CLK	500			ns
$T_{CLK/2}$	Start of data output	Rising edge of CLK shifts out one bit at a time	500			ns
$t_{DOvalid}$	Data output valid	Time between rising edge of CLK and data output valid			413	ns
$t_{DOtristate}$	Data output tri-state	After the last bit DO changes back to “tri-state”			100	ns
t_{CSn}	Pulse width of CSn	CSn =high; To initiate read-out of next angular position	500			ns
f_{CLK}	Read-out frequency	Clock frequency to read out serial data	>0		1	MHz
Pulse Width Modulation Output						
f_{PWM}	PWM frequency	Signal period = 4098µs ±5% at T_{AMB} = 25ºC	232	244	256	Hz
		Signal period = 4098µs ±10% at T_{AMB} = -40 to +150ºC	220	244	268	
PW_{MIN}	Minimum pulse width	Position 0d; angle 0 degree	0.90	1	1.10	µs
PW_{MAX}	Maximum pulse width	Position 4098d; angle 359.91 degrees	3686	4096	4506	µs
Programming Conditions						
t_{PROG}	Programming time per bit	Time to prog. a singe fuse bit	10		20	µs
t_{CHARGE}	Refresh time per bit	Time to charge the cap after t_{PROG}	1			µs
f_{LOAD}	LOAD frequency	Data can be loaded at n x 2µs			500	kHz
f_{READ}	READ frequency	Read the data from the latch			2.5	MHz
f_{WRITE}	WRITE frequency	Write the data to the latch			2.5	MHz

8 Detail Description

The AS5145 is manufactured in a CMOS standard process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip.

The integrated Hall elements are placed around the center of the device and deliver a voltage representation of the magnetic field at the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5145 provides accurate high-resolution absolute angular position information. For this purpose a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals.

The DSP is also used to provide digital information at the outputs MagINCn and MagDECn that indicate movements of the used magnet towards or away from the device's surface. A small low cost diametrically magnetized (two-pole) standard magnet provides the angular position information (see Figure 17).

The AS5145 senses the orientation of the magnetic field and calculates a 12-bit binary code. This code can be accessed via a Synchronous Serial Interface (SSI). In addition, an absolute angular representation is given by a Pulse Width Modulated signal at pin 12 (PWM). This PWM signal output also allows the generation of a direct proportional analog voltage, by using an external Low-Pass-Filter.

The AS5145 is tolerant to magnet misalignment and magnetic stray fields due to differential measurement technique and Hall sensor conditioning circuitry.

Mode_Index Pin

The Mode_Index pin activates or deactivates an internal filter, that is used to reduce the analog output noise.

Activating the filter (Mode pin = LOW or open) provides a reduced output noise of 0.03º rms. At the same time, the output delay is increased to 384µs. This mode is recommended for high precision, low speed applications.

Deactivating the filter (Mode pin = HIGH) reduces the output delay to 96µs and provides an output noise of 0.06º rms. This mode is recommended for higher speed applications.

Setup the Mode pin affects the following parameters:

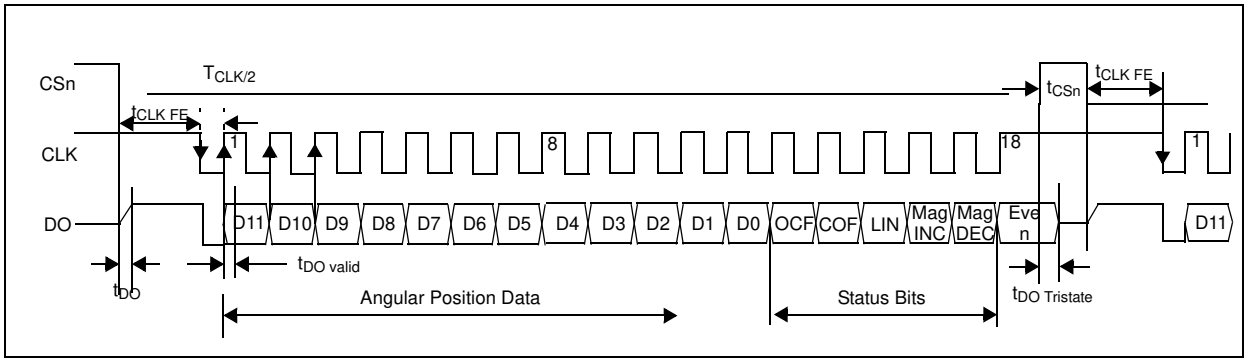
Table 7. Slow and fast mode parameters

Parameter	Slow Mode (mode= low or open)	Fast Mode (mode=high, V_{DD}= 5V)
sampling rate	2.61 kHz (384 µs)	10.42 kHz (96µs)
transition noise (1 sigma)	≤ 0.03º rms	≤ 0.06º rms
output delay	384µs	96µs
max. speed @ 4096 samples/rev	38 rpm	153 rpm
max. speed @ 1024 samples/rev	153 rpm	610 rpm
max. speed @ 256 samples/rev	610 rpm	2441 rpm
max. speed @ 64 samples/rev	2441 rpm	9766 rpm

Note: A change of the Mode during operation is not allowed. The setup must be constant during power up and during operation.

Synchronous Serial Interface (SSI)

Figure 5. Synchronous serial interface with absolute angular position data



If CSn changes to logic low, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out will be initiated.

- After a minimum time $t_{CLK\ FE}$, data is latched into the output shift register with the first falling edge of CLK.
- Each subsequent rising CLK edge shifts out one bit of data.
- The serial word contains 18 bits, the first 12 bits are the angular information D[11:0], the subsequent 6 bits contain system information, about the validity of data such as OCF, COF, LIN, Parity and Magnetic Field status (increase/ decrease).
- A subsequent measurement is initiated by a “high” pulse at CSn with a minimum duration of tCSn.

Data Content

D11:D0 absolute angular position data (MSB is clocked out first)

OCF (Offset Compensation Finished), logic high indicates the finished Offset Compensation Algorithm

COF (Cordic Overflow), logic high indicates an out of range error in the CORDIC part. When this bit is set, the data at D11:D0 is invalid. The absolute output maintains the last valid angular value.

This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

LIN (Linearity Alarm), logic high indicates that the input field generates a critical output linearity.
When this bit is set, the data at D11:D0 may still be used, but can contain invalid data. This warning may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

Even Parity bit for transmission error detection of bits 1…17 (D11…D0, OCF, COF, LIN, MagINC, MagDEC)

Placing the magnet above the chip, angular values increase in clockwise direction by default.

Data D11:D0 is valid, when the status bits have the following configurations:

Table 8. Status Bit Outputs

OCF	COF	LIN	Mag INC	Mag DEC	Parity
1	0	0	0	0	Even checksum of bits 1:15
			0	1	
			1	0	
			1	1	

Note: MagInc=MagDec=1 is only recommended in YELLOW mode (see Table 9)

Z-axis Range Indication (Push Button Feature, Red/Yellow/Green Indicator)

The AS5145 provides several options of detecting movement and distance of the magnet in the Z-direction. Signal indicators MagINCn and MagDECn are available both as hardware pins (pins #1 and 2) and as status bits in the serial data stream (see Figure 5).

In the default state, the status bits MagINC, MagDec and pins MagINCn, MagDECn have the following function:

Table 9. Magnetic field strength red-yellow-green indicator

Status Bits			Hardware Pins		OPT: Mag CompEn = 1 (Red-Yellow-Green)
Mac INC	**Mag DEC**	**LIN**	**Mac INCn**	**Mag DECn**	**Description**
0	0	0	Off	Off	No distance change Magnetic input field OK (GREEN range, ~45…75mT)
1	1	0	On	Off	YELLOW range: magnetic field is ~ 25…45mT or ~75…135mT. The AS5145 may still be operated in this range, but with slightly reduced accuracy.
1	1	1	On	On	RED range: magnetic field is ~<25mT or >~135mT. It is still possible to operate the AS5145 in the red range, but not recommended.
All other combinations			n/a	n/a	Not available

Note: Pin 1 (MagINCn) and pin 2 (MagDECn) are active low via open drain output and require an external pull-up resistor. If the magnetic field is in range, both outputs are turned off.

The two pins may also be combined with a single pull-up resistor. In this case, the signal is high when the magnetic field is in range. It is low in all other cases (see Table 9).

Incremental Mode

The AS5145 has an internal interpolator block. This function is used if the input magnetic field is to fast and a code position is missing. In this case an interpolation is done.

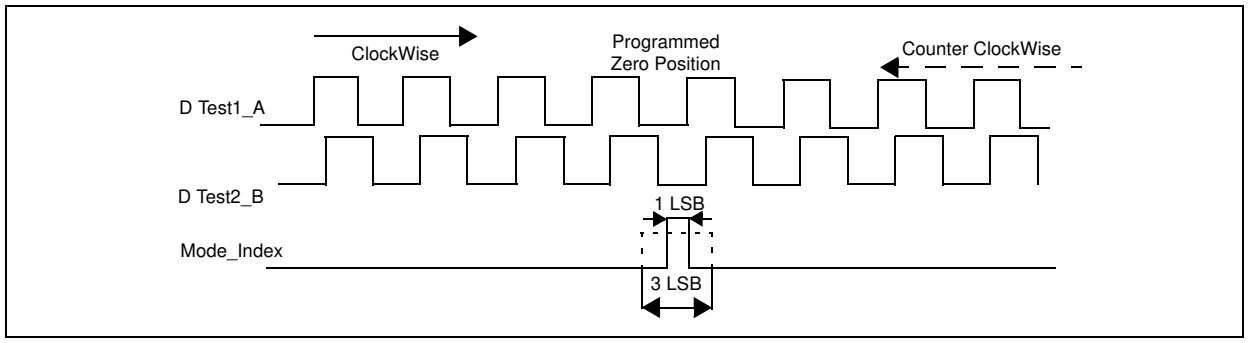
With the OTP bits OutputMd0 and OutputMd1 a specific mode can be selected. For the available pre-programmed incremental versions (10bit and 12bit), these bits are set during test at austriamicrosystems. These settings are permanent and can not be recovered.

A change of the incremental mode (WRITE command) during operation could cause problems. A power-on-reset in between is recommended. During operation in incremental mode it is recommended setting CSn = High, to disable the SSI-Interface.

Table 10. Incremental Resolution

Mode	Description	Output Md1	Output Md0	Resolution	DTest1_A and DTest2_B Pulses	Index Width
Default mode	AS5145 function **DTEST1_A** and **DTEST2_B** are not used. The **Mode_Index** pin is used for selection of the decimation rate (low speed/high speed).	0	0			
10 bit Incremental mode (low DNL)	**DTEST1_A** and **DTEST2_B** are used as **A** and **B** signal. In this mode the **Mode_Index** Pin is switched from input to output and will be the **Index** Pin. The decimation rate is set to 64 (fast mode) and cannot be changed from external.	0	1	10	256	1/3 LSB
12 bit Incremental mode (high DNL)		1	0	12	1024	
Sync mode	In this mode a control signal is switched to **DTEST1_A** and **DTEST2_B**.	1	1			

Figure 6. Incremental Output

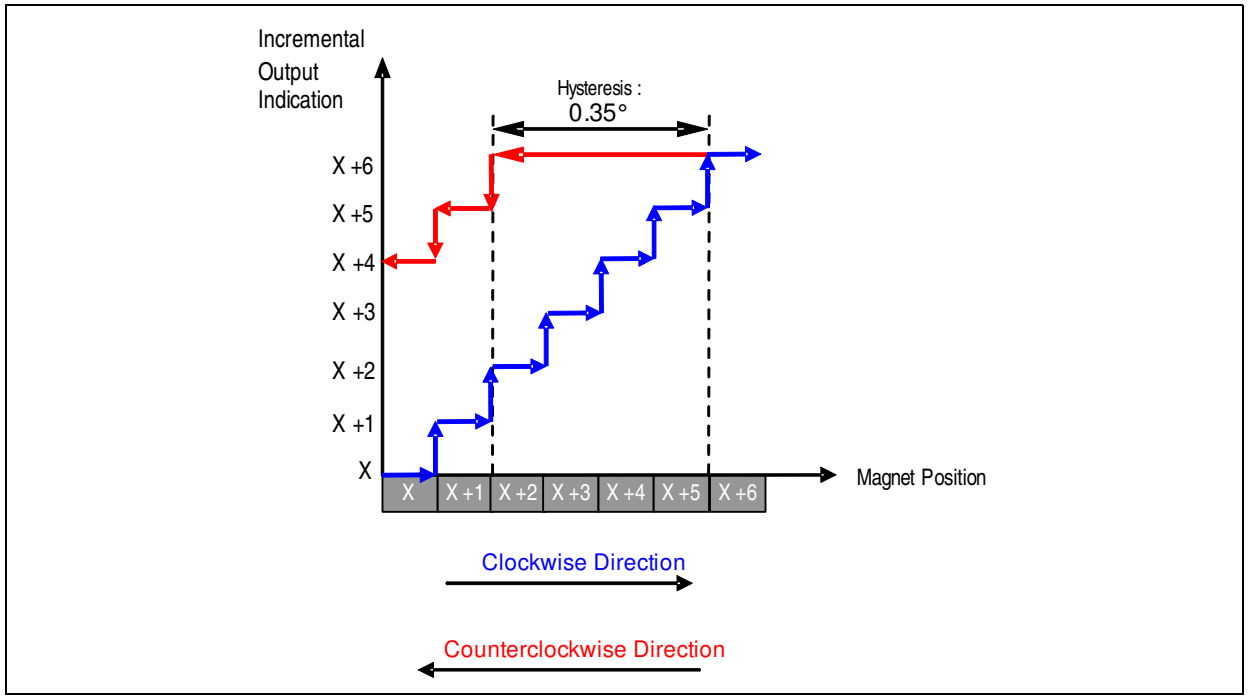


The hysteresis trimming is done at the final test (factory trimming) and set to 4 LSB, related to a 12 bit number.

Incremental Output Hysteresis

To avoid flickering incremental outputs at a stationary magnet position, a hysteresis is introduced. In case of a rotational direction change, the incremental outputs have a hysteresis of 4 LSB. Regardless of the programmed incremental resolution, the hysteresis of 4 LSB always corresponds to the highest resolution of 12 bit. In absolute terms, the hysteresis is set to 0.35 degrees for all resolutions. For constant rotational directions, every magnet position change is indicated at the incremental outputs (see Figure 7). For example, if the magnet turns clockwise from position “x+3“ to “x+4“, the incremental output would also indicate this position accordingly. A change of the magnet’s rotational direction back to position “x+3“ means that the incremental output still remains unchanged for the duration of 4 LSB, until position “x+2“is reached. Following this direction, the incremental outputs will again be updated with every change of the magnet position.

Figure 7. Hysteresis Window for Incremental Outputs



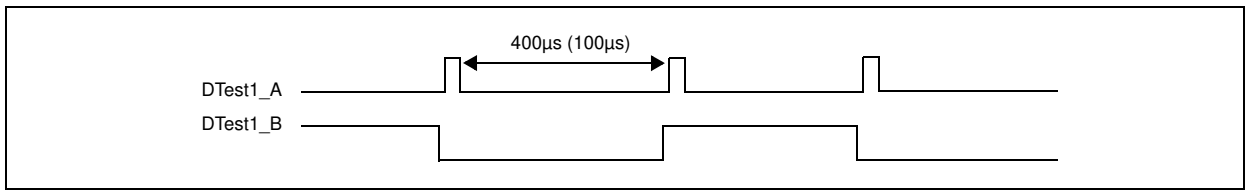
Incremental Output Validity

During power on the incremental output is kept stable high until the offset compensation is finished and the CSn is low (internal Pull Up) the first time. In quadrature mode A = B = Index = high indicates an invalid output. If the interpolator recognizes a difference larger than 128 steps between two samples it holds the last valid state. The interpolator synchronizes up again with the next valid difference. This avoids undefined output burst, e.g. if no magnet is present.

Sync Mode

This mode is used to synchronize the external electronic with the AS5145. In this mode two signals are provided at the pins DTEST1_A and DTEST2_B. By setting of Md0=1 and Md1=1 in the OTP register, the Sync Mode will be activated.

Figure 8. DTest1_A and DTest2_B



Every rising edge at DTEST1_A indicates that new data in the device is available. With this signal it is possible to trigger an external customer Microcontroller (interrupt) and start the SSI readout. DTEST2_B indicates the phase of available data.

Sin/Cosine Mode

This mode can be enabled by setting the OTP Factory-bit FS2. If this mode is activated the 16 bit sinus and 16 bit cosines digital data of both channels will be switched out. Due to the high resolution of 16 bits of the data stream an accurate calculation can be done externally. In this mode the open drain outputs of DTEST1_A and DTEST2_B are switched to push-pull mode. At Pin MagDECn the clock impulse, at Pin MagINCn the Enable pulse will be switched out. The Pin PWM indicates, which phase of signal is being presented. The mode isn't available in the default mode.

Daisy Chain Mode

The Daisy Chain mode allows connection of several AS5145's in series, while still keeping just one digital input for data transfer (see "Data IN" in Figure 9). This mode is accomplished by connecting the data output (DO; pin 9) to the data input (PDIO; pin 8) of the subsequent device. The serial data of all connected devices is read from the DO pin of the first device in the chain. The length of the serial bit stream increases with every connected device, it is n * (18+1) bits: n= number of devices. e.g. 38 bit for two devices, 57 bit for three devices, etc.

The last data bit of the first device (Parity) is followed by a dummy bit and the first data bit of the second device (D11), etc. see Figure 10

Figure 9. Daisy Chain hardware configuration

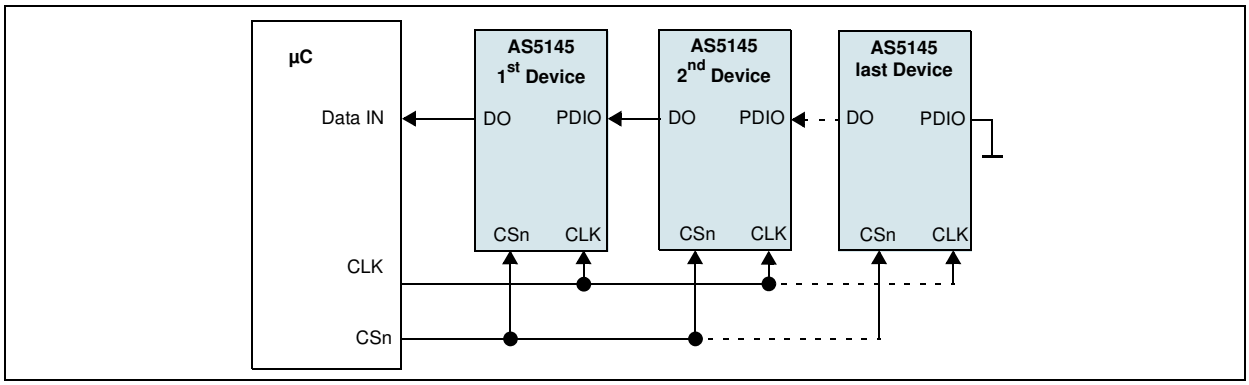
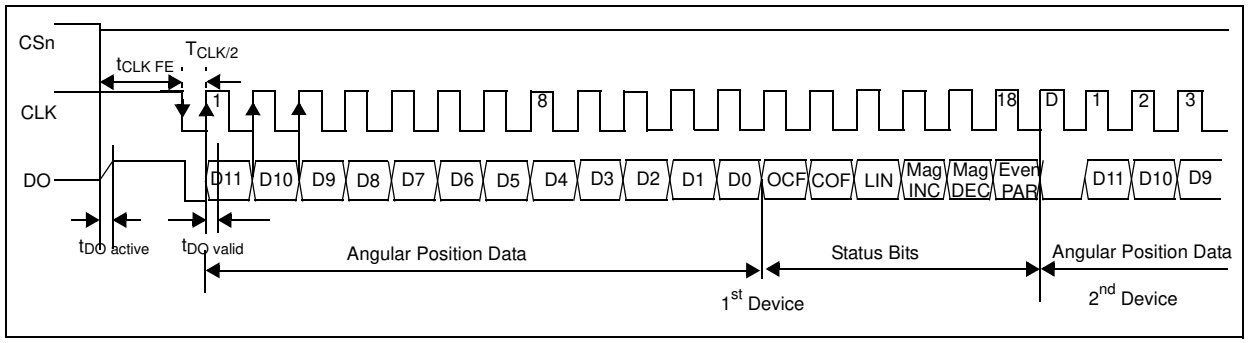


Figure 10. Daisy Chain mode data transfer



Pulse Width Modulation (PWM) Output

The AS5145 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle. For angle position 0 to 4094

$$Position = \frac{t_{on} \cdot 4098}{(t_{on} + t_{off})} - 1 \qquad (EQ\ 1)$$

Examples:

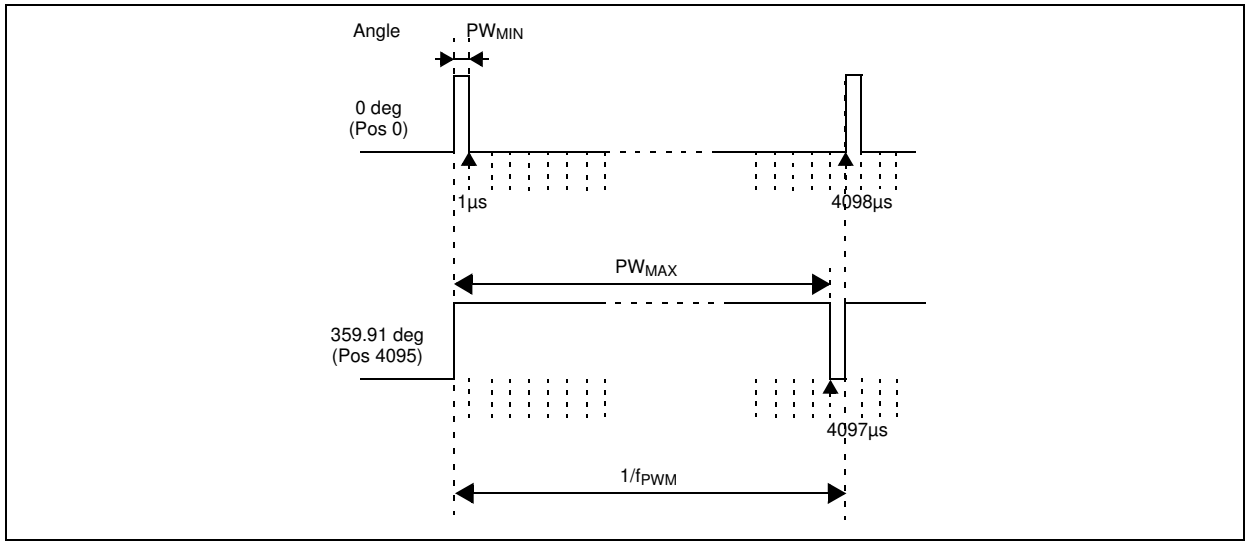
1. An angle position of 180° will generate a pulse width ton = 2049µs and a pause toff of 2049 µs resulting in Position = 2048 after the calculation: 2049 * 4098 / (2049 + 2049) -1 = 2048
2. An angle position of 359.8° will generate a pulse width ton = 4095µs and a pause toff of 3 µs resulting in Position = 4094 after the calculation: 4095 * 4098 / (4095 + 3) -1 = 4094

Exception:

1. An angle position of 359.9° will generate a pulse width ton = 4097µs and a pause toff of 1 µs resulting in Position = 4096 after the calculation: 4097 * 4098 / (4097 + 1) -1 = 4096

The PWM frequency is internally trimmed to an accuracy of ±5% (±10% over full temperature range). This tolerance can be cancelled by measuring the complete duty cycle as shown above.

Figure 11. PWM output signal



Changing the PWM Frequency

The PWM frequency of the AS5145 can be divided by two by setting a bit (PWMhalfEN) in the OTP register (see Programming the AS5145 on page 20). With PWMhalfEN = 0 the PWM timing is as shown in Table 11:

Table 11. PWM signal parameters (default mode)

Symbol	Parameter	Typ	Unit	Note
f_{PWM}	PWM frequency	244	Hz	Signal period: 4097µs
PW_{MIN}	MIN pulse width	1	µs	- Position 0d - Angle 0 deg
PW_{MAX}	MAX pulse width	4097	µs	- Position 4095d - Angle 359.91 deg

When PWMhalfEN = 1, the PWM timing is as shown in Table 12:

Table 12. PWM signal parameters with half frequency (OTP option)

Symbol	Parameter	Typ	Unit	Note
f_{PWM}	PWM frequency	122	Hz	Signal period: 8194µs
PW_{MIN}	MIN pulse width	2	µs	- Position 0d - Angle 0 deg
PW_{MAX}	MAX pulse width	8194	µs	- Position 4095d - Angle 359.91 deg

Analog Output

An analog output can be generated by averaging the PWM signal, using an external active or passive low pass filter. The analog output voltage is proportional to the angle: 0º= 0V; 360º = V_{DD}5V.

Using this method, the AS5145 can be used as direct replacement of potentiometers.

Figure 11: Simple 2nd order passive RC low pass filter

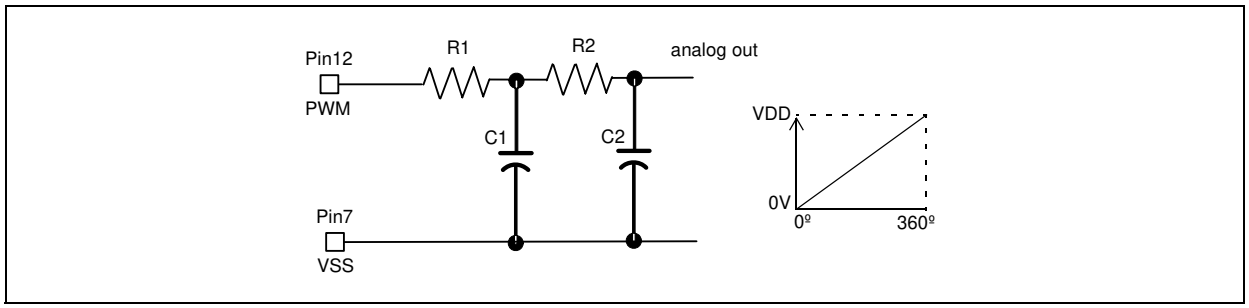


Figure 11 shows an example of a simple passive low pass filter to generate the analog output.

$$R1,R2 \geq 10k\Omega \qquad C1,C2 \geq 2.2\mu F / 6V \qquad \text{(EQ 2)}$$

R1 should be greater than or equal to 4k7 to avoid loading of the PWM output. Larger values of Rx and Cx will provide better filtering and less ripple, but will also slow down the response time.

9 Application Information

Programming the AS5145

After power-on, programming the AS5145 is enabled with the rising edge of CSn with PDIO = high and CLK = low.

The AS5145 programming is a one-time-programming (OTP) method, based on poly silicon fuses. The advantage of this method is that a programming voltage of only 3.3V to 3.6V is required for programming (either with 3.3V or 5V supply).

The OTP consists of 52 bits, of which 21 bits are available for user programming. The remaining 31 bits contain factory settings and a unique chip identifier (Chip-ID).

A single OTP cell can be programmed only once. Per default, the cell is “0”; a programmed cell will contain a “1”. While it is not possible to reset a programmed bit from “1” to “0”, multiple OTP writes are possible, as long as only unprogrammed “0”-bits are programmed to “1”.

Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command at any time. This setting will be cleared and overwritten with the hard programmed OTP settings at each power-up sequence or by a LOAD operation. Use application note AN514X_10 to get more information about the programming options.

The OTP memory can be accessed in the following ways:

- **Load Operation:** The Load operation reads the OTP fuses and loads the contents into the OTP register. A Load operation is automatically executed after each power-on-reset.
- **Write Operation:** The Write operation allows a temporary modification of the OTP register. It does not program the OTP. This operation can be invoked multiple times and will remain set while the chip is supplied with power and while the OTP register is not modified with another Write or Load operation.
- **Read Operation:** The Read operation reads the contents of the OTP register, for example to verify a Write command or to read the OTP memory after a Load command.
- **Program Operation:** The Program operation writes the contents of the OTP register permanently into the OTP ROM.
- **Analog Readback Operation:** The Analog Readback operation allows a quantifiable verification of the programming. For each programmed or unprogrammed bit, there is a representative analog value (in essence, a resistor value) that is read to verify whether a bit has been successfully programmed or not.

Zero Position Programming

Zero position programming is an OTP option that simplifies assembly of a system, as the magnet does not need to be manually adjusted to the mechanical zero position. Once the assembly is completed, the mechanical and electrical zero positions can be matched by software. Any position within a full turn can be defined as the permanent new zero position.

For zero position programming, the magnet is turned to the mechanical zero position (e.g. the “off”-position of a rotary switch) and the actual angular value is read.

This value is written into the OTP register bits Z35:Z46 (see Figure 12).

Note: The zero position value may also be modified before programming, e.g. to program an electrical zero position that is 180º (half turn) from the mechanical zero position, just add 2048 to the value read at the mechanical zero position and program the new value into the OTP register.

OTP Memory Assignment

Table 13. OTP Bit Assignment

Bit	Symbol	Function	
	mbit1	Factory Bit 1	
51	PWMhalfEN_Index width	PMW frequency Index pulse width	Customer Section
50	MagCompEn	Alarm mode (programmed by austriamicrosystems to 1)	
49	pwmDIS	Disable PWM	
48	Output Md0	Default, 10 bit inc, 12 bit inc Sync mode	
47	Output Md1		
46	Z0	12 bit Zero Position	
:	:		
35	Z11		
34	CCW	Direction	
33	RA0	Redundancy Address	
:	:		
29	RA4		
28	FS 0	Factory Bit	Factory Section
27	FS 1		
26	FS 2		
25	FS 3		
24	FS 4		
23	FS 5		
:	:		
20	FS 8		
19	FS 9		
18	FS 10		
17	ChipID0	18 bit Chip ID	ID Section
16	ChipID1		
:	:		
0	ChipID17		
	mbit0	Factory Bit 0	

User selectable settings

The AS5145 allows programming of the following user selectable options:

- **PWMhalfEN_Indexwidth**: Setting this bit, the PWM pulse will be divided by 2, in case of quadrature incremental mode A/B/Index setting of Index impulse width from 1 LSB to 3LSB
- **Output Md0:** Setting this bit enables sync- or 10bit incrememantal mode (see Table 10).
- **Output Md1:** Setting this bit enables sync- or 12bit incrememantal mode (see Table 10).
- **Z [11:0]:** Programmable Zero / Index Position

- **CCW:** Counter Clockwise Bit
  ccw=0 – angular value increases in clockwise direction
  ccw=1 – angular value increases in counterclockwise direction
- **RA [4:0]:** Redundant Address: an OTP bit location addressed by this address is always set to “1” independent of the corresponding original OTP bit setting

OTP Default Setting

The AS5145 can also be operated without programming. The default, un-programmed setting is:

- **Output Md0, Output MD1:** 00= Default mode
- **Z0 to Z11:** 00 = no programmed zero position
- **CCW:** 0 = clockwise operation
- **RA4 to RA0:**0 = no OTP bit is selected
- **MagCompEN:** 1 = The green/yellow Mode is enabled

Redundancy

For a better programming reliability a redundancy is implemented. In case when the programming of one bit failed this function can be used. With an address RA(4:0) one bit can be selected and programmed.

Table 14. Redundancy addressing

Address	PWMhalfEN_Indexwidth	MagCompEN	pwmDIS	Output Md0	Output Md1	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	Z9	Z10	Z11	CCW
00000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00001	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00010	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00011	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00100	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00101	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
00110	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
00111	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
01000	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
01001	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
01010	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
01011	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
01100	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
01101	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
01110	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
01111	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
10000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
10001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
10010	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
10101	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

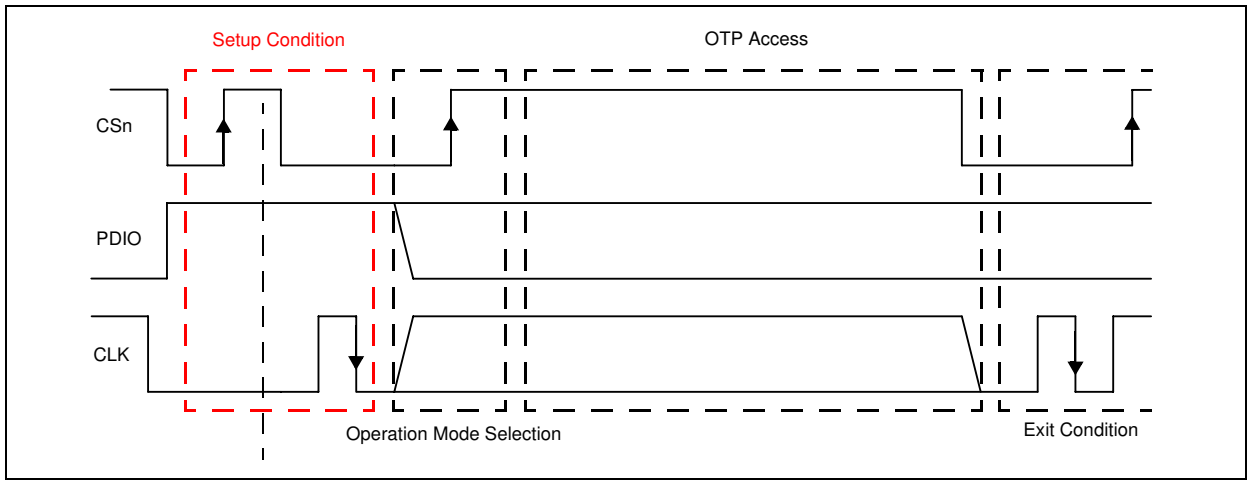
Redundant programming option

In addition to the regular programming, a redundant programming option is available. This option allows that one selectable OTP bit can be set to “1” (programmed state) by writing the location of that bit into a 5-bit address decoder. This address can be stored in bits RA4..RA0 in the OTP user settings.

Example: setting RA4…0 to “00001” will select bit 51 = PWhalfEN_Indexwidth, “00010” selects bit 50 = MagCompEN, “10010” selects bit 34 =CCW, etc.

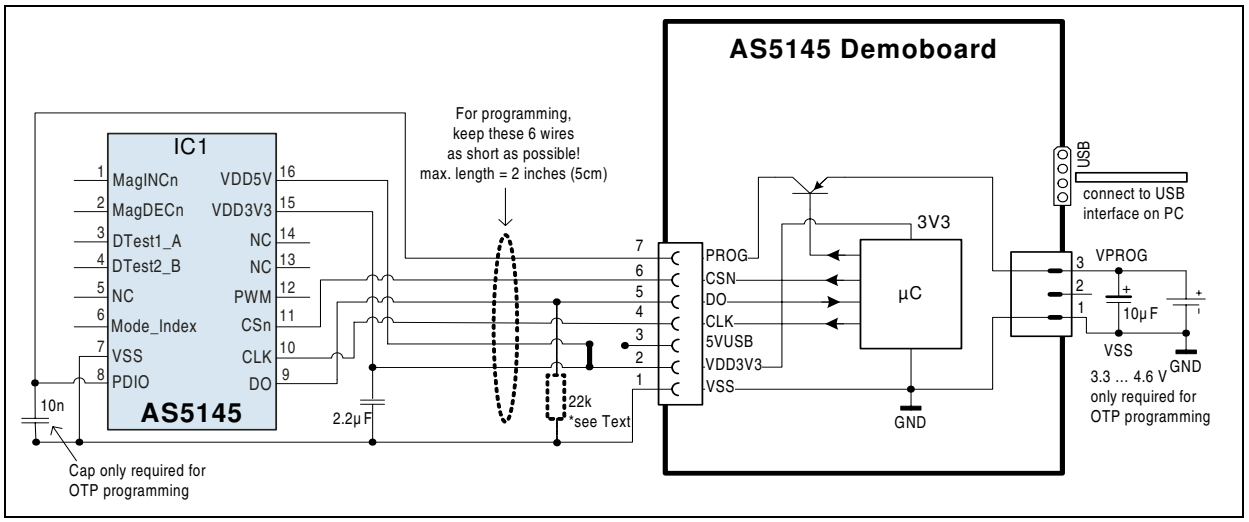
OTP register entry and exit condition

Figure 12. OTP access timing diagram



To avoid accidental modification of the OTP during normal operation, each OTP access (Load, Write, Read, Program) requires a defined entry and exit procedure, using the CSn, PDIO and CLK signals as shown in Figure 12.

Figure 13. OTP programming connection



Alignment Mode

The alignment mode simplifies centering the magnet over the center of the chip to gain maximum accuracy.

Alignment mode can be enabled with the falling edge of CSn while PDIO = logic high (see Figure 14). The Data bits D11-D0 of the SSI change to a 12-bit displacement amplitude output. A high value indicates large X or Y displacement, but also higher absolute magnetic field strength. The magnet is properly aligned, when the difference between highest and lowest value over one full turn is at a minimum.

Under normal conditions, a properly aligned magnet will result in a reading of less than 128 over a full turn. The MagINCn and MagDECn indicators will be = 1 when the alignment mode reading is < 128. At the same time, both hardware pins MagINCn (#1) and MagDECn (#2) will be pulled to VSS. A properly aligned magnet will therefore produce a MagINCn = MagDECn = 1 signal throughout a full 360º turn of the magnet.

Stronger magnets or short gaps between magnet and IC may show values larger than 128. These magnets are still properly aligned as long as the difference between highest and lowest value over one full turn is at a minimum.

The Alignment mode can be reset to normal operation by a power-on-reset (disconnect / re-connect power supply) or by a falling edge on CSn with PDIO = low.

Figure 14. Enabling the alignment mode

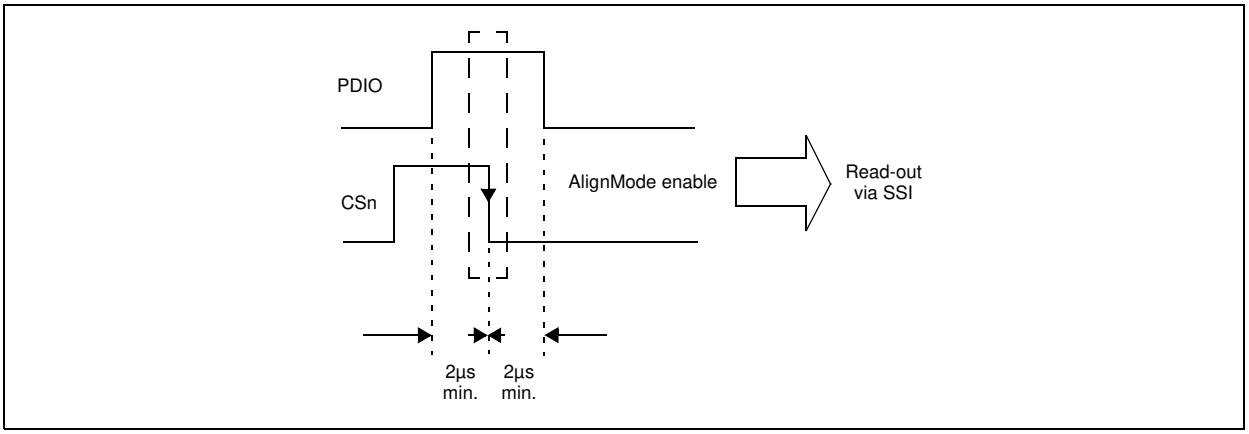
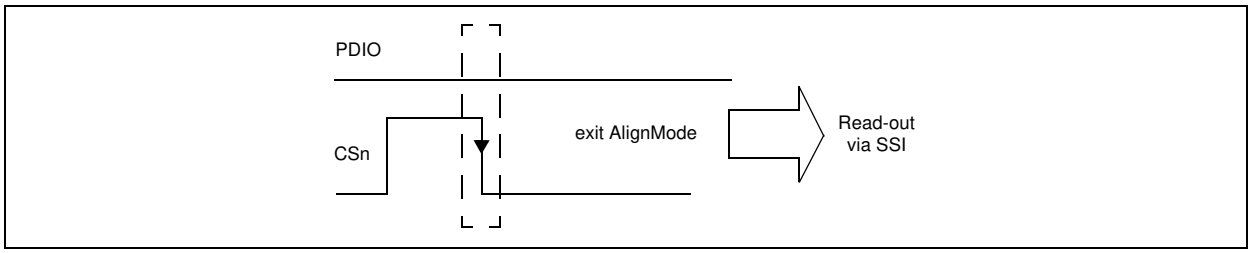


Figure 15. Exiting alignment mode



3.3V / 5V Operation

The AS5145 operates either at 3.3V ±10% or at 5V ±10%. This is made possible by an internal 3.3V Low-Dropout (LDO) Voltage regulator. The internal supply voltage is always taken from the output of the LDO, meaning that the internal blocks are always operating at 3.3V.

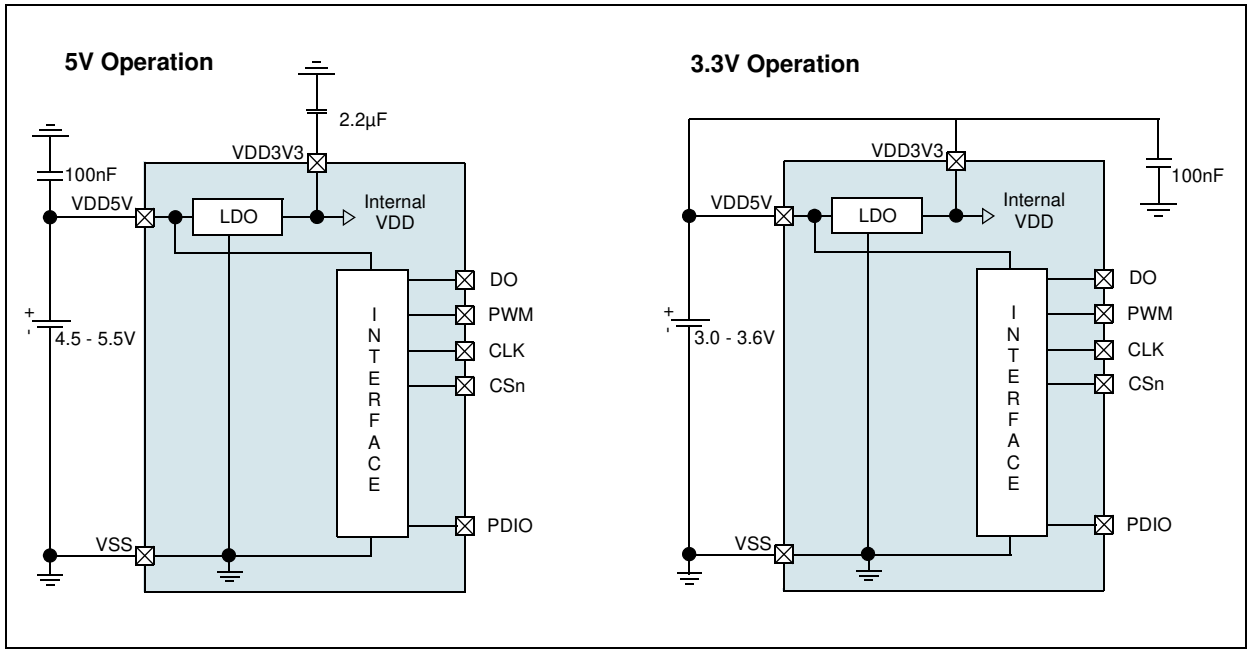
For 3.3V operation, the LDO must be bypassed by connecting VDD3V3 with VDD5V (see Figure 16).

For 5V operation, the 5V supply is connected to pin VDD5V, while VDD3V3 (LDO output) must be buffered by a 1...10µF capacitor, which is supposed to be placed close to the supply pin ((see Figure 16) with recommended 2.2µF).

Note: The VDD3V3 output is intended for internal use only It must not be loaded with an external load.

The output voltage of the digital interface I/O's corresponds to the voltage at pin VDD5V, as the I/O buffers are supplied from this pin.

Figure 16. Connections for 5V / 3.3V supply voltages



A buffer capacitor of 100nF is recommended in both cases close to pin VDD 5V. Note that pin VDD 3V3 must always be buffered by a capacitor. It must not be left floating, as this may cause an instable internal 3.3V supply voltage which may lead to larger than normal jitter of the measured angle.

Selecting Proper Magnet

Typically the magnet should be 6mm in diameter and 2.5mm in height. Magnetic materials such as rare earth AlNiCo/ SmCo5 or NdFeB are recommended. The magnetic field strength perpendicular to the die surface has to be in the range of ±45mT…±75mT (peak).

The magnet's field strength should be verified using a gauss-meter. The magnetic field Bv at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±45mT…±75mT(see Figure 17).