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AS5247

14-Bit Dual-Die On-Axis Magnetic Rotary Position Sensor with 11-Bit Binary Incremental Pulse Count

General Description

The AS5247 is a high-resolution redundant rotary position sensor for fast absolute angle measurement over a full 360-degree range. This new position sensor is equipped with a revolutionary integrated dynamic angle error compensation (DAEC™) with almost 0 latency.

The robust design of the device suppresses the influence of any homogenous external stray magnetic field. A standard 4-wire SPI serial interface allows a host microcontroller to read 14-bit absolute angle position data from the AS5247 and to program non-volatile settings without a dedicated programmer.

Incremental movements are indicated on a set of ABI signals with a maximum resolution of 2048 steps / 512 pulses per revolution. The resolution of the ABI signal is programmable to 1024 steps / 256 pulses per revolution.

Brushless DC (BLDC) motors are controlled through a standard UVW commutation interface with a programmable number of pole pairs from 1 to 7. The absolute angle position is also provided as PWM-encoded output signal.

The AS5247 supports embedded self-diagnostics including magnetic field strength too high, magnetic field strength too low or lost magnet, and other related diagnostic features.

The AS5247 is available as a dual die in a compact MLF-40 7x7 package.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5247, 14-bit Dual-Die On-Axis Magnetic Rotary Position Sensor with 11-bit Binary Incremental Pulse Count are listed below:

Figure 1:
Added Value of Using the AS5247

Benefits	Features
• Easy to use – saving costs on DSP	• DAEC™ Dynamic angle error compensation
• Good resolution for motor and position control	• 14-bit core resolution
• Versatile choice of the interface	• Independent output interfaces: SPI, ABI, UVW, PWM

Benefits	Features
• No programmer needed (via SPI command)	• Zero position, configuration programmable
• Supports safety-critical applications	• Self-Diagnostics and redundancy
• Lower system costs (no shielding)	• Immune to external stray field

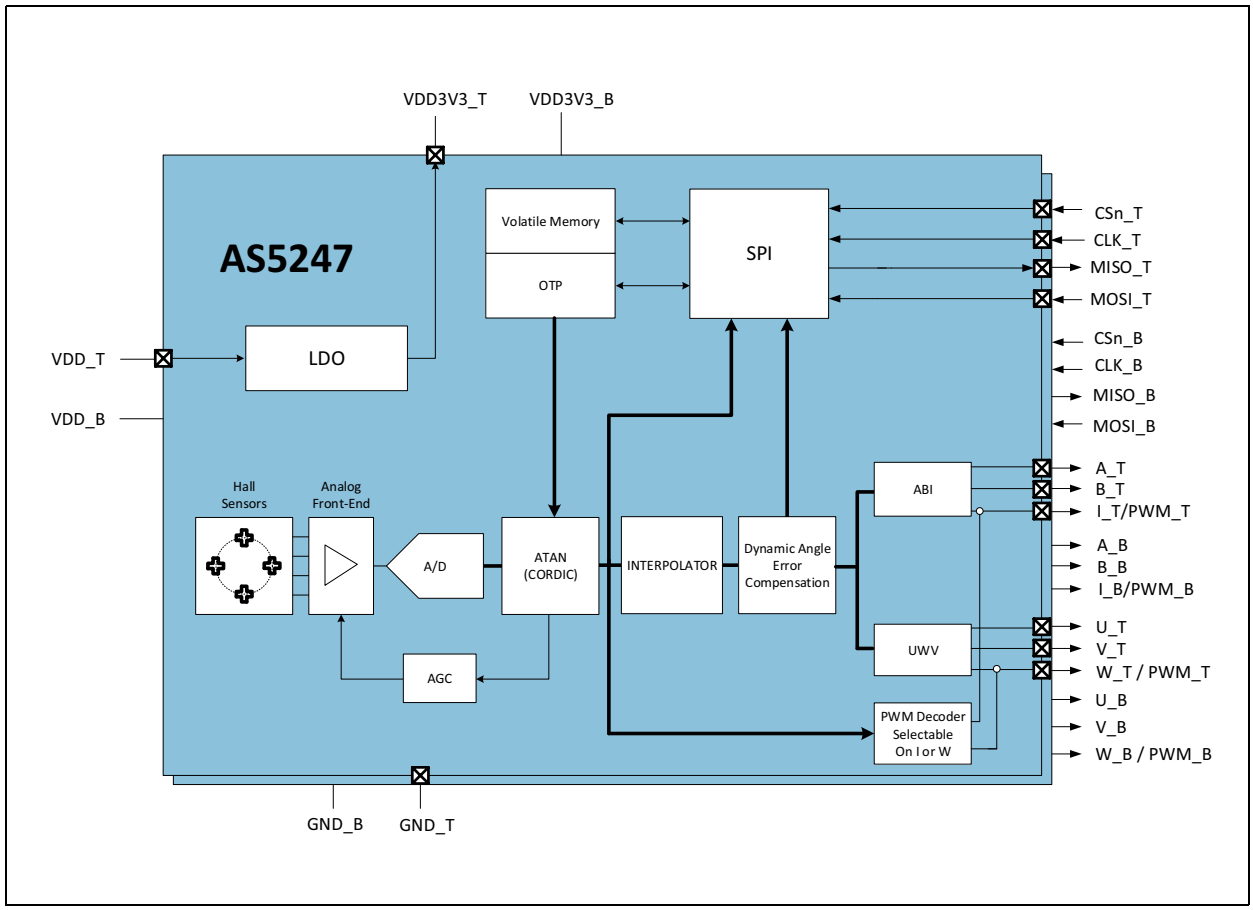
Applications

The AS5247 has been designed to support BLDC motor commutation for the most challenging and safety-critical automotive applications (AEC-Q100 grade 0 automotive qualified) such as electric power steering (EPS), transmission (gearbox, actuator), brake (actuator) and starter & alternator.

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS5247 Block Diagram



Pin Assignment

The suffix on the signal name indicates which of the two internal chips is connected to the pin (T = top die, B = bottom die). The package contains two identical chips, and no pins are shared by both chips.

Figure 3:
MLF 40 Pin Assignment

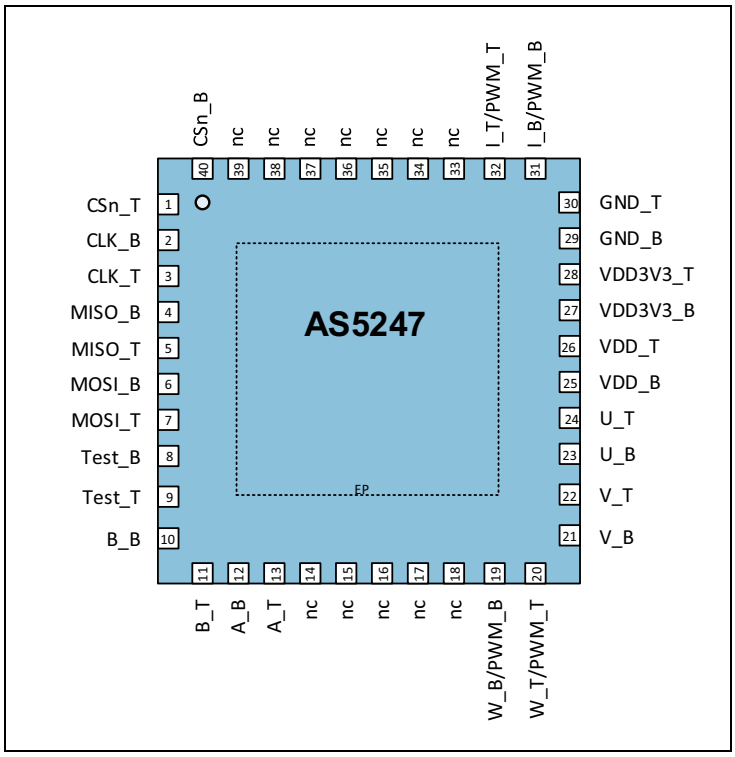


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	CSn_T	Digital Input	SPI chip select (active low)
2	CLK_B	Digital Input	SPI Clock
3	CLK_T	Digital Input	SPI Clock
4	MISO_B	Digital Output	SPI master data input, slave output
5	MISO_T	Digital Output	SPI master data input, slave output
6	MOSI_B	Digital Input	SPI master data output, slave input
7	MOSI_T	Digital Input	SPI master data output, slave input
8	Test_B		Test pin. Connected to ground
9	Test_T		Test pin. Connected to ground
10	B_B	Digital Output	Incremental signal B
11	B_T	Digital Output	Incremental signal B
12	A_B	Digital Output	Incremental Signal A

Pin Number	Pin Name	Pin Type	Pin Description
13	A_T	Digital Output	Incremental Signal A
14	nc		Not connected
15	nc		Not connected
16	nc		Not connected
17	nc		Not connected
18	nc		Not connected
19	W_B/PWM_B	Digital Output	Commutation signal W or PWM encoded output
20	W_T/PWM_T	Digital Output	Commutation signal W or PWM encoded output
21	V_B	Digital Output	Commutation signal V
22	V_T	Digital Output	Commutation signal V
23	U_B	Digital Output	Commutation signal U
24	U_T	Digital Output	Commutation signal U
25	VDD_B	Power Supply	5V power supply voltage for on-chip regulator
26	VDD_T	Power Supply	5V power supply voltage for on-chip regulator
27	VDD3V3_B	Power Supply	3.3V on-chip low-dropout (LDO) output. Requires an external decoupling capacitor (1uF)
28	VDD3V3_T	Power Supply	3.3V on-chip low-dropout (LDO) output. Requires an external decoupling capacitor (1uF)
29	GND_B	Power Supply	Ground
30	GND_T	Power Supply	Ground
31	I_B/PWM_B	Digital Output	Index signal or PWM encoded output
32	I_T/PWM_T	Digital Output	Index signal or PWM encoded output
33	n.c		
34	n.c		

Pin Number	Pin Name	Pin Type	Pin Description
35	n.c		
36	n.c		
37	n.c		
38	n.c		
39	n.c		
40	CSn_B		SPI chip select (active low)

Note(s) and/or Footnote(s):

1. Floating state of a digital input is not allowed.
2. If SPI is not used, a Pull up resistor on CSn is required.
3. If SPI is not used, a Pull down resistor on CLK and MOSI is required.
4. If SPI is not used, the pin MISO can be left open.
5. If ABI, UVW or PWM is not used, the pins can be left open.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Parameters regarding normal operation of the sensor are listed in section Electrical Characteristics.

Figure 5:
Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Note
DC supply voltage at VDD pin	VDD5	-0.3	7.0	V	
DC supply voltage at VDD3V3 pin	VDD3	-0.3	5.0	V	
DC supply voltage at GND pin	VSS	-0.3	0.3	V	
Input pin voltage	Vin		VDD+0.3	V	
Input current (latch-up immunity)	Iscr	-100	100	mA	Norm: AEC-Q100-004
Electrostatic discharge	ESD	±2		kV	Norm: AEC-Q100-002
Total power dissipation (all supplies and outputs)	Pt		150	mW	
Ambient temperature 5V0	Ta5V0	-40	150	°C	In the 5.0V power supply mode only
Ambient temperature 3V3	Ta3V3	-40	150	°C	In the 3.3V power supply mode if NOISESET=1
Programming temperature	TaProg	5	45	°C	Programming @ room temperature (25°C ± 20°C)
Storage temperature	T_strg	-55	150	°C	
Package body temperature	T_body		260	°C	Norm: IPC/JEDEC J-STD-020
Relative humidity non-condensing	RH_{NC}	5	85	%	
Moisture sensitivity level	MSL	3			Represents a maximum floor lifetime of 168h

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Positive supply voltage	5.0V operation mode	4.5	5.0	5.5	V
VDD3V3	Positive supply voltage	3.3V operation mode; only from -40°C to 125°C	3.0	3.3	3.6	V
VDD3V3_150	Positive supply voltage	3.3V operation mode; only from -40°C to 150°C (Noiseset Bit has to be set)	3.0	3.3	3.6	V
VDD_Burn	Positive supply voltage	Supply voltage required for programming in 3.3V operation	3.3		3.5	V
VREG	Regulated Voltage	Voltage at VDD3V3 pin if VDD ≠ VDD3V3	3.2	3.4	3.6	V
IDD	Supply current	Only for one die. Must be multiplied by 2			15	mA
VIH	High-level input voltage		0.7 × VDD			V
VIL	Low-level input voltage				0.3 × VDD	V
VOH	High-level output voltage		VDD - 0.5			
VOL	Low-level output voltage				VSS + 0.4	V
I_Out	Current on digital output A, B, I, U, V, W				1	mA
I_Out_MISO	Current on digital output MISO				4	mA
C_L	Capacitive load on digital output				50	pF

Magnetic Characteristics

Figure 7:
Magnetic Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bz	Orthogonal magnetic field strength, normal operating mode	Required orthogonal component of the magnetic field strength measured at the die's surface along a circle of 1.1mm	35		70	mT

Note(s) and/or Footnote(s):

1. It is possible to operate the AS5247 below 35mT with reduced noise performance.

System Characteristics

Figure 8:
System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Core resolution			14		bit
RES_ABI	Resolution of the ABI interface	Programmable with register setting (ABIRES)	10		11	bit
INL_{OPT} @ 25°C	Non-linearity, optimum placement of the magnet				±0.9	degree
$INL_{DIS+TEMP}$	Non-linearity @ displacement of magnet and temperature -40°C to 150°C	Assuming N35H Magnet (D=8mm, H=3mm) 500um displacement in x and y z-distance @ 2000um			±1.4	degree
ONL	RMS output noise (1 sigma)	Orthogonal component for the magnetic field within the specified range (Bz), NOISESET= 0			0.068	degree
ONH	RMS output noise (1 sigma) on SPI, ABI and UVW interfaces	Orthogonal component for the magnetic field within the specified range (Bz), NOISESET= 1			0.082	degree

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ON_PWM	RMS output noise (1 sigma) on PWM interface	Orthogonal component for the magnetic field within the specified range (Bz)			0.068	degree
t_{delay}	System propagation delay –core	Reading angle via SPI	90		110	µs
t_{delay_DAEC}	System propagation delay after dynamic angle error correction.	At ABI and UVW interfaces	1.5		1.9	µs
t_{sampl}	Sampling rate	Refresh rate at SPI	202	222	247	ns
DAE_{1700}	Dynamic angle error	At 1700 RPM constant speed			0.02	degree
DAE_{max}	Dynamic angle error	At 14500 RPM constant speed			0.18	degree
DAE_{acc}	Dynamic angle error at constant acceleration (25krad/s^2)	25k radians/s^2 constant acceleration			0.175	degree
MS	Maximum speed				14500	RPM

Reference magnet: N35H, 8mm diameter; 3mm thickness

Timing Characteristics

Figure 9:
Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pon}	Power-on time	Not tested, guaranteed by design. Time between VDD > VDDmin and the first valid outcome			10	ms

Detailed Description

The AS5247 is a Hall-effect magnetic sensor using a CMOS lateral technology. The lateral Hall sensors convert the magnetic field component perpendicular to the surface of the chip into a voltage.

The signals from the Hall sensors are amplified and filtered by the analog front-end (AFE) before being converted by the analog-to-digital converter (ADC). The output of the ADC is processed by the hardwired CORDIC (coordinate rotating digital computer) block to compute the angle and magnitude of the magnetic vector. The intensity of the magnetic field (magnitude) is used by the automatic gain control (AGC) to adjust the amplification level for compensation of the temperature and magnetic field variations.

The internal 14-bit resolution is available by readout register via the SPI interface. The resolution on the ABI output can be programmed for 10 or 11bits.

The Dynamic Angle Error Compensation block corrects the calculated angle regarding latency, by using a linear prediction calculation algorithm. At constant rotation speed the latency time is internally compensated by the AS5247, reducing the dynamic angle error at the SPI, ABI and UVW outputs. The AS5247 allows selecting between a UVW / ABI output and a PWM-encoded interface on the W-pin or the I-pin.

At higher speeds, the interpolator fills in missing ABI pulses and generates the UVW signals with no loss of resolution. The non-volatile settings in the AS5247 can be programmed through the SPI interface without any dedicated programmer.

Power Management

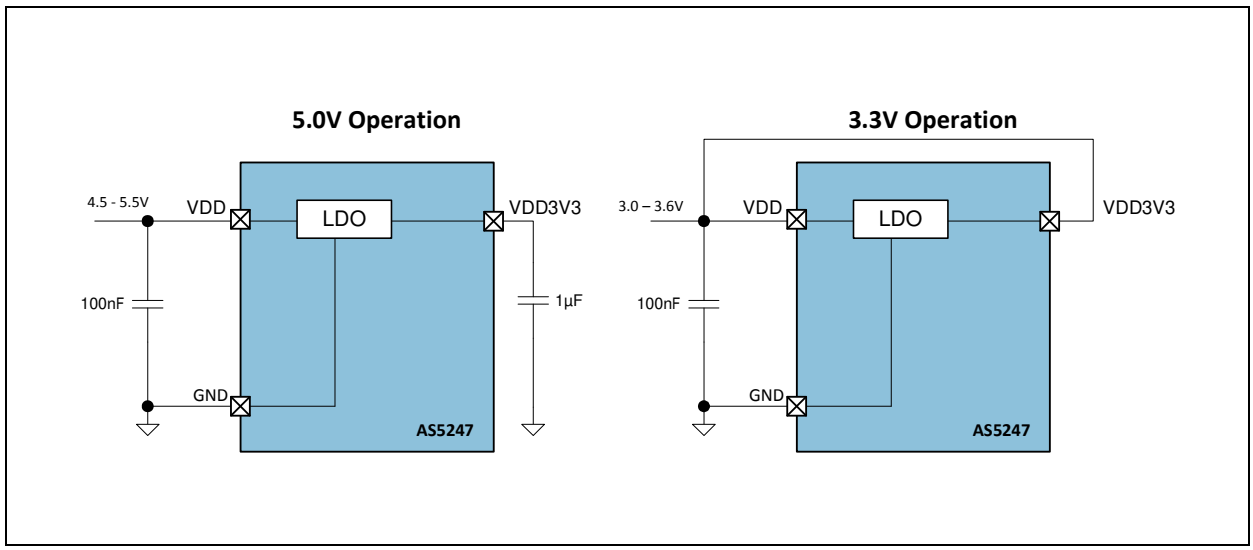
The AS5247 can be either powered from a 5.0V supply using the on-chip low-dropout regulator or from a 3.3V voltage supply. The LDO regulator is not intended to power any other loads, and it needs a 1 µF capacitor to ground located close to the chip for decoupling as shown in Figure 11.

In 3.3V operation, VDD and VDD3V3 must be tied together. In this configuration, normal noise performance (ONL) is available at reduced maximum temperature (125°C) by clearing NOISESET to 0 (default configuration). When NOISESET is set to 1, the full temperature range is available with reduced noise performance (ONH).

Figure 10:
Temperature Range and Output Noise in 3.3V and 5.0V Mode

VDD (V)	NOISESET	Temperature Range (°C)	RMS Output Noise (degree)
5.0	0	-40 ~ 150	0.068
3.3	0	-40 ~ 125	0.068
3.3	1	-40 ~ 150	0.082

Figure 11:
5.0V and 3.3V Power Supply Options



After applying power to the chip, the power-on time (tpon) must elapse before the AS5247 provides the first valid data.

Dynamic Angle Error Compensation

The AS5247 uses 4 integrated Hall sensors on Bottom Die and Top Die, which produce a voltage proportional to the orthogonal component of the magnetic field to the die. These voltage signals are amplified, filtered, and converted into the digital domain to allow the CORDIC digital block to calculate the angle of the magnetic vector. The propagation of these signals through the analog front-end and digital back-end generates a fixed delay between the time of measurement and the availability of the measured angle at the outputs. This latency generates a dynamic angle error, represented by the product of the angular speed ω and the system propagation delay (tdelay):

(EQ1) $DAE = \omega \times tdelay$

The dynamic angle compensation block calculates the current magnet rotation speed (ω) and multiplies it with the system propagation delay (tdelay) to determine the correction angle to reduce this error. At constant speed, the residual system propagation delay is tdelay_ DAEC.

The angle represented on the PWM interface is not compensated by the Dynamic Angle Error Compensation algorithm. It is also possible to disable the Dynamic Angle Error Compensation with the DAECDIS setting. Disabling the Dynamic Angle Error Compensation gives a noise benefit of 0.016 degree rms. This setting can be advantageous for low speed (under 100 RPM) respectively static positioning applications.

SPI Interface (slave)

The SPI interface is used by a host microcontroller (master) to read or write the volatile memory, as well as to program the non-volatile OTP registers. The AS5247 SPI only supports slave operation mode. It communicates at clock rates up to 10 MHz.

The AS5247 SPI uses mode=1 (CPOL=0, CPHA=1) to exchange data. As shown in Figure 12, a data transfer starts with the falling edge of CSn (CLK is low). The AS5247 samples MOSI data on the falling edge of CLK. SPI commands are executed at the end of the frame (rising edge of CSn). The bit order is MSB first. Data is protected by parity.

SPI Timing

The AS5247 SPI timing is shown in Figure 12.

Figure 12:
SPI Timing Diagram

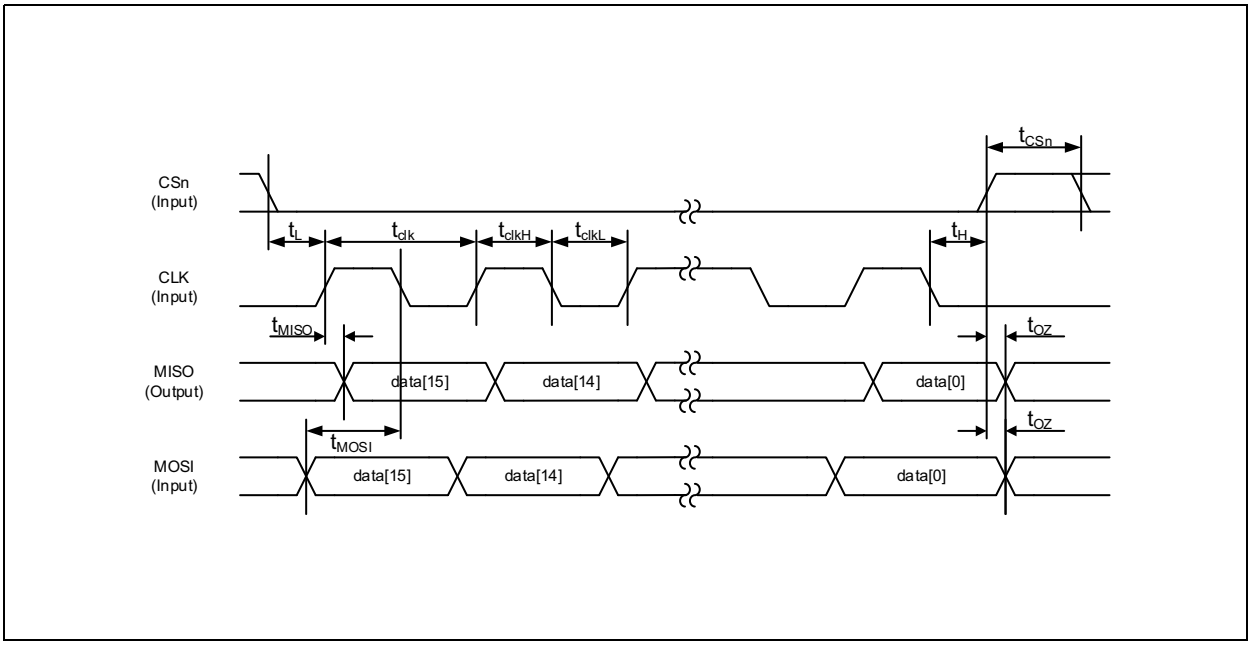


Figure 13:
SPI Timing

Parameter	Description	Min	Max	Units
t_L	Time between CSn falling edge and CLK rising edge	350		ns
t_{clk}	Serial clock period	100		ns
t_{clkL}	Low period of serial clock	50		ns
t_{clkH}	High period of serial clock	50		ns
t_H	Time between last falling edge of CLK and rising edge of CSn	tclk/2		ns
t_{CSn}	High time of CSn between two transmissions	350		ns
t_{MOSI}	Data input valid to falling clock edge	20		ns
t_{MISO}	CLK edge to data output valid		51	ns
t_{OZ}	Release bus time after CS rising edge.		10	ns

SPI Transaction

An SPI transaction consists of a 16-bit command frame followed by a 16-bit data frame. Figure 14 shows the structure of the command frame.

Figure 14:
SPI Command Frame

Bit	Name	Description
15	PARC	Parity bit (even) calculated on the lower 15 bits of command frame
14	R/W	0: Write 1: Read
13:0	ADDR	Address to read or write

To increase the reliability of communication over the SPI, an even parity bit (PARC) must be generated and sent. A wrong setting of the parity bit causes an parity bit error which is shown the PARERR bit in the error flag register. The parity bit is calculated from the lower 15 bits of the command frame. The 16-bit command consists of a register address and read/write bit which indicates if the transaction is a read or write and the parity bit. Figure 15 shows the read data frame.

Figure 15:
SPI Read Data Frame

Bit	Name	Description
15	PARD	Parity bit (even) calculated on the lower 15 bits of the read data frame
14	EF	0: No command frame error command occurred 1: Error occurred
13:0	DATA	Data

The data is sent on the MISO pin. The parity bit PARD is calculated by the AS5247 of the lower 15 bits of data frame. If an error is detected in the previous SPI command frame, the EF bit is set high. The SPI read is sampled on the rising edge of CSn and the data is transmitted on MISO with the next read command, as shown in Figure 16.

Figure 16:
SPI Read

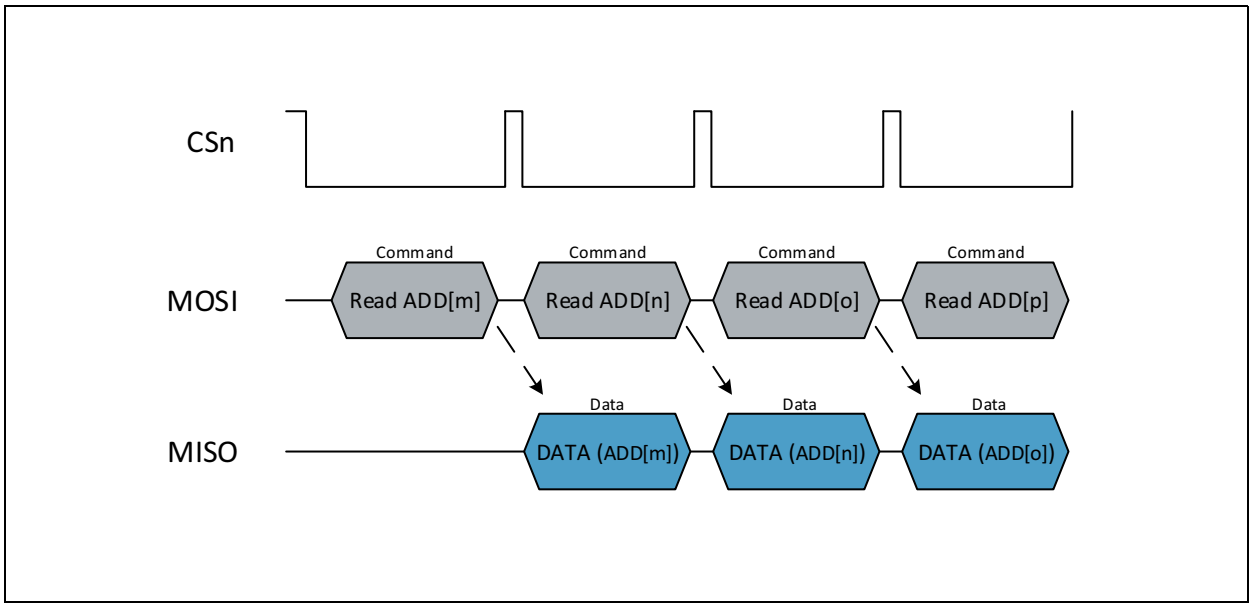


Figure 17:
SPI Write Data Frame

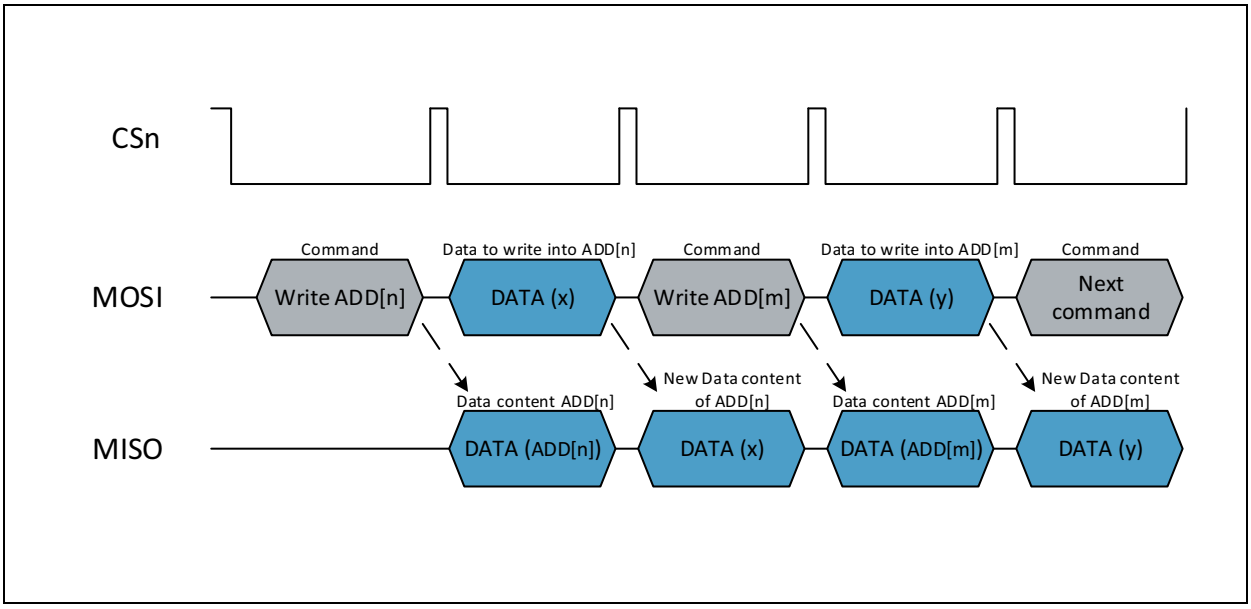
Bit	Name	Description
15	PARC	Parity bit (even)
14	0	Always low
13:0	DATA	Data

The parity bit PARC is calculated from the lower 15 bits of data frame.

In a SPI write transaction, the write command frame is followed by a write data frame at MOSI. The write data frame consists of the new content of register which address is defined in the command frame.

During the new content is transmitted on MOSI by the write data frame, the old content is send on MISO. At the next command on MOSI the actual content of the register is transmitted on MISO, as shown in Figure 18.

Figure 18:
SPI Write Transaction



Volatile Registers

The volatile registers are shown in Figure 19. Each register has a 14-bit address.

Figure 19:
Volatile Register Table

Address	Name	Default	Description
0x0000	NOP	0x0000	No operation
0x0001	ERRFL	0x0000	Error register
0x0003	PROG	0x0000	Programming register
0x3FFC	DIAAGC	0x0180	Diagnostic and AGC
0x3FFD	MAG	0x0000	CORDIC magnitude
0x3FFE	ANGLEUNC	0x0000	Measured angle without dynamic angle error compensation
0x3FFF	ANGLECOM	0x0000	Measured angle with dynamic angle error compensation

Reading the NOP register is equivalent to a nop (no operation) instruction for the AS5247.

Figure 20:
ERRFL (0x0001)

Name	Read/Write	Bit Position	Description
PARERR	R	2	Parity error
INVCOMM	R	1	Invalid command error: set to 1 by reading or writing an invalid register address
FRERR	R	0	Framing error: is set to 1 when a non-compliant SPI frame is detected

Reading the ERRFL register automatically clears its contents (ERRFL=0x0000).

Figure 21:
PROG (0x0003)

Name	Read/Write	Bit Position	Description
PROGVER	R/W	6	Program verify: must be set to 1 for verifying the correctness of the OTP programming
PROGOTP	R/W	3	Start OTP programming cycle
OTPREF	R/W	2	Refreshes the non-volatile memory content with the OTP programmed content
PROGEN	R/W	0	Program OTP enable: enables programming the entire OTP memory

The PROG register is used for programming the OTP memory. (See programming the zero position.)

Figure 22:
DIAAGC (0x3FFC)

Name	Read/Write	Bit Position	Description
MAGL	R	11	Diagnostic: Magnetic field strength too low; AGC=0xFF
MAGH	R	10	Diagnostic: Magnetic field strength too high; AGC=0x00
COF	R	9	Diagnostic: CORDIC overflow
LF	R	8	Diagnostics: Loops Finished LF=0:internal offset loops not ready regulated LF=1:internal offset loop finished
AGC	R	7:0	Automatic gain control value

Figure 23:
MAG (0x3FFD)

Name	Read/Write	Bit Position	Description
MAG	R	13:0	CORDIC magnitude information

Figure 24:
ANGLEUNC (0x3FFE)

Name	Read/Write	Bit Position	Description
ANGLEUNC	R	13:0	Angle information without dynamic angle error compensation

Figure 25:
ANGLECOM (0x3FFF)

Name	Read/Write	Bit Position	Description
ANGLECOM	R	13:0	Angle information with dynamic angle error compensation.

Non-Volatile Registers (OTP)

The OTP (One-Time Programmable) memory is used to store the absolute zero position of the sensor and the customer settings permanently in the sensor IC. SPI write/read access is possible several times for all Non-Volatile Registers (soft write). Soft written register content will be lost after a hardware reset. The programming itself can be done just once. Therefore the content of the Non-Volatile Registers is stored permanently in the sensor. The register content is still present after a hardware reset and cannot be overwritten. For a correct function of the sensor the OTP programming is not required. If no configuration or programming is done, the Non-Volatile Registers are in the default state 0x0000.

Figure 26:
Non-Volatile Register Table

Address	Name	Default	Description
0x0016	ZPOSM	0x0000	Zero position MSB
0x0017	ZPOSL	0x0000	Zero position LSB/MAG diagnostic
0x0018	SETTINGS1	0x0000	Custom setting register1
0x0019	SETTINGS2	0x0000	Custom setting register 2
0x001A	RED	0x0000	Redundancy register

Figure 27:
ZPOSM (0x0016)

Name	Read/Write/Program	Bit Position	Description
ZPOSM	R/W/P	7:0	8 most significant bits of the zero position

Figure 28:
ZPOSL (0x0017)

Name	Read/Write/Program	Bit Position	Description
ZPOSL	R/W/P	5:0	6 least significant bits of the zero position
comp_l_error_en	R/W/P	6	This bit enables the contribution of MAGH (Magnetic field strength too high) to the error flag
comp_h_error_en	R/W/P	7	This bit enables the contribution of MAGL (Magnetic field strength too low) to the error flag

Figure 29:
SETTINGS1 (0x0018)

Name	Read/Write/Program	Bit Position	Description
IWIDTH	R/W/P	0	Width of the index pulse I (0 = 3LSB, 1 = 1LSB)
NOISESET	R/W/P	1	Noise setting
DIR	R/W/P	2	Rotation direction
UVW_ABI	R/W/P	3	Defines the PWM Output (0 = ABI is operating, W is used as PWM 1 = UVW is operating, I is used as PWM)
DAECDIS	R/W/P	4	Disable Dynamic Angle Error Compensation (0 = DAE compensation on, 1 = DAE compensation off)
Dataselect	R/W/P	6	This bit defines which data can be read form address 16383dec (3FFFhex). 0 → ANGLECOM 1 → ANGLEUNC
PWMon	R/W/P	7	enables PWM (setting of UVW_ABI Bit necessary)

Figure 30:
SETTINGS2 (0x0019)

Name	Read/Write/Program	Bit Position	Description
UVWPP	R/W/P	2:0	UVW number of pole pairs (000=1, 001=2, 010=3, 011=4, 100=5, 101=6, 110=7,111=7)
HYS	R/W/P	4:3	Hysteresis for 11 Bit ABI Resolution: (00=3LSB, 01= 2LSB,10=1LSB,11=no hysteresis) for 10 Bit ABI Resolution: (00=2LSB, 01= 1LSB,10=no Hysteresis LSB,11=3LSB)
ABIRES	R/W/P	5	Resolution of ABI (0=11 bits, 1=10 bits)

The hysteresis is in terms of the chosen resolution (11 bits vs. 10bits) The ABIRES resolution does not affect the UVW signals.

Figure 31:
RED(0x001A)

Name	Read/Write/Program	Bit Position	Description
RED	R/W/P	4:0	Redundancy bits. This field enables with force to high one bit of the Non-Volatile register map after a non-successful burning. For more details please refer to the application note “AS5147_ApplicationNote_ RedundancyBits”

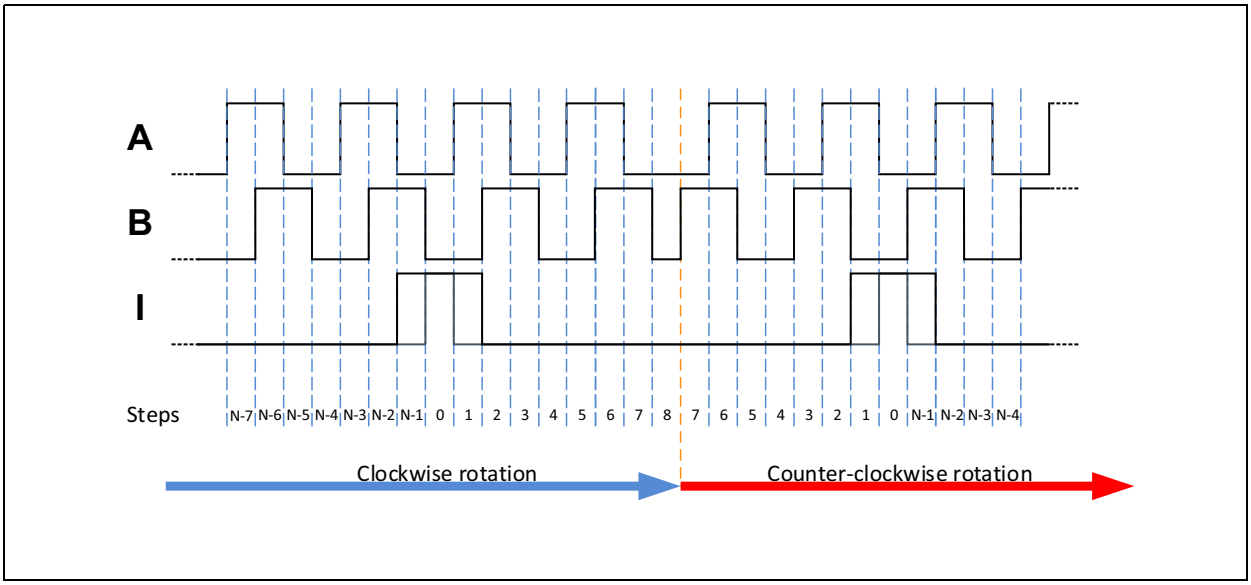
ABI Incremental Interface

The AS5247 can send the angle position to the host microcontroller through an incremental interface. This interface is available simultaneously with the other interfaces. By default, the incremental interface is set to work at the highest resolution (11 bits), which corresponds to 2048 steps per revolution or 512 pulses per revolution (ppr). This resolution can be cut in half using the OTP bit ABIRES, which results in 1024 steps per revolution or 256 pulses per revolution.

The phase shift between the A and B signals indicates the rotation direction: clockwise (A leads, B follows) or counterclockwise (B leads, A follows). The DIR bit can be used to invert the sense of the rotation direction. During the power-on time, all three ABI signals are high.

The IWIDTH setting programs the width of the index pulse from 3 LSB (default) to 1 LSB.

Figure 32:
ABI Signals at 11 Bit Resolution



Note(s) and/or Footnote(s):

1. N = 2048 for 11-bit resolution, and N = 1024 for 10-bit resolution.
2. Index pulse width 3 LSB and index pulse width 1 LSB (dashed line) are shown in the diagram.

The Figure 32 shows the ABI signal flow if the magnet rotates in clockwise direction and counter-clockwise direction (DIR=0). In case of clockwise rotation when the magnet is rotating to the right hand side, the angle value is increasing. Clockwise rotation direction is defined as shown in Figure 44.

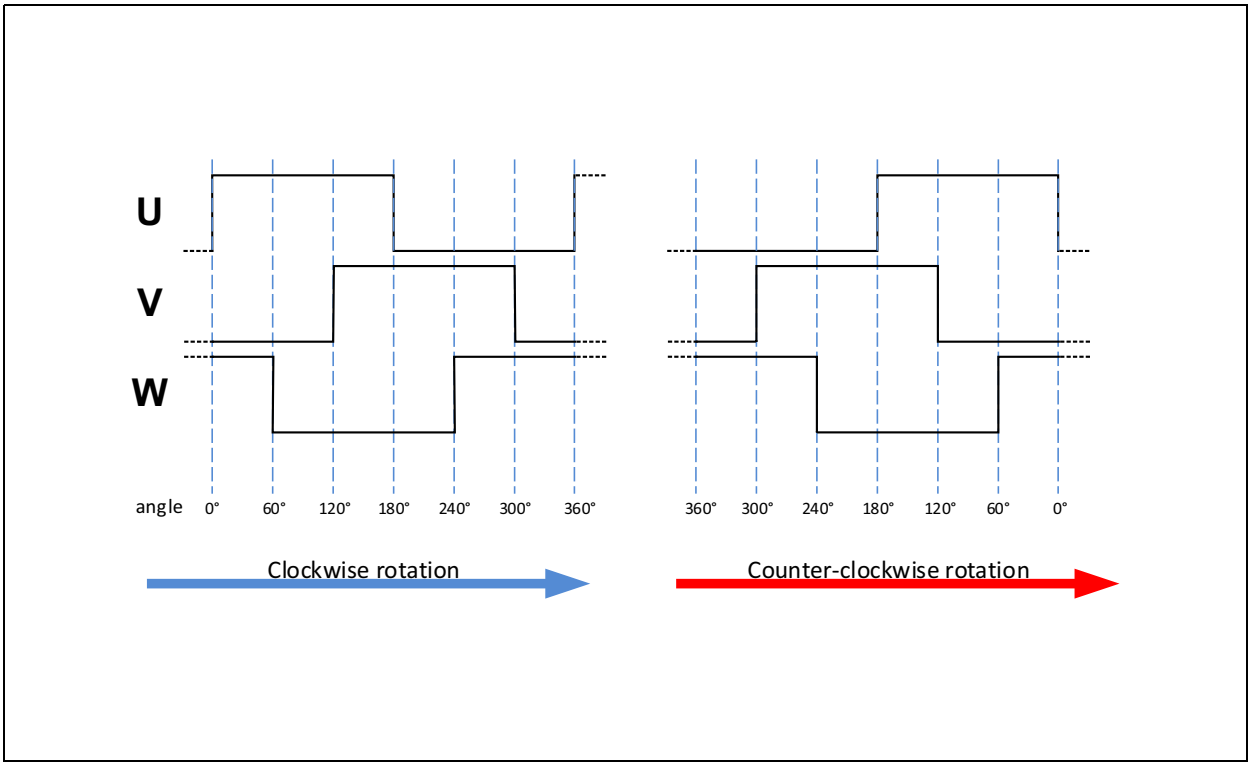
UVW Commutation Interface

The AS5247 can emulate the UVW signals generated by the three discrete Hall switches commonly used in BLDC motors.

The UVWPP field in the SETTINGS register selects the number of pole pairs of the motor (from 1 to 7 pole pairs). The UVW signals are generated with 14-bit resolution.

During the power-on time, the UVW signals are low.

Figure 33:
UVW Signals



The Figure 33 shows the UVW signal flow if the magnet rotates in clockwise direction and counter-clockwise direction (DIR=0). In case of clockwise rotation when the magnet is rotating to the right hand side, the angle value is increasing. Clockwise rotation direction is defined as shown in Figure 44. With the bit DIR, it is possible to invert the rotation direction.

PWM

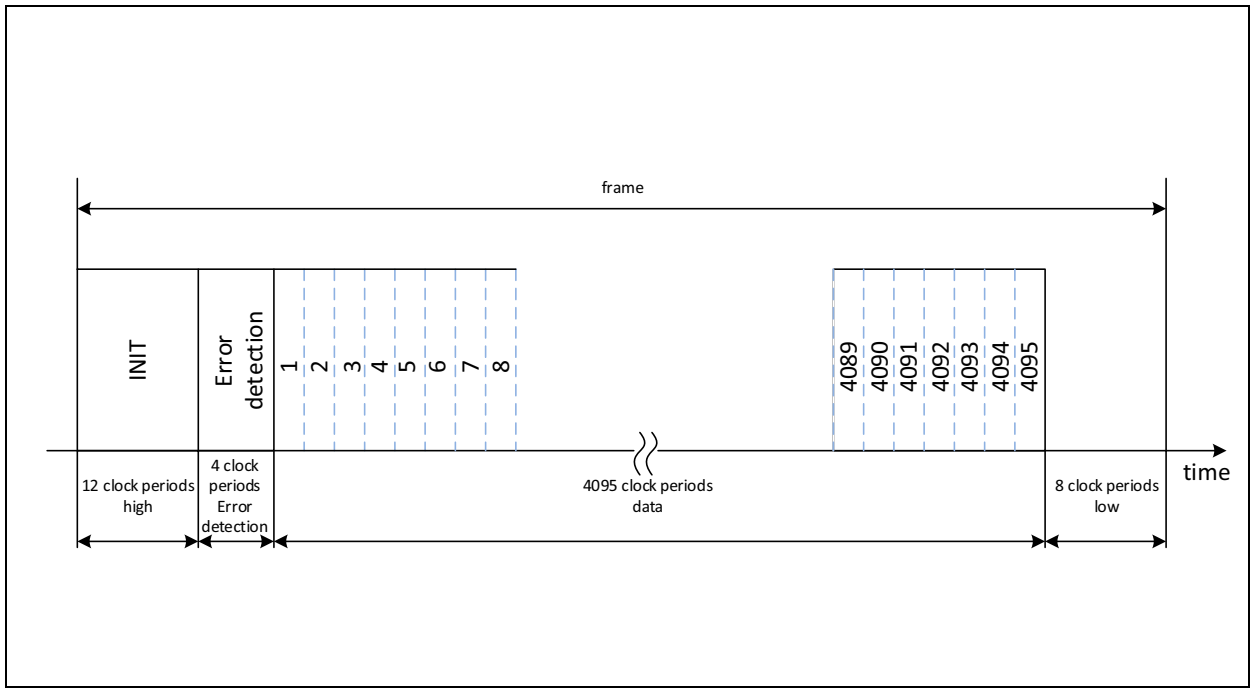
The PWM can be enabled with the bit setting PWMon. The PWM encoded signal is displayed on the pin W or the pin I. The bit setting UVW_ABI defines which output is used as PWM. The PWM output consists of a frame of 4119 PWM clock periods, as shown in Figure 34. The PWM frame has the following sections:

- 12 PWM Clocks for INIT
- 4 PWM Clocks for Error detection
- 4095 PWM clock periods of data
- 8 PWM clock periods low

The angle is represented in the data part of the frame with a 12-bit resolution. One PWM clock period represents 0.088 degree and has a typical duration of 444 ns.

If the embedded diagnostic of the AS5247 detects any error, the PWM interface displays only 12 clock periods high (0.3% duty-cycle). Respectively the 4 clocks for error detection are forced to low.

Figure 34:
Pulse Width Modulation Encoded Signal



Hysteresis

The width of the hysteresis can be programmed. Two HYS bits are available in the SETTINGS2 register for configuration. Figure 35 shows the available settings based on the selected ABI resolution (ABIRES).

Figure 35:
Hysteresis Settings

HYS	HYSTERESIS with 11 Bit ABI Resolution	HYSTERESIS with 10 Bit ABI Resolution
00	3	2
01	2	1
10	1	0
11	0	3

Automatic Gain Control (AGC) and CORDIC Magnitude

The AS5247 uses AGC to compensate for variations in the magnetic field strength due to changes of temperature, air gap between the chip and the magnet, and demagnetization of the magnet. The automatic gain control value can be read in the AGC field of the DIAAGC register. Within the specified input magnetic field strength (Bz), the Automatic Gain Control works in a closed loop and keeps the CORDIC magnitude value (MAG) constant. Below the minimum input magnetic field strength, the CORDIC magnitude decreases and the MAGL bit is set.

Diagnostic Features

The AS5247 supports embedded self-diagnostics.

MAGH: Magnetic field strength too high, set if AGC = 0x00. This indicates the non-linearity error may be increased.

MAGL: Magnetic field strength too low, set high if AGC = 0xFF. This indicates the output noise of the measured angle may be increased.

COF: CORDIC overflow. This indicates the measured angle is not reliable.

LF: Offset compensation completed. At power-up, an internal offset compensation procedure is started, and this bit is set when the procedure is completed.

Full Redundancy for application with high safety requirements

LF Error / COF Error

In case of an LF or COF error, all outputs are changing into a safe state:

SPI Output: Information in the DIAAGC (0x3FFC) register. The angle information is still valid.

Error State PWM Output:

The PWM Clock Periods for Error Detection are forced to low. In addition the angle value is not valid (all 4096 Clock periods, showing the angle value, are forced to low). The PWM Error detection is shown at PWM Clock Period 13, 14, 15 and 16, see Figure 34.

Error State ABI Outputs:

ABI output is forced to high (111).

Error State UVW Outputs:

UVW output is forced to low (000).

MAGH Error / MAGL Error

Default diagnostic setting for MAGH error /MAGL error:

In case of a MAGH error or MAGL error, there is no safe state on the PWM, ABI or UVW outputs if comp_h_error_en is 0 and comp_l_error_en is 0.

The error flags can be read out with the DIAAGC (0x3FFC) register.

Enhanced diagnosis setting for MAGH error / MAGL error:

In case of a MAGH error or MAGL error, the PWM, ABI or UVW outputs are going into a safe state if comp_h_error_en is 1 and comp_l_error_en is 1.The device is operating with the performance as explained in chapter Diagnostic Features.

SPI Output: Information in the DIAAGC (0x3FFC) register. The angle information is still valid, if the MAGH or MAGL error flag is on.

Error State PWM Output:

The PWM Clock Periods for Error Detection are forced to low. In addition the angle value is not valid (all 4096 Clock periods, showing the angle value, are forced to low). The PWM Error detection is shown at PWM Clock Period 13, 14, 15 and 16, see Figure 34.

Error State ABI Outputs:

ABI output is forced to high (111).

Error State UVW Outputs:

UVW output is forced to low (000).

Important: When comp_h_error_en and/or comp_l_error_en is enabled, a marginal magnetic field input can cause toggling of MAGH or MAGL which will lead to toggling of the ABI/UVW outputs between operational mode and failure mode.