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AS5270

High-Resolution On-Axis Magnetic Angular Position Sensor

General Description

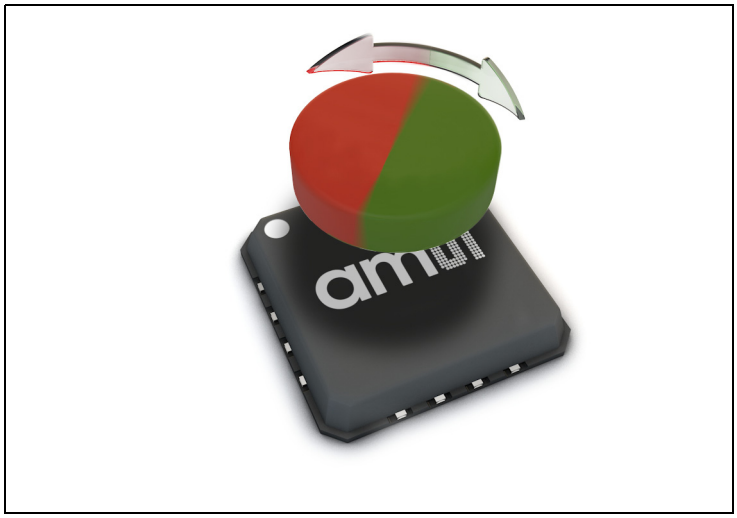
The AS5270 is a dual-die, high-resolution angular position sensor for precise absolute angle measurement. The AS5270 is available with an analog output interface (AS5270A) or a digital output interface (AS5270B). The latter can be programmed as a PWM or a SENT-compliant output interface.

Based on a Hall sensor technology, this device measures the orthogonal component of the flux density (Bz) over a full-turn rotation and compensates for external stray magnetic fields with a robust architecture based on a 14-bit sensor array and analog front-end (AFE). A sub-range can be programmed to achieve the best resolution for the application. To measure the angle, only a simple two-pole magnet rotating over the center of the package is required. The magnet may be placed above or below the device. The absolute angle measurement provides an instant indication of the magnet's angular position. The AS5270 operates at a supply voltage of 5V, and the supply and output pins are protected against overvoltage up to +20V. In addition the supply pins are protected against reverse polarity up to −20V.

The AS5270A is a stacked dual-chip for high-reliability redundant operation. In this device, two chips are aligned and encapsulated in the same package. Separate pins are provided for each chip, so no electrical fault in the device can affect both chips.

Ordering Information and *Content Guide* *appear at end of datasheet.*

Figure 1:
Typical Arrangement of AS5270 and a Magnet



Key Benefits and Features

The benefits and features of this device are listed below:

Figure 2:
Added Value of Using AS5270

Benefits	Features
• Resolve small angular excursion with high accuracy	• 12-bit resolution @90° minimum arc
• Accurate angle measurement	• Low output noise, low inherent INL
• Higher durability and lower system costs (no shield needed)	• Magnetic stray field immunity
• Enabler for safety critical applications	• Functional safety, diagnostics, dual redundant chip
• Suitable for automotive applications	• AEC-Q100 Grade 0 qualified

Applications

The AS5270 is ideal for automotive applications like brake and gas pedals, throttle valve and tumble flaps, steering angle sensors, chassis ride, EGR, fuel-level measurement systems, 2/4WD switch, and contactless potentiometers.

Block Diagram

The functional blocks of the AS5270A and AS5270B are shown below:

Figure 3:
Functional Blocks of the AS5270A

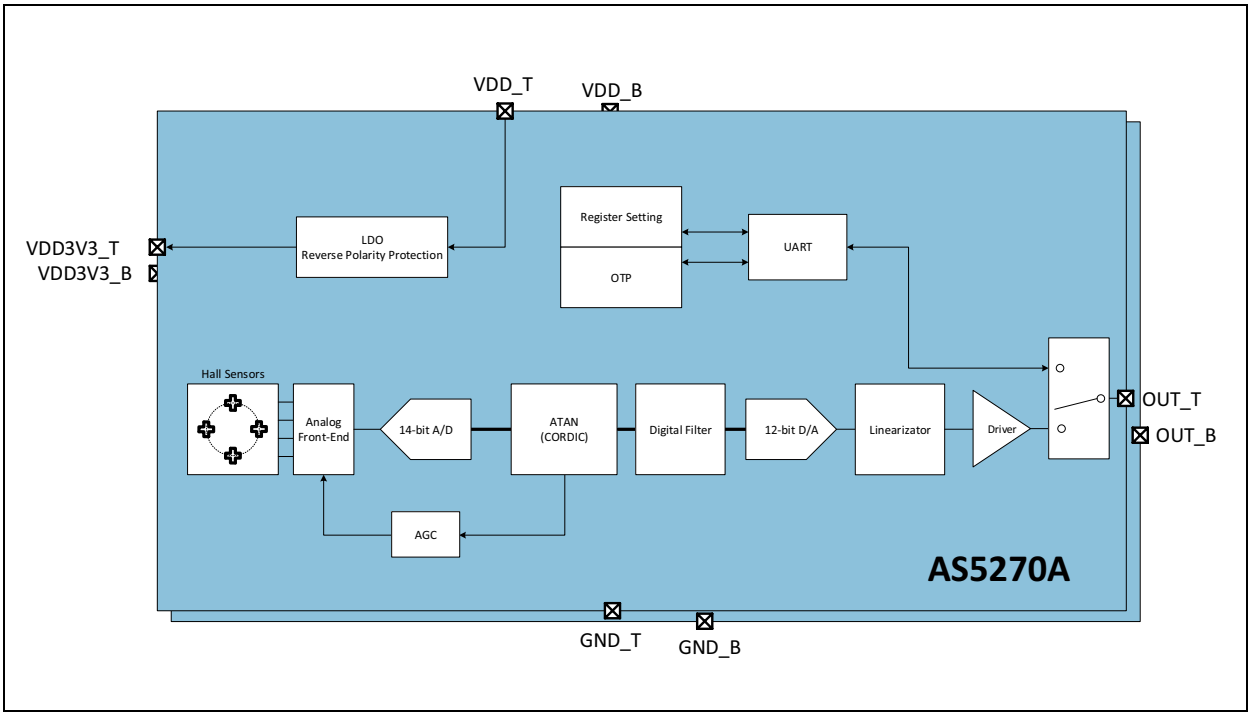
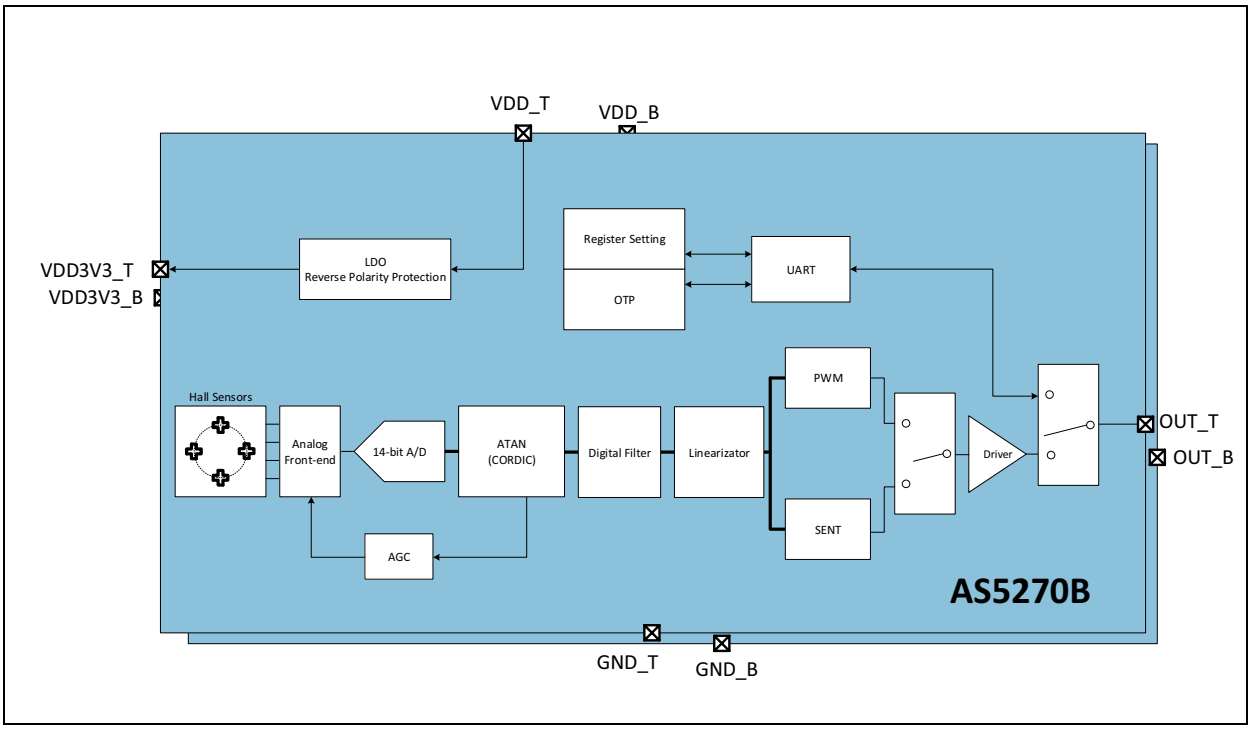


Figure 4:
Functional Blocks of the AS5270B



Pin Assignments

The suffix on the signal name indicates which of the two internal chips is connected to the pin (T = top die, B = bottom die). The package contains two identical chips, and no pins are shared by both chips.

Figure 5:
AS5270A/B Pin Assignment (Top View, MLF-16)

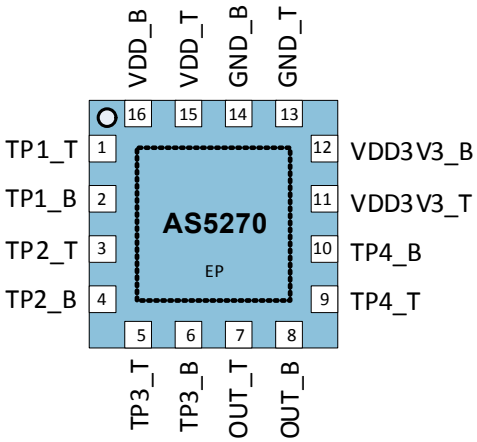


Figure 6:
AS5270A/B Pin Description (MLF-16)

Pin Number MLF-16	Pin Name	Pin Type	Description	Comments
1	TP1_T	n.a.	Test pin	Connected to ground
2	TP1_B	n.a.	Test pin	Connected to ground
3	TP2_T	n.a.	Test pin	Leave open
4	TP2_B	n.a.	Test pin	Leave open
5	TP3_T	n.a.	Test pin	Connected to ground
6	TP3_B	n.a.	Test pin	Connected to ground
7	OUT_T	Analog output (AS5270A) Digital output (AS5270B)	Output interface die 1	AS5270A: Analog output AS5270B: PWM or SENT output
8	OUT_B	Analog output (AS5270A) Digital output (AS5270B)	Output interface die 2	AS5270A: Analog output AS5270B: PWM or SENT output

Pin Number MLF-16	Pin Name	Pin Type	Description	Comments
9	TP4_T	n.a.	Test pin	To be connected to OUT_T if both OUT_T and OUT_B are connected to a pull-down or pull-up resistor. To be connected to the output pin (OUT_T or OUT_B, respectively) which is connected to the pull-down resistor in case OUT_T and OUT_B are connected one to a pull-down resistor and the other to a pull-up resistor.
10	TP4_B	n.a.	Test pin	To be connected to OUT_B if both OUT_T and OUT_B are connected to a pull-down or pull-up resistor. To be connected to the output pin (OUT_T or OUT_B, respectively) which is connected to the pull-down resistor in case OUT_T and OUT_B are connected one to a pull-down resistor and the other to a pull-up resistor.
11	VDD3V3_T	Supply	Positive supply die 1	
12	VDD3V3_B	Supply	Positive supply die 2	
13	GND_T	Supply	Ground die 1	
14	GND_B	Supply	Ground die 2	
15	VDD_T	Supply	Positive supply die 1	
16	VDD_B	Supply	Positive supply die 2	
EP			Exposed pad	Must be connected to ground

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	DC Supply Voltage at VDD pin	-20	20	V	Not operational
VOUT	External DC voltage at OUT pin	-0.3	20	V	Permanent
VDIFF	DC voltage difference between VDD and OUT	-20	20		
VREGOUT	DC voltage at the VDD3V3 pin	-0.3	5.0	V	
ISCR	Input Current (latch-up immunity)	-100	100	mA	AEC-Q100-004
Continuous Power Dissipation (T_{AMB} = 70°C)					
P_T	Continuous Power Dissipation		300	mW	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±2		kV	AEC-Q100-002

Symbol	Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions					
T_{AMB}	Operating Temperature Range	-40	150	°C	Ambient temperature
T_{STRG}	Storage Temperature Range	-55	125	°C	150°C for 1000h
T_{BODY}	Package Body Temperature		260	°C	The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168 hours

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 8:
Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Positive supply voltage		4.5	5.0	5.5	V
VREG	Regulated Voltage	VDD3V3 should not be loaded by any external DC current	3.3	3.45	3.6	V
IDD_A	Supply current AS5270A	AGC=255 (no magnet placed); 2 times for AS5270A	4		12	mA
IDD_B	Supply current AS5270B	AGC=255 (no magnet placed); 2 times for AS5270B	4		10	mA
ISTART	Supply current at start-up	VREG = 2.25V	2.5	5	10	mA
TSUP	Start-up time	Functional mode			10	ms

Note(s):

1. The given tolerances for external components need to be assured over the whole operation conditions range and also over lifetime. Overall condition: T_{AMB}= -40°C to 150°C, VDD=4.5V to 5.5V; Components spec; unless otherwise noted.

Figure 9:
Electrical System Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CRES	Core resolution				14	bit
ARES	Analog resolution (AS5270A)	Range > 90°			12	bit
DRES	Digital resolution (AS5270B)				12	bit
INLopt	Integral non-linearity (optimum)	Best aligned reference magnet(2) at 25°C over full turn 360°	-0.5		0.5	deg
INLtemp	Integral non-linearity (optimum)	Best aligned reference magnet(2) over temperature -40°C to 150°C over full turn 360°	-0.9		0.9	deg
INL	Integral non-linearity	Best aligned reference magnet* over temperature -40°C to150°C over full turn 360° and displacement	-1.4		1.4	deg
ON	Output noise peak to peak	Static conditions - filter on			1	LSB
ST	Sampling time			125		µs

Note(s):

1. T_{AMB}= -40°C to 150°C, VDD = 4.5V to 5.5V (5Voperation), Magnetic Characterization; unless otherwise noted.
2. Reference magnet: NdFeB, 8 mm diameter, 2.5 mm thickness

Figure 10:
Power Management - Supply Monitor - Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDUVTH	VDD undervoltage upper threshold		3.5	4.0	4.5	V
VDDUVTL	VDD undervoltage lower threshold		3.0	3.5	4.0	V
VDDUV	VDD undervoltage hysteresis		300	500	900	mV
UVDT	VDD undervoltage detection time		10	50	250	µs
UVRT	Undervoltage recovery time		10	50	250	µs
VDDOVTH	VDD overvoltage upper threshold		6.0	6.5	7.0	V
VDDOVTL	VDD overvoltage lower threshold		5.5	6.0	6.5	V
VDDOH	VDD overvoltage hysteresis		300	500	900	V
OVDT	VDD overvoltage detection time	From the time VDD exceeding 5.5V	500	1000	2000	µs
OVRT	VDD overvoltage recovery time	From the time VDD returning from VDD > 5.5V to normal operating voltage (4.5V < VDD < 5.5V)	500	1000	2000	µs
TDETWD	WatchDog error detection time				12	ms

Figure 11:
Magnetic Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bz	Orthogonal magnetic field strength	Required orthogonal component of the magnetic field strength measured at the package surface along a circle of 1.25 mm MFER = 0	30		70	mT
BzE	Orthogonal magnetic field strength –Extended mode	Required orthogonal component of the magnetic field strength measured at the package surface along a circle of 1.25mm MFER = 1	10		90	mT
Disp(2)	Displacement radius	Offset between defined device center and magnet axis. Dependent on the selected magnet.		0.5		mm

Note(s):

1. T_{AMB} = -40° to 150°C, VDD = 4.5V to 5.5V, unless otherwise noted.
2. Reference magnet: NdFeB, 6 mm diameter, 2.5 mm thickness

Figure 12:
Electrical and Timing Characteristics Analog Output (AS5270A)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INLOS	INL output stage		-6		+6	LSB
DNLOS	DNL output stage		-5		+5	LSB
RERR	Ratiometricity error		-0.5%		0.5%	VDD
BVPU	Output voltage broken VDD with pull-up resistor	Pull-up resistor must be in the specified range (see Figure 31)	96		100	%VDD
BGPD	Output voltage broken ground with pull-down resistor	Pull-down resistor must be in the specified range (see Figure 31)	0		4	%VDD
OSSCG	Output short-circuit current GND	OUT = GND	5	10	20	mA
OSSCV	Output short-circuit current VDD	OUT = VDD	-20	-10	-5	mA
OSSDT	Output short-circuit detection time	OUT = GND or OUT = VDD	20	200	600	µs
OSSRT	Output short-circuit recovery time		2	5	20	ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OLCH	Output level clamping high	Output current at OUT pin -3 mA	96			%VDD
OLCL	Output level clamping low	Output current at OUT pin 3 mA			4	%VDD
OSPSR	Output stage positive step response (driver only)	From 0 to 90%VDD, measured at OUT pin, with RPUOUT = 4.7kΩ, CLOAD = 1nF, VDD = 5V			250	µs
OSNSR	Output stage negative step response (driver only)	From VDD to 10%VDD, measured at OUT pin, with RPUOUT = 4.7kΩ, CLOAD = 1nF, VDD = 5V			250	µs
OSTD	Output stage temperature drift	Of value at mid code, info parameter not tested in production	-0.2		0.2	%

Note(s):

1. For each code the ratiometricity error is defined as follows:
   VOUTRATE=((VOUTact – (VOUTtyp*(VDDact/ VDDtyp)))/VDDtyp)*100
   Where
   - VOUTact is the actual output voltage
   - VOUTtyp is the typical output voltage
   - VDDact is the actual supply voltage
   - VDDtyp is the typical supply voltage

Figure 13:
Electrical and Timing Characteristics PWM Output (AS5270B)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PWMSSOCG	Short-circuit output current	OUT = GND	5	10	20	mA
PWMSSOCV	Short-circuit output current	OUT = VDD	-20	-10	-5	mA
PWMSSDT	PWM short-circuit detection time	OUT = GND or OUT = VDD			5	PWM clock cycles
PWMSSRT	PWM short circuit recovery time			6		PWM clock cycles
BKPWMVOH	PWM output voltage high in broken condition	Broken VDD or broken GND, OUT = high, RPU = 10kΩ, PWMVOH=VDD-VOUT	0		0.4	V
BKPWMVOL	PWM output voltage low in broken condition	Broken VDD or broken GND, OUT = low, RPD = 10kΩ	0		0.4	V
PWMF7	PWM frequency	PWMFR = 111	112.5	125	137.5	Hz
PWMF6	PWM frequency	PWMFR = 110	180	200	220	Hz
PWMF5	PWM frequency	PWMFR = 101	225	250	275	Hz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PWMF4	PWM frequency	PWMFR = 100	360	400	440	Hz
PWMF3	PWM frequency	PWMFR = 011	450	500	550	Hz
PWMF2	PWM frequency	PWMFR = 010	720	800	880	Hz
PWMF1	PWM frequency	PWMFR = 001	900	100	1100	Hz
PWMF0	PWM frequency	PWMFR = 000	1800	2000	2200	Hz
PWMVOH	PWM output voltage level high	IOUT = 5 mA, PWMVOH = VDD - VOUT	0		0.4	V
PWMVOL	PWM output voltage level low	IOUT = 5 mA	0		0.4	V
PWMSRF	PMM slew rate fast	Between 25% and 75% of VDD, RPUOUT = 4.7kΩ, CLOUT1 = 1nF, PWMSR = 0	1	2	4	V/µs
PWMSRS	PMM slew rate slow	Between 25% and 75% of VDD, RPUOUT = 4.7kΩ, CLOUT1 = 1nF, PWMSR = 1	0.5	1	2	V/µs

Timing Characteristics

Figure 14:
Electrical and Timing Characteristics SENT Output (AS5270B)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SENTSSOC	SENT short-circuit output current	OUT = 20V	10	20	40	mA
SENTSSOC	SENT short-circuit output current	OUT = 0V	-40	-20	-10	mA
BKSENTVOH	SENT output voltage in broken condition	Broken VDD or broken GND, RPU = 50kΩ, SENT constantly high	0		1.2	V
SENTVOH	SENT output voltage high		4.1			
SENTVOL	SENT output voltage low				0.5	V
SENTFT	SENT fall time				6.5	µs
SENTRT	SENT rise time				18	µs

Figure 15:
Electrical and Timing Characteristics UART Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UARTVIH	UART high level input voltage		70			%VDD
UARTVIL	UART low level input voltage				30	%VDD
UARTVOH	UART high level output voltage		VDD - 0.5V			V
UARTVOL	UART low level output voltage				0.5	V
UARTBRLIM	UART Baud rate		2400		9600	Baud

Detailed Description

The AS5270 is a Hall-based rotary magnetic position sensor using a CMOS technology. The lateral Hall sensor array converts the magnetic field component perpendicular to the surface of the chip into a voltage.

The signals coming from the Hall sensors are first amplified and filtered before being converted by the analog-to-digital converter (ADC). The output of the ADC is processed by the CORDIC block (Coordinate-Rotation Digital Computer) to compute the angle and magnitude of the magnetic field vector. The sensor and analog front-end (AFE) section works in a closed loop alongside an AGC to compensate for temperature and magnetic field variations. The calculated magnetic field strength (MAG), the automatic gain control (AGC) and the angle can be read through the output pin (OUT) in UART mode.

The magnetic field coordinates provided by the CORDIC block are fed to a digital filter which reduces noise. A linearization block generates the transfer function, including linearization. The AS5270 is available with three different output interfaces: analog ratiometric (AS5270A), digital PWM or SENT (AS5270B).

The output of the AS5270 can be programmed to define a starting position (zero angle) and a stop position (maximum angle). An embedded linearization algorithm allows reducing the system INL error due, for example, to mechanical misalignment, magnet imperfections, etc.

The AS5270 can be programmed through the OUT pin with a UART interface which allows writing an on-chip non-volatile memory (OTP) where the specific settings are stored. The AS5270 can be programmed by the **ams** programming tool, both at the component and board level.

Register Description

Figure 16:
Non-Volatile Memory Register Description

Address	Bit Position	Field	Description
0x0A	7:0	CUSTID0	Customer ID byte 0
0x0B	7:0	CUSTID1	Customer ID byte 1
0x0C	7:0	CUSTID2	Customer ID byte 2
0x0D	7:0	CUSTID3	Customer ID byte 3
0x0E	0	PWMINV	PWM inverted
	1	PWMSR	PWM slew rate (0 = PWM slew rate fast PWMSRF, 1 = PWM slew rate slow PWMSRS)
	3:2	DIGOS	Digital output stage (00 = PWM push-pull 01 = PWM pull-down 10 = PWM pull-up 11 = SENT) It applies to the AS5710B only
	6:4	RBKDEB	Read-back debouncing
	7	n.a	No use
0x0F	0	FBS	Failure band selection (0 = lower failure band, 1 = upper failure band)
	2:1	HYST	Hysteresis across the brake point
	4:3	QUAD	Quadrant selection
	7:5	PWMFR	PWM frequency selection
0x10	1:0	PWMRTH	PWM rising threshold tbd
	3:2	PWMFTH	PWM falling threshold tbd
	7:4	SENTMID	SENT Message ID
0x11	4:0	SENTTK	SENT tick
	5	SENTESM	Enable SENT serial message
	6	SENTPP	SENT pause pulse enable (0 = disable, 1 = enable)
	7	SENTRC	SENT rolling counter enable (0 = disable, 1 = enable)
0x12	3:0	n.a	No use. Default 0
	7:4	n.a	No use. Default 0

Address	Bit Position	Field	Description
0x13	3:0	n.a	No use. Default 0
	7:4	n.a	No use. Default 0
0x14	7:0	CLMPH	Clamping level high Reg 0x14[0] =LSB Reg 0x15[3]=MSN
0x15	3:0		
	7:4	CLMPL	Clamping level low Reg 0x15[4] =LSB Reg 0x16[7]=MSN
0x16	7:0		
0x17	7:0	PPOFFSET	Post processing offset Reg 0x17[0] =LSB Reg 0x19[3]=MSB
0x18	7:0		
0x19	3:0		
	7:4	PPGAIN	Post processing gain Reg 0x19[4] =LSB Reg 0x1B[3]=MSB
0x1A	7:0		
0x1B	4:0		
	7:5	BP	Break point Reg 0x1B[5] =LSB Reg 0x1D[2]=MSB
0x1C	7:0		
0x1D	2:0		
	3	MFER	Magnetic field extended range (1 = Bz, 0= BzE)
	4	AER	Angle extended range (set to 1 if the maximum angle excursion is smaller than 22 degree)
	6:5	FILTER	Post processing filter
	7	CUSLOCK	Customer settings lock
0x1E	7:0	SIGN	Signature for error correction code

Figure 17:
Volatile Memory Register Description

Address	Bit Position	Field	R/W	Description
0x22	7:0	DAC12IN	R/W	Input word of the 12-bit output DAC (Reg0x23[3] = MSB, Reg0x22[0] = LSB)
0x23	3:0		R/W	
	4	DAC12INSEL	R/W	DAC 12 input buffer selection
	5	DSPRN	R/W	Digital signal processing reset
	6	GLOAD	R/W	Enable of gload
	7	-	-	Not used
0x32	7:0	ANGLECORDIC	R	Angle of the CORDIC output block. (Reg0x33[5] = MSB, Reg0x32[0] = LSB)
0x33	5:0			
	7:6	-	-	Not used
0x34	7:0	MAG	R	CORDIC magnitude
0x35	7:0	AGC	R	AGC value
0x36	7:0	ANGLEFILTER	R	Angle of the digital filter output block (Reg0x37[3] = MSB, Reg0x36[0] = LSB)
0x37	3:0			
0x37	7:4	-	-	Not used

Figure 18:
Special Functions

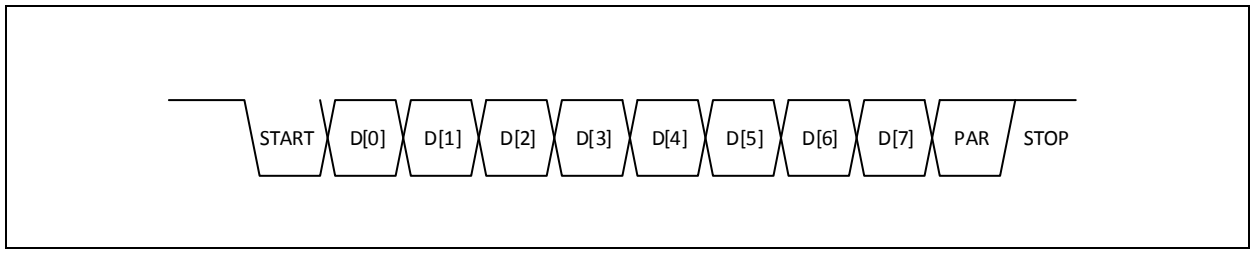
Address	Bit Position	Field	Description
0x60	7:0	P2F	Pass-to-functions, see UART
0x61	7:0		
0x62	7:0	BURNOTP	Permanently burn OTP, see UART
0x63	7:0		

UART Interface

The AS5270 is equipped with a UART interface, which allows reading and writing the registers as well as permanently programming the non-volatile memory (OTP). By default (factory setting) the AS5270 is in the so-called *Communication Mode* and the UART is connected at the output pin (OUT). In this mode, it is possible to configure the register settings. In this mode, the device is in open-drain mode and therefore a pull-up resistor has to be connected on the output.

The UART interface allows reading and writing two consecutive addresses. The standard UART sequence consists of four frames. Each frame begins with a start bit (START), which is followed by 8 data bits (D[0:7]), one parity bit (PAR), and a stop bit (STOP), as shown in Figure 19.

Figure 19:
UART Frame



The PAR bit is even parity calculated over the data bits (D[0:7]). Each frame is transferred from LSB to MSB.

The four frames are shown in Figure 20.

Figure 20:
UART Frame Sequence

Frame Number	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
1	0x55							
2	R/W	ADDRESS						
3	DATA1							
4	DATA2							

The first frame is the synchronization frame and consists of D[0:7] = 0xAA followed by the parity bit (PAR=0) and the stop bit. This frame synchronizes the baud rate between the AS5270 and the host microcontroller.

The second frame contains the read/write command (D[7] = 0 Write, D[7] = 1 Read) and the address of the register (D[6:0] = ADDRESS).

The content of the third and fourth frames (DATA1 and DATA2) will be written to or read from the location specified by ADDRESS and ADDRESS+1, respectively.

Figure 21 and Figure 22 show examples of read and write.

Figure 21:
Example of Write (Reg[0x22] = 0x18, Reg[0x23] = 0xA2)

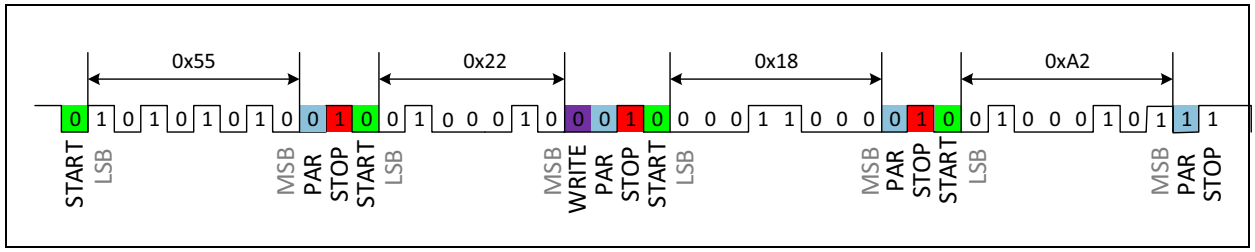
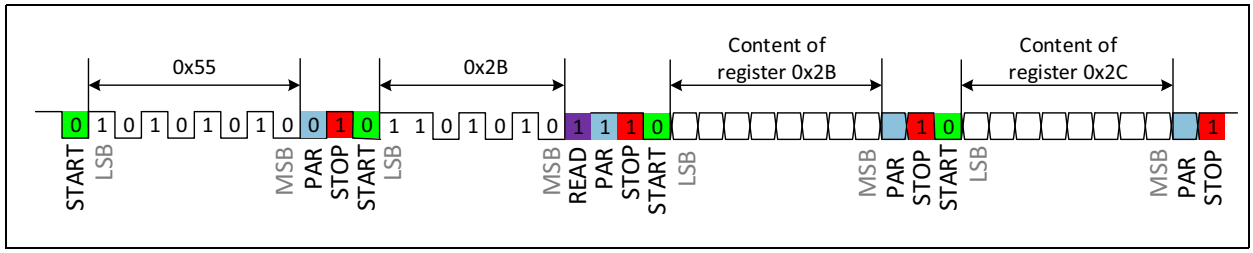


Figure 22:
Example of Read (Reg[0x2B], Reg[0x2C])



Exiting Communication Mode

Communication mode is exited and operational mode is entered with a Pass-to-function (P2F) command, by writing to the virtual registers 0x60 and 0x61:

P2F: write(0x60) = 0x70, write(0x61) = 0x51

No more commands can be sent after sending this command, because the device is permanently placed in operational mode.

Burning the OTP Registers

The BURNOTP command writes the OTP registers with their programmed values. The command is issued by writing to virtual registers 0x62 and 0x63:

BURNOTP: write(0x62) = 0x70, write(0x63) = 0x51

Customer ID

A specific identifier chosen by the user can be stored in the non-volatile memory. This identifier consists of 4 bytes and can be stored in the locations CUSTID0, CUSTID1, CUSTID2, and CUSTID3.

Output Linear Transfer Function

A linear transfer function controls the state of the output in response to the absolute orientation of the external magnet. The parameters which control this function are shown in Figure 24.

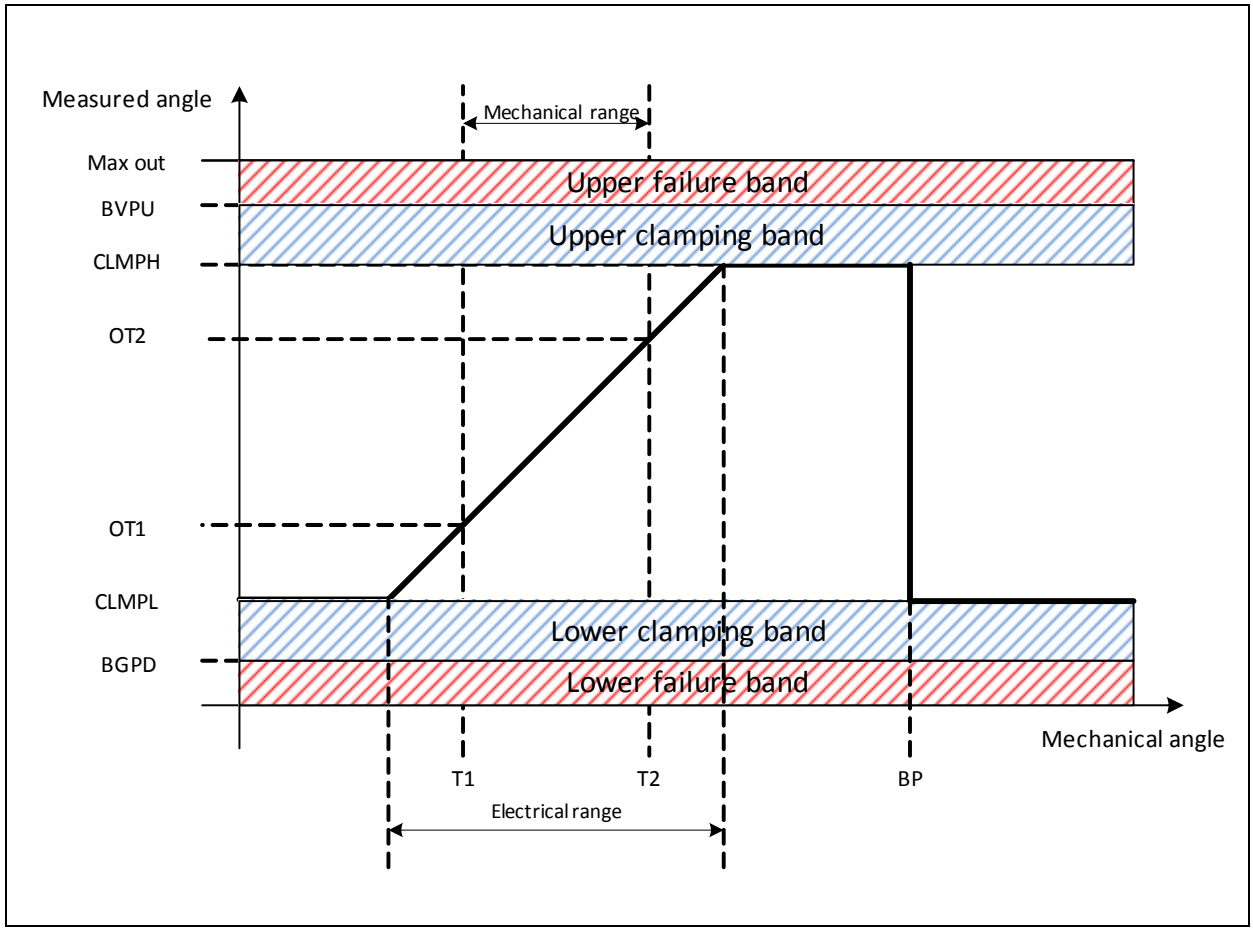
Figure 23:
Transfer Function Control Parameters

Symbol	Parameter	Resolution [bit]
T1	Mechanical angle starting point	14
T2	Mechanical angle stop point	14
OT1	Output at the starting point (T1)	12
OT2	Output at the stop point (T2)	12
CLMPL	Clamping level low	12
CLMPH	Clamping level high	12
BP	Breakpoint	14

As shown in the Figure 24, the parameters T1, T2, OT1, and OT2 define the input-to-output linear transfer function. The dedicated programmer for the AS5270 uses the parameters from Figure 23 to generate the corresponding settings CLMPL, CLMPHH, PPOFFSET, PPGAIN and BP (see Figure 24).

The clamping level parameters CLMPL and CLMPH define the absolute minimum and maximum level of the output. Both clamping levels can be set with the 9 LSBs out of the 12-bit output resolution. This means that the maximum value for CLMPL is one eighth, while CLMPH minimum value is seven-eighths of the output diagnostic. CLMPL and CLMPH must always be set outside of the lower and upper diagnostic failure band defined by the output broken wire voltage (see Figure 24: BGPD and BVPU).

Figure 24:
Output Transfer Function



The breakpoint BP sets the discontinuity point where the output jumps from one clamping level to the other. It is strongly recommended to set the breakpoint at the maximum distance from the start and stop position (T1 and T2). To handle the case of a full turn, a hysteresis function across the breakpoint can be used to avoid sudden jumps between the lower and upper clamping level.

Figure 25:
Hysteresis Setting

HYST	Hysteresis LSBs
00	0
01	56
10	91
11	137

The hysteresis LSB is based on the core resolution (14-bit). The AS5270 features a programmable digital filter. As shown in Figure 25 in a static condition (no change of the input), the static error band is ±0.5 LSB (at 12-bit resolution). Whenever an input step occurs, the output (measured angle) follows the input (mechanical angle) entering a certain error band within the step response time. From the time when the output is within the static error band the output takes 1000 ms to settle to the static error band achieving again ±0.5 LSB output noise. The filter is not usable in 360° range, if the Hysteresis setting is on.

Figure 26:
Step Response

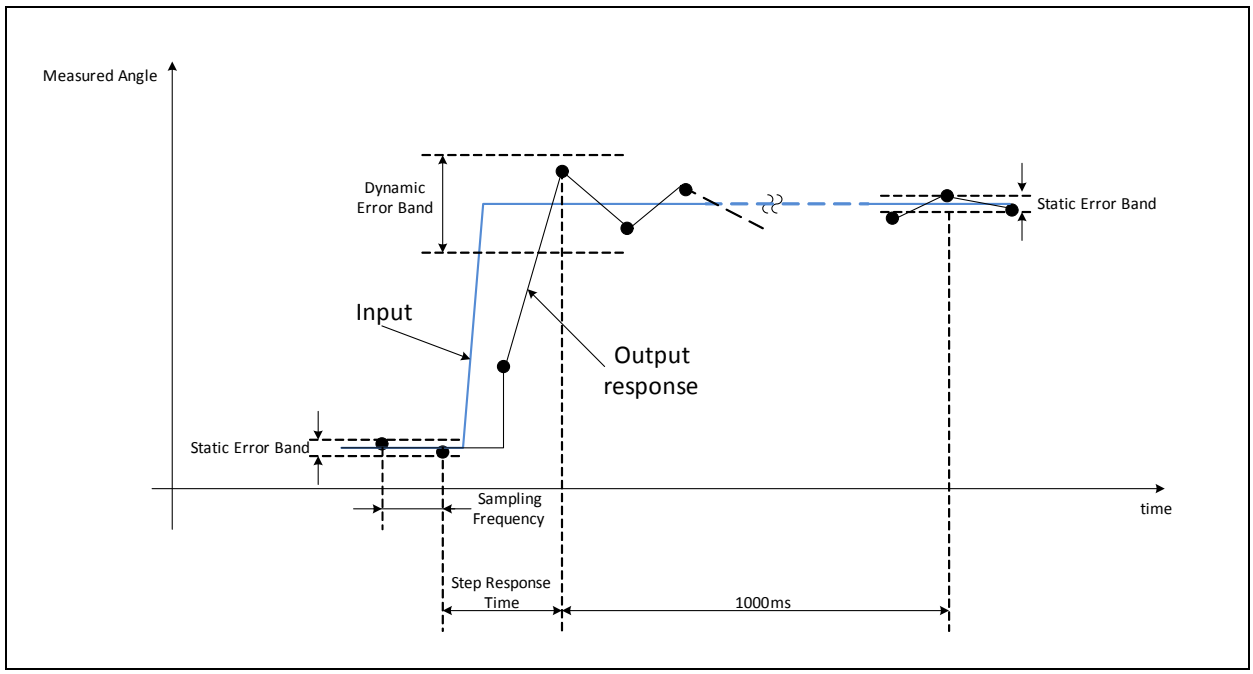


Figure 27:
FILTER Setting

FILTER	Dynamic Error Band [LSB]	Step Response Time [µs]
00	Filter off	Not applicable
01	23	5 CORDIC cycles

The FBS setting allows selecting the failure band (lower or upper) when the output goes into diagnostic mode.

Multiple Quadrants

The multiple quadrants option allows repeating the same output control parameters up to 4 times over the full turn rotation as shown in the Figure 29, Figure 30, and Figure 31. The QUAD parameter sets the number of quadrants, as shown in the Figure 28.

Figure 28:
Number of Quadrants

QUADEN	Number of Quadrants
00	Single
01	Double
10	Triple
11	Quadruple

Figure 29:
Dual Quadrant Mode

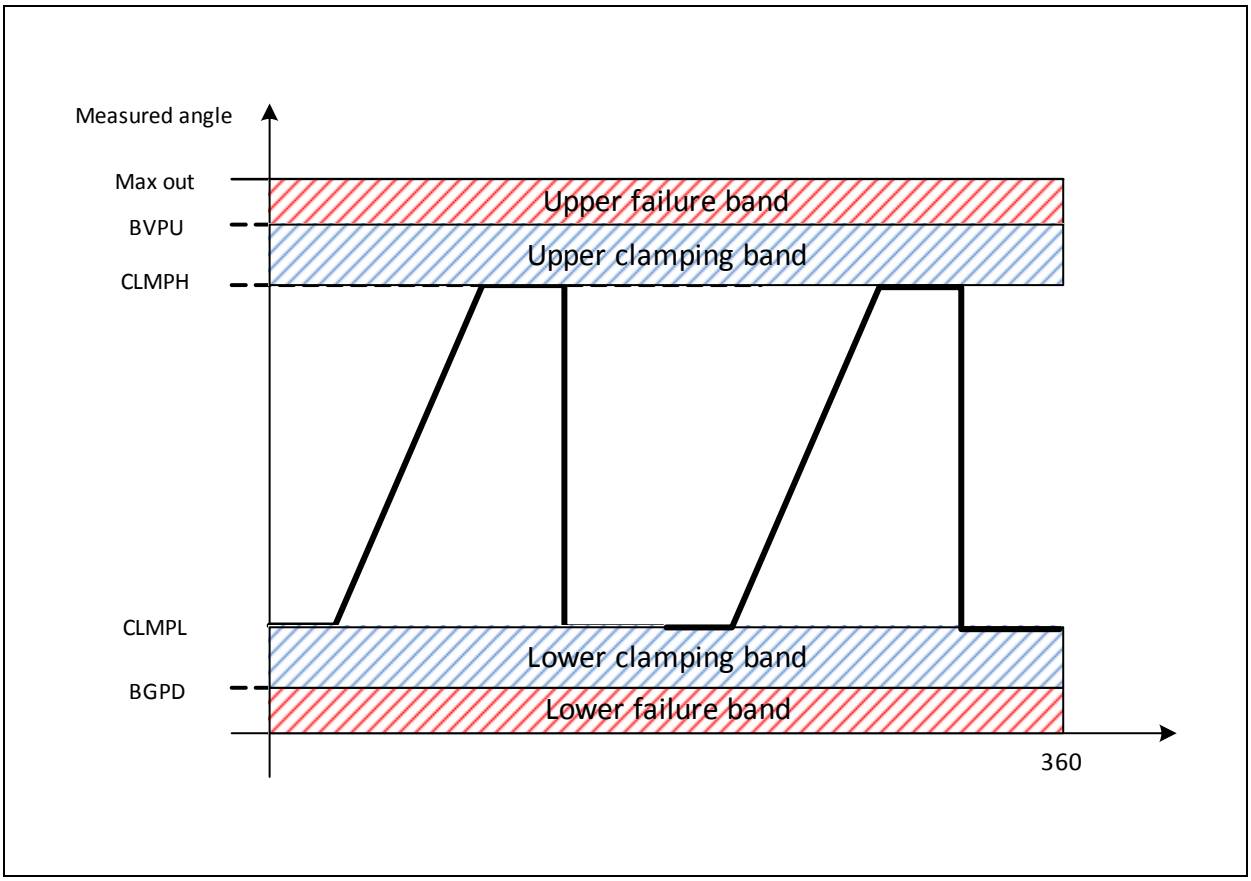


Figure 30:
Triple Quadrant Mode

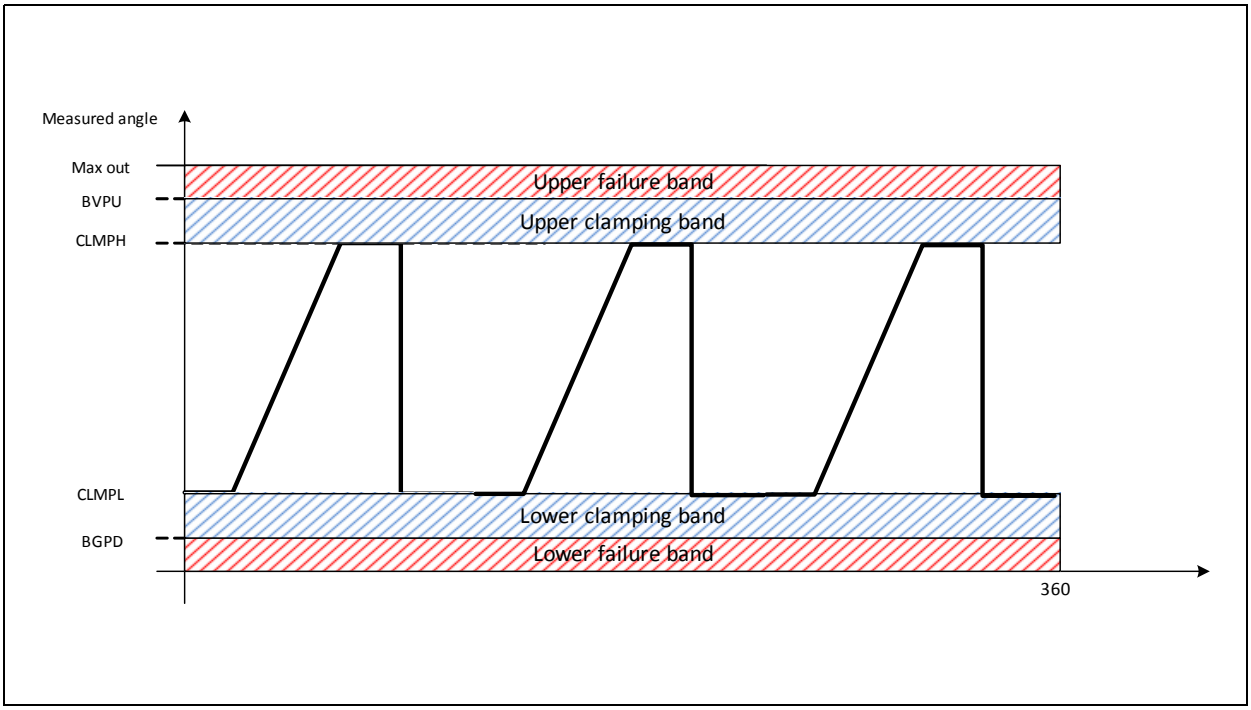
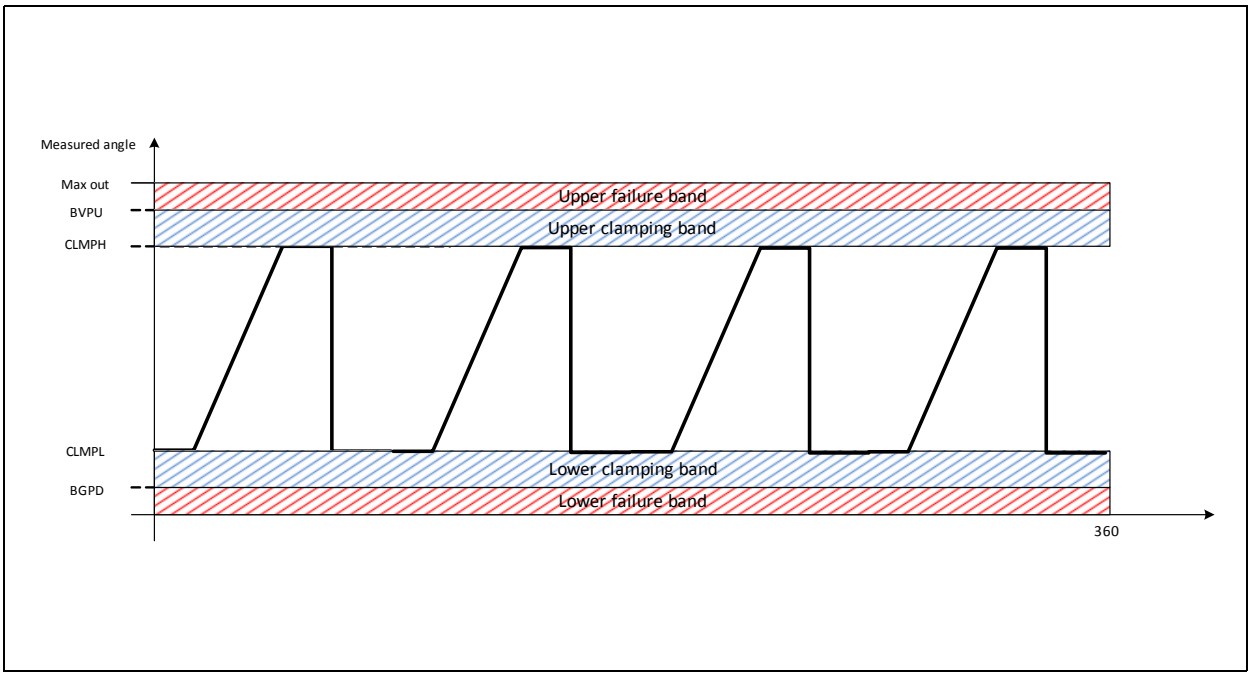


Figure 31:
Quadruple Quadrant Mode



Extended Magnetic Input Range

The magnetic input field range can be boosted with the MFER bit. The extended magnetic field allows increasing the maximum air gap between the AS5270 and the magnet.

More information can be found in the Application Note.

Analog Output (AS5270A)

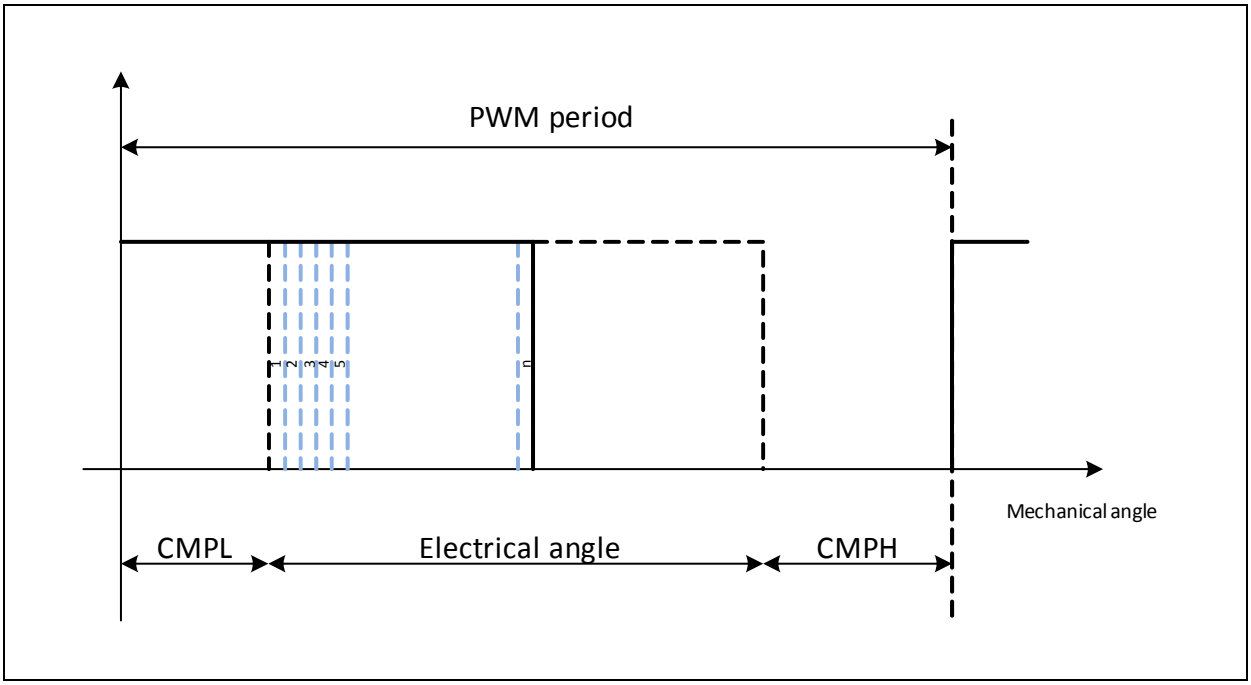
The AS5270A provides a linear analog ratiometric output signal. The output buffer features a push-pull analog output stage which can be loaded with a pull-down or a pull-up resistor. The output voltage represents the angular orientation of the magnet above the AS5270A on a linear absolute scale and is ratiometric to VDD.

PWM Output (AS5270B)

The AS5270B has a PWM output. With the DIGOS setting, the PWM output stage can be programmed as a push-pull, pull-down, or pull-up driver. The duty-cycle of each pulse is proportional to the absolute anglar position of the external magnet.

The PWM signal consists of a frame of 4096 clock periods as shown in Figure 32. The PWM frame begins with a certain number of clocks high, defined by the CLMPL, which is followed by the electrical angle information. The frame ends with a certain number of clock pulses low, as defined by the CLMPH. It is possible to invert the frame using the PWMINV setting.

Figure 32:
Pulse Width Modulation Frame



The PWMFR setting sets the duration of the PWM frequency.

The PWMSR setting chooses between fast and slow steps.