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AS5601

12-Bit Programmable Contactless Encoder

General Description

The AS5601 is an easy-to-program magnetic rotary position sensor with incremental quadrature (A/B) and 12-bit digital outputs. Additionally, the PUSH output indicates fast airgap changes between the AS5601 and magnet which can be used to implement a contactless pushbutton function in which the knob can be pressed to move the magnet toward the AS5601.

This AS5601 is designed for contactless encoder applications, and its robust design rejects the influence of any homogenous external stray magnetic fields.

Based on planar Hall sensor technology, this device measures the orthogonal component of the flux density (Bz) from an external magnet.

The industry-standard I^2C interface supports user programming of non-volatile parameters in the AS5601 without requiring a dedicated programmer.

The AS5601 also provides a smart low-power mode which automatically reduces power consumption

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5601, 12-bit Programmable Contactless Encoder are listed below:

Figure 1:
Added Value of Using AS5601

Benefits	Features
• Highest reliability and durability	• Contactless angle measurement insensitive to dust and dirt
• Simple programming	• Simple user-programmable zero position and device configuration
• Flexible choice of the number of A/B pulses per revolution	• Quadrature output configurable from 8 up to 2048 positions
• Contactless pushbutton functionality	• Pushbutton output by detecting sudden airgap changes
• Low power consumption	• Automatic entry into low-power mode
• Easy setup	• Automatic magnet detection
• Small form factor	• SOIC-8 package
• Robust environmental tolerance	• Wide temperature range: -40°C to 125°C

Applications

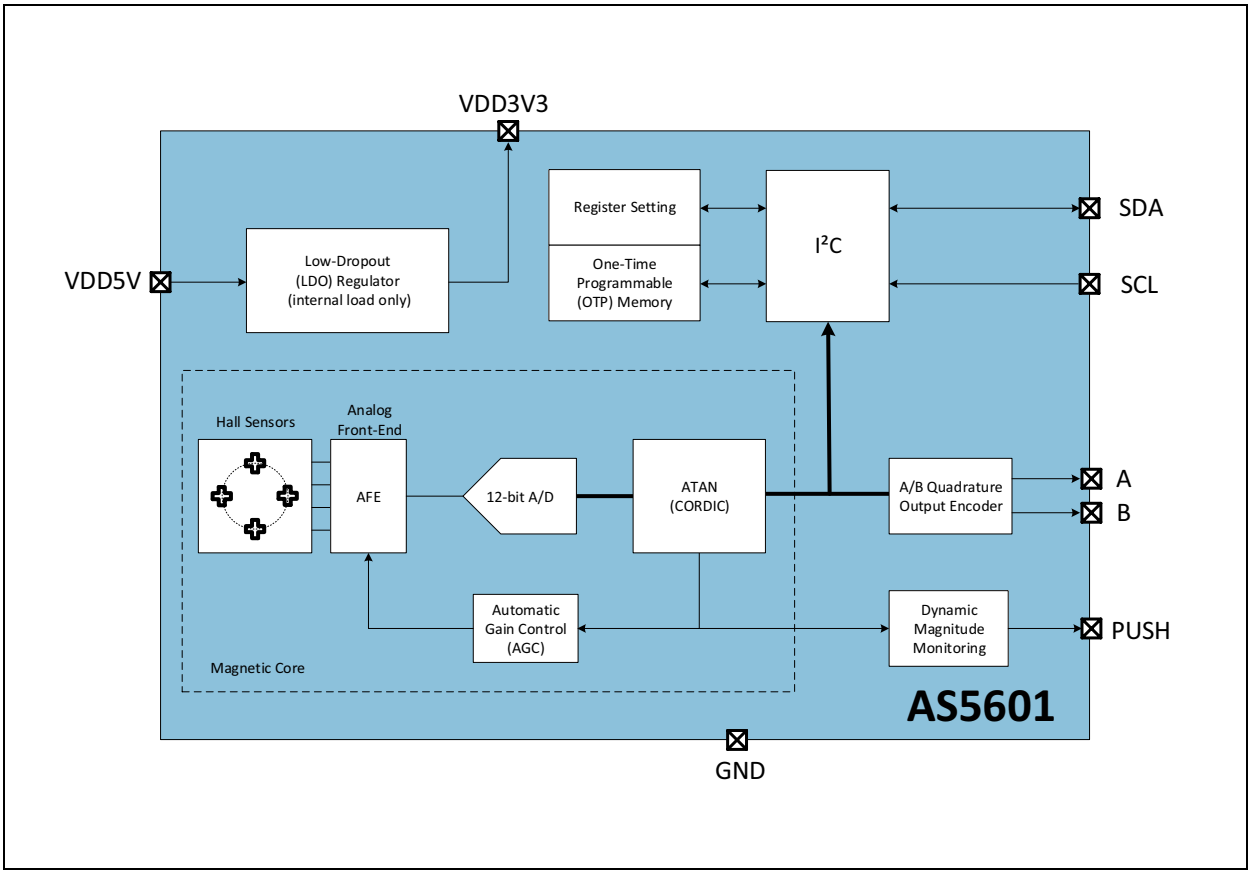
The AS5601 is ideally suited for:

- Encoder replacement
- Contactless rotary knobs with push buttons
- Other angular position measurement solutions

Block Diagram

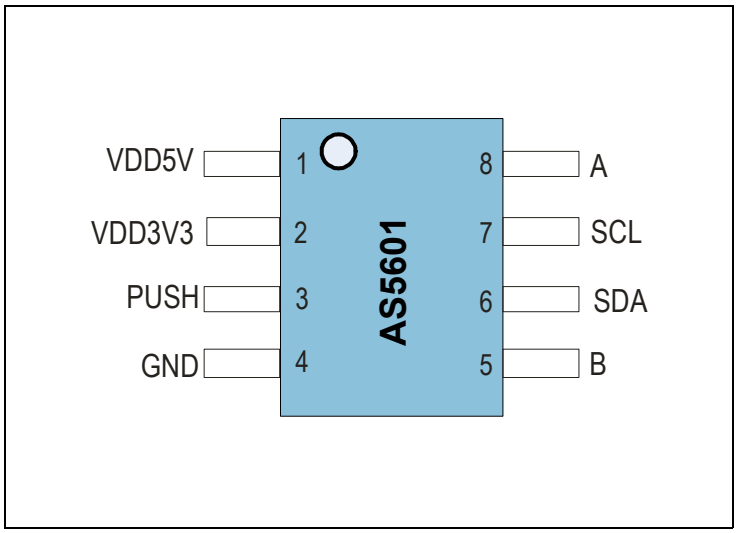
The functional blocks of this device are shown below:

Figure 2:
AS5601 Block Diagram



Pin Assignments

Figure 3:
SOIC-8 Pin-Out



Pin Description

Figure 4:
Pin Description

Pin Number	Name	Type	Description
1	VDD5V	Supply	Positive voltage supply in 5V mode
2	VDD3V3	Supply	Positive voltage supply in 3.3V mode (requires an external 1-µF decoupling capacitor in 5V mode)
3	PUSH	Digital output	Contactless pushbutton function output
4	GND	Supply	Ground
5	B	Digital output	Quadrature incremental signal B
6	SDA	Digital input/output	I^2C Data
7	SCL	Digital input	I^2C Clock
8	A	Digital output	Quadrature incremental signal A

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD5V	DC supply voltage at VDD5V pin	-0.3	6.1	V	5.0V operation mode
VDD3V3	DC supply voltage at VDD3V3 pin	-0.3	4.0	V	3.3V operation mode
VAIO	Voltage at all digital or analog pins	-0.3	VDD + 0.3	V	
I_{SCR}	Input current (latch-up immunity)	-100	100	mA	JESD78
Continuous Power Dissipation (T_A = 70°C)					
P_T	Continuous power dissipation		50	mW	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge HBM (human body model)	±1		kV	MIL 883 E method 3015.7
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage temperature range	-55	125	°C	
T_{BODY}	Package body temperature		260	°C	ICP/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn)
RH_{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level	3			ICP/JEDEC J-STD-033

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Operating Conditions

Figure 6:
System Electrical Characteristics and Temperature Range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD5V	Positive supply voltage in 5.0V mode	5.0V operation mode	4.5	5.0	5.5	V
		During OTP burn procedure(2)				
VDD3V3	Positive supply voltage in 3.3V mode	3.3V operation mode	3.0	3.3	3.6	V
		During OTP burn procedure(2)	3.3	3.4	3.5	V
IDD	Supply current in NOM (1)	PM = 00 Always on			6.5	mA
IDD_LPM1	Supply current in LPM1 (1)	PM = 01 Polling time = 5 ms			3.4	mA
IDD_ LPM2	Supply current in LPM2 (1)	PM = 10 Polling time = 20 ms			1.8	mA
IDD_ LPM3	Supply current in LPM3 (1)	PM = 11 Polling time = 100 ms			1.5	mA
IDD_BURN	Supply current per bit for burn procedure	Initial peak, 1 µs			100	mA
		Steady burning, <30 µs			40	mA
T_A	Operating temperature		-40		125	°C
T_P	Programming temperature		20		30	°C

Note(s):

1. For typical magnetic field (60 mT) excluding current delivered to the external load and tolerance on polling times.
2. For OTP burn procedure the supply line source resistance should not exceed 1Ohm.

Digital Inputs and Outputs

Figure 7:
Digital Inputs and Outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_IH	High-level input voltage		0.7 × VDD			V
V_IL	Low-level input voltage				0.3 × VDD	V
V_OH	High-level output voltage		VDD - 0.5			V
V_OL	Low-level output voltage				0.4	V
I_O	Output current for A, B, and PUSH		-2		2	mA
C_L	Capacitive load for A, B, and PUSH				50	pF
I_LKG	Leakage current				±1	µA

Timing Characteristics

Figure 8:
Timing Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_DETWD	Watchdog detection time	WD = 1	57	60	63	seconds
T_PU	Power-up time				10	ms
F_S	Sampling rate				150	µs
T_SETTL1	Settling time	SF = 00			2.2	ms
T_SETTL2	Settling time	SF = 01			1.1	ms
T_SETTL3	Settling time	SF = 10			0.55	ms
T_SETTL4	Settling time	SF = 11			0.286	ms

Magnetic Characteristics

Figure 9:
Magnetic Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Bz	Orthogonal magnetic field strength, regular output noise ON_SLOW and ON_FAST	Required orthogonal component of the magnetic field strength measured at the die's surface along a circle of 1 mm	30	60	90	mT
Bz_ERROR	Minimum required orthogonal magnetic field strength, magnet detection level				8	mT

System Characteristics

Figure 10:
System Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Core Resolution			12		bit
RES_AB	A/B output resolution		8		2048	positions
VMAX_AB	Maximum rotation speed for incremental output	Continuous Rotation ≥ 360deg (1), (2)			456	rpm
INL_BL	System INL	Deviation from best line fit; 360° maximum angle, no magnet displacement, no zero-programming performed			±1	degree
ON_SLOW	RMS output noise (1 sigma)	Orthogonal component for the magnetic field within the specified range Bz, after 2.2 ms; SF = 00			0.015	degree
ON_FAST	RMS output noise (1 sigma)	Orthogonal component for the magnetic field within the specified range Bz, after 286 µs; SF = 11			0.043	degree

Note(s):

1. An infinite fast change <180deg results in angle output with maximum configured update frequency.
2. An infinite fast change >= 180deg results in angle output to the shortest next absolute position with maximum configured update frequency. e.g. A change from 0 to 270deg will be indicated as angle output from 0 to -90deg.

Detailed Description

The AS5601 is a Hall-based rotary magnetic position encoder that converts the magnetic field component perpendicular to the surface of the chip into voltages which are used to produce incremental A/B outputs and absolute position indication in registers that can be read over an industry-standard I^2C bus.

The analog signals from the Hall sensors are first amplified and filtered before being converted by the analog-to-digital converter (ADC) into binary data. The output of the ADC is processed by the hardwired CORDIC block (Coordinate Rotation Digital Computer) to compute the angle and magnitude of the magnetic field vector. The intensity of the magnetic field is used by the automatic gain control (AGC) to adjust the amplification level to compensate for temperature and magnetic field variations.

The angle value provided by the CORDIC algorithm is used by the internal logic to generate the incremental quadrature signals A and B. The magnitude and AGC value is dynamically monitored and generates the PUSH output for fast changes of the airgap between the magnet and the AS5601. Very slow changes are suppressed to provide a robust and reliable pushbutton output that tolerates temperature variation and magnet degradation.

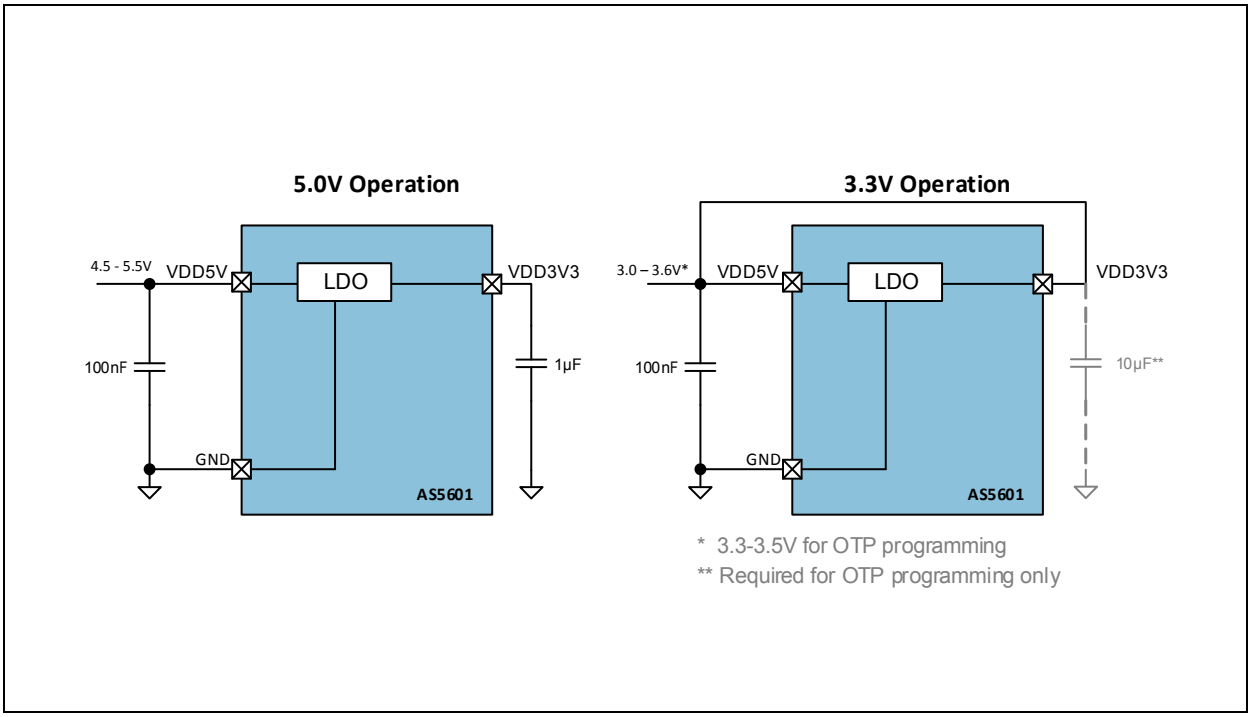
The AS5601 is programmed through an industry-standard I^2C interface to write an on-chip one-time programmable (OTP) memory. This interface can be used to program a zero angle and to configure the chip.

Power Management

The AS5601 is powered from a 5.0V supply using the on-chip LDO regulator, or it can be powered directly from a 3.3V supply. The internal LDO is not intended to power other external ICs and needs a 1µF capacitor to ground, as shown in Figure 11.

In 3.3V operation, the VDD5V and VDD3V3 pins must be tied together. VDD is the voltage level present at the VDD5V pin.

Figure 11:
5.0V and 3.3V Power Supply Options



I²C Interface

The AS5601 supports the 2-wire Fast-mode Plus I²C-slave protocol in device mode, in compliance with the NXP Semiconductors (formerly Philips Semiconductors) specification UM10204. A device that sends data onto the bus is a transmitter and a device receiving data is a receiver. The device that controls the message is called a master. The devices that are controlled by the master are called slaves. A master device generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions that control the bus. The AS5601 always operates as a slave on the I²C bus. Connections to the bus are made through the open-drain I/O lines SDA and the input SCL. Clock stretching is not included.

The host MCU (master) initiates data transfers. The 7-bit slave address of the AS5601 is 0x36 (0110110 in binary).

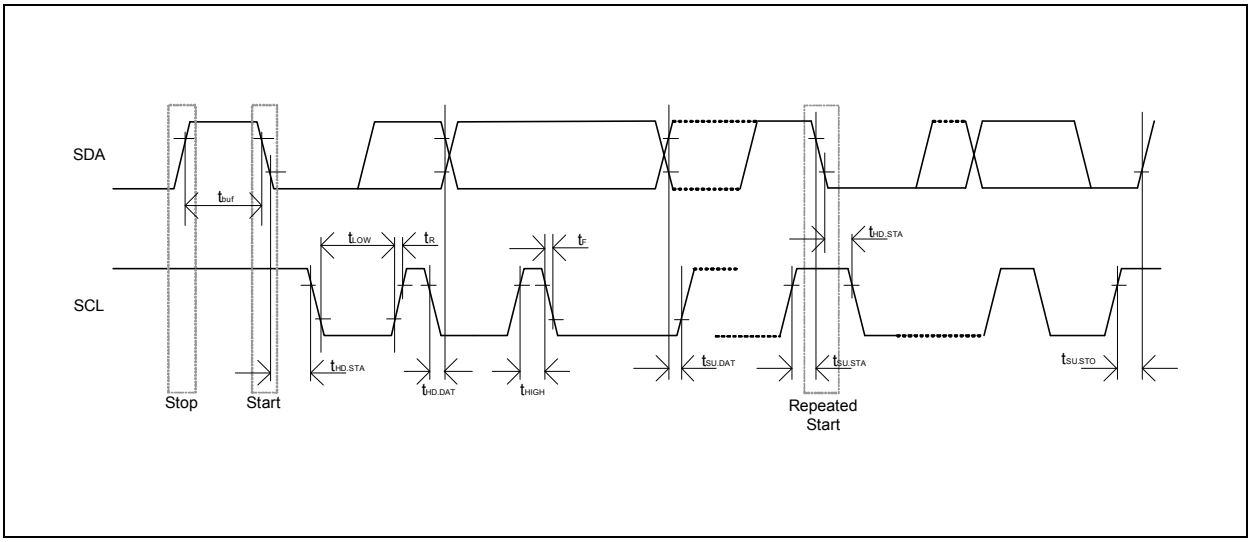
Supported Modes

- Random/Sequential read
- Byte/Page write
- Automatic increment (ANGLE register)
- Standard-mode
- Fast-mode
- Fast–mode Plus

The SDA signal is the bidirectional data line. The SCL signal is the clock generated by the I²C bus master to synchronize sampling data from SDA. The maximum SCL frequency is 1 MHz. Data is sampled on the rising edge of SCL.

I²C Interface Operation

Figure 12:
I²C Electrical Specifications



I²C Electrical Specification

Figure 13:
I²C Electrical Specifications

Symbol	Parameter	Conditions	Min	Max	Units
VIL	Logic low input voltage		-0.3	0.3 x VDD	V
VIH	Logic high input voltage		0.7 x VDD	VDD + 0.3	V
VHYS	Hysteresis of Schmitt trigger inputs	VDD > 2.5V	0.05 x VDD		V
VOL	Logic low output voltage (open-drain or open-collector) at 3 mA sink current	VDD > 2.5V		0.4	V
IOL	Logic low output current	VOL = 0.4V	20		mA
t_{OF}	Output fall time from VIHmax to VILmax		10	120 (1)	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter			50 (2)	ns
I_I	Input current at each I/O Pin	Input voltage between 0.1 x VDD and 0.9 x VDD	-10	+10 (3)	µA
C_B	Total capacitive load for each bus line			550	pF
$C_{I/O}$	I/O capacitance (SDA, SCL) (4)			10	pF

Note(s):

1. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used this has to be considered for bus timing.
2. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
3. I/O pins of Fast-mode and Fast-mode Plus devices must not load or drive the SDA and SCL lines if VDD is switched OFF.
4. Special-purpose devices such as multiplexers and switches may exceed this capacitance because they connect multiple paths together.

I²C Timing

Figure 14:
I²C Timing

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCLK}	SCL clock frequency			1.0	MHz
t_{BUF}	Bus free time (time between the STOP and START conditions)		0.5		µs
$t_{HD;STA}$	Hold time; (Repeated) START condition (1)		0.26		µs
t_{LOW}	Low phase of SCL clock		0.5		µs
t_{HIGH}	High phase of SCL clock		0.26		µs
$t_{SU;STA}$	Setup time for a Repeated START condition		0.26		µs
$t_{HD;DAT}$	Data hold time (2)			0.45	µs
$t_{SU;DAT}$	Data setup time (3)		50		ns
t_R	Rise time of SDA and SCL signals			120	ns
t_F	Fall time of SDA and SCL signals		10	120 (4)	ns
$t_{SU;STO}$	Setup time for STOP condition		0.26		µs

Note(s):

1. After this time, the first clock is generated.
2. A device must internally provide a minimum hold time of 120 ns (Fast-mode Plus) for the SDA signal (referred to the VIH_{min} of SCL) to bridge the undefined region of the falling edge of SCL.
3. A Fast-mode device can be used in a standard-mode system, but the requirement $t_{SU;DAT}$ = 250 ns must be met. This is automatic if the device does not stretch the low phase of SCL. If such a device does stretch the low phase of SCL, it must drive the next data bit on SDA ($t_{Rmax} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns) before SCL is released.
4. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, this has to be considered for bus timing.

I²C Modes

Invalid Addresses

There are two addresses used to access an AS5601 register. The first is the slave address used to select the AS5601. All I²C bus transactions include a slave address. The slave address of the AS5601 is 0x36 (0110110 in binary). The second address is a word address sent in the first byte transferred in a write transaction. The word address selects a register on the AS5601. The word address is loaded into the address pointer on the AS5601. During subsequent read transactions and subsequent bytes in the write transaction, the address pointer provides the address of the selected register. The address pointer is incremented after each byte is transferred, except for certain read transactions to special registers.

If the user sets the address pointer to an invalid word address, the address byte is not acknowledged (the A bit is high). Nevertheless, a read or write cycle is possible. The address pointer is increased after each byte.

Reading

When reading from an invalid address, the AS5601 returns all zeros in the data bytes. The address pointer is incremented after each byte. Sequential reads over the whole address range are possible including address overflow.

Automatic increment of the address pointer for ANGLE, RAW ANGLE, and MAGNITUDE registers:

These are special registers which suppress the automatic increment of the address pointer on reads, so a re-read of these registers requires no I²C write command to reload the address pointer. This special treatment of the pointer is effective only if the address pointer is set to the high byte of the register.

Writing

A write to an invalid address is not acknowledged by the AS5601, although the address pointer is incremented. When the address pointer points to a valid address again, a successful write accessed is acknowledged. Page write over the whole address range is possible including address overflow.

Supported Bus Protocol

Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever SCL is high. Changes in the data line while SCL is high are interpreted as START or STOP conditions.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both SDA and SCL remain high.

Start Data Transfer

A change in the state of SDA from high to low while SCL is high defines the START condition.

Stop Data Transfer

A change in the state of SDA from low to high while SCL is high defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, SDA is stable for the duration of the high phase of SCL. The data on SDA must only be changed during the low phase of SCL. There is one clock period per bit of data.

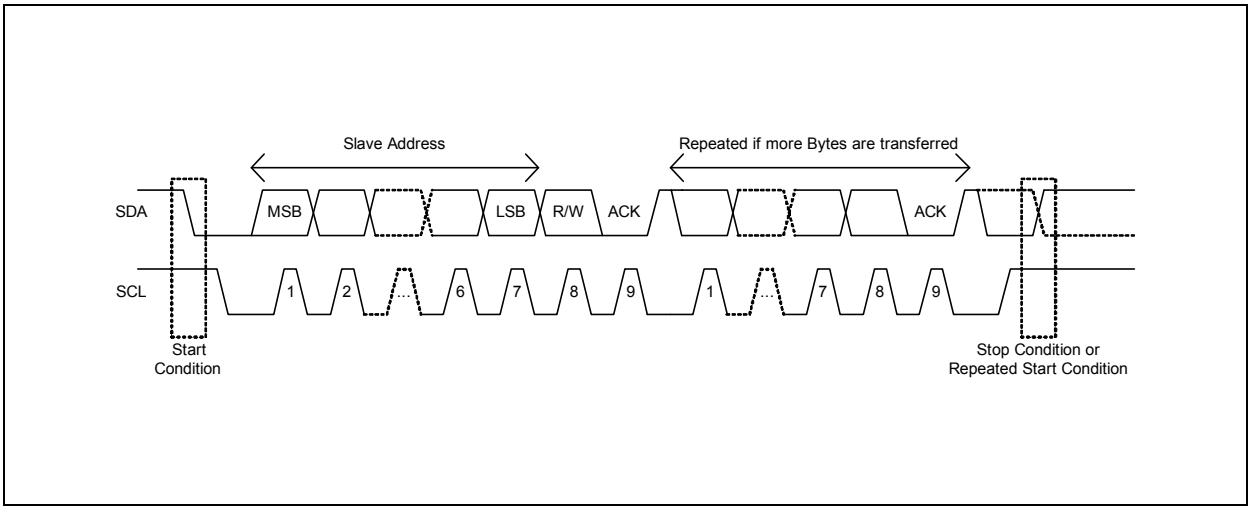
Each I^2C bus transaction is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the I^2C bus master. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each I^2C slave device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The I^2C bus master device must generate an extra clock period for this acknowledge bit.

A slave that acknowledges must pull down SDA during the acknowledge clock period in such a way that SDA is stable low during the high phase of the acknowledge clock period. Of course, setup and hold times must be taken into account. A master must signal an end of a read transaction by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave SDA high to enable the master to generate the STOP condition.

Figure 15:
Data Read



Depending on the state of the R/W bit, two types of data transfer are possible:

Data Transfer from a Master Transmitter to a Slave Receiver

The first byte transmitted by the master is the slave address, followed by R/W = 0. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. If the slave does not understand the command or data it sends a not acknowledge (NACK). Data is transferred with the most significant bit (MSB) first.

Data Transfer from a Slave Transmitter to a Master Receiver

The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a NACK is returned. The master generates all of the SCL clock periods and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Because a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

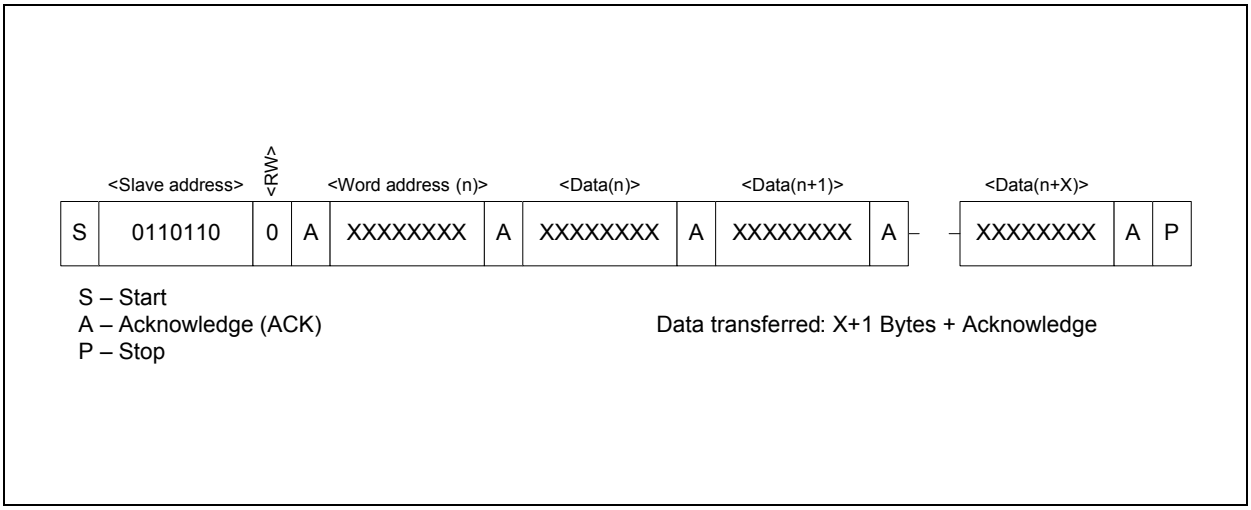
AS5601 Slave Modes

Slave Receiver Mode (Write Mode)

Serial data and clock are received through SDA and SCL. Each byte is followed by an acknowledge bit or by a NACK depending on whether the address pointer selects a valid address. START and STOP conditions are recognized as the beginning and end of a bus transaction. The slave address byte is in the first byte received after the START condition. The 7-bit AS5601 address is 0x36 (0110110 in binary).

The 7-bit slave address is followed by the direction bit (R/W), which, for a write, is 0 (low). After receiving and decoding the slave address byte, the slave device drives an acknowledge on SDA. After the AS5601 acknowledges the slave address and write bit, the master transmits a register address (word address) to the AS5601. This is loaded into the address pointer on the AS5601. If the address is a valid readable address, the AS5601 answers by sending an acknowledge (A bit low). If the address pointer selects an invalid address, a NACK is sent (A bit high). The master may then transmit zero or more bytes of data. If the address pointer selects an invalid address, the received data are not stored. The address pointer will increment after each byte transferred whether or not the address is valid. If the address pointer reaches a valid position again, the AS5601 answers with an acknowledge and stores the data. The master generates a STOP condition to terminate the write transaction.

Figure 16:
Data Write (Slave Receiver Mode)



Slave Transmitter Mode (Read Mode)

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the AS5601 will drive data on SDA. START and STOP conditions are recognized as the beginning and end of a bus transaction. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS5601 address. The 7-bit slave address is followed by the direction bit (R/W), which, for a read, is 1 (high). After receiving and decoding the slave address byte, the slave device drives an acknowledge on the SDA line. The AS5601 then begins to transmit data starting with the register address pointed to by the address pointer. If the address pointer is not written before the initiation of a read transaction, the first address that is read is the last one stored in the address pointer. The AS5601 must receive a not acknowledge (NACK) to end a read transaction.

Figure 17:
Data Read (Slave Transmitter Mode)

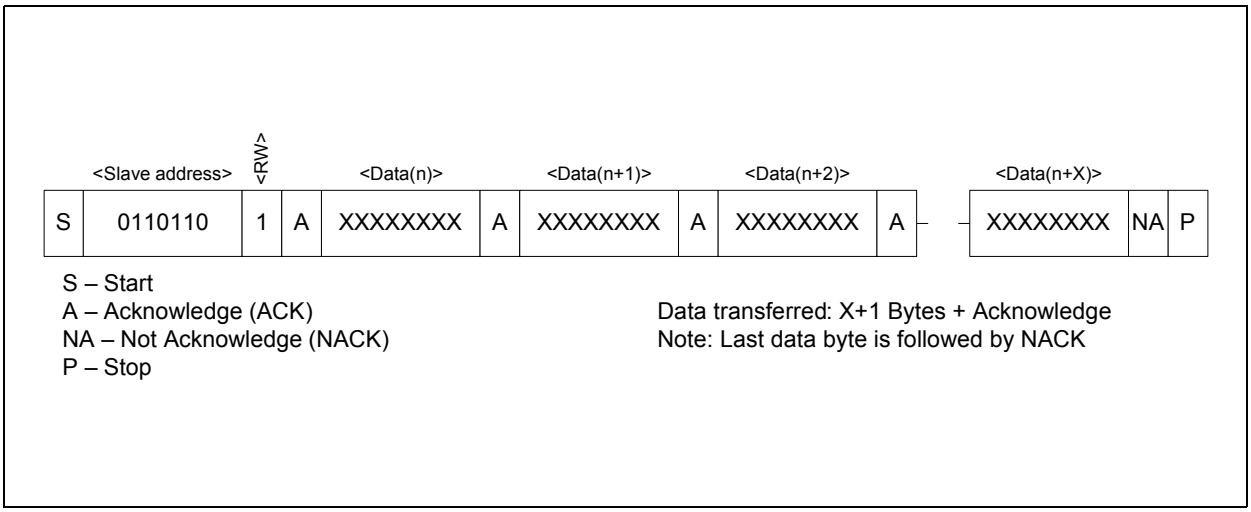
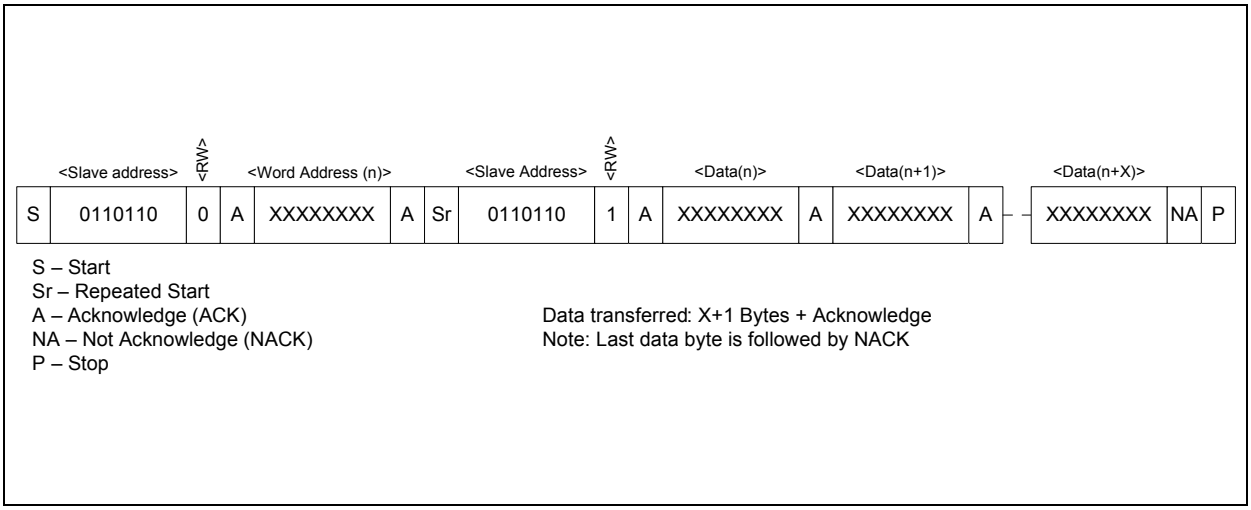


Figure 18:
Data Read with Address Pointer Reload (Slave Transmitter Mode)



SDA and SCL Input Filters

Input filters for SDA and SCL inputs are included to suppress noise spikes of less than 50 ns.

Register Description

The following registers are accessible over the serial I²C interface. The 7-bit device address of the AS5601 is 0x36 (0110110 in binary). To permanently program a configuration, a non-volatile memory (OTP) is provided.

Figure 19:
Register Map

Address	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration Registers (1), (2)										
0x00	ZMCO	R							ZMCO(1:0)	
0x01	ZPOS	R/W/P					ZPOS(11:8)			
0x02			ZPOS(7:0)							
0x07	CONF	R/W/P			WD	FTH(2:0)			SF(1:0)	
0x08							HYST(1:0)		PM(1:0)	
0x09	ABN	R/W/P					ABN(3:0)			
0x0A	PUSHTHR	R/W/P	PUSHTHR(7:0)							
Output Registers										
0x0C	RAW ANGLE	R					RAW ANGLE(11:8)			
0x0D		R	RAW ANGLE(7:0)							
0x0E	ANGLE	R					ANGLE(11:8)			
0x0F		R	ANGLE(7:0)							
Status Registers										
0x0B	STATUS	R			MD	ML	MH			
0x1A	AGC	R	AGC(7:0)							
0x1B	MAGNITUDE	R					MAGNITUDE (11:8)			
0x1C		R	MAGNITUDE(7:0)							
Burn Command										
0xFF	BURN	W	Burn_Angle = 0x80; Burn_Setting = 0x40							

Note(s):

1. To change a configuration, read out the register, modify only the desired bits and write the new configuration. Blank fields may contain factory settings.
2. During power-up, configuration registers are reset to the permanently programmed value. Not programmed bits are zero.

ZPOS Registers

These registers are used to configure the zero position (ZPOS). This register is used to align the electric grid of the incremental output with the mechanical grid of an encoder switch.

CONF Register

The CONF register supports customizing the AS5601. Figure 20 shows the mapping of the CONF register.

PUSHTHR Register

This register is used to set-up the contactless pushbutton function. This register must be adjusted according to the airgap and magnet configuration. The swing of the pushbutton function can be found by subtracting the AGC value of the pressed button from the AGC value of the released button. The threshold value for the contactless pushbutton should be half of the swing.

Figure 20:
CONF and ABN Mapping

Name	Bit Position	Description
CONF Mapping		
PM(1:0)	1:0	Power Mode 00 = NOM, 01 = LPM1, 10 = LPM2, 11 = LPM3
HYST(1:0)	3:2	Hysteresis 00 = OFF, 01 = 1 LSB, 10 = 2 LSBs, 11 = 3 LSBs
SF(1:0)	9:8	Slow Filter 00 = 16x (1); 01 = 8x; 10 = 4x; 11 = 2x
FTH(2:0)	12:10	Fast Filter Threshold 000 = slow filter only, 001 = 6 LSBs, 010 = 7 LSBs, 011 = 9 LSBs,100 = 18 LSBs, 101 = 21 LSBs, 110 = 24 LSBs, 111 = 10 LSBs
WD	13	Watchdog Timer 0 = OFF, 1 = ON (automatic entry into LPM3 low-power mode enabled)
ABN Mapping		
ABN(3:0)	3:0	Output Positions and Update Rate 0000 : 8 (61 Hz) 0001 : 16 (122 Hz) 0010 : 32 (244 Hz) 0011 : 64 (488 Hz) 0100 : 128 (976 Hz) 0101 : 256 (1.9 kHz) 0110 : 512 (3.9 kHz) 0111 : 1024 (7.8 kHz) others : 2048 (15.6 kHz))

Note(s):

1. Forced in Low Power Mode (LPM)

ANGLE/RAW ANGLE Register

The RAW ANGLE register contains the unscaled and unmodified angle. The scaled output value is available in the ANGLE register.

Note(s): The ANGLE register has a 10-LSB hysteresis at the limit of the 360 degree range to avoid discontinuity points or toggling of the output within one rotation.

STATUS Register

The STATUS register provides bits that indicate the current state of the AS5601.

Figure 21:
STATUS Register

Name	State When Bit Is High
MH	AGC minimum gain overflow, magnet too strong
ML	AGC maximum gain overflow, magnet too weak
MD	Magnet was detected

AGC Register

The AS5601 uses automatic gain control (AGC) in a closed loop to compensate for variations of the magnetic field strength due to changes of temperature, airgap between IC and magnet, and magnet degradation. The AGC register indicates the gain. For the most robust performance, the gain value should be in the center of its range. The airgap of the physical system can be adjusted to achieve this value.

In 5V operation, the AGC range is 0-255 counts. The AGC range is reduced to 0-128 counts in 3.3V mode.

MAGNITUDE Register

The MAGNITUDE register indicates the magnitude value of the internal CORDIC output.

Non-Volatile Memory (OTP)

The non-volatile memory is used to permanently program the configuration. To program the non-volatile memory, the I^2C interface is used. The programming can be either performed in the 5V supply mode or in the 3.3V operation mode but using a minimum supply voltage of 3.3V and a 10 µF capacitor at the VDD3V3 pin to ground. This 10 µF capacitor is needed only during the programming of the device. Two different commands are used to permanently program the device:

Burn_Angle Command (ZPOS)

The host microcontroller can perform a permanent programming of ZPOS with a BURN_ANGLE command. To perform a BURN_ANGLE command, write the value 0x80 into register 0xFF. The BURN_ANGLE command can be executed up to 3 times. ZMCO shows how many times ZPOS have been permanently written.

This command may only be executed if the presence of the magnet is detected (MD = 1).

Burn_Setting Command (CONF)

The host microcontroller can perform a permanent writing of CONFIG with a BURN_SETTING command. To perform a BURN_SETTING command, write the value 0x40 into register 0xFF.

The BURN_ SETTING command can be performed only one time.

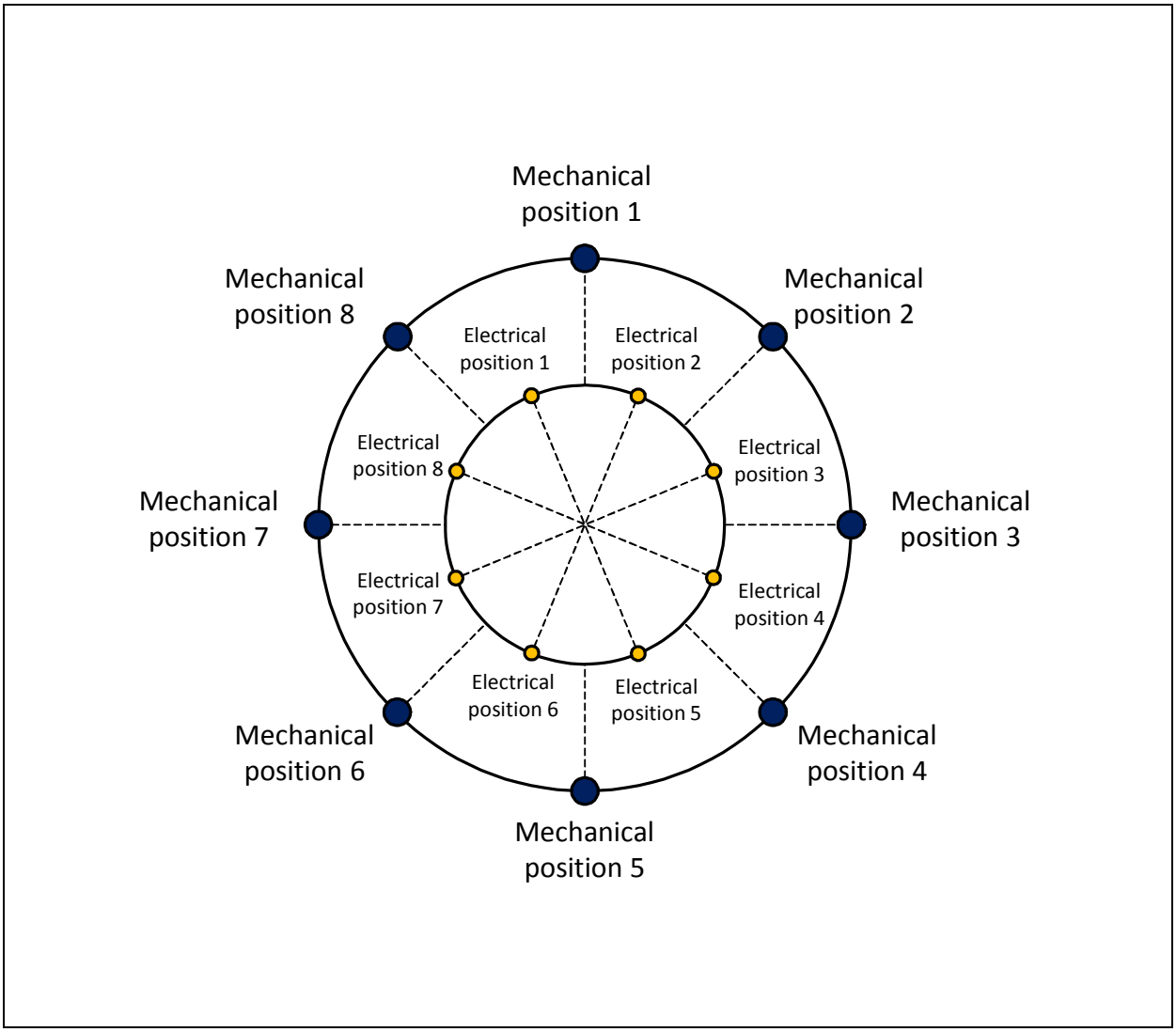
Zero Position and Resolution Programming

A fundamental feature is to program the zero position (ZPOS) of the magnetic position encoder. This is required to adjust the A/B outputs to the mechanical pattern (grid) of a contactless encoder by setting the count transitions (transition of A and or B) between two adjacent mechanical positions. An example of a 3-bit contactless encoder is shown in Figure 22.

The electrical positions represent the positions where an A or B transition occurs. The zero position can be placed in correspondence of one of the electrical positions (yellow).

A BURN_ANGLE command can be executed up to 3 times to permanently program the zero position. It can only be executed if the presence of the magnet is detected (MD = 1).

Figure 22:
Zero Position Setting of 3-Bit Encoder



The configuration procedure for a rotary encoder is shown below in Figure 23.

Figure 23:
Zero Position and Resolution Programming Procedure

Use the correct hardware configuration as shown in Figure 34	
Step 1	Power up the AS5601.
Step 2	Configure the desired number of positions using ABN(3:0).
Step 3	The mechanical configuration snapped into the grid. Read out the actual RAW ANGLE. Calculate the compensation value to adjust the mechanical grid and the encoder angle. Refer to Figure 22 and Figure 24. Write the compensation value into ZPOS. Wait at least 1ms.
Step 4	Write the required setting into the configuration register CONF and PUSHTHR. Wait at least 1 ms.
Proceed with Step 5 to permanently program the configuration.	
Step 5	Perform a BURN_ANGLE command to permanently program the zero position. Wait at least 1 ms.
Step 6	Perform a Burn_Setting command to permanently program the configuration. Wait at least 1 ms.
Step 7	Verify the BURN commands: Write the commands 0x01, 0x11 and 0x10 sequentially into the register 0xFF to load the actual OTP content. Read and verify the permanently programmed registers to verify that the BURN_SETTINGS and BURN_ANGLE command was successful.
Step 8	Read and verify the permanently programmed registers again after a new power-up cycle.

Note(s):

1. After each register command, the new setting is effective at the output at least 1 ms later.
2. It is highly recommended to perform a functional test after this procedure.
3. At least 1 ms after each register command the new setting is effective at the output.
4. The BURN_ANGLE command can be executed up to 3 times and only if the presence of the magnet is detected (MD = 1).

Quadrature Encoder Output

With the setting ABN(3:0) it is possible to configure the number of positions of the quadrature output. An example for a configuration with 8 positions is shown below.

Figure 24:
Example Quadrature Output for 8 Positions