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# AS7000

## Biosensor

## General Description

The AS7000 device provides a flexible analog front end for light sensing applications. The photodiode input circuit can be configured in different ways to guarantee best tradeoff between speed and sensitivity for a large number of different sensing applications.

*Ordering Information and Content Guide appear at end of datasheet.*

## Key Benefits and Features

The benefits and features of AS7000, Biosensor are listed below:

**Figure 1:**
**Added Value of Using AS7000**

| Benefits | Features |
|---|---|
| • Allows smallest application size e.g. narrow HRM measurement band | • Single device integrated optical solution<br>• Integrated 32bit Cortex-M0 processor |
| • Good HRM measurement quality | • Low noise analog optical front end |
| • Additional information for end user | • Analog electrical front end (e.g. for NTC or GSR) |
| • Long operating time | • Hardware sequencer to offload processor<br>• Adjustable LED driver with current control |
| • Works reliably with ambient light | • Synchronous detector |

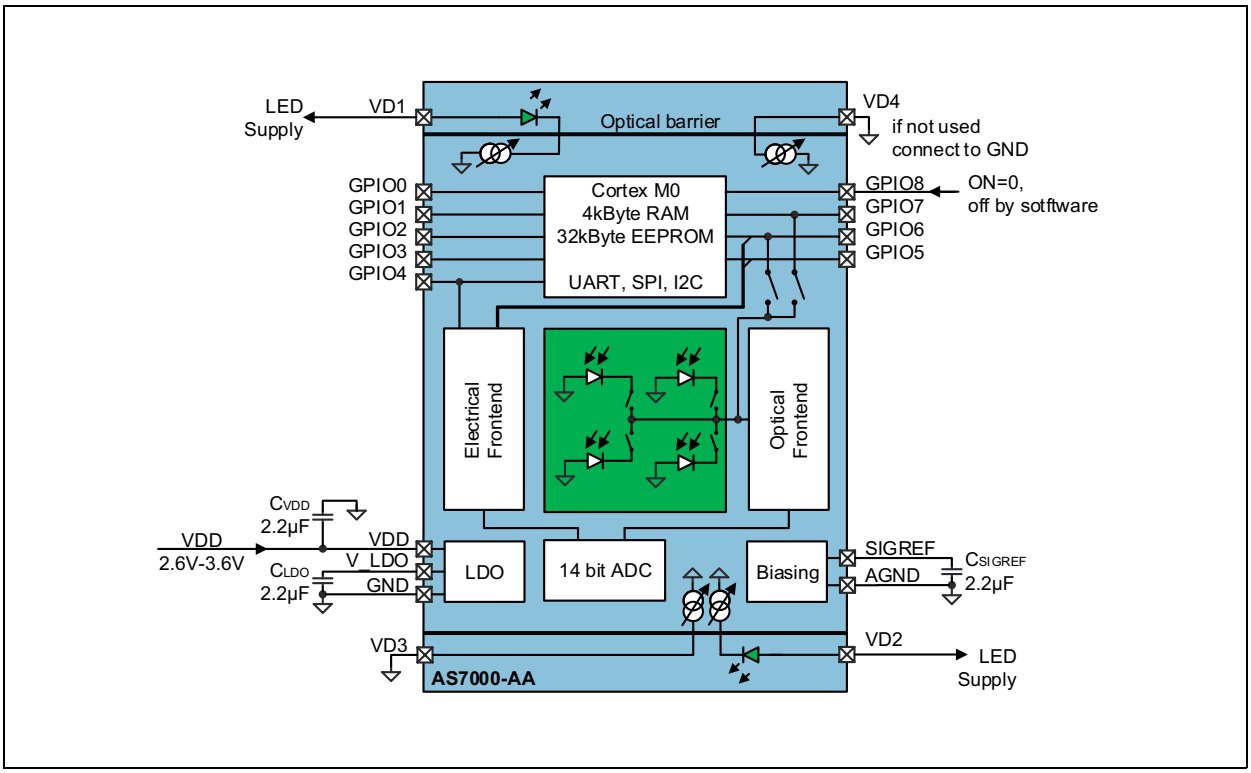
## Applications

The device is suitable for optical sensor platform.

## Block Diagram

The functional blocks of this device are shown below:

**Figure 2:**
**Application Schematic AS7000-AA**



# Pin Assignments

**Figure 3:**
**Optical Module Pinout (Top View) – AS7000-AA**

**Optical Module Pinout:**
This drawing is not to scale

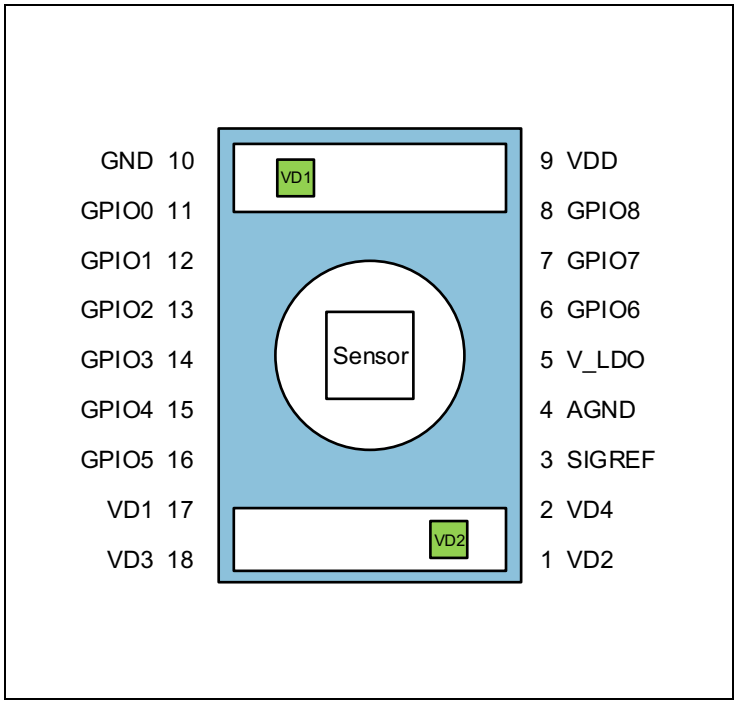



**Figure 4:**
**Pin Description**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | VD2 | Supply voltage for LED D2 – connect unused current sinks to GND |
| 2 | VD4 | Supply voltage for LED D4 – connect unused current sinks to GND |
| 3 | SIGREF | Analog reference output. Connect 2.2µF capacitor to GND (e.g. 0402 sized capacitor GRM153R60J225ME95 from Murata – needs to have >1µF specified for 1.0V voltage bias); do not load externally The typical operating voltage on this pin is 0.6V (sigref_en=1) |
| 4 | AGND | Analog ground. Connect to low noise GND |
| 5 | V_LDO | 1.9V output voltage. Connect 2.2µF capacitor to GND (e.g. 0402 sized capacitor GRM153R60J225ME95 from Murata – needs to have >1µF with 1.0V voltage bias); do not load externally |
| 6 | GPIO6 | General purpose input/output |
| 7 | GPIO7 | General purpose input/output |
| 8 | GPIO8 | General purpose input/output |
| 9 | VDD | Supply voltage. |
| 10 | GND | Power supply ground. All voltages are referenced to GND. |

| Pin Number | Pin Name | Description |
|---|---|---|
| 11 | GPIO0 | General purpose input/output |
| 12 | GPIO1 | General purpose input/output |
| 13 | GPIO2 | General purpose input/output |
| 14 | GPIO3 | General purpose input/output |
| 15 | GPIO4 | General purpose input/output |
| 16 | GPIO5 | General purpose input/output |
| 17 | VD1 | Supply voltage for LED D1 – connect unused current sinks to GND |
| 18 | VD3 | Supply voltage for LED D3 – connect unused current sinks to GND |

## Absolute Maximum Ratings

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**
**Absolute Maximum Ratings(1)**

| Symbol | Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|---|
| **Electrical Parameters** | | | | | |
| VDD | Supply voltage to ground | | 3.63V | V | |
| V_LDO | Supply voltage to ground | | 1.98V max. VDD+0.3V | V | |
| $V_{IN}$ | Input pin voltage to ground, all pins except VD1/VD2/VD3/VD4 | -0.3 | VDD+0.3V max. 3.8V | V | |
| $V_{IN-VD1-4}$ | Input pin voltage to ground, pins VD1/VD2/VD3/VD4 | -0.3 | 5.5 | V | |
| $V_{INLDO}$ | Input pin voltage to ground, pin SIGREF | -0.3 | V_LDO+0.3V max. 1.98V | V | |
| $I_{SCR}$ | Input current (latch-up immunity) | -100 | 100 | mA | JEDEC JESD78 |
| **Electrostatic Discharge** | | | | | |
| $ESD_{HBM}$ | All pins except VD1/VD2/VD3 and VD4 | ±1.0 | | kV | Electrostatic discharge HBM: JEDEC JESD22-A114F |
| | Pins VD1/VD2/VD3 and VD4 | ±350 | | V | |

| Symbol | Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|---|
| **Temperature Ranges and Storage Conditions** | | | | | |
| $T_{AMB}$ | Operating temperature | -30 | 70 | °C | |
| $T_{STRG}$ | Storage temperature range | -40 | 85 | °C | |
| $T_{BODY}$ | Package body temperature | | 260 | °C | IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." |
| $RH_{NC}$ | Relative humidity non-condensing | 5 | 85 | % | |
| MSL | Moisture sensitivity level | 3 | | | Maximum floor life time of 168h |

**Note(s):**

1. All optical customer designs shall be reviewed by **ams** before production.

## Electrical Characteristics

VDD=2.6 to 3.6V, typ. values are at $T_{AMB}$=25°C (unless otherwise specified).

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 6:**
**Operating Conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VDD | Supply voltage | | 2.6 | 3.3 | 3.6 | V |
| VLED | LED Supply voltage | VD1, VD2, VD3, VD4 if a LED is used | | | 5.0 | V |
| $V_{LDO}$ | LDO voltage, generated by AS7000 | Pin V_LDO | | 1.9 | | V |
| $T_{AMB}$ | Operating free-air temperature | | –30 | | 70 | °C |
| IDD | Supply current | CPU + EEPROM running at 16MHz; from 1.8V supply; all periphery blocks off | | 1.4 | | mA |
| | | CPU in sleep mode, 16MHz oscillator running; all periphery blocks off | | 360 | | µA |
| | | ADC 14bit; only during conversion | | 2 | | mA |
| | | Photodiode amplifier and Optical front end | | 430 | | µA |
| | | Electrical front end | | 180 | | µA |
| | | LED current sink per channel 25mA range | | 210 | | µA |
| | | LED current sink per channel 50mA and 100mA range | | 340 | | µA |
| | | Deep sleep mode (1), (2) 512Hz oscillator running, LDO operating, processor powered | | 25 | | µA |
| | | Power down (3) GPIO8=VDD. | | 0.8 | | µA |
| VOL | GPIO0-8 output low voltage | With 3 mA load<br>With 6 mA load | 0<br>0 | | 0.4<br>0.8 | V |
| VOH | GPIO0-8 output high voltage | With 6 mA load, VDD>3.0V | 2.4 | | VDD | V |

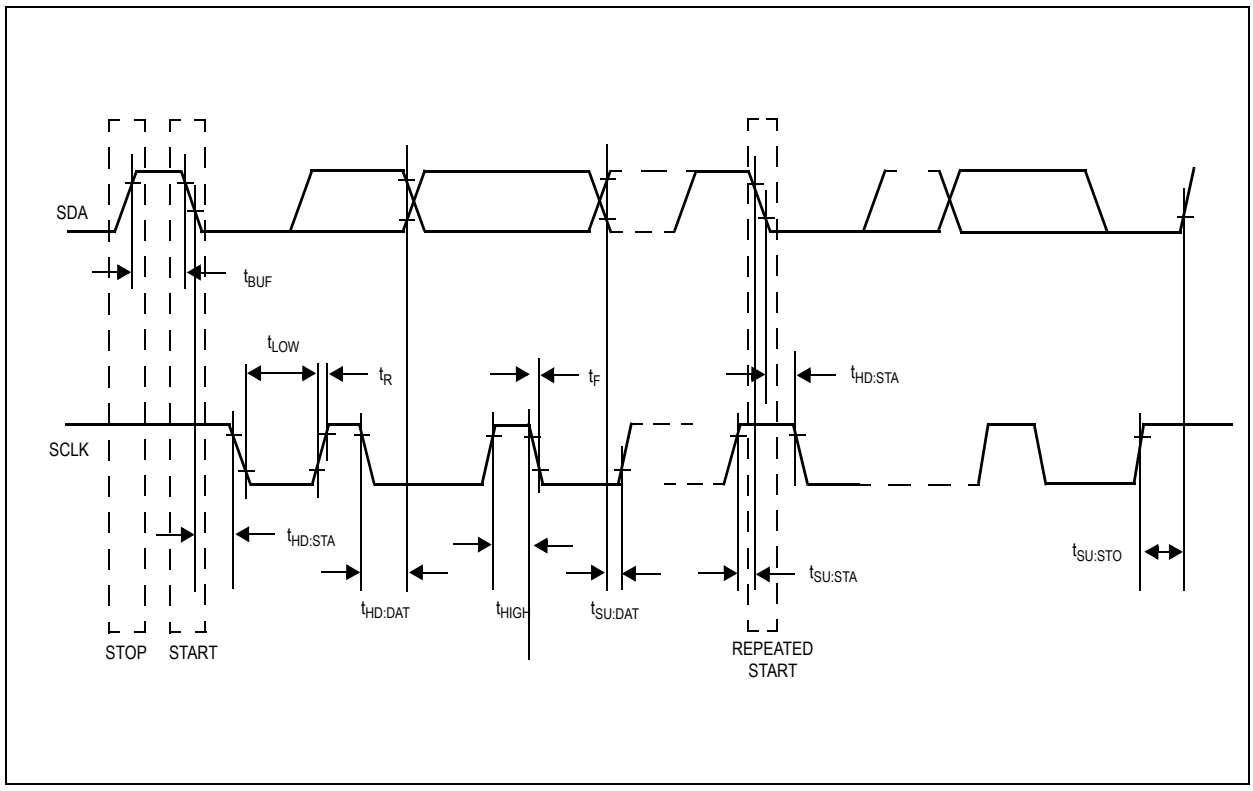
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VIH | GPIO0-8 input high voltage | | 1.25 | | | V |
| VIL | GPIO0-8 input low voltage | | | | 0.54 | V |
| $R_{PULLUP}$ | Pullup Resistor to VDD | On GPIO0…8 if bit gpioX_pd=1 where X=0…8 | | 75 | | kΩ |
| $R_{PULLDOWN}$ | Pulldown Resistor to GND | On GPIO0…8 if bit gpioX_pd=2 where X=0…8 | | 75 | | kΩ |
| ILEAK1 | GPIO0-8 | | –1 | | 1 | µA |
| ILEAK2 | VD1-4 pins | At 5.0 V, $T_{AMB}$=25°C | | | 2 | µA |
| E_f16M | Tolerance of internal 16MHz oscillator | $T_{AMB}$>0°C | -2 | | +2 | % |
| E_f3k2 | Tolerance of internal 512Hz oscillator | | -35 | | +25 | % |
| **EEPROM** | | | | | | |
| $n_{CYCLES}$ | Number of write cycles | | 100 | | | cycles |
| $t_{RETENTION}$ | Data retention time | At maximum 65°C | | | 10 | years |
| **I²C Mode Timings (SCL / SDA Programmable to GPIO Pins – See I²C Mode)** | | | | | | |
| $f_{SCLK}$ | SCL clock frequency | | 0 | | 400 | |
| $t_{BUF}$ | Bus free time between a STOP and START condition | | 1.3 | | | kHz |
| $t_{HD:STA}$ | Hold time (repeated) START condition (3) | | 0.6 | | | µs |
| $t_{LOW}$ | LOW period of SCL clock | | 1.3 | | | µs |
| $t_{HIGH}$ | HIGH period of SCL clock | | 0.6 | | | µs |
| $t_{SU:STA}$ | Setup time for a repeated START condition | | 0.6 | | | µs |
| $t_{HD:DAT}$ | Data hold time (4) | | 0 | | 0.9 | µs |
| $t_{SU:DAT}$ | Data Setup Time (5) | | 100 | | | ns |
| $t_R$ | Rise time of both SDA and SCL signals | | 20 | | 300 | ns |
| $t_F$ | Fall time of both SDA and SCL signals | | 20 | | 300 | ns |
| $t_{SU:STO}$ | Setup time for STOP condition | | 0.6 | | | µs |
| $C_B$ | Capacitive load for each bus Line | CB — total capacitance of one bus line in pF | | | 400 | pF |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{I/O}$ | I/O capacitance (SDA, SCL) | | | | 10 | pF |

**Note(s):**

1. Deep sleep mode. Use **ams** SDK (software development kit) to enter deep sleep, wakeup with low on GPIO8 pin (if gpio8_wakeup_en=1) or high on GPIO7 (if gpio7_wakeup_en=1) or 512Hz oscillator sleep_timer.
2. GPIO0-8 configured to draw minimum current (software dependent).
3. Power down mode. Entered by setting enter_powerdown=1; No oscillator running. Wakeup with low on GPIO8 pin (always) or high on GPIO7 (if gpio7_wakeup_en=1).
4. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IHMIN}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
5. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ = to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_R$ max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

**Figure 7:**
**I²C Mode Timing Diagram**




**I²C Mode Timing Diagram:** This figure shows the different timings required for I²C communication.

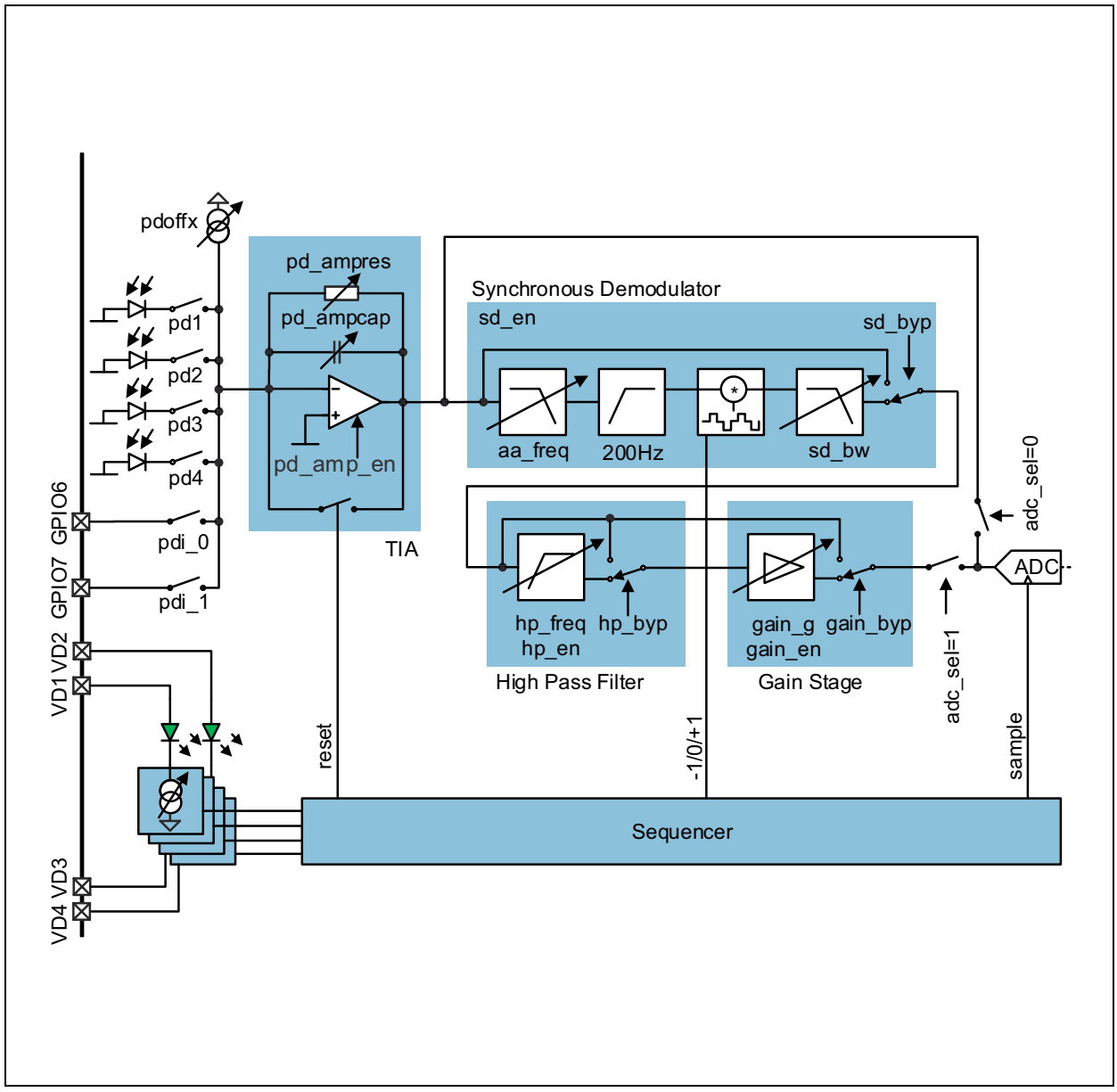
**Note(s):**

1. SCL / SDA Programmable to GPIO Pins – See I²C Mode.

# Detailed Description

## Optical Analog Front End

**Figure 8:**
**Optical Analog Front End – AS7000-AA Configuration**




**Note(s):**

1. Dual Green LED Configuration is shown.

The number of LEDs inside the module depends on the application – Figure 8 shows 2 LEDs. If a LED is not populated, the current sink is connected directly to the pin (VD3 and VD4 in above figure).

## LEDs

### AS7000-AA Dual Green LED Configuration

Two green LEDs are used (pins VD1/VD2). The other two current sinks are available on pins VD3 and VD4.

### LED Characteristics

**Figure 9:**
**LED Characteristics at $T_{AMB}$ =25°C**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Green LED (AS7000-AA)** | | | | | | |
| $I_{LED\_GREEN}$ | Allowed operating LED current range (1) | Continuous | 0 | | 50 | mA |
| | | 1/10 duty cycle @ 1 kHz | | | 100 | mA |
| $VF_{LED\_GREEN}$ | Forward voltage (2) | $I_{LED}$=20mA | 2.9 | 3.2 | | V |
| $VF_{LED+DRIVER\_GREEN}$ | Voltage on VD1/VD2 where operation of the LED and current source is guaranteed | $I_{LED}$= 10mA | | | 3.6 | V |
| | | $I_{LED}$= 50mA | | | 4.5 | |
| $\lambda p_{\_GREEN}$ | Dominant wavelength | | | 527 | | nm |
| $\Delta\lambda 1/2_{\_GREEN}$ | Spectral halfwidth | | | 35 | | nm |

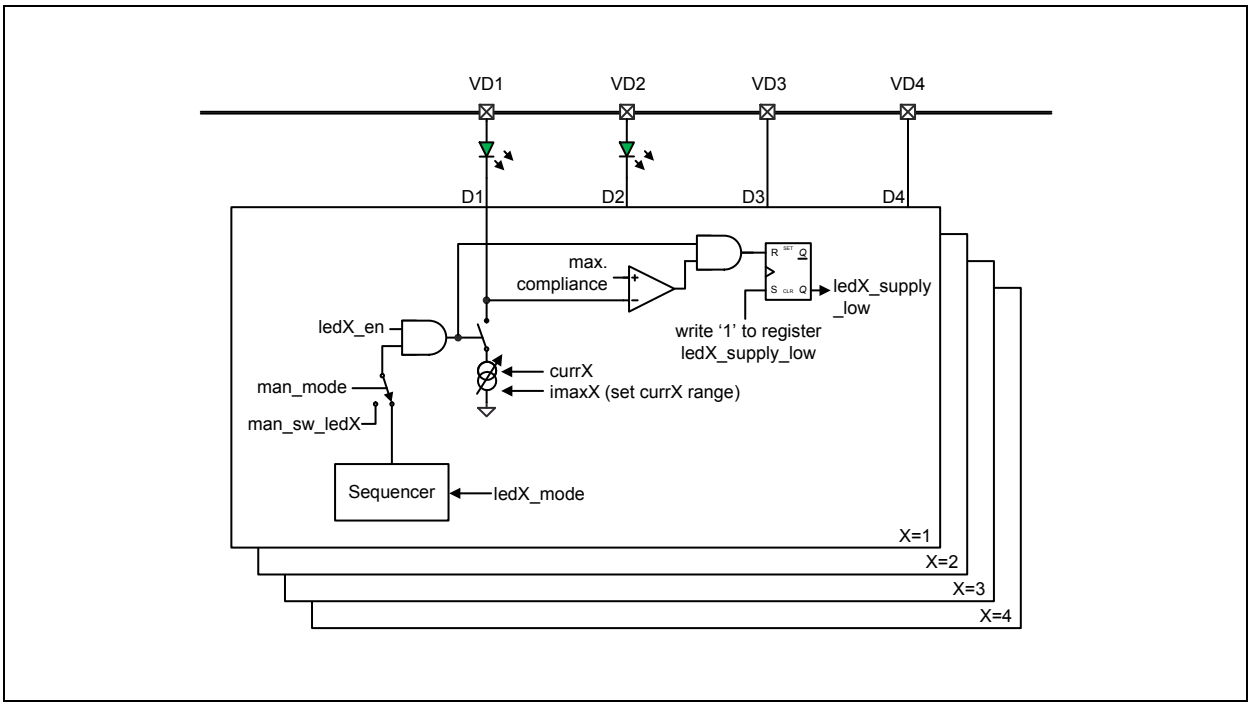
**Note(s):**

1. The maximum allowed LED current (DC and peak) is specified for 25°C. Lower values apply for higher temperatures.
2. Add 280mV and use LED current range ≤100mA for designing the VD1/VD2 LED supply (DC-DC converter).

### *LED-Driver*

The four LED-driver outputs can be controlled manually or by the built in sequencer. See Optical Front End Operating Modes

**Figure 10:**
**LED Drivers**




**Note(s):**

1. Dual Green LED Configuration.

**Figure 11:**
**Operating Characteristics of Each LED Current Sink, VDD=3V, $T_{AMB}$=25°C (unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LED1/2/3/4}$ | LED output current range | imax1/2/3/4 = 00<br>imax1/2/3/4 = 01<br>imax1/2/3/4 = 10 | 0<br>0<br>0 | | 25<br>50<br>100 | mA<br>mA<br>mA |
| | Tolerance | 25mA range<br>imax1/2/3/4 = 00 | -5 | | 5 | % |
| | | 50mA range<br>imax1/2/3/4 = 01 | -10 | | 10 | |
| | | 100mA range (1)<br>imax1/2/3/4 = 10 | -10 | | 10 | |
| V_Dmin | Output voltage compliance | Voltage compliance of current sinks D1,D2,D3,D4 | | 0.28 | | V |
| V_Dmax | Output voltage maximum | Pins VD1, VD2, VD3 and VD4 | | 5 | 5.5 | V |

**Note(s):**

1. Not production tested. Only guaranteed by lab characterization.

### *LED Configuration Registers*

For ledX_supply_low registers see register AFE_PD_CFG.

**Figure 12:**
**AFE_LED_CFG**

| 0x00: AFE_LED_CFG | | | | | |
|---|---|---|---|---|---|
| **Field** | **Name** | **Rst** | **Type** | **Description** | |
| 18 | sigref_en | 0 | RW | Signal reference: Is required for all analog blocks<br>0...Disable signal reference<br>1...Enable signal reference | |
| 11 | led4_en | 0 | RW | 0...Disables LED4 output source.<br>1...Enables LED4 output source. | |
| 10 | led3_en | 0 | RW | 0...Disables LED3 output source.<br>1...Enables LED3 output source. | |
| 9 | led2_en | 0 | RW | 0...Disables LED2 output source.<br>1...Enables LED2 output source. | |
| 8 | led1_en | 0 | RW | 0...Disables LED1 output source.<br>1...Enables LED1 output source. | |
| 7:6 | imax4 | 1 | RW | Defines IMAX of LED4. | |
| | | | | **Setting** | **IMAX** |
| | | | | 0 | 25mA |
| | | | | 1 | 50mA |
| | | | | 2 | 100mA |
| | | | | 3 | Do not use |
| 5:4 | imax3 | 1 | RW | Defines IMAX of LED3. same encoding as imax4 | |
| 3:2 | imax2 | 1 | RW | Defines IMAX of LED2. same encoding as imax4 | |
| 1:0 | imax1 | 1 | RW | Defines IMAX of LED1. same encoding as imax4 | |

The LED_CFG register is used to configure the operating mode of the LED outputs.

### *AFE_LED_CURR Register (Addr: 0x04)*

The AFE_LED_CURR defines the LED output current.

**Figure 13:**
**AFE_LED_CURR Register**

| Addr: 0x04 | | AFE_LED_CURR | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Description** |
| 31:24 | curr4 | 0x00 | R/W | LED4 output current – do not use code=0 (will generate no output current)<br>ILED4 = (curr4 + 1) * imax4 / 256 |
| 23:16 | curr3 | 0x00 | R/W | LED3 output current – do not use code=0 (will generate no output current)<br>ILED3 = (curr3 + 1) * imax3 / 256 |
| 15:8 | curr2 | 0x00 | R/W | LED2 output current – do not use code=0 (will generate no output current)<br>ILED2 = (curr2 + 1) * imax2 / 256 |
| 7:0 | curr1 | 0x00 | R/W | LED1 output current – do not use code=0 (will generate no output current)<br>ILED1 = (curr1 + 1) * imax1 / 256 |

**Figure 14:**
**AFE_MAN_SEQ_CFG**

<table>
<tr><th colspan="10">0x20: AFE_MAN_SEQ_CFG</th></tr>
<tr><th>Field</th><th>Name</th><th>Rst</th><th>Type</th><th colspan="6">Description</th></tr>
<tr><td>26</td><td>man_mode</td><td>0</td><td>RW</td><td colspan="6">0...Enables Sequencer<br>1...Enables Manual control of optical front end</td></tr>
<tr><td>23</td><td>man_sw_itg</td><td>0</td><td>RW</td><td colspan="6">If man_mode=1<br>0...All integrator capacitors are shorted. Integrator is reset<br>1...Integrator capacitors are charging up. Integrator is running</td></tr>
<tr><td>22</td><td>man_sw_led4</td><td>0</td><td>RW</td><td colspan="6">If man_mode=1<br>0...LED output D4 disabled. (High impedance)<br>1...LED output D4 enabled</td></tr>
<tr><td>21</td><td>man_sw_led3</td><td>0</td><td>RW</td><td colspan="6">If man_mode=1<br>0...LED output D3 disabled. (High impedance)<br>1...LED output D3 enabled</td></tr>
<tr><td>20</td><td>man_sw_led2</td><td>0</td><td>RW</td><td colspan="6">If man_mode=1<br>0...LED output D2 disabled. (High impedance)<br>1...LED output D2 enabled</td></tr>
<tr><td>19</td><td>man_sw_led1</td><td>0</td><td>RW</td><td colspan="6">If man_mode=1<br>0...LED output D1 disabled. (High impedance)<br>1...LED output D1 enabled</td></tr>
<tr><td rowspan="7">18:17</td><td rowspan="7">diode_ctrl</td><td rowspan="7">0</td><td rowspan="7">RW</td><td colspan="6">Connection of Photodiodes PD1, PD2, PD3, PD4 to the photodiode amplifier.<br>0...PD1-PD4 are connected<br>1...PD1 synchronous to LED1, PD2 sync/to LED2, PD3 sync/to LED3, PD4 sync/to LED4<br>2...PD1 synchronous to LED1, PD2 sync/to LED1, PD3 sync/to LED2, PD4 sync/to LED2<br>3...PD1 synchronous to LED1, PD2 sync/to LED1, PD3 sync/to LED4, PD4 sync/to LED4<br>Note that AFE_PD_CFG.pdX takes precedence - to turn OFF one photo diode, the respective bit (pd1…pd4) has to be de-asserted in the AFE_PD_CFG register.</td></tr>
<tr><td>AFE_PD_CFG.pdX</td><td>diode_ctrl</td><td>Photo Diode1</td><td>Photo Diode2</td><td>Photo Diode3</td><td>Photo Diode4</td></tr>
<tr><td>0</td><td>xx</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1</td><td>00</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td></tr>
<tr><td>1</td><td>01</td><td>LED1</td><td>LED2</td><td>LED3</td><td>LED4</td></tr>
<tr><td>1</td><td>10</td><td>LED1</td><td>LED1</td><td>LED2</td><td>LED2</td></tr>
<tr><td>1</td><td>11</td><td>LED1</td><td>LED1</td><td>LED4</td><td>LED4</td></tr>
</table>

| 0x20: AFE_MAN_SEQ_CFG | | | | | |
|---|---|---|---|---|---|
| **Field** | **Name** | **Rst** | **Type** | **Description** | |
| 13 | dma_disable | 0 | RW | ADC DMA disable<br>1...ADC result has to be read from adc_data<br>0...ADC result(s) is/are written to memory | |
| 12:10 | led4_mode | 0 | RW | LED4 mode | |
| | | | | **Setting** | **Behavior** |
| | | | | 0 | Always OFF |
| | | | | 1 | Always ON when sequencer is active |
| | | | | 2 | Controlled by sequencer |
| | | | | 3 | Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc. |
| | | | | 4 | Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc. |
| | | | | 5 | Controlled by sequencer, only ON in every fourth iteration, starting at 3: 3, 7, 11 etc. |
| 9:7 | led3_mode | 0 | RW | LED3 mode | |
| | | | | **Setting** | **Behavior** |
| | | | | 0 | Always OFF |
| | | | | 1 | Always ON when sequencer is active |
| | | | | 2 | Controlled by sequencer |
| | | | | 3 | Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc. |
| | | | | 4 | Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc. |
| | | | | 5 | Controlled by sequencer, only on in every fourth iteration, starting at 2: 2, 6, 10 etc. |

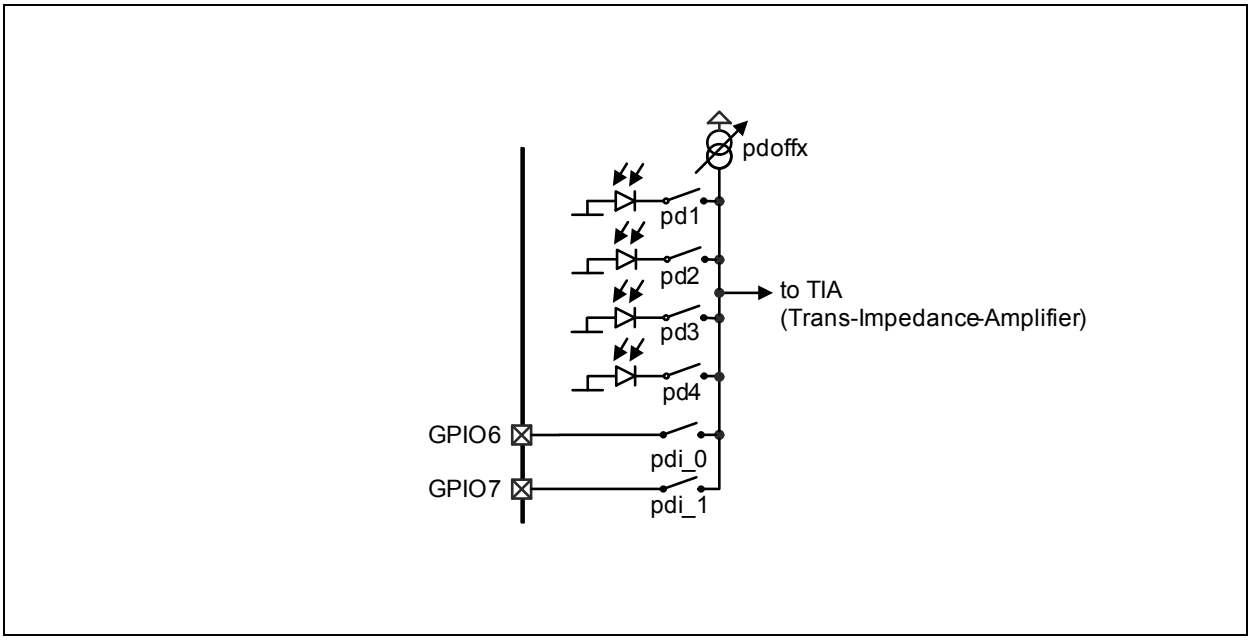
| 0x20: AFE_MAN_SEQ_CFG | | | | | |
|---|---|---|---|---|---|
| **Field** | **Name** | **Rst** | **Type** | **Description** | |
| 6:4 | led2_mode | 0 | RW | LED2 mode | |
| | | | | **Setting** | **Behavior** |
| | | | | 0 | Always OFF |
| | | | | 1 | Always ON when sequencer is active |
| | | | | 2 | Controlled by sequencer |
| | | | | 3 | Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc. |
| | | | | 4 | Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc. |
| | | | | 5 | Controlled by sequencer, only ON in every fourth iteration, starting at 1: 1, 5, 9 etc. |
| 3:1 | led1_mode | 0 | RW | LED1 mode | |
| | | | | **Setting** | **Behavior** |
| | | | | 0 | Always OFF |
| | | | | 1 | Always ON when sequencer is active |
| | | | | 2 | Controlled by sequencer |
| | | | | 3 | Controlled by sequencer, only ON in even iterations: 0, 2, 4 etc. |
| | | | | 4 | Controlled by sequencer, only ON in odd iterations: 1, 3, 5 etc. |
| | | | | 5 | Controlled by sequencer, only ON in every fourth iteration, starting at 0: 0, 4, 8 etc. |
| 0 | seq_en | 0 | RW | 0...Disables sequencer<br>1...Enables sequencer | |

### *Photodiode Selection*

In order to have flexible arrangement of the use photodiodes, PD1-PD4 can be individually connected to the photodiode amplifier input. The optional offset current allows cancellation of constant light sources like sunlight. In case of an external photodiode or any other sensor with (low) current output, the pins GPIO6 and GPIO7 can be used as input.

Additionally the sequencer can control the diodes – see diode_ctrl described in register AFE_MAN_SEQ_CFG .

**Figure 15:**
**Photodiode Selection**



### *AFE_PD_CFG Register (Addr: 0x08)*

The AFE_PD_CFG register is used to configure the input to the photo amplifier.

**Figure 16:**
**AFE_PD_CFG Register**

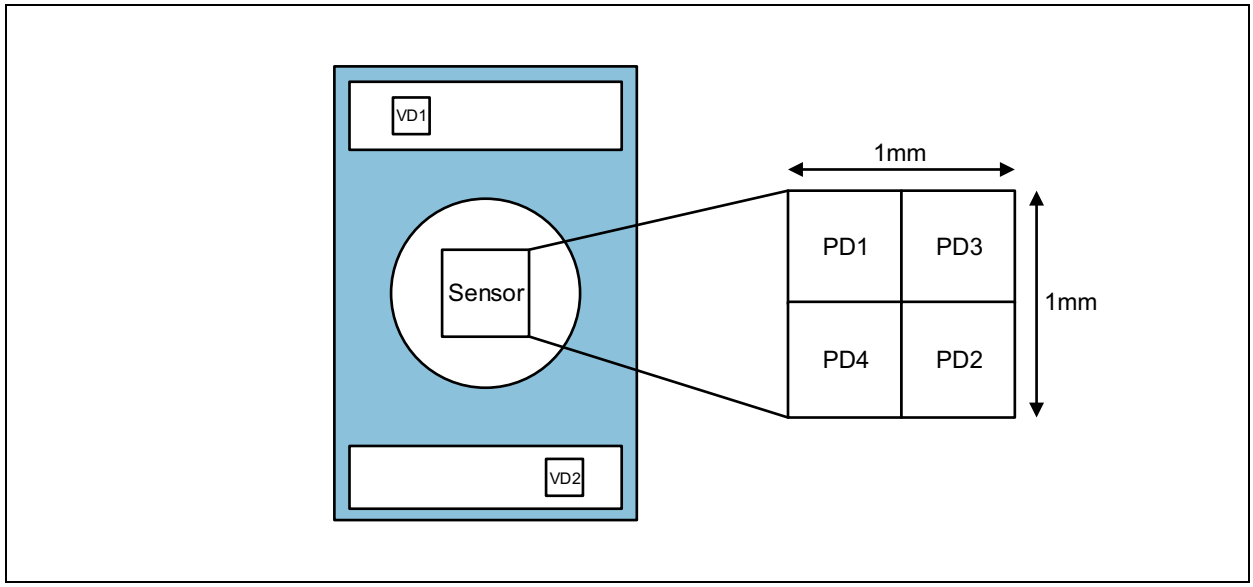
| Addr: 0x08 | | AFE_PD_CFG | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Description** |
| 25 | sd_hld | 0 | R/W | SD hold<br>0 …Output of synchronous demodulator is forced to SIGREF if not set to +1 or -1<br>1… Output of synchronous demodulator is tristated if not set to +1 or -1 |
| 23 | led4_ supply_low | 0 | SC_WS (1) | If this bit is cleared, LED4 current sink voltage was below its compliance voltage |
| 22 | led3_ supply_low | 0 | SC_WS (1) | If this bit is cleared, LED3 current sink voltage was below its compliance voltage. |
| 21 | led2_ supply_low | 0 | SC_WS (1) | If this bit is cleared, LED2 current sink voltage was below its compliance voltage. |
| 20 | led1_ supply_low | 0 | SC_WS (1) | If this bit is cleared, LED1 current sink voltage was below its compliance voltage. |
| 15:8 | pdoffx | 0x00 | R/W | Input offset current<br>Ioffset = pdoffx*10nA<br>00000000…Offset source is turned OFF |
| 5 | pd4 | 0 | R/W | 0 …Photodiode PD4 is disconnected from photo amplifier<br>1 …Photodiode PD4 is connected to photo amplifier (as defined in diode_ctrl) |
| 4 | pd3 | 0 | R/W | 0 …Photodiode PD3 is disconnected from photo amplifier<br>1 …Photodiode PD3 is connected to photo amplifier (as defined in diode_ctrl) |
| 3 | pd2 | 0 | R/W | 0 …Photodiode PD2 is disconnected from photo amplifier<br>1 …Photodiode PD2 is connected to photo amplifier (as defined in diode_ctrl) |
| 2 | pd1 | 0 | R/W | 0 …Photodiode PD1 is disconnected from photo amplifier<br>1 …Photodiode PD1 is connected to photo amplifier (as defined in diode_ctrl) |
| 1 | pdi_1 | 0 | R/W | 0 …GPIO7-input is disconnected from photo amplifier<br>1 …GPIO7-input is connected to photo amplifier |
| 0 | pdi_0 | 0 | R/W | 0 …GPIO6-input is disconnected from photo amplifier<br>1 …GPIO6-input is connected to photo amplifier |

**Note(s):**

1. SC_WS: Self clear, write sets: These registers are reset by the hardware. Set to '1' before using them.

## Photodiode Characteristics

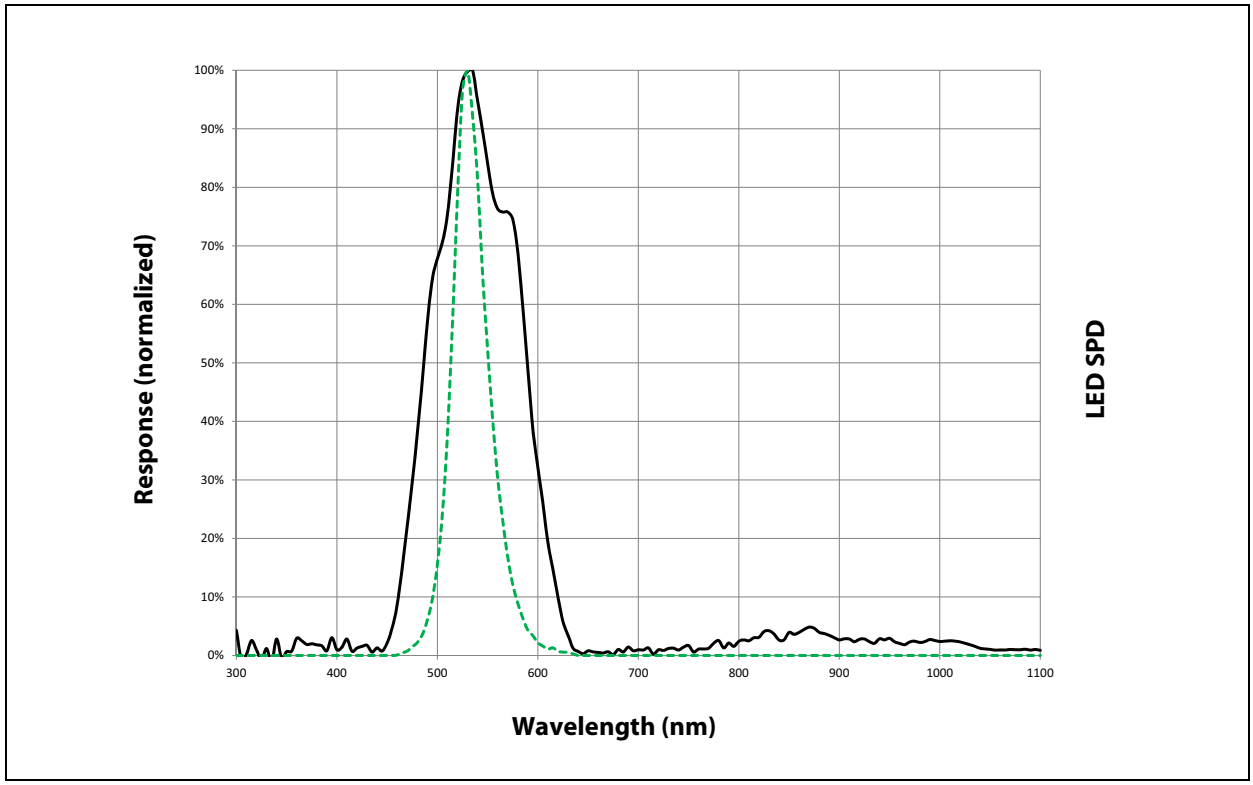
**Figure 17:**
**Photodiode Arrangement**




**Note(s):**

1. Orientation as in Figure 115 or Figure 3.

**Figure 18:**
**AS7000-AA Photodiode Sensitivity (Solid Black) and LED Emission Spectrum (Dotted Green) – Dual Green LED Configuration**




**Note(s):**

1. Perpendicular light source.
2. LEDs and Filters are shown for Dual Green LED Configuration.

**Figure 19:**
**Operating Characteristics of Each Photodiode, VDD=3V, $T_{AMB}$=25°C (unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Re | Irradiance responsivity | $\lambda_p$=525nm, 4 photodiodes used pd1/2/3/4=1, gain_g=4x, gain_en=1, pd_ampres=7MΩ dual green LED configuration filters | | 76 | | mV/ (µW /cm$^2$) |
| Id | Dark current | $E_e$=0 | 0 | | 1 | nA |
| Ios | Extrapolated offset current | | –1 | | 1 | nA |

**Note(s):**

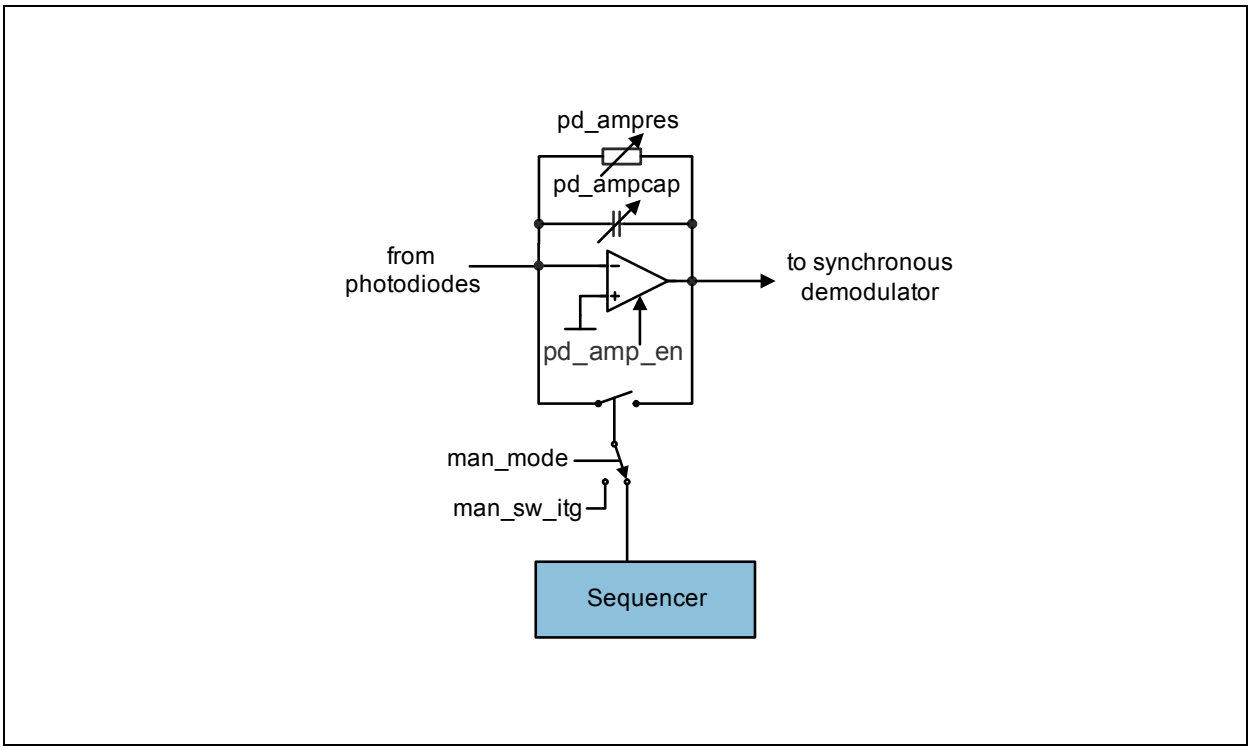
1. For monochromatic light of 555nm, one lux corresponds to 0.146 µW/cm2. That is, one obtains 6.5 lux per µW/cm2

### *Photodiode Trans-Impedance Amplifier (TIA)*

The photodiode amplifier can be configured in three different modes:

- Photocurrent to frequency converter
- Photocurrent to voltage converter
- Photocurrent integrator

**Figure 20:**
**Trans-Impedance-Amplifier (TIA)**




The integration time $t_{INT}$ is defined either by the sequencer (man_mode=0) of manually through the bit sw_itg if man_mode=1.

**Figure 21:**
**Settings for the Programming of the TIA**

| pd_ampres | pd12341 | pd_ampcap | pd_ampcomp | pd_ampvo | Gain |
|---|---|---|---|---|---|
| 1 | 1…4 | 13 | 1 | 15 | 1V/µA |
| 2 | 1…4 | 7 | 1 | 15 | 2V/µA |
| 3 | 1…4 | 5 | 1 | 15 | 3V/µA |
| 4 | 1…2 | 2 | 0 | 15 | 5V/µA |
| | 3…4 | 3 | | | |
| 5 | 1…2 | 2 | 0 | 15 | 7V/µA |
| | 3…4 | 3 | | | |
| 6 | 1 | 1 | 0 | 15 | 10V/µA |
| | 2…4 | 2 | | | |
| 7 | 1…2 | 1 | 0 | 15 | 15V/µA |
| | 3…4 | 2 | | | |
| **Low Bandwidth Mode** | | | | | |
| 5 | 1…4 | 31 | 3 | 15 | 7V/µA |
| **Integrating Mode (pd_ampres=0)** | | | | | |
| 0 | 1…4 | 10 | 3 | 15 | 1V/pQ |
| 0 | 1…4 | 20 | 3 | 15 | 1/2V/pQ |
| 0 | 1…4 | 30 | 3 | 15 | 1/3V/pQ |

**Note(s):**

1. pd1234 … number of active photodiodes (for example, pd1=1, pd2=0, pd3=1, pd4=0 -> pd1234=2)

### *AFE_PD_AMPCFG Register (Addr: 0x0c)*

The AFE_PD_AMPCFG register is used to configure the operating mode of the photo-amplifier

**Figure 22:**
**AFE_PD_AMPCFG Register**

| Addr: 0x0c | | AFE_PD_AMPCFG | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Description** |
| 31 | pd_amp_en | 0 | R/W | 0…Activates power down mode of photo-amplifier<br>1…Enables photo-amplifier |
| 13:10 | pd_amp_vo | 15 | R/W | Opamp offset. Use **ams** device drivers – these automatically configure this register. |
| 9:8 | pd_ ampcomp | 3 | R/W | Opamp compensation. Use **ams** device drivers – these automatically configure this register. |
| 7:5 | pd_ampres | 0x0 | R/W | Feedback resistor<br>000…No resistor in feedback of amplifier<br>001…1MΩ<br>010…2MΩ<br>011…3MΩ<br>100…5MΩ<br>101…7MΩ<br>110…10MΩ<br>111…15MΩ |
| 4:0 | pd_ampcap | 0x0 | R/W | Feedback capacitor – automatically set by **ams** device drivers for modes using pd_ampres not 000b.<br>Capacitor = pd_ampcap*0.1pF |

For registers man_mode and man_sw_itg see AFE_MAN_SEQ_CFG .

### *Voltage Mode of the Photodiode Amplifier*

The output voltage of the photodiode amplifier is depending on the feedback component:

**(EQ1)** Feedback resistor: $U_{out} = I_{photo} \cdot R_{fb}$

**(EQ2)** Feedback capacitor: $U_{out} = I_{photo} \cdot \frac{t_{INT}}{C_{fb}}$

**Note(s):** The integration time $t_{INT}$ is defined either by the sequencer (man_mode=0) of manually through the bit sw_itg if man_mode=1.
For the synchronous demodulator only use the resistive feedback.

**Figure 23:**
**Difference Between Resistive and Capacitive Feedback**