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AS7221

Calibrated XYZ Chromatic Manager for Network Enabled Smart Lighting

General Description

The AS7221 Smart Lighting Manager device is part of the **ams** Cognitive Lighting™ family of products that enable lights to be "aware" and adapt to their surroundings, autonomously adapting to human lighting and energy conservation needs. The device is equipped with an advanced Cognitive Lighting Engine (CLE) to optimize, chromatic white/color tuning, daylight harvesting and lumen maintenance via a combination of PWM and/or 0-10V controls with dimming ballasts. Direct connection to a local sensor network (LSN), enables connectivity with standard occupancy sensors, dimmers or communications bridges.

AS7221 XYZ chromatic white/color sensing provides mapping to x, y (z) of the CIE 1931 2-dimensional color gamut coordinates and scales the coordinates to the CIE 1976 u'v' coordinate system. The AS7221 integrates standard observer filters into standard silicon via nano-optic deposited interference filters which deliver high-stability over time and temperature. The LGA package includes a built in aperture to control light entering the sensor array. Integrated intelligence enables lifetime CCT calibration to within 2-4 Macadam steps.

The AS7221 connects to standard 0-10V dimmers inputs and drives 0-10V dimming ballasts/drivers to enable a highly cost-effective white tunable current-steering luminaire design with a single-channel constant current ballast. Direct PWM inputs can also interface to standard LED drivers or multi-channel ballasts for constant voltage LED lighting architectures.

A UART interface is provided for configuration, control and management of the CLE. This UART interface responds to simple Smart Lighting Set commands.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of this device are listed below:

Figure 1:
Added Value of Using AS7221

Benefits	Features
• Accurate control of variable CCT and spectrally tunable lighting	• Calibrated XYZ tri-stimulus color sensing for direct translation to CIE 1931/1976 standard observer color maps
• Automatic spectral and lumen maintenance over temperature and time	• Autonomous color point and lumen output adjustment resulting in automatic spectral and lumen maintenance
• Direct serial interface for connection to standard networks	• Simple UART interface for connection to network hardware clients for protocols such as Bluetooth, ZigBee and WiFi
• Simple lamp or luminaire configuration and commissioning using defined command set	• Smart Lighting Command Set (SLCS) uses simple text-based commands to control and configure a wide variety of functions
• Compatible with standard dimmer controls and occupancy sensors	• Directly interfaces to 0-10V dimmer controls and standard occupancy sensors
• Directly interfaces to LED driver via PWM	• Built-in PWM generator to dim LED lamps and luminaires • 12-bit resolution for precise dimming down to 1%
• Directly interfaces to ballast via 0-10V	• 0-10V analog output for control of conventional dimming ballasts in a current steering design
• Small package, wide operating range with critical optics built-in	• 20-pin LGA package 4.5mm x 4.7mm x 2.5mm with integrated aperture • -40°C to 85°C

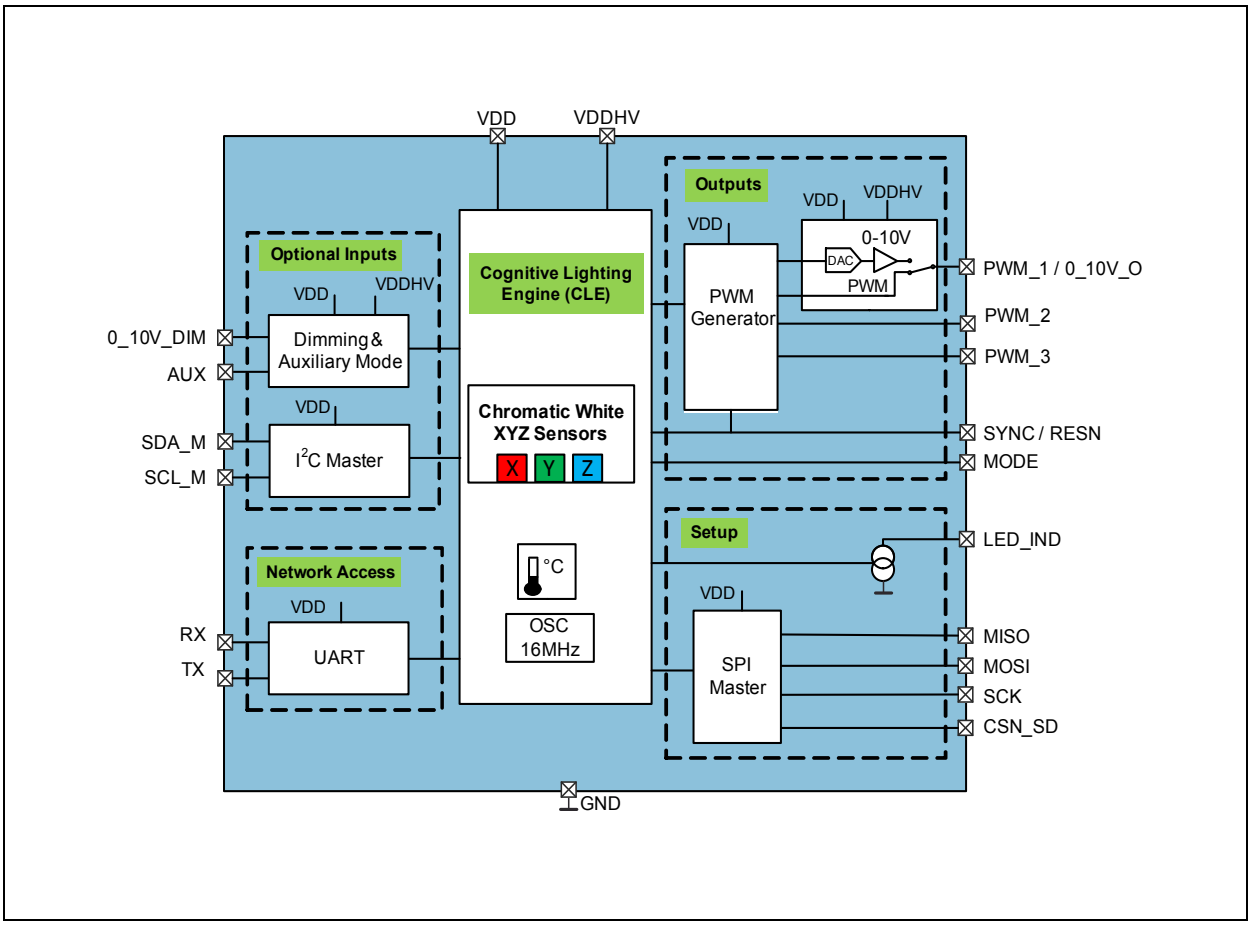
Applications

Autonomous, networked solid-state lighting manager for variable CCT and daylight harvesting:

- Integrated smart lighting control of variable CCT white lighting solutions
- Luminaires intended to meet California Title 24 daylighting requirements
- Commercial, retail, and residential white/color changing LED lighting systems
- Networked lighting systems with IoT sensor expandability

Block Diagram

Figure 2:
Functional Blocks of AS7221



Functional Blocks of AS7221: The AS7221 provides closed loop chromatic white sensing and PWM tuning while interfacing to local and network controls.

Pin Assignments

Figure 3:
Pin Diagram of AS7221 (Top View)

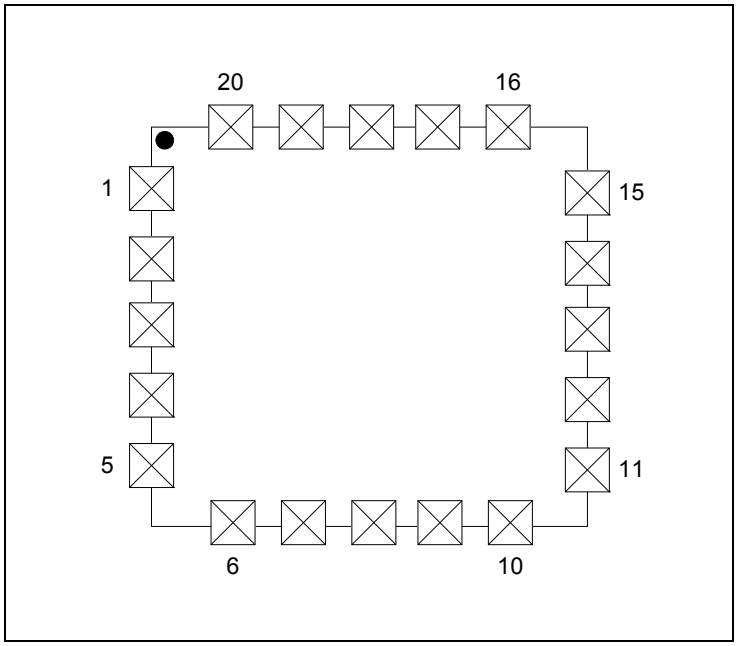


Figure 4:
Pin Description of AS7221 (20 Pin LGA)

Pin Number	Pin Name	Description
1	PWM_3	Digital PWM 3
2	SYNC/RESN	Active low (with internal pull-up to VDD)
3	SCK	SPI serial clock
4	MOSI	SPI MOSI
5	MISO	SPI MISO
6	CSN_EE	Chip select for the required external serial flash memory, active low
7	CSN_SD	Chip select for SD Card interface, active low
8	AUX	Auxiliary mode input pin
9	SCL_M	I^2C master clock pin
10	SDA_M	I^2C master data pin
11	RX	UART RX pin
12	TX	UART TX pin
13	0_10V_DIM	0-10V input dimming pin

Pin Number	Pin Name	Description
14	VDDHV	High Voltage Supply
15	MODE	Mode selection pin
16	GND	Ground
17	VDD	Low Voltage Supply
18	LED_IND	LED Driver output for Indicator LED, current sink
19	PWM_1	Digital PWM 1
	0_10V_O	0-10V output pin
20	PWM_2	Digital PWM 2

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device is not designed for high energy UV (ultraviolet) environments, including upward looking outdoor applications, which could affect long term optical performance.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD_MAX}	Supply Voltage VDD	-0.3	5	V	Pin VDD to GND, Low Voltage pin
V_{DDHV_MAX}	Supply Voltage VDDHV	-0.3	20	V	Pin VDDHV to GND, High Voltage pin
V_{DD_IO}	Input/Output Pin Voltage	-0.3	VDD + 0.3	V	Low Voltage pins to GND
V_{DDHV_IO}	Input/Output Pin Voltage	-0.3	VDDHV + 0.3	V	High Voltage pins to GND
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JESD78D
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±1000		V	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM	±500		V	JESD22-C101F
Temperature Ranges and Storage Conditions					
T_{strg}	Storage Temperature	-40	85	°C	
T_{body}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non hermetic Solid State Surface Mount Devices”
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a 168 hour max. floor lifetime

Electrical Characteristics

All limits are guaranteed with VDD = 3.3V, VDDHV = 12V, T_{AMB} = 25°C. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. If VDD and VDDHV are to be the same voltage, they must be sourced by the same 2.97-3.6V supply.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General Operating Conditions						
VDD	Low Voltage Operating Supply		2.97	3.3	3.6	V
VDDHV	High Voltage Operating Supply		VDD	12	15	V
T_{AMB}	Operating Temperature		-40	25	85	°C
I_{VDD}	Operating Current				5	mA
Internal RC Oscillator						
F_{OSC}	Internal RC Oscillator Frequency		15.7	16	16.3	MHz
t_{JITTER} (1)	Jitter	@25°C			1.2	ns
0-10V Output (0_10V_O pin)						
R_{OUT_10}	Resistive Load		1			kΩ
I_{S_10}	Source Current		10			mA
I_{SINK_10}	Sink Current		-10			mA
I_{LEAK_HV}	HV Output Leakage Current	VIN=12V, DAC & PWM1 both disabled	-1.6		-0.73	mA
C_{LOAD_10}	Capacitive Load				100	pF
V_{OUT_10} (2)	Output Swing		0		10	V
AUX Input						
AUX_{IN}	AUX Input Voltage	For 100% AUX A/D conversion		3.0		V
R_{IN_AUX}	Analog Input Resistance		168	240	312	kΩ
0-10V Input						
R_{IN_HV}	Analog Input Resistance	VDDHV ≥ 12V	138	200	315	kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temperature Sensor						
D_{TEMP}	Absolute Accuracy of the Internal Temperature Measurement		-8.5		8.5	°C
Indicator LED						
I_{IND}	LED Current		1		8	mA
I_{ACC}	Accuracy of Current		-30		30	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V
Digital Inputs and Outputs						
I_{IH}, I_{IL}	Logic Input Current	Vin=0V or VDD	-1		1	µA
I_{IL} SYNC/RESN	Logic Input Current (SYNC/RESN pin)	Vin=0V	-1		-0.2	mA
V_{IH}	CMOS Logic High Input		0.7* VDD		VDD	V
V_{IL}	CMOS Logic Low Input		0		0.3* VDD	V
V_{OH}	CMOS Logic High Output	I=1mA			VDD-0.4	V
V_{OL}	CMOS Logic Low Output	I=1mA			0.4	V
t_{RISE} (1)	Current Rise Time	C(Pad)=30pF			5	ns
t_{FALL} (1)	Current Fall Time	C(Pad)=30pF			5	ns

Note(s):

1. Guaranteed, not production tested
2. For VDDHV>10.5, output max is 10V, else output max tracks VDDHV

Figure 7:
AS7221 I²C Master Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C Interface						
f_{SCLK}	SCL Clock Frequency			100	400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HD:STA}$	Hold Time (Repeated) START		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	CB — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

Figure 8:
I²C Master Timing Diagram

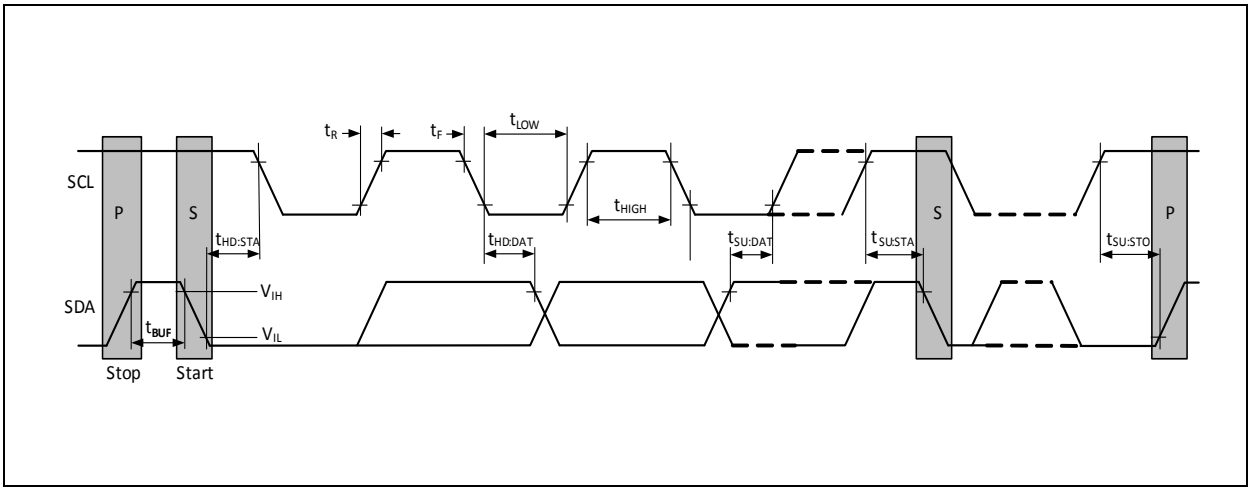


Figure 9:
AS7221 SPI Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI Interface						
f_{SCK}	Clock Frequency		0		16	MHz
t_{SCK_H}	Clock High Time		40			ns
t_{SCK_L}	Clock Low Time		40			ns
t_{SCK_RISE}	SCK Rise Time		5			ns
t_{SCK_FALL}	SCK Fall Time		5			ns
t_{CSN_S}	CSN Setup Time	Time between CSN high-low transition to first SCK high transition	50			ns
t_{CSN_H}	CSN Hold Time	Time between last SCK falling edge and CSN low-high transition	100			ns
t_{CSN_DIS}	CSN Disable Time		100			ns
t_{DO_S}	Data-Out Setup Time		5			ns
t_{DO_H}	Data-Out Hold Time		5			ns
t_{DI_V}	Data-In Valid		10			ns

Figure 10:
SPI Master Write Timing Diagram

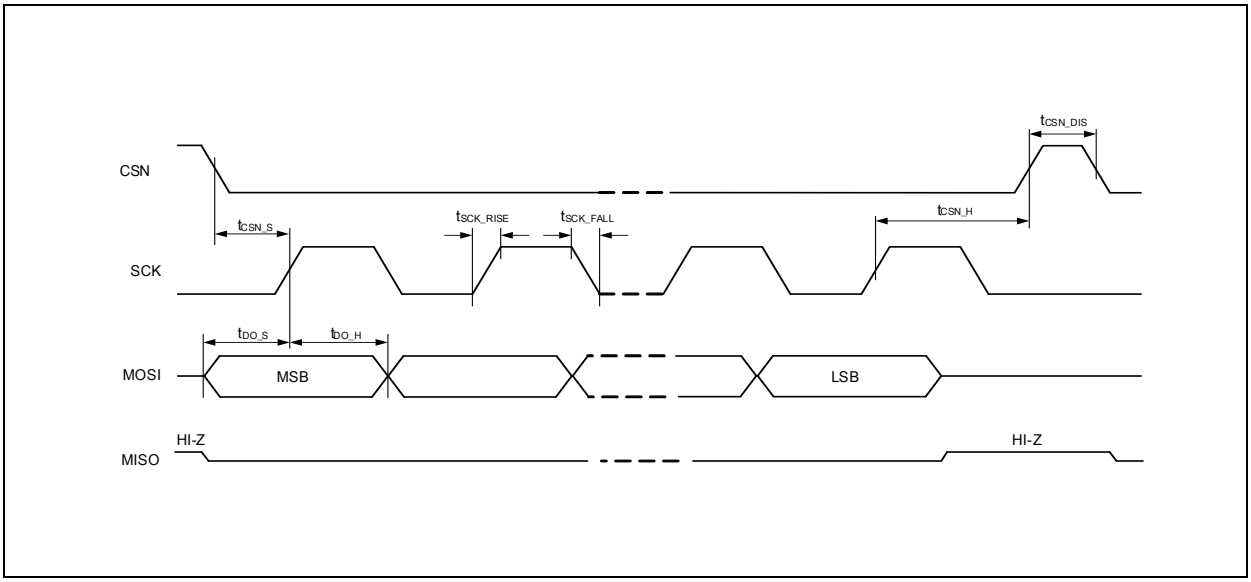


Figure 11:
SPI Master Read Timing Diagram

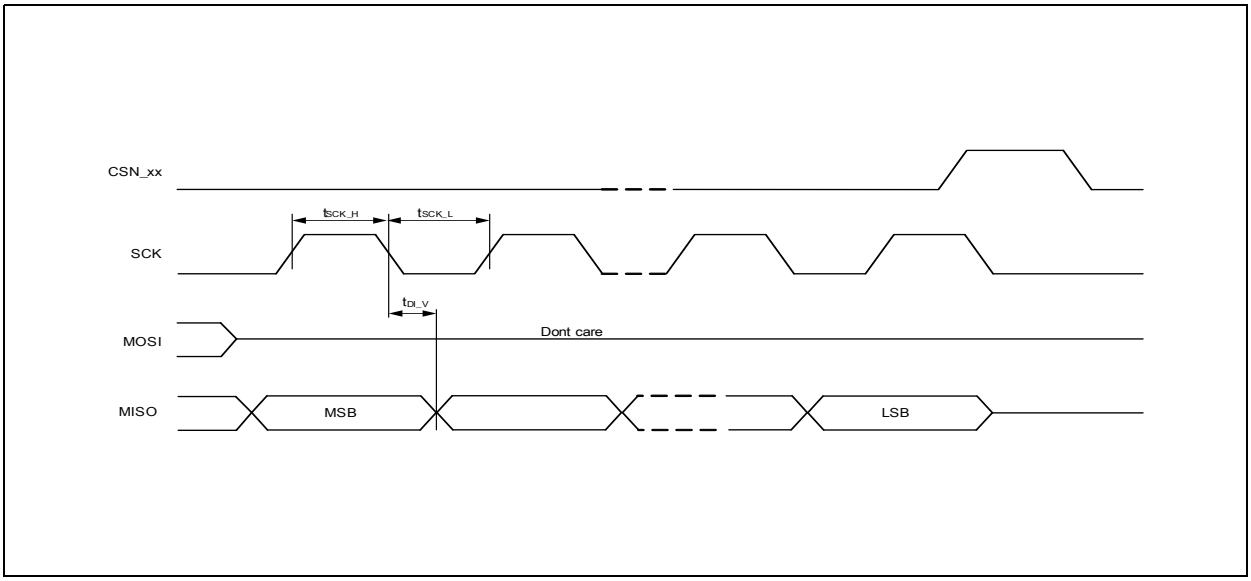


Figure 12:
Typical Spectral Responsivity

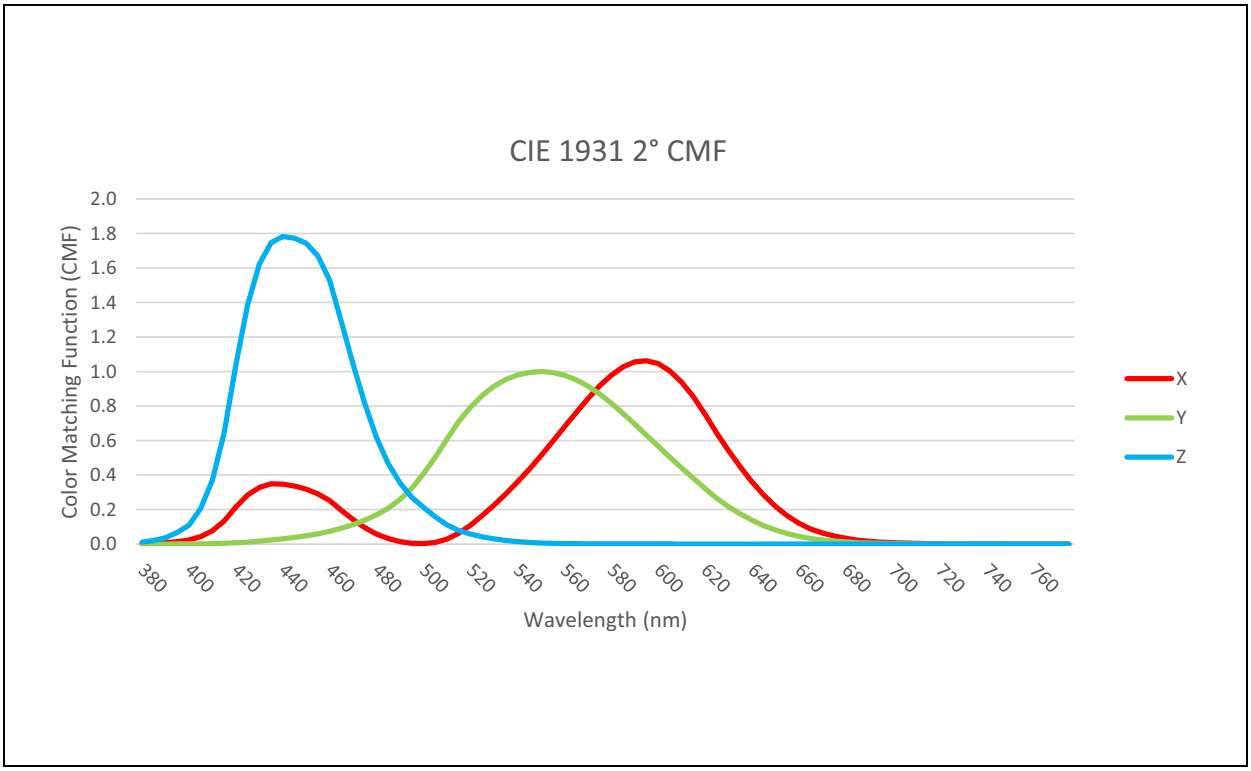


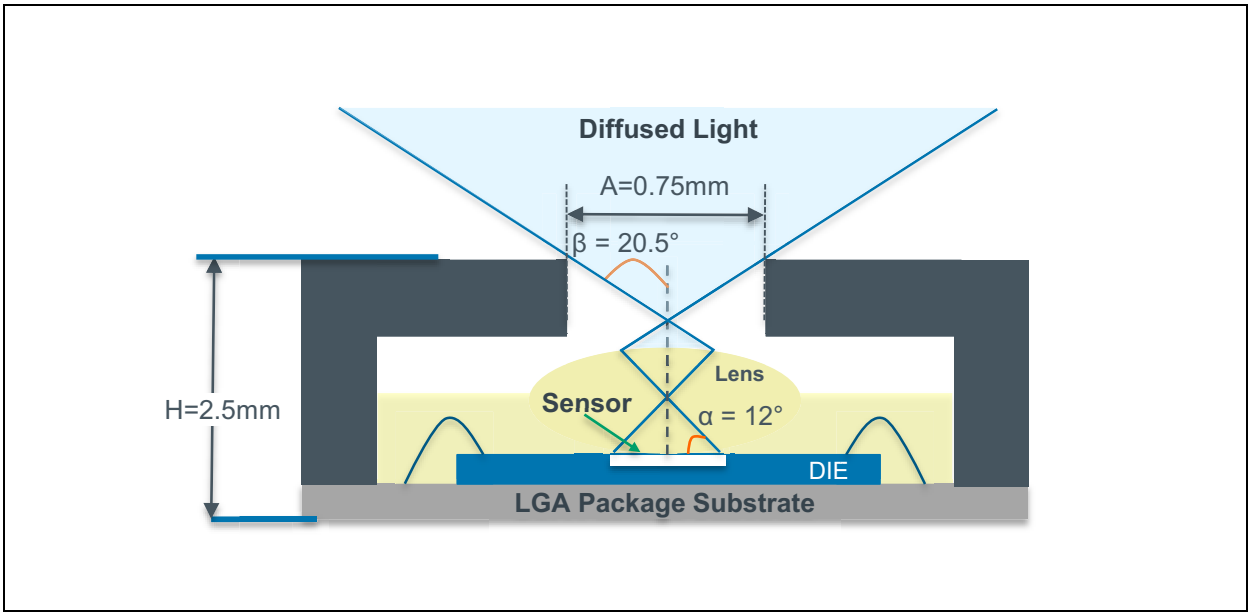
Figure 13:
AS7221 Optical Characteristics

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Unit
Color_m(2)	Color Measurement Accuracy	White Light CCT=2700K, 3500K, 4500K and 5700K		0.002		du'v'
Z_count	Z Channel Count Accuracy	White light CCT = 5700K	3.375	4.5	5.625	counts/ ($\mu W/cm^2$)

Note(s):

1. Typical values at Lux ≥50, Integration time=400.4ms, Gain=1x, T_{AMB} = 25°C.
2. Calibration and measurements are made using diffused light.

Figure 14:
AS7221 LGA Average Field of View



Detailed Description

AS7221 Smart Lighting Manager - Overview

The Cognitive Light Engine (CLE) is the “brains” of the Smart Lighting Manager. The CLE constantly processes information from the calibrated XYZ chromatic white/color sensor, network access and inputs while controlling outputs. AS7221 initial setup and ongoing parameter storage is automatically done by software within the required external serial flash memory, via SPI bus.

XYZ color point response is accomplished via standard observer interference filters which are extremely stable over time and temperature. To ensure accuracy, the AS7221 LGA package contains an internal aperture that limits the sensor average field of view (AFOV) of ± 20.5°, as shown in the figure above. External optics can be used as needed to expand or reduce this built in AFOV.

Overall AS7221 timing generation uses an on chip 16MHz temperature compensated oscillator for master clock timing.

Refer to the separate AS7221 User Guide as well as the **ams** Smart Lighting Command Set document for additional usage and setup information.

Figure 15:
AS7221 Solution Chart

Solution Required			Device Orientation (from luminaire light source)	
Chromatic Color Maintenance	Lumen Maintenance	Daylighting	AS7221	TSL45315 (optional)
√	√	×	↑ (into luminaire)	× (not required)
√	√	√	↑ (into luminaire)	↓ (into room)

XYZ Chromatic White Color Sensor

The XYZ chromatic white/color sensor, part of the AS7221 Cognitive Light Engine (CLE), is a next-generation digital color sensor device. The sensor contains an integrating analog-to-digital converter (16-bit resolution ADC), which integrates current from photodiodes. Upon completion of the conversion cycle, the result is transferred to the corresponding data registers. Transfers are double-buffered to ensure integrity of the data is maintained.

Standard observer interference filters realize the XYZ response, which enables both a no life-time drift and very high temperature stability. Note the AS7221 LGA package contains an internal aperture that provides a package field of view (PFOV) of ± 20.5°. External optics can be used as needed to expand or reduce this built in PFOV.

AS7221 Inputs

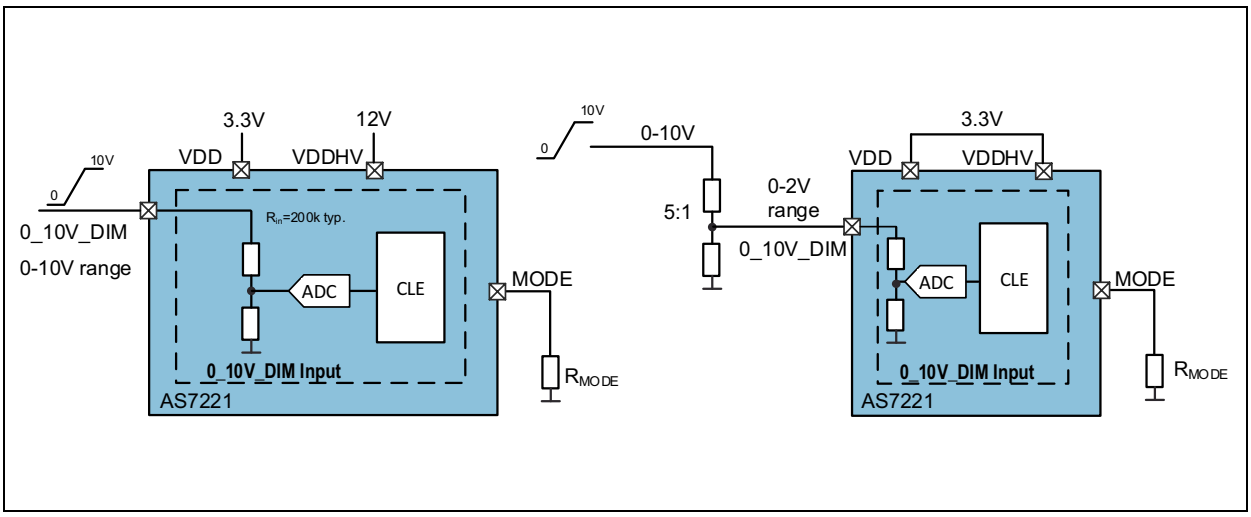
Figure 16:
VDDHV Based Settings for Inputs

VDDHV	Dimming
10.5-15V	Direct input for 0_10V_DIM, dimming input
2.97-10V (1)	External 5:1 resistor divider for 0-10V_DIM, dimming input (2)

Note(s):

1. For VDDHV <= 3.6V, VDDHV and VDD should be tied together.
2. With external dividers connected to 0-10V inputs, the max voltage to the device input is 2V.

Figure 17:
0-10V Dimming Pin Input

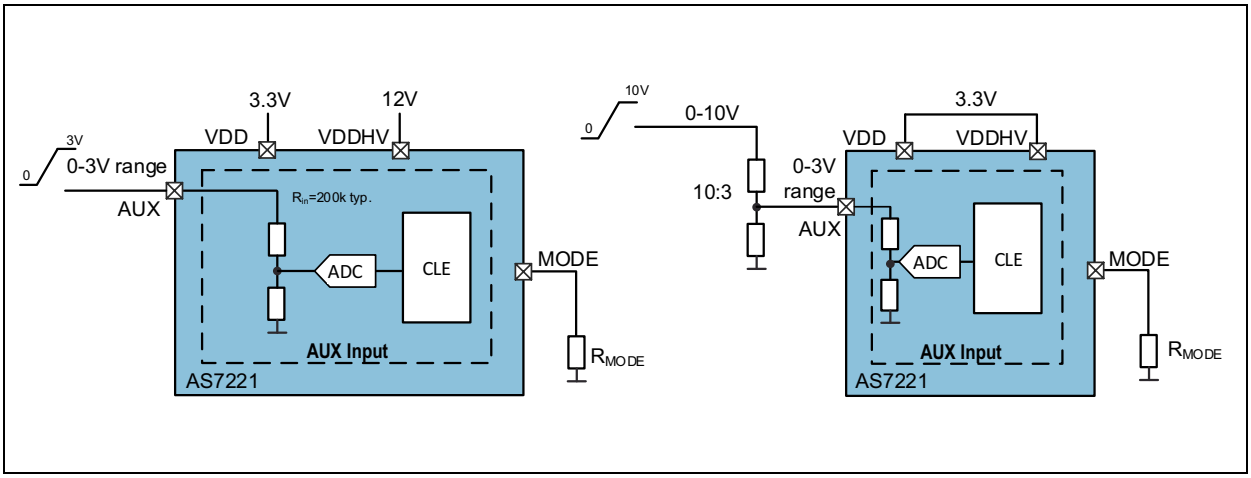


For the AS7221, dimming can be accomplished from either the input pin (0_10V_DIM) or network command via the UART. For network commanded dimming, using the AS7221 Smart Lighting Command set, the UART interface is used.

Local hardware inputs can be provided by, for example, a slide control dimmer. The 0-10V DIM analog input signal is downscaled by the AS7221 with an internal voltage divider and converted to a 10 bit digital value, 0V=full dimming, 10V=no dimming. When using the internal voltage divider the voltage at the VDDHV pin has to be higher than 10V.

If a second supply is not available, VDDHV and VDD are tied together and the downscale has to be done by an external resistor divider. The maximum range in the downscaled input is limited to 2V. Hence to accept a full range 10V signal the input resistor divider has to be 5:1 ratio. Dependent on the level at pin VDDHV the Smart Lighting Manager automatically selects either the internal or the external voltage divider. Refer to the Figures above and below. If the 0_10V_DIM pin is not used, an external resister pull-up connecting it to VDDHV is recommended.

Figure 18:
AUX Pin Input



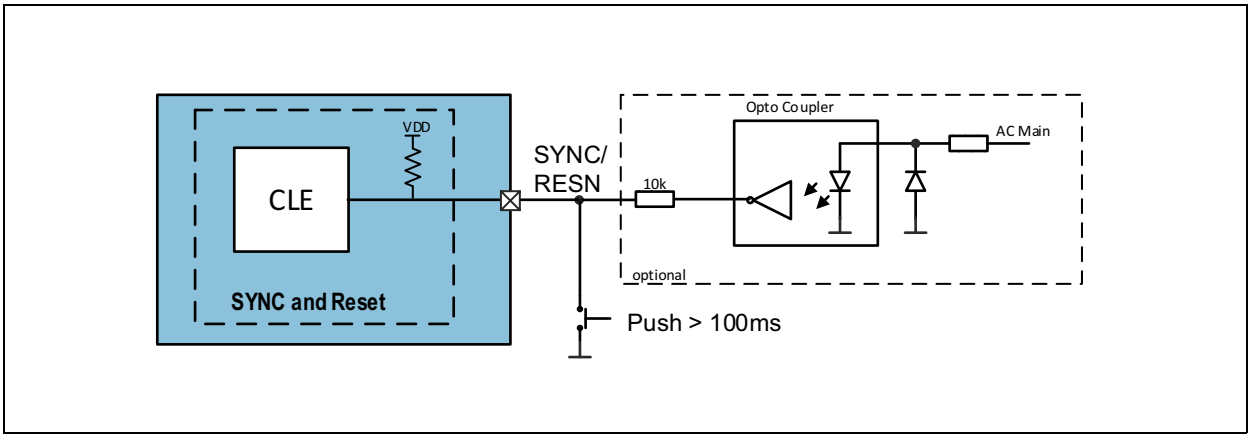
The AUX input is used as a sensor input to allow additional control, in addition to the 0-10V slider dimming function the 0_10V_DIM pin does. The sensed AUX voltage is scaled and used to multiply the dimming scale. The auxiliary sensor input (AUX) has a 0-3V range for its default analog sensing mode. With this 0-3V range external ranges such as 0-10V can be accommodated using external resister divider networks such as a 10:3 network for a 0-10V occupancy sensor. The AUX pin can also be configured for digital sensing (0, 1 where 1=VDD). Refer to the separate AS7221 User Guide for detailed design information for AUX usage. If the AUX pin is not used, an external resistor pull-up connecting it to VDD is recommended.

External sensors with native support by the AS7221 can be added via the I^2C master interface. For example the **ams** TSL45315 can be used to add Daylighting operation to the

AS7221. Once the TSL45315 is detected by the AS7221, and the Daylighting is activated by using the ATDL=1 command, Daylighting operation begins.

Synchronization and Reset

Figure 19:
Synchronization and Reset Circuit



Synchronization and Reset Circuit: AS7221 provides optional synchronization of the PWMs. This sync signal can be derived from the AC mains to enable all luminaires in a room to be synchronized to prevent beat frequency flicker. If the SYNC pin is left open, synchronization is automatically disabled by the internal pull-up connected to the SYNC/RESN pin.

Refer to the Figure above. When pulled down for more than 100ms the SYNC/RESN pin will reset the AS7221 Smart Lighting Manager. In this case the push-button "overrides" the output of the opto-coupler. Therefore a resistor should be placed in series with the opto-coupler.

AS7221 Outputs

The AS7221 outputs, used to control dimming and LED warm/cool strings, can be configured as either three PWM outputs, two PWMs and one analog output, or two PWMs. The PWMs are 12 bit and factory set to 888 Hz. Refer to the Figure below.

The three PWM outputs, PWM_1, PWM_2 and PWM_3 all switch with the same frequency, but are not simultaneous for better EMI performance.

The PWM_1 output can be set to either analog (0-VDDHV) or digital (0-VDDHV) dimming. Analog dimming range is 0-100%. Digital Dimming range is 0-100%. PWM2 and PWM3 are used for cool white and warm white LED color controlling. Either string can be warm or cool as the AS7221 automatically configures string color type. Range is 0-100% for both PWM2 and PWM3.

To set the desired device operation MODE use the appropriate R_{MODE} resistor, also shown in the Figure below.

Figure 20:
Outputs

MODE	R_{MODE}	Setting	Outputs	
			PWM_1/0_10V_O	PWM_2 and PWM_3
0	100 Ω	0-10V analog	Analog 0-VDDHV (1)	Digital PWMs (0-VDD)
1	470 Ω	0-10V digital	Digital PWM (0-VDDHV) (1)	Digital PWMs (0-VDD)
2	1000 Ω	Digital 2-CH color tuning	n.a.	Digital PWMs (0-VDD), w/Dimming

Note(s):

1. For VDDHV>10.5, output max is 10V, else output max tracks VDDHV.

Indicator LED

An LED, connected to pin LED_IND, is used to indicate programming progress of the device. During programming of the AS7221 via an external SD card, the indicator LED starts blinking operation. When programming is finished the indicator LED stays on.
The LED_IND pin is set for 1mA operation by the AS7221 factory firmware, and is not under user control.

Refer to the separate **ams** document for a complete description of AS7221 Firmware Update Methodology.

UART and Smart Lighting Command Interface

The UART block implements the TX and RX signals as defined in the RS-232 / V.24 standard communication protocol.

UART Feature List

- Full Duplex Operation (Independent Serial Receive and Transmit Registers) with FIFO buffer of 8 bytes for each.
- Factory set to 115.2k Baud
- Supports Serial Frames with 8 Data Bits, no Parity and 1 Stop Bit.

Operation

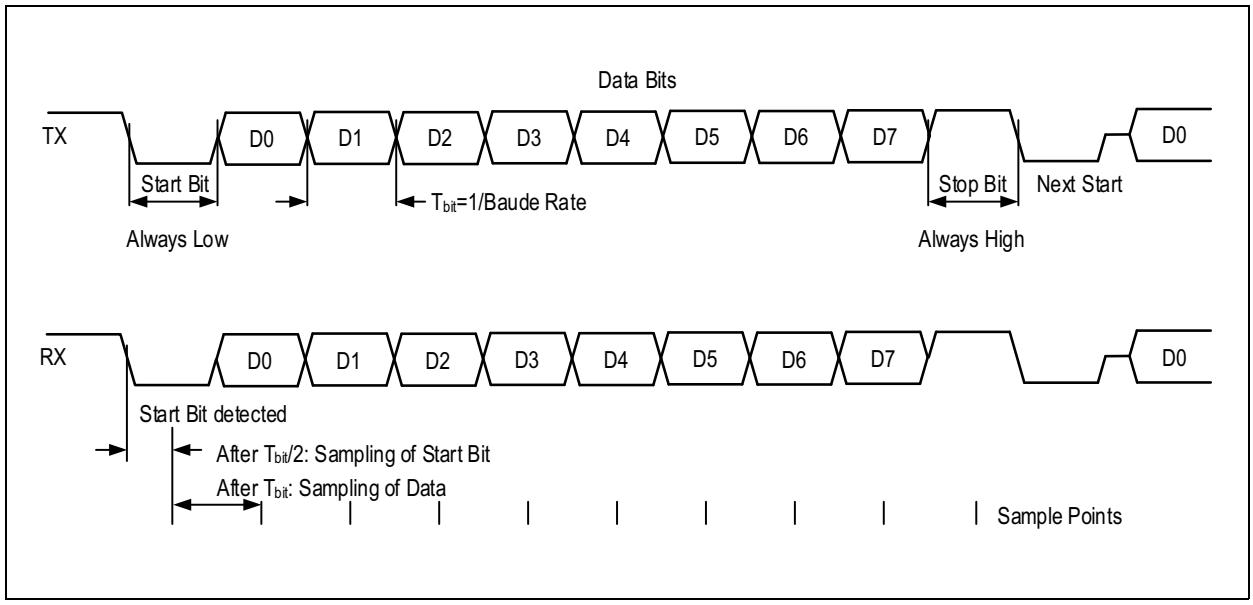
Transmission

If data is available in the transmit FIFO, it will be moved into the output shift register and the data will be transmitted at the configured Baud Rate, starting with a Start Bit (logic zero) and followed by a Stop Bit (logic one).

Reception

At any time, with the receiver being idle, if a falling edge of a start bit is detected on the input, a byte will be received and stored in the receive FIFO. The following Stop Bit will be checked to be logic one.

Figure 21:
UART Protocol



Smart Lighting Command Interface

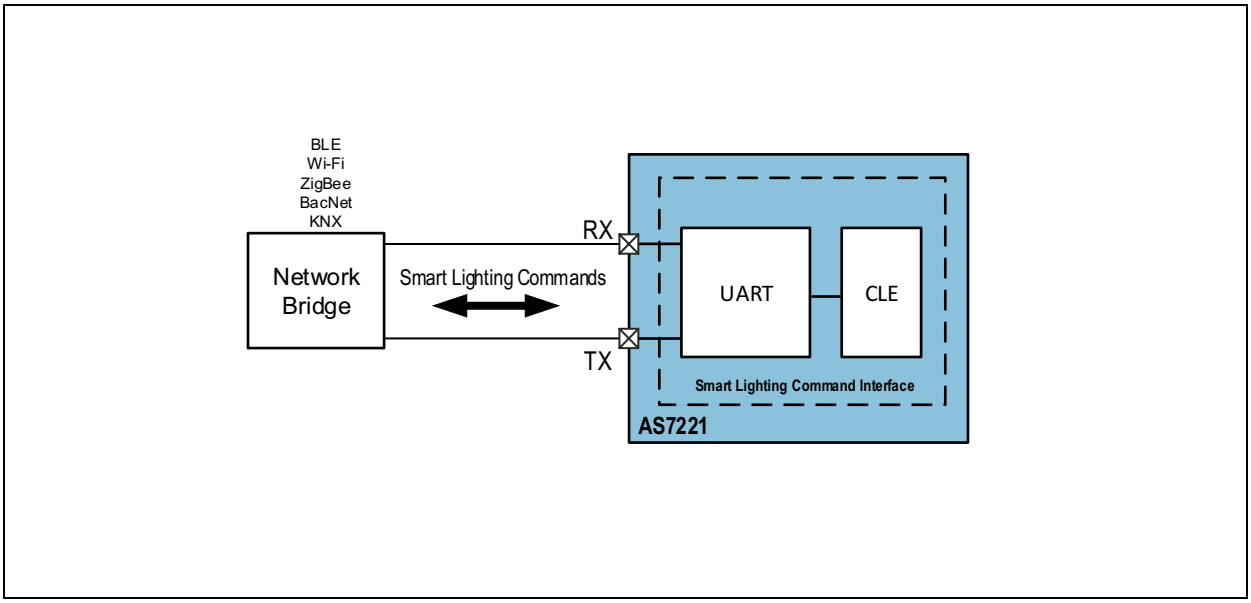
The network interface on the Smart Lighting Manager supporting the Smart Lighting Commands is the UART interface. The Smart Lighting Manager adapts the concept of a simple command set for lighting control and configuration. The Smart Lighting Manager uses a text-based serial command interface as popularized by the “AT Command” model used in early Hayes modems.

For example:

- Set the desired daylight LUX level target:
  ATLUXT = 500 >> OK

The “Smart Lighting Command Interface”, shown below between the network interface and the core of the system, provides access to the Smart Lighting Manager’s lighting control and configuration functions

Figure 22:
Smart Lighting Command Interface



Refer to the separate **ams** AS7221 Smart Lighting Command Set document for the complete command set and usage.

I²C Master Interface (Local Sensor Interface)

The I²C Master interface can be used to connect external sensors (such as daylight, occupancy, CO sensors, etc.). Refer to the separate **ams** Application Note for external sensor usage with the AS7221.

I²C Feature List

Clock is set to 100kHz

7+1-bit addressing mode.

Write formats: Single-Byte-Write, Page-Write

Read formats: Random-Read, Sequential-Read

I²C Protocol

Figure 23:
I²C Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
SW	Slave address for write	R	Slave address
SR	Slave address for read	R	Slave address
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No acknowledge	R	1 bit
Data	Data/write	R	8 bit
Data (n)	Data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Slave increment word address	R	During acknowledge

The above I²C symbol definition table describes the symbols used in the following Read and Write descriptions.

I²C Write Access

Byte Write and Page Write formats are used to write data to the slave.

Figure 24:
I²C Byte Write

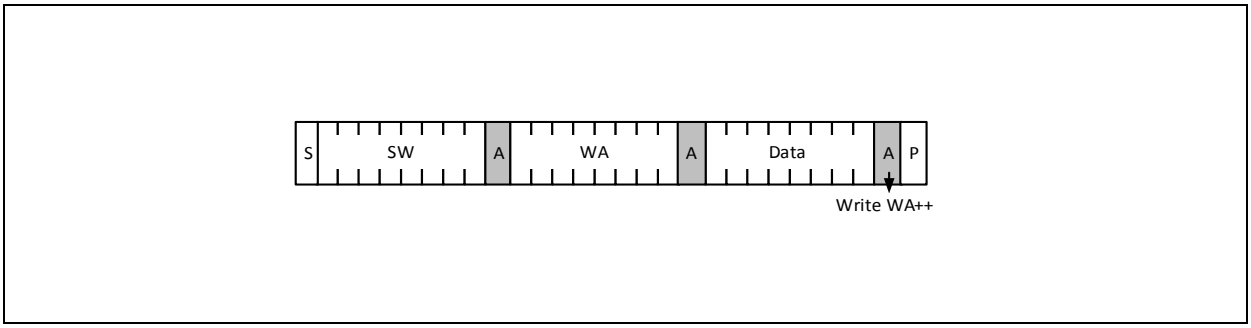
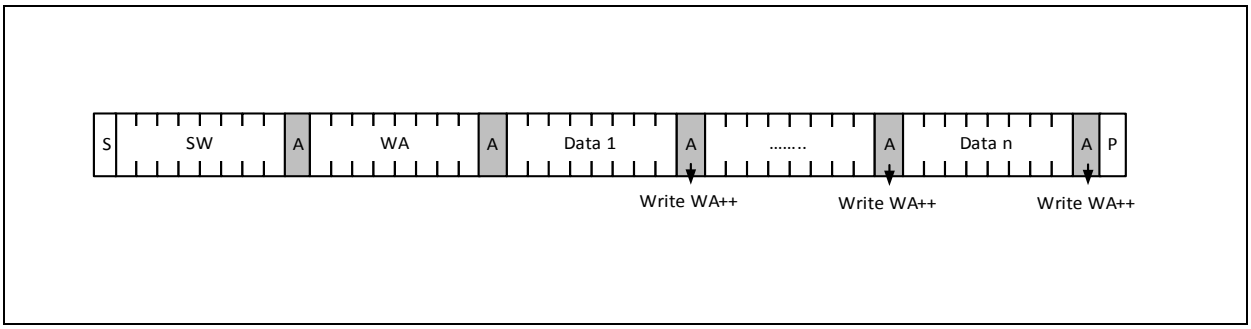


Figure 25:
I²C Page Write



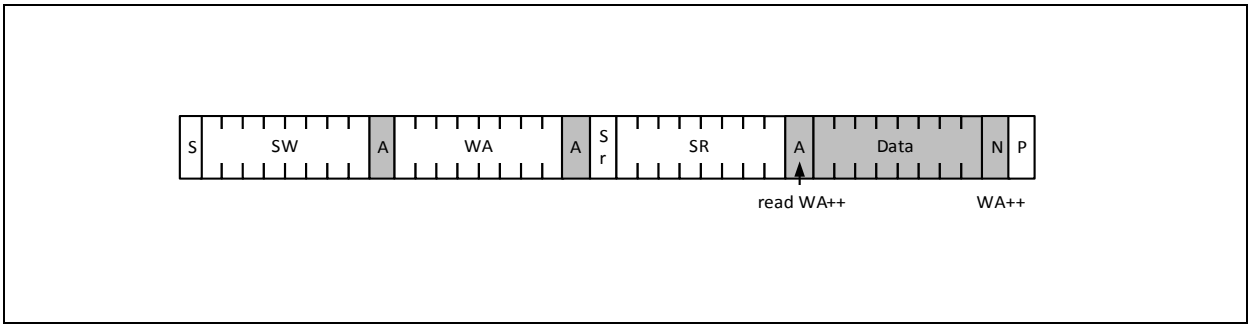
The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

I²C Read Access

Random, Sequential and Current Address Read are used to read data from the slave.

Figure 26:
I²C Random Read

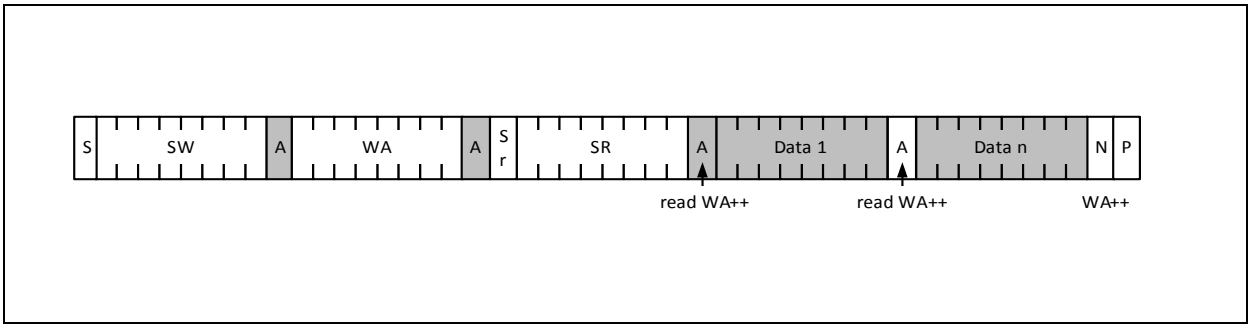


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 27:
I²C Sequential Read



I²C Sequential Read: Shows the format of an I²C sequential read access.

Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledgement from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

The AS7221 is compatible to the NXP two wire specifications.
www.nxp.com/documents/user_manual/UM10204.pdf

Version 4.0 Feb 2012 for standard mode and fast mode.

Application Information

Schematics

Figure 28:
Chromatic Color Tuning with Networking and Spectral Sensing

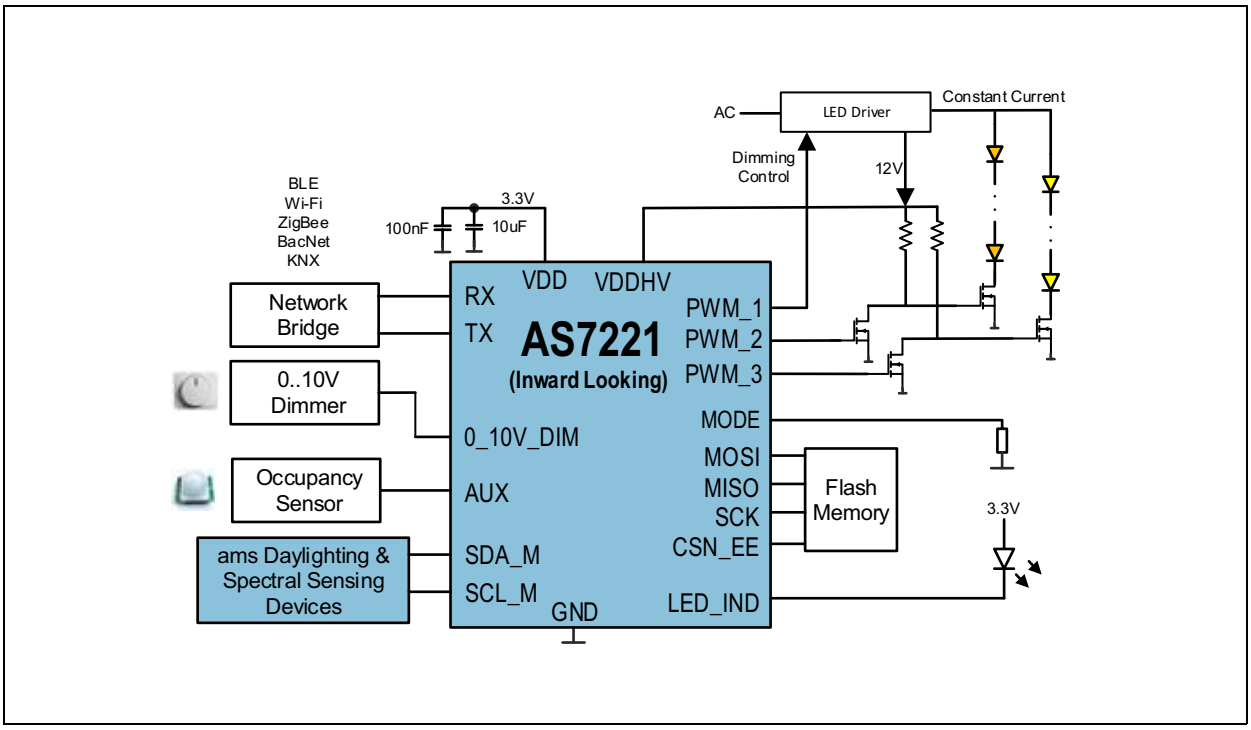
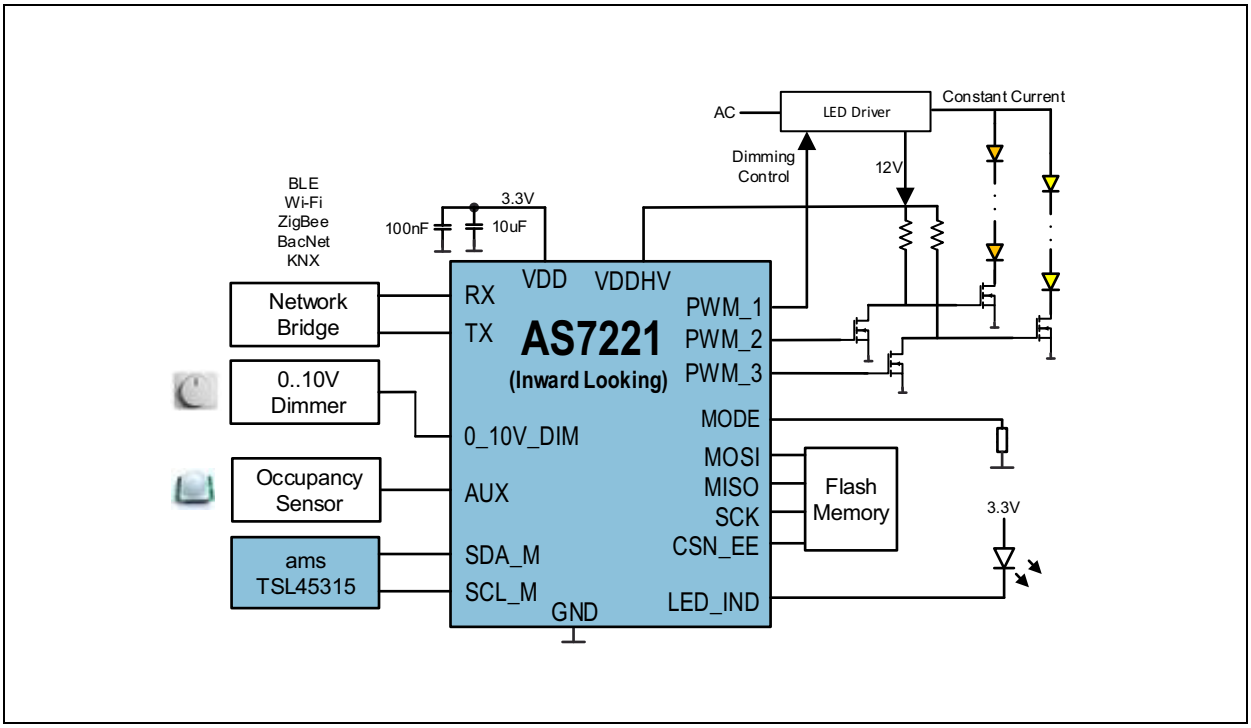
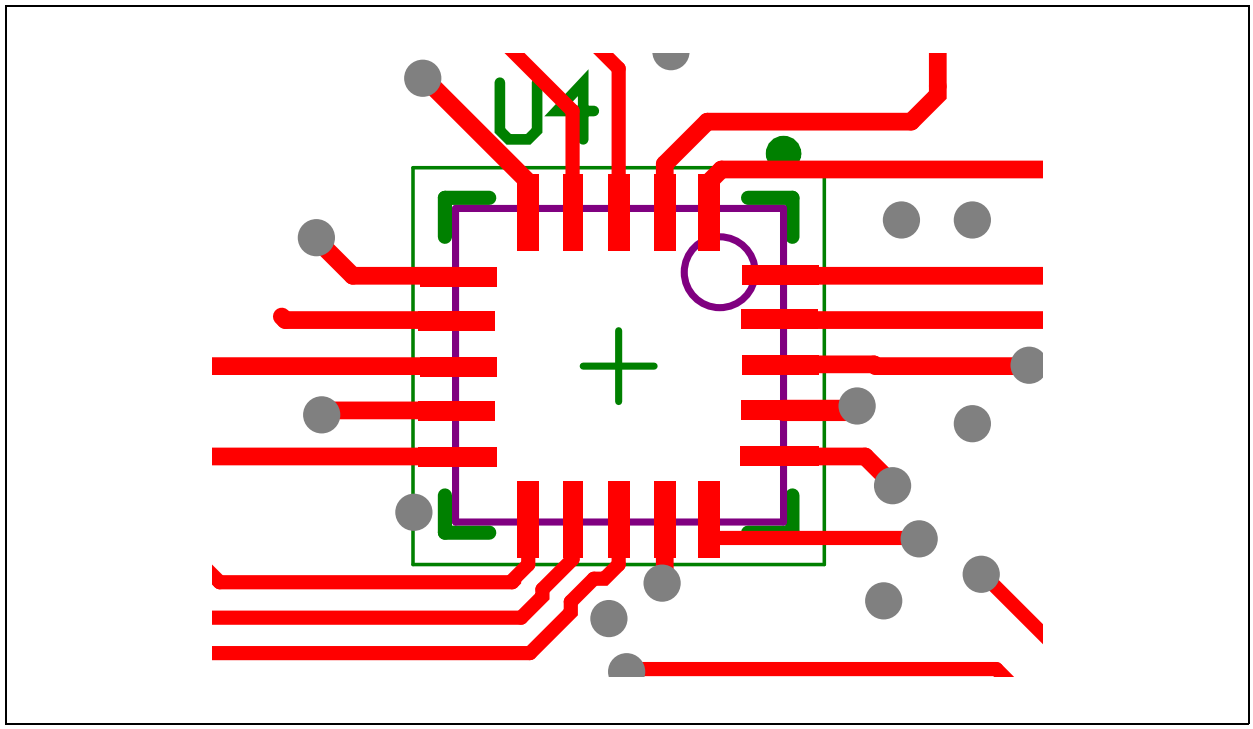


Figure 29:
LED Chromatic Color Tuning with Daylighting



PCB Layout

Figure 30:
Typical Layout Routing



In order to prevent interference, avoid trace routing feedthroughs with exposure directly under the AS7221. An example routing is illustrated in the diagram.

The AS7221 Smart Lighting Integration Kit (SLIK) demo board with schematic and PCB layout documentation is available from **ams** for additional design information.