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AS7225

Calibrated XYZ Chromatic Smart Lighting Director

General Description

The AS7225 Smart Lighting Director incorporates an embedded digital tri-stimulus chromatic 'calibrated for life' nano-optic sensor providing direct CIE1931 XYZ and CIE 1976 u'v' coordinate mapping. Adaptive algorithmic support enables a companion microprocessor to implement closed-loop, autonomous adjustment of variable CCT and daylight responsive LED lamps and luminaires. The AS7225 arrives pre-calibrated, and is designed for rapid integration into white-tunable and daylight responsive luminaire designs, delivering directives to the local microprocessor via an industry-standard I^2C bus.

An additional on-chip I^2C master provides native support for select **ams** sensors, such as the TSL4531 for combining in-looking CCT tunable director functions with outward-looking ambient light sensing and daylighting control. The AS7225 integrates standard-observer filters onto the silicon via nano-optic deposited interference filters which deliver high-stability over time and temperature. The LGA package includes a built in aperture to control light entering the sensor array. Integrated intelligence enables lifetime CCT calibration to within 2-4 Macadam steps.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of this device are listed below:

Figure 1:
Added Value of Using AS7225

Benefits	Features
• Provides accurate external host MCU supervision of variable CCT and spectrally tunable lighting	• Integrated intelligence with XYZ tri-stimulus color sensing for direct translation to CIE 1931 standard observer color map
• Uses accurate XYZ sensed data to provide a host MCU, with its own PWMs, simple to use directives for closed loop tuned LED lighting	• Automatically directs external warm and cool white PWM controlled LED strings for chromatic LED luminaire tuning. Also directs dimming (combined with PWM color tuning)
• Automatic spectral and lumen maintenance over temperature and time	• Supports autonomous color point and lumen output adjustment resulting in automatic spectral and lumen maintenance

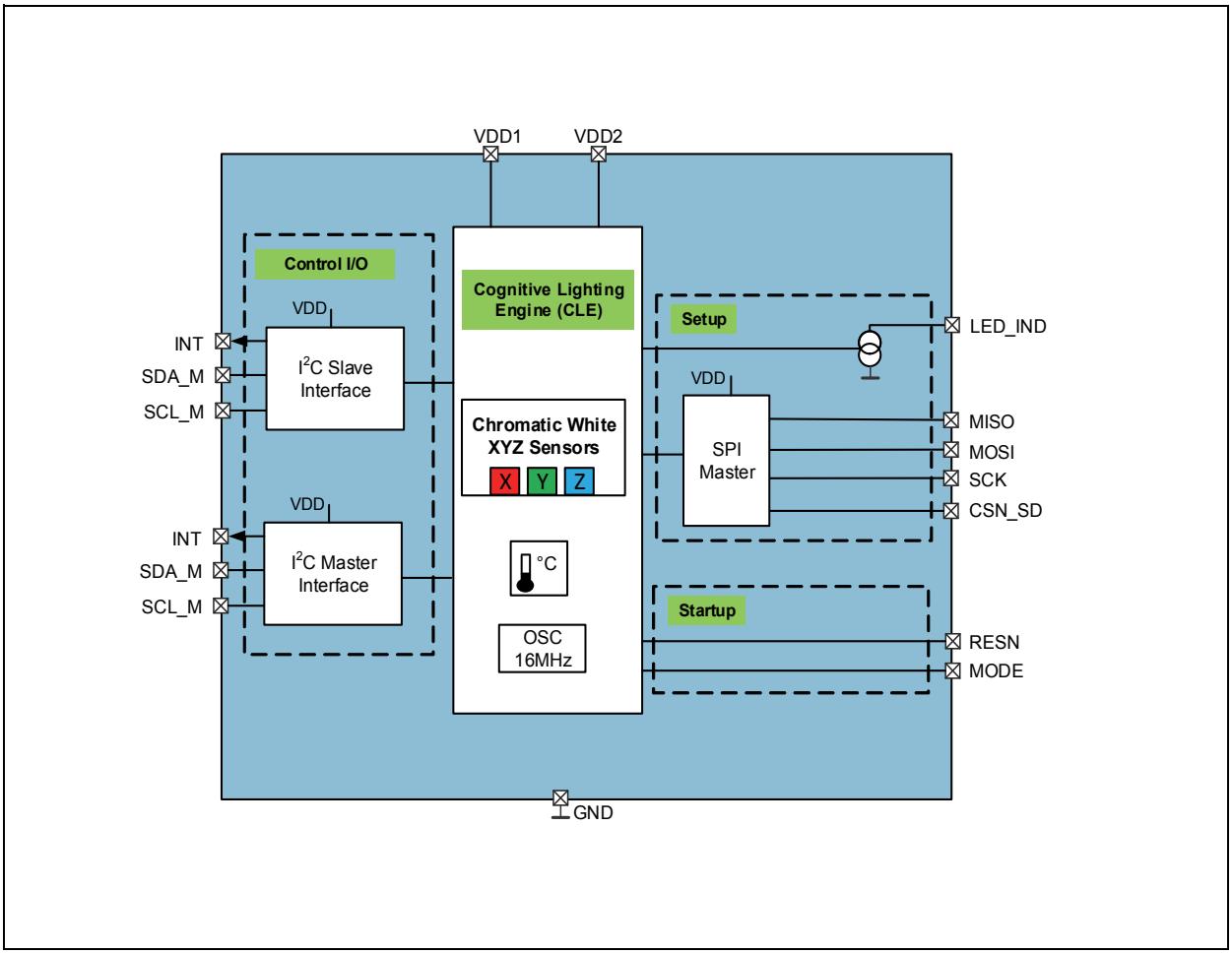
Benefits	Features
• Provides direct register based access to closed loop tuning directives	• I^2C slave digital Interface
• Used to interface other **ams** sensors with native support by the AS7225 (e.g. TSL4531 for adding Daylighting operation)	• I^2C master digital interface
• Rapid luminaire integration	• Simple register-based commands to control and configure key light-tuning supervisory and IoT sensor expansion functions
• Complete data on lighting environment	• Readable registers for CIE 1931 and 1975 color-point coordinates, CCT, duv and lux
• Calibrated sensing with minimal drift over time or temperature	• Chromatic white color realized by silicon interference filters
• Small package, with build in aperture	• 20-pin LGA package 4.5mm x 4.7mm x 2.5mm, -40°C to 85°C

Applications

- Variable CCT chromatic tuning luminaires and systems
- Daylighting-responsive luminaires and systems
- Commercial, retail, and residential white tunable/Kelvin-changing LED lighting systems
- Networked smart lighting systems

Block Diagram

Figure 2:
Functional Blocks of AS7225



Block Diagram: The AS7225 Directs real-time closed loop Chromatic White sensing and PWM tuning to an external host MCU via I^2C.

Pin Assignments

Figure 3:
Pin Diagram of AS7225 (Top View)

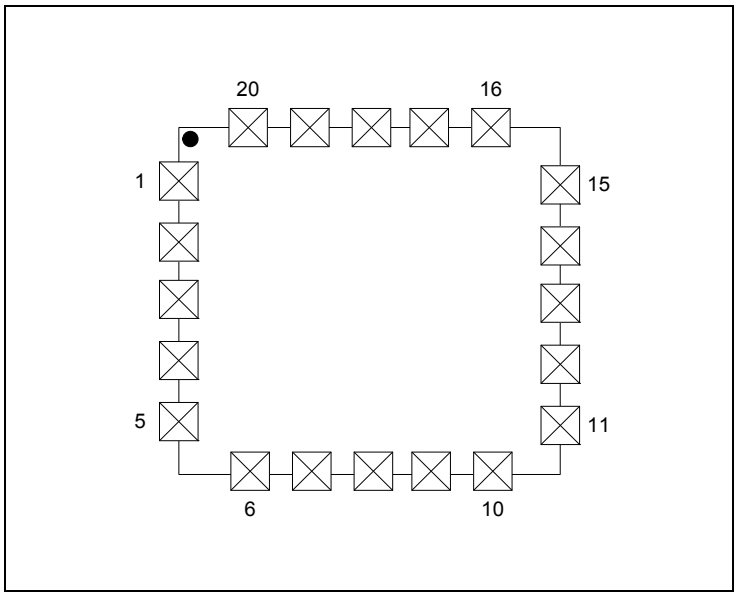


Figure 4:
Pin Description of AS7225 (20 pin LGA)

Pin Number	Pin Name	Description
1	NF	Not Functional, do not connect or route to pin
2	RESN	Reset pin, active low
3	SCK	SPI serial clock
4	MOSI	SPI MOSI
5	MISO	SPI MISO
6	CSN_EE	Chip select for the required external serial flash memory, active low
7	CSN_SD	Chip select for SD Card interface, active low
8	NF	Not Functional, do not connect or route to pin
9	SCL_M	I^2C master clock pin
10	SDA_M	I^2C master data pin
11	SCL_S	I^2C slave clock pin
12	SDA_S	I^2C slave data pin
13	INT	INT (interrupt) is active Low
14	VDD2	VDD Voltage Supply

Pin Number	Pin Name	Description
15	MODE	Mode selection pin. Set to MODE=0 via 100Ω resistor. Other Modes are reserved.
16	GND	Ground
17	VDD1	VDD Voltage Supply
18	LED_IND	LED Driver output for Indicator LED, current sink
19	NF	Not Functional, do not connect or route to pin
20	NF	Not Functional, do not connect or route to pin

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device is not designed for high energy UV (ultraviolet) environments, including upward looking outdoor applications, which could affect long term optical performance.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD_MAX}	Supply Voltage VDD	-0.3	5	V	Pins VDD1 and VDD1 must be sourced from the same supply voltage
V_{DD_IO}	Input/Output Pin Voltage	-0.3	VDD + 0.3	V	Low Voltage pins to GND
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JESD78D
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±1000		V	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM	±500		V	JSD22-C101F
Temperature Ranges and Storage Conditions					
T_{strg}	Storage Temperature	-40	85	°C	
T_{body}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a 168 hour max. floor lifetime

Electrical Characteristics

All limits are guaranteed with VDD = VDD1 = VDD2 = 3.3V, T_{AMB} = 25°C. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.
VDD1 and VDD2 must be sourced from the same 2.7-3.6V supply source.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General Operating Conditions						
VDD	Low Voltage operating Supply		2.7	3.3	3.6	V
T_{AMB}	Operating Temperature		-40	25	85	°C
I_{VDD}	Operating Current				5	mA
Internal RC Oscillator						
F_{OSC}	Internal RC oscillator frequency		15.7	16	16.3	MHz
t_{JITTER} (1)	Jitter	@25°C			1.2	ns
Temperature Sensor						
D_{TEMP}	Absolute accuracy of the internal temperature measurement		-8.5		8.5	°C
Indicator LED						
I_{IND}	LED Current		1		8	mA
I_{ACC}	Accuracy of Current		-30		30	%
V_{LED}	Voltage range of connected LED	Vds of current sink	0.3			V
Digital Inputs and Outputs						
V_{IH}	CMOS Logic High Input		0.7* VDD		VDD	V
V_{IL}	CMOS Logic Low Input		0		0.3* VDD	V
V_{OH}	CMOS Logic High Output	I=1mA			VDD-0.4	V
V_{OL}	CMOS Logic Low Output	I=1mA			0.4	V
I_{Ih}, I_{IL}	Logic Input Current	Vin=0V or VDD	-1		1	µA
t_{RISE} (1)	Current rise time	C(Pad)=30pF			5	ns
t_{FALL} (1)	Current fall time	C(Pad)=30pF			5	ns

Note(s):

1. Guaranteed, not production tested

Figure 7:
AS7225 I²C Slave Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C Interface						
f_{SCLK}	SCL Clock Frequency		0		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HD:STA}$	Hold Time (Repeated) START		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	CB — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

Figure 8:
I²C Slave Timing Diagram

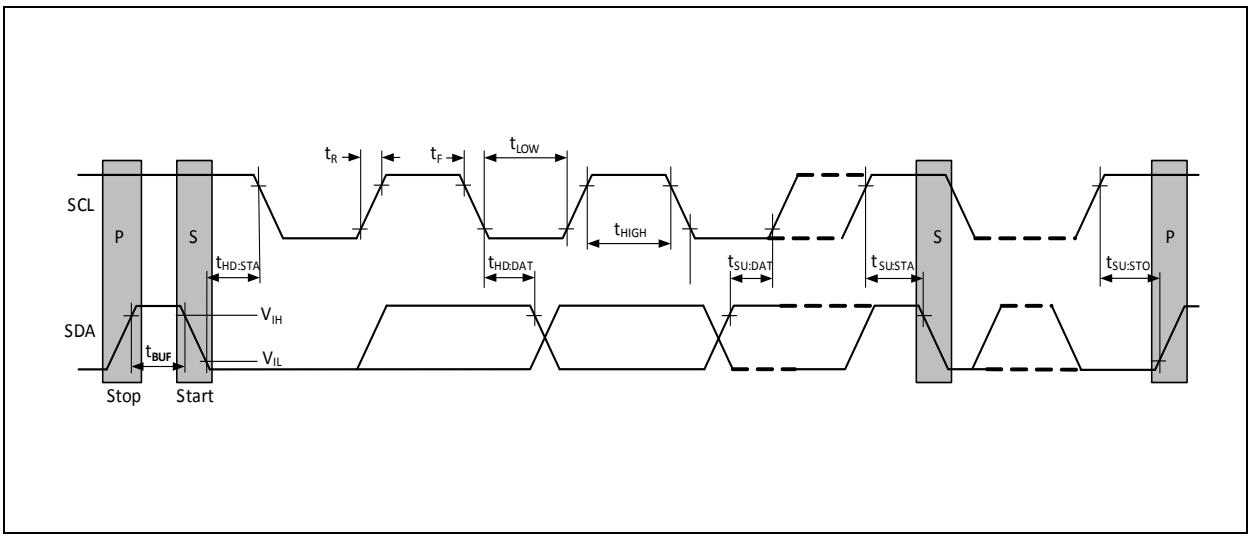


Figure 9:
AS7225 I²C Master Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C Interface						
f_{SCLK}	SCL Clock Frequency			100	400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HD:STA}$	Hold Time (Repeated) START		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	CB — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

Figure 10:
I²C Master Timing Diagram

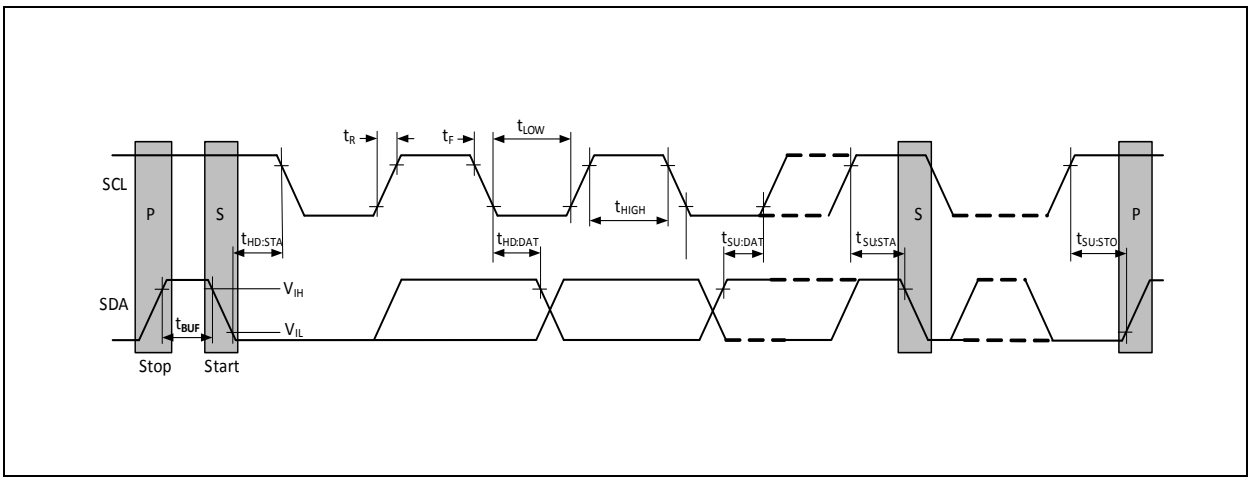


Figure 11:
AS7225 SPI Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI Interface						
f_{SCK}	Clock frequency		0		16	MHz
t_{SCK_H}	Clock high time		40			ns
t_{SCK_L}	Clock low time		40			ns
t_{SCK_RISE}	SCK rise time		5			ns
t_{SCK_FALL}	SCK fall time		5			ns
t_{CSN_S}	CSN setup time	Time between CSN high-low transition to first SCK high transition	50			ns
t_{CSN_H}	CSN hold time	Time between last SCK falling edge and CSN low-high transition	100			ns
t_{CSN_DIS}	CSN disable time		100			ns
t_{DO_S}	Data-out setup time		5			ns
t_{DO_H}	Data-out hold time		5			ns
t_{DI_V}	Data-in valid		10			ns

Figure 12:
SPI Master Write Timing Diagram

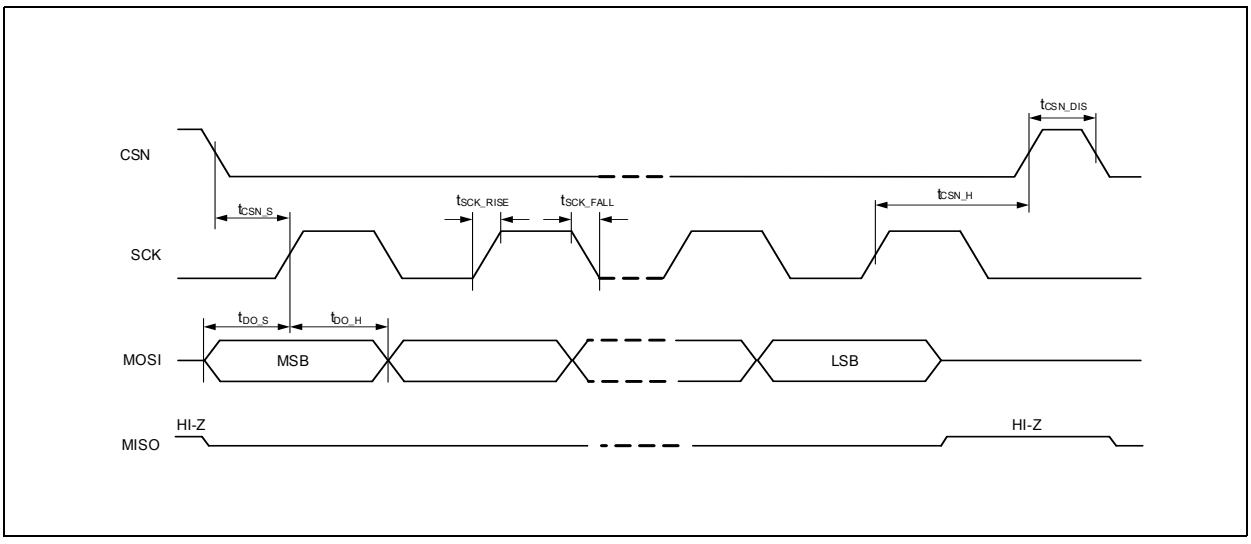


Figure 13:
SPI Master Read Timing Diagram

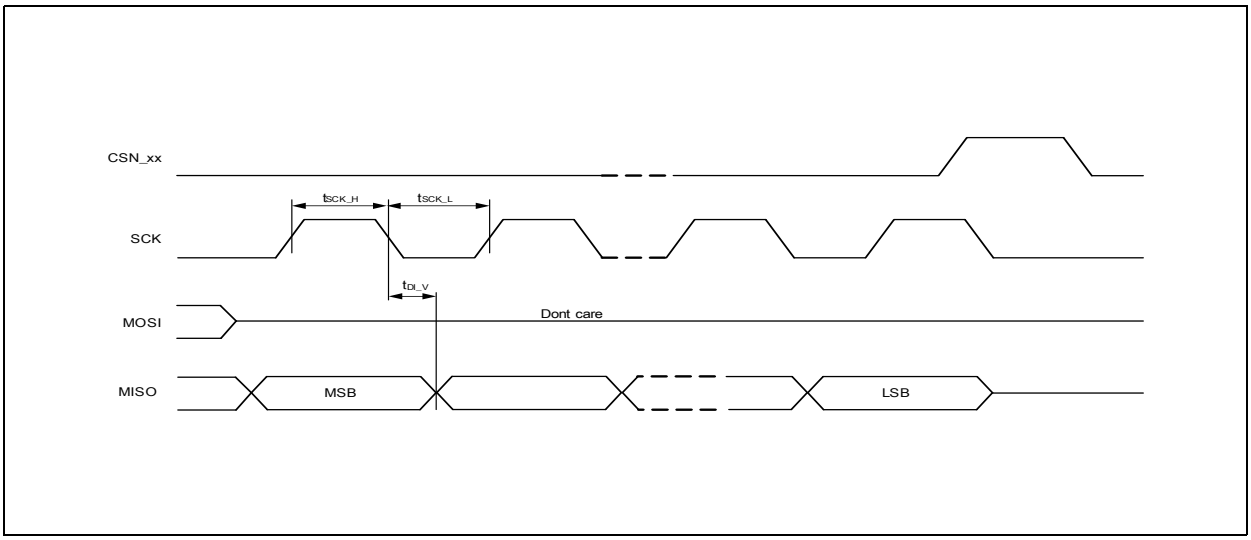


Figure 14:
Typical Spectral Responsivity

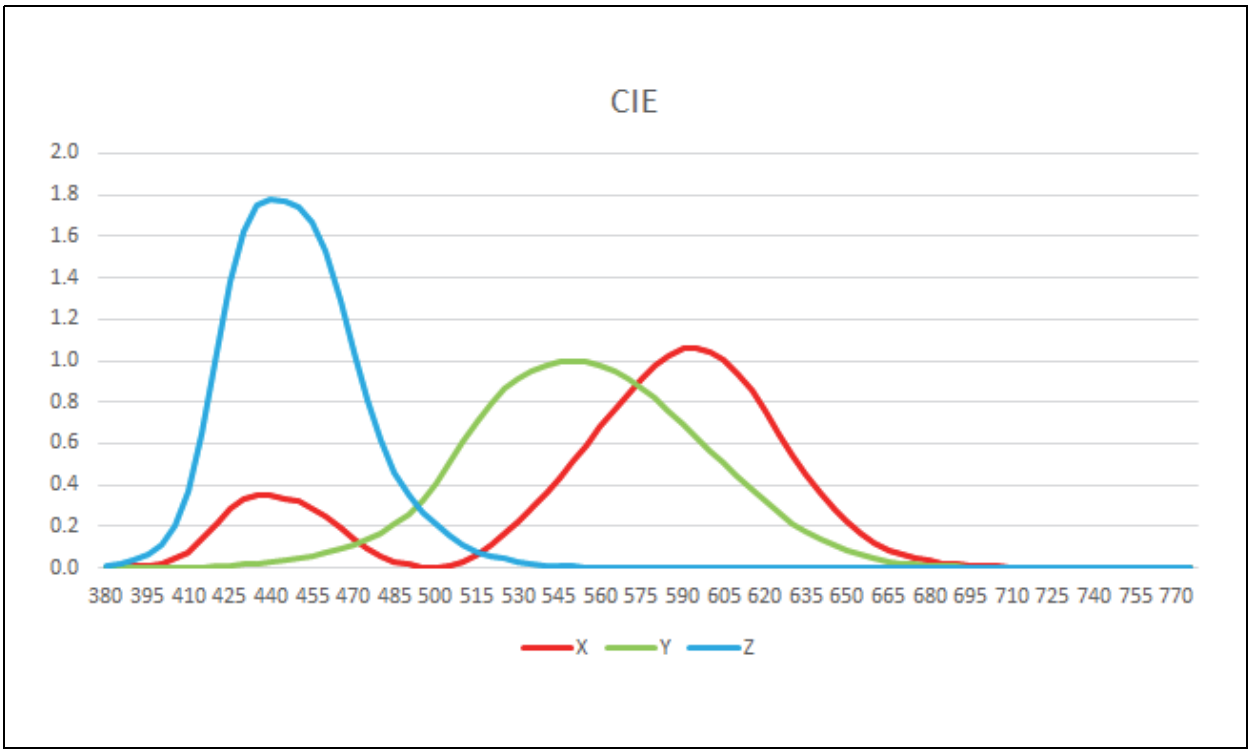


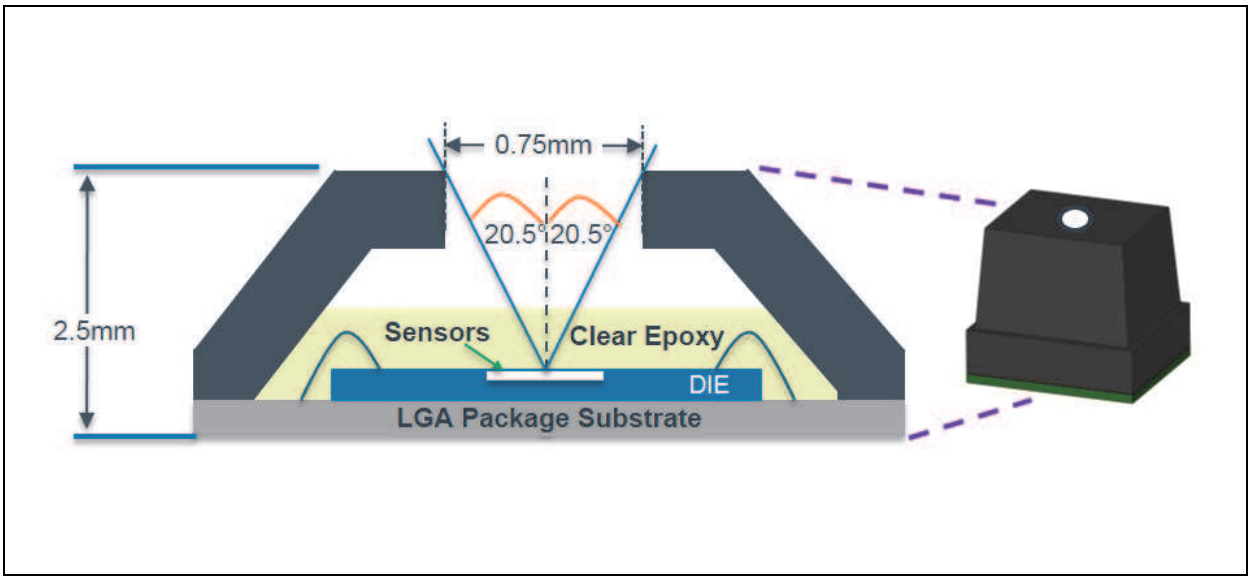
Figure 15:
AS7225 Optical Characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
Color_m (2)	Color measurement accuracy	White Light CCT = 2700K, 3500K, 4500K and 5700K		0.002		du'v'
Z_count	Z channel count accuracy	White Light CCT = 5700K	3.375	4.5	5.625	counts/ ($\mu W/cm^2$)

Note(s):

1. Typical values at Lux ≥50, Integration time=400.4ms, Gain=1x, T_{AMB} = 25°C.
2. Calibration and measurements are made using diffused light

Figure 16:
AS7225 LGA Package Field of View



Detailed Description

AS7225 XYZ Chromatic White Color Director

The AS7225 serves as a White Color Director for a companion host MCU. This provides high level calculated white color tuning control loop information for external LED channel PWMs via I^2C registers. Director operation also provides selectable dimming information for either PWM based or independent luminaire dimming designs.

The integrated tri-stimulus sensing element is designed to meet the XYZ standard observer response compliant with the CIE 1931 standard. The device uses a 16-bit integrating analog-to-digital converter which integrates current from photodiodes. To ensure integrity of the data, upon completion of an integration cycle, results are transferred to double-buffered registers.

XYZ color point response is accomplished via standard observer interference filters which are extremely stable over time and temperature. To ensure accuracy, the AS7225 LGA package contains an internal aperture that limits the sensor field of view (PFOV) of ± 20.5°, as shown in the figure above. External optics can be used as needed to expand or reduce this built in PFOV.

For Daylight operation the AS7225 can be used two ways. As a standalone device pointing out of the luminaire, or if pointing inward for white color, it can support daylighting operation by using an I^2C master connected **ams** TSL4531 for ambient light sensing. In either case the AS7225 is the Daylighting engine and directs the external MCU.

Overall AS7225 timing generation uses an on chip 16MHz temperature compensated oscillator for master clock timing.

MODE Pin

The AS7225 MODE pin must be connected to ground (GND) via a 100Ω resistor (1%) to set the AS7225 mode of operation. All other MODEs (using other resistor values) are reserved.

Indicator LED

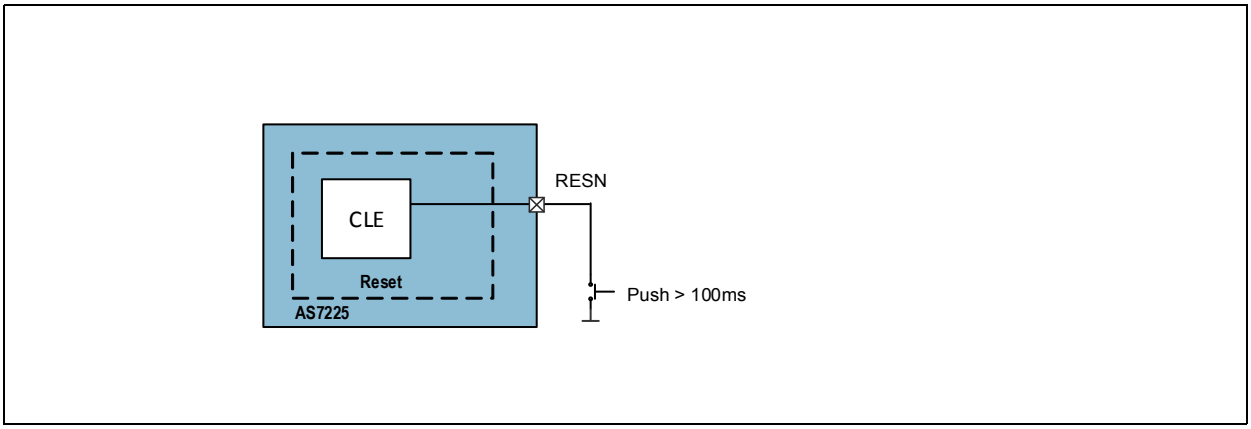
An LED, connected to pin LED_IND, is used to indicate programming progress of the device. During programming of the AS7225 via an external SD card, the indicator LED starts blinking operation. When programming is finished the indicator LED stays on. The LED_IND pin is set for 1mA LED operation by the AS7225 factory firmware, and is not under user control.

Refer to the separate **ams** document for a complete description of AS7225 Firmware Update Methodology.

Reset

Pulling down the RESN pin for longer than 100ms resets the AS7225.

Figure 17:
Reset Circuit



Interrupt Operation

Register bits DATA_RDY and PWM_RDY and the INT pin are used to monitor sensor integration activity complete and whether PWM target information is available for the MCU. If the interrupt register bit for either are enabled (RDY_INT = 1, PWM_INT =1) then when either of these activities become active, indicating available data, the INT pin is pulled low in addition to setting the ready register bit(s). The INT Line is released when the appropriate control register (CONV_Control and/or DIR_ Control) is read. DATA_RDY is cleared to 0 when any of the sensor registers X, Y, Z are read. For multi-byte sensor data (2 or 4 bytes), after the 1st byte is read the remaining get shadow buffer protected in case an integration cycle completes just after the 1st byte is read.

I²C Slave Interface

Interface and control can be accomplished through an I²C compatible slave interface to a set of registers that access device control functions and output data. These control and output registers on the AS7225 are, in reality, implemented as *virtual* registers in software. The actual I²C slave hardware registers number only three and are described in the table below. The steps necessary to access the virtual registers defined in the pages that follow are explained in pseudocode for external I²C master writes and reads below.

I²C Feature List

- Fast mode (400kHz) and standard mode (100kHz) support.
- 7+1-bit addressing mode.
- Write format: Byte.
- Read format: Byte.

Figure 18:
I²C Slave Device Address and Physical Registers

Entity	Description	Note
Device Slave Address	8-bit Slave Address	Byte = 1001001x (device address = 49 hex) x= 1 for Master Read (byte = 93 hex) x= 0 for Master Write (byte = 92 hex)
STATUS Register	I²C slave interface STATUS register. Read-only.	Register Address = 0x00 Bit 1: TX_VALID 0 -> New data may be written to WRITE register 1 -> WRITE register occupied. Do NOT write. Bit 0: RX_VALID 0 -> No data is ready to be read in READ register. 1 -> Data byte available in READ register.
WRITE Register	I²C slave interface WRITE register. Write-only.	Register Address = 0x01 8-Bits of data written by the I²C Master intended for receipt by the I²C slave. Used for both *virtual* register addresses and write data.
READ Register	I²C slave interface READ register. Read-only.	Register Address = 0x02 8-Bits of data to be read by the I²C Master.

I²C Virtual Register Write Access

I²C Virtual Resister Byte Write, detailed below, shows the pseudocode necessary to write virtual registers on the AS7225. Note that, because the actual registers of interest are realized as virtual registers, a means of indicating whether there is a pending read or write operation of a given virtual register is needed. To convey this information, the most significant bit of the virtual register address is used as a marker. If it is 1, then a write is pending, otherwise the slave is expecting a virtual read operation. The pseudocode illustrates the proper technique for polling of the I²C slave status register to ensure the slave is ready for each transaction.

I²C Virtual Register Byte Write

Pseudocode

Poll I²C slave STATUS register;
If TX_VALID bit is 0, a write can be performed on the interface;
Send a virtual register address and set the MSB of the register address to 1 to indicate the pending write;
Poll I²C slave STATUS register;
If TX_VALID bit is 0, the virtual register address for the write has been received and the data may now be written;
Write the data.

Sample Code:

```
#define I2C_AS72XX_SLAVE_STATUS_REG     0x00
#define I2C_AS72XX_SLAVE_WRITE_REG      0x01
#define I2C_AS72XX_SLAVE_READ_REG       0x02
#define I2C_AS72XX_SLAVE_TX_VALID       0x02
#define I2C_AS72XX_SLAVE_RX_VALID       0x01

void i2cm_AS72xx_write(uint8_t virtualReg, uint8_t d)
{
        volatile uint8_tstatus;

        while (1)
{
                // Read slave I2C status to see if the write buffer is ready.
                status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG);

                if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                        // No inbound TX pending at slave.  Okay to write now.
                        break ;
        }
        // Send the virtual register address (setting bit 7 to indicate a pending write).
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, (virtualReg | 0x80)) ;

        while (1)
{
                // Read the slave I2C status to see if the write buffer is ready.
                status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

                if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                        // No inbound TX pending at slave.  Okay to write data now.
                        break ;
        }
        // Send the data to complete the operation.
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, d) ;
}
```

I²C Virtual Register Read Access

I²C Virtual Register Byte Read, detailed below, shows the pseudocode necessary to read virtual registers on the AS7225. Note that in this case, reading a virtual register, the register address is not modified.

I²C Virtual Register Byte Read

Pseudocode

```
Poll I²C slave STATUS register;
If TX_VALID bit is 0, the virtual register address for the read may be written;
Send a virtual register address;
Poll I²C slave STATUS register;
If RX_VALID bit is 1, the read data is ready;
Read the data.
```

Sample Code:

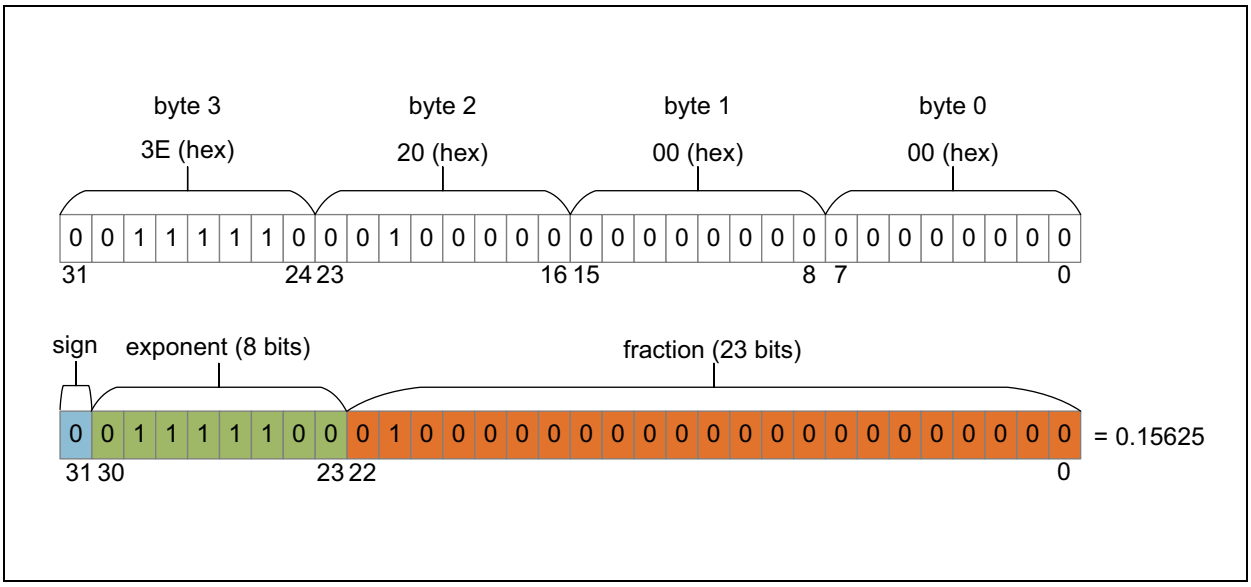
```
uint8_t i2cm_AS72xx_read(uint8_t virtualReg)
{
	volatile uint8_t status, d ;

	while (1)
{
		// Read slave I2C status to see if the read buffer is ready.
		status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

		if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
			// No inbound TX pending at slave.  Okay to write now.
			break ;
	}
	// Send the virtual register address (setting bit 7 to indicate a pending write).
	i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, virtualReg) ;

	while (1)
{
		// Read the slave I2C status to see if our read data is available.
		status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

		if ((status & I2C_AS72XX_SLAVE_RX_VALID) != 0)
			// Read data is ready.
			break ;
	}
	// Read the data to complete the operation.
	d = i2cm_read(I2C_AS72XX_SLAVE_READ_REG) ;
	return d ;s
}
```

The details of the `i2cm_read()` and `i2cm_write()` functions in previous Figures are dependent upon the nature and implementation of the external I²C master device.

4-Byte Floating-Point (FP) Registers

In addition to single and two byte, several 4 byte registers (hex) are shown in the tables starting below. Here is an example of how the registers are used to represent floating point data (based on the IEEE 754 standard):

Figure 19:
Example of the IEEE 754 Standard



The floating point (FP) value assumed by 32 bit binary32 data with a biased exponent e (the 8 bit unsigned integer) and a 23 bit fraction is (for the above example):

$$\text{(EQ1)} \quad FPvalue = (-1)^{sign}\left(1 + \sum_{i=1}^{23} b_{23-i}2^{-i}\right) \times 2^{(e-127)}$$

$$\text{(EQ2)} \quad FPvalue = (-1)^{0}\left(1 + \sum_{i=1}^{23} b_{23-i}2^{-i}\right) \times 2^{(124-127)}$$

$$\text{(EQ3)} \quad FPvalue = 1 \times (1 + 2^{-2}) \times 2^{(-3)} = 0.15625$$

I²C Virtual Register Set

The Figure below provides a summary of the AS7225 I²C register set. Figures after that provide additional register details. All register data is hex, and all multi-byte entities are Big Endian (most significant byte is situated at the lowest register address).

Multiple byte registers (2 byte integer or 4 byte floating point) must be read in the order of ascending register addresses (low to high). And if capable of being written to, must also be written in the order of ascending register addresses.

Figure 20:
I²C Virtual Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Device Version Registers									
0x00	HW_V_H								
0x01	HW_V_L								
0x02	FW_V_H								
0x03	FW_V_L								
General Setup and Control Registers									
0x04	CONV_Control	OVFL	RDY_INT	GAIN		RSVD		DATA_RDY	RST
0x05	INTEG_T								
0x06	Device_Temp								
0x08	LED_String_ Init	RSVD					SLH	LEARN	FRST
Director Operation Registers									
0x64	DIR_Control	NUM_CHAN			PWM_INT	CT_EN	DL_EN	START	PWM_ RDY
0x65	DIR_Setup	RSVD				PWM2	PWM1	CT_MODE	
0x50	DIR_CH_1_L								
0x51	DIR_CH_1_H								
0x52	DIR_CH_2_L								
0x53	DIR_CH_2_H								
0x60	DIR_CCTT_L								
0x61	DIR_CCTT_H								
0x62	DIR_LUXT_L								
0x63	DIR_LUXT_H								

0x66	DIR_LUX_ MAX_L								
0x67	DIR_LUX_ MAX_H								
0x44: 0x47	X_Scale								
0x48: 0x4B	Y_Scale								
0x4C: 0x4F	Z_Scale								
0x70: 0x73	X_D_Scale								
0x74: 0x77	Y_D_Scale								
0x78: 0x7B	Z_D_Scale								
Calibrated Sensor Result Registers									
0x14: 0x17	Cal_X								
0x18: 0x1B	Cal_Y								
0x1C: 0x1F	Cal_Z								
0x20: 0x23	Cal_x_1931								
0x24: 0x27	Cal_y_1931								
0x28: 0x2B	Cal_u_pri								
0x2C: 0x2F	Cal_v_pri								
0x30: 0x33	Cal_u								
0x34: 0x37	Cal_v								
0x38: 0x3B	Cal_DUV								
0x3C	Cal_LUX_L								

0x3D	Cal_LUX_H								
0x3E	Cal_CCT_L								
0x3F	Cal_CCT_H								

Hardware Version Registers

These byte registers are used together as HW_V_H: HW_V_L

Figure 21:
Hardware Version Registers

Addr: 0x00		HW_V_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device Type	01000000	R	Device type number
Addr: 0x01		**HW_V_L**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	HW Version	00011001	R	Hardware version number

Firmware Version Registers

These byte registers are used together as FW_V_H: FW_V_L

Figure 22:
Firmware Version Registers

Addr: 0x02		FW_V_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Major Version	-	R	Major version
3:0	Minor Version	-	R	Minor version [5:2]

Addr: 0x03		FW_V_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Minor Version	-	R	Minor version [0:1]
5:0	Sub Version	-	R	Sub version

Figure 23:
CONV_Control Register

Addr: 0x04/0x84 (R/W)		CONV_Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	OVFL	0	R	1 = At least one of the sensor channels has saturated (overflow). Solution is to reduce Gain or Integration time. Cleared (=0) after read if set. Cleared (=0) after device reset.
6	RDY_INT	0	R/W	1 = Interrupt pin will be driven low when DATA_RDY bit is set. 0 = DATA_RDY bit does not set interrupt.
5:4	GAIN	00	R/W	Sensor Channel Gain Setting (all sensors, Read/Write 00=1x Gain; 01=3.7x; 10=16x; 11=64x
3:2	RSVD	00		Reserved, do not use
1	DATA_RDY	0	R	1= Conversion Data Ready to read, sets INT active if interrupt is enabled. Can be polled independent of INT usage. Cleared (=0) after read if set. Cleared (=0) after device reset.
0	RST	0	R/W	Soft Reset, set to 1 for soft reset. Goes to 0 when complete.

Figure 24:
INTEG_T Register

Addr: 0x05/0x85 (R/W)		INTEG_T		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	INTEG_T	-	R/W	Sensor Integration time = <value>*2.8ms (valid value range 1-255)

Figure 25:
Device_Temp Register

Addr: 0x06		Device_Temp		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device_Temp	-	R	Device internal temperature (1 byte). Byte is a hex integer value, in °C.

LED String Initialization Register

LED string initialization must be performed at least once, and is initiated by the AS7225 if the SLH bit=0. While in LEARN operation LUX and CCT targets from the host MCU are ignored. Once complete Director based tuning, with MCU set LUX and CCT targets, can begin. String Learn History is stored in persistent memory, so if a FRST is performed a LEARN operation will be initiated. After SLH=1, the MCU can initiate a LEARN by setting LEARN=1.

Figure 26:
LED String Initialization Register

Addr: 0x08/0x88 (R/W)		LED_String_Init		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	RSVD	00000		Reserved, do not use
2	SLH	0	R	String Learn History. If set to 1, a prior LEARN operation has been performed. SLH value is stored in persistent memory but will be cleared if a FRST operation is performed.
1	LEARN	0	R/W	If=1 Directs the MCU through an LED String Learn operation: • Learns Warm and Cool LED string numbers (string 1 or 2) • Learns Warm and Cool LED string CCT values • Learns max LUX LEARN is set by the AS7225 automatically if SLH=0. After SLH=1, the MCU can set it at any time to initiate another Learn.
0	FRST	0	R/W	Factory Reset. Setting to 1 clears persistent memory data and then performs a soft reset. Goes to 0 when complete.

Figure 27:
DIR_Control Register

Addr: 0x64/0xE4 (R/W)		DIR_Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
All bits except bit 0 are set (or read) by the external MCU. Bit 0 is read only by the external MCU				
7:5	NUM_CHAN	010	R/W	010 = 2 channels (PWM1-PWM2) 001 = 1 channel (PWM1 only, which is used for Daylighting if no TSL4531 is attached. Daylighting bit must be set to 1.) (all other 7:5 values are reserved)
4	PWM_INT	0	R/W	When 1 = INT pin will be driven low when PWM_RDY is set 0 = INT pin will not be driven low when PWM_RDY is set
3	CT_EN	1	R/W	1 = overall Color Tuning function enabled 0 = disabled
2	DL_EN	1	R/W	1 = Daylighting function enabled 0 = disabled
1	START	0	R/W	1=host MCU has completed last directive and is ready for AS7225 conversion start. Cleared by AS7225 automatically after being set, and at device reset.
0	PWM_RDY	0	R/W	1=New PWM target value directives are ready for the MCU. To return to 0 it must be set to 0 by the host MCU.

Figure 28:
DIR_Setup Register

Addr: 0x65/0xE5 (R/W)		DIR_Setup		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
All bits except bits 7:4 are set (or read) by the external MCU				
7:4	RSVD	0000	-	Reserved, do not use
3	PWM2	1	R/W	Set =1 for color tuning with PWM2 Set =0 for no color tuning with PWM2
2	PWM1	1	R/W	Set =1 for color tuning with PWM1 Set =0 for no color tuning with PWM1
1:0	CT_MODE	00	R/W	00 = Set to CCT Tuning mode (all other 1:0 settings are reserved)

Director Channel_1 Result Registers

These byte registers are used together as DIR_CH_1_H: DIR_CH_1_L

In Color Tuning Operation:
The registers create a 16 bit integer value from 0 to 65535 representing a PWM (Color + Dimming) tuning percentage between 0.00 and 100.00%.

Example: 0001101001001111 = 1A4F= 6735 = 10.28%

In Daylighting Operation (single PWM and no TSL4531):
The registers create a 16 bit integer value from 0 to 65535 representing a PWM Lux tuning percentage between 0.00 and 100.00%.

Figure 29:
Director Channel_1 Result Registers

Addr: 0x50		DIR_CH_1_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_CH_1_L	00000000	R	Channel 1 low byte
Addr: 0x51		**DIR_CH_1_H**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	DIR_CH_1_H	00000000	R	Channel 1 high byte