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AS7261

XYZ Chromatic White Color Sensor + NIR with Electronic Shutter and Smart Interface

General Description

The AS7261is a chromatic white color sensor providing direct XYZ color coordinates consistent with the CIE 1931 2° Standard Observer color coordinates. It also maps the XYZ coordinates to the x, y (Y) of the 2-dimensional color gamut and scales the coordinates to the CIE 1976 u'v' coordinate system.

The device provides accurate Correlated Color Temperature (CCT) measurements and provides color point deviation from the black body curve for white light color in the delta u' v' coordinate system. It also integrates a Near-IR channel for other applications. LED drivers with programmable currents are provided for electronic shutter applications.

The AS7261 integrates Gaussian filters into standard CMOS silicon via Nano-optic deposited interference filter technology and is packaged in an LGA package that provides a built in aperture to control the light entering the sensor array.

Control and spectral data access is implemented through either the I^2C register set, or with a high level AT Spectral Command set via a serial UART.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS7261, XYZ Chromatic White Color Sensor + NIR with Electronic Shutter and Smart Interface are listed below:

Figure 1:
AS7261 Benefits and Features

Benefits	Features
• Calibrated Chromatic white data	• XYZ • xy data (CIE 1931) • DUV, u'v', uv (CIE 1976) • CCT, LUX
• Simple text-based command interface via UART, or direct register read and write with interrupt on sensor ready option on I^2C	• UART or I^2C slave digital Interface
• Lifetime-calibrated sensing with minimal drift over time or temperature	• Filter set realized by silicon interference filters
• No additional signal conditioning required	• 16-bit ADC with digital access

Benefits	Features
• Electronic shutter control/synchronization	• Programmable LED drivers
• Low voltage operation	• 2.7V to 3.6V with I²C interface
• Small, robust package, with built-in aperture	• 20-pin LGA package 4.5mm x 4.7mm x 2.5mm • -40°C to 85°C temperature range

Applications

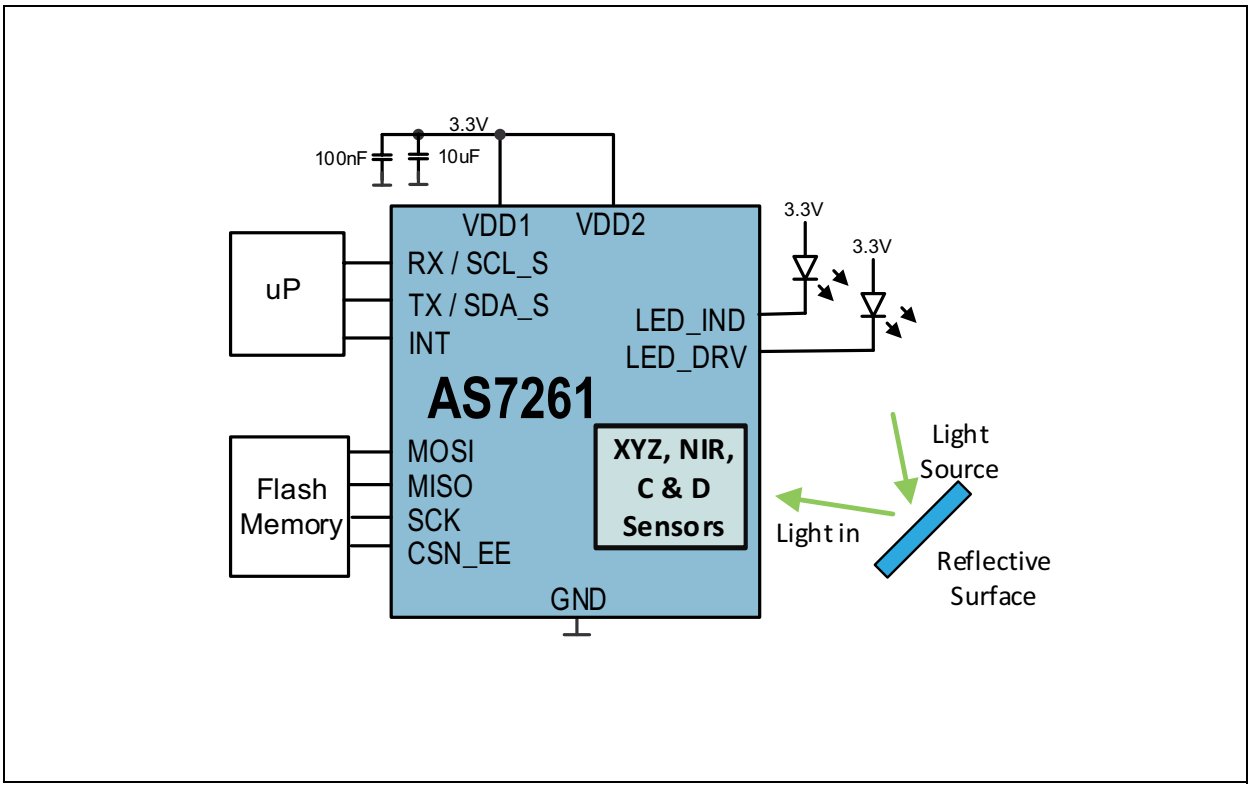
The AS7261 applications include:

- Color measurement and absorbance
- Color matching and identification
- Precision color tuning/calibration

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS7261 Chromatic White Color System



Pin Assignments

The device pin assignments are described below.

Figure 3:
AS7261 Pin Diagram (Top View)

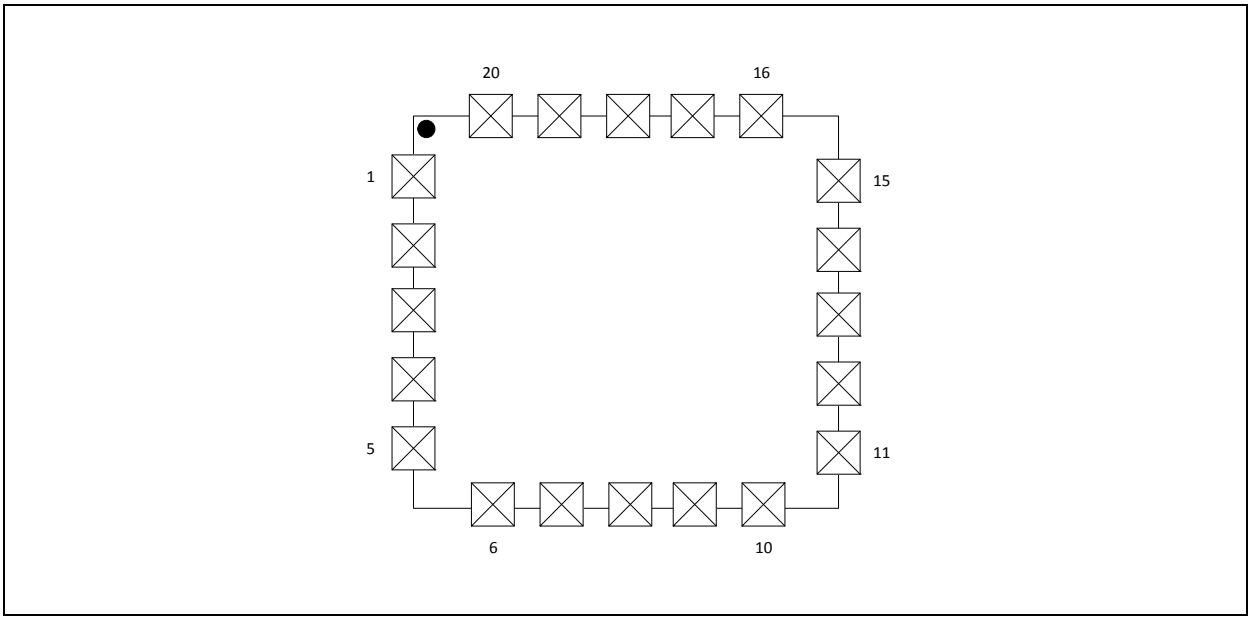


Figure 4:
AS7261 Pin Description

Pin #	Pin Name	Description
1	NC	Not functional. Do not connect
2	RESN	Reset, active LOW
3	SCK	SPI serial clock
4	MOSI	SPI master out slave in
5	MISO	SPI master in slave out
6	CSN_EE	Chip Select for external serial Flash memory, Active LOW
7	CSN_SD	Chip Select for SD Card Interface, Active LOW
8	I2C_ENB	Select UART (Low) or I^2C (High) Operation
9	NF	Not Functional. Do not connect.

Pin #	Pin Name	Description
10	NF	Not Functional. Do not connect.
11	RX/SCL_S	RX (UART) or SCL_S (I^2C Slave) Depending on I2C_ENB
12	TX/SDA_S	TX (UART) or SDA_S (I^2C Slave) Depending on I2C_ENB
13	INT	Interrupt, Active LOW
14	VDD2	Voltage Supply
15	LED_DRV	LED Driver Output for Driving LED, Current Sink
16	GND	Ground
17	VDD1	Voltage Supply
18	LED_IND	LED Driver Output for Indicator LED, Current Sink
19	NF	Not Functional. Do not connect.
20	NF	Not Functional. Do not connect.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD1_MAX}	Supply voltage VDD1	-0.3	5	V	Pin VDD1 to GND
V_{DD2_MAX}	Supply voltage VDD2	-0.3	5	V	Pin VDD2 to GND
V_{DD_IO}	Input/output pin voltage	-0.3	VDD + 0.3	V	Input/output pin to GND
I_scr	Input current (latch-up immunity)	±100		mA	JESD78D
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge HBM	±1000		V	JS-001-2014
ESD_{CDM}	Electrostatic discharge CDM	±500		V	JSD22-C101F
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature range	-40	85	°C	
T_{body}	Package body temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	3			Represents a 168 hours max. floor life time

Electrical Characteristics

All limits are guaranteed with VDD = VDD1 = VDD2 = 3.3V, T_{AMB} = 25°C. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.VDD1 and VDD2 must be sourced from the same power supply.

Figure 6:
AS7261 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General Operating Conditions						
VDD1 /VDD2	Voltage operating supply	UART interface	2.97	3.3	3.6	V
VDD1 /VDD2	Voltage operating supply	I^2C interface	2.7	3.3	3.6	V
T_{AMB}	Operating temperature		-40	25	85	°C
I_{VDD}	Operating current				5	mA
Internal RC Oscillator						
F_{OSC}	Internal RC oscillator frequency		15.7	16	16.3	MHz
t_{JITTER}	Internal clock jitter	@25°C			1.2	ns
Temperature Sensor						
D_{TEMP}	Absolute accuracy of the internal temperature measurement		-8.5		8.5	°C
Indicator LED						
I_{IND}	LED current		1		8	mA
I_{ACC}	Accuracy of current		-30		30	%
V_{LED}	Voltage range of connected LED	Vds of current sink	0.3		VDD	V
LED_DRV						
I_{LED1}	LED current		12.5		100	mA
I_{ACC}	Accuracy of current		-10		10	%
V_{LED}	Voltage range of connected LED	Vds of current sink	0.3		VDD	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital Inputs and Outputs						
$I_{IL\ RESN}$	Logic input current (RESN pin)	Vin=0V	-1		-0.2	mA
V_{IH}	CMOS logic high input		0.7* VDD		VDD	V
V_{IL}	CMOS logic low input		0		0.3* VDD	V
V_{OH}	CMOS logic high output	I=1mA			VDD-0.4	V
V_{OL}	CMOS logic low output	I=1mA			0.4	V
t_{RISE} (1)	Current rise time	C(Pad)=30pF			5	ns
t_{FALL} (1)	Current fall time	C(Pad)=30pF			5	ns

Note(s):

1. Guaranteed, not tested in production.

Timing Characteristics

Figure 7:
AS7261 I²C Slave Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C Interface						
f_{SCLK}	SCL Clock Frequency		0		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HD:STA}$	Hold Time (Repeated) START		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	CB — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

Figure 8:
I²C Slave Timing Diagram

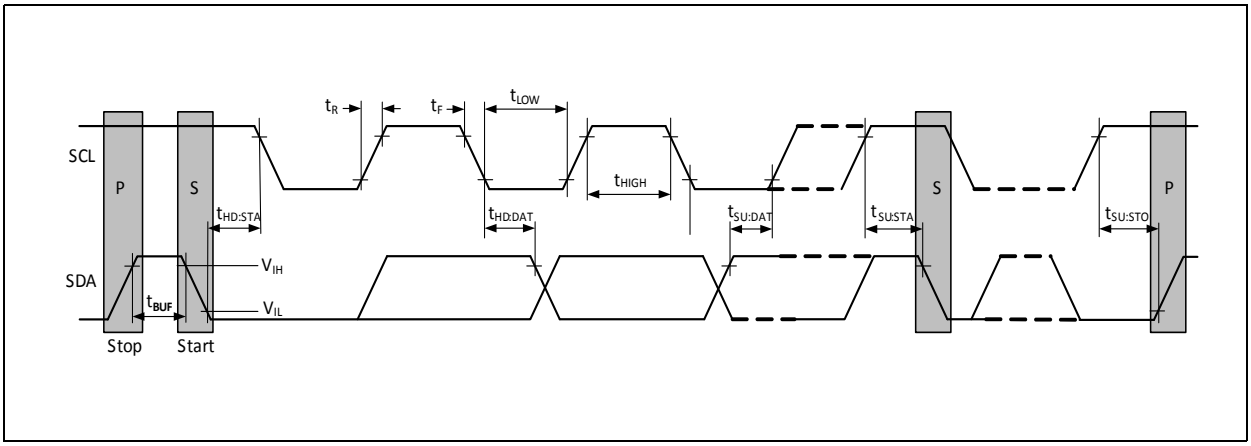


Figure 9:
AS7261SPI Slave Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI Interface						
f_{SCLK}	Clock Frequency		0		16	MHz
t_{SCK_H}	Clock high time		40			ns
t_{SCK_L}	Clock low time		40			ns
t_{SCK_RISE}	SCK rise time		5			ns
t_{SCK_FALL}	SCK fall time		5			ns
t_{CSN_S}	CSN setup time	Time between CSN high-low transition to first SCK high transition	50			ns
t_{CSN_H}	CSN hold time	Time between last SCK falling edge and CSN low-high transition	100			ns
t_{CSN_DIS}	CSN disable time		100			ns
t_{DO_S}	Data-out setup time		5			ns
t_{DO_H}	Data-out hold time		5			ns
t_{DI_V}	Data-in valid		10			ns

Figure 10:
SPI Master Write Timing Diagram

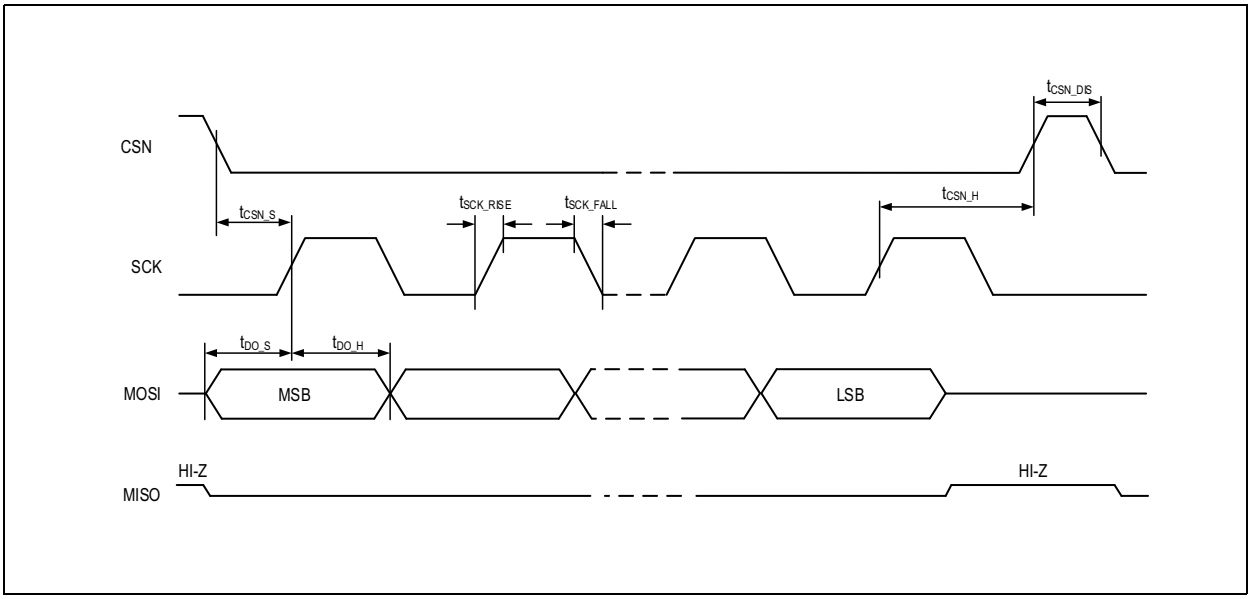
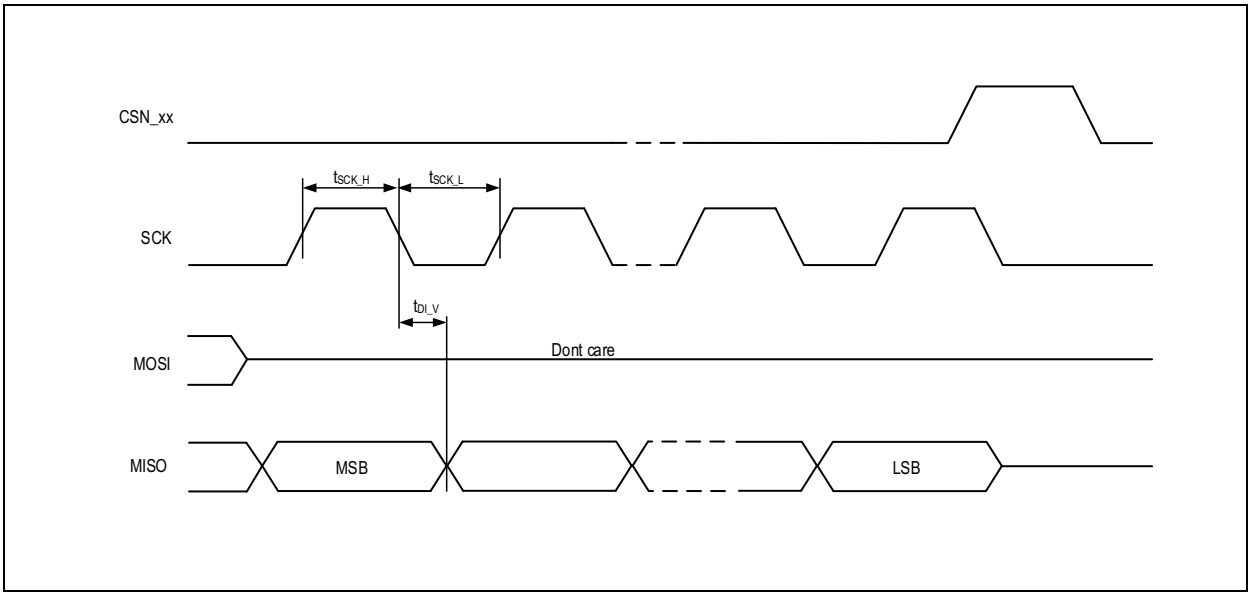


Figure 11:
SPI Master Read Timing Diagram



Typical Optical Characteristics

Figure 12:
Spectral Responsivity

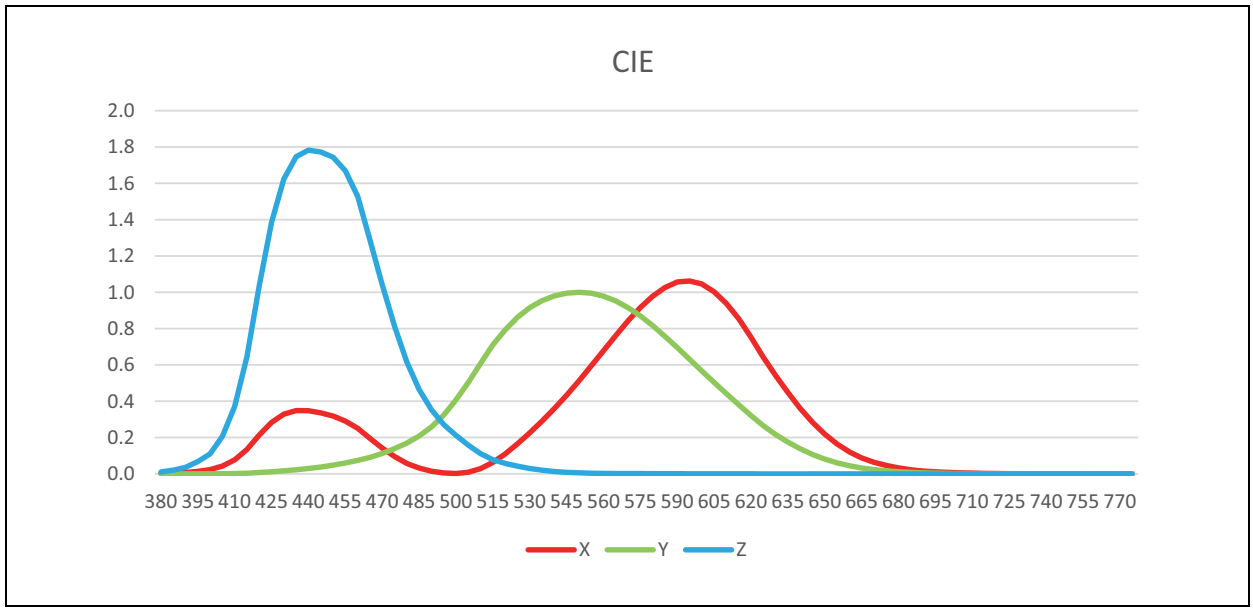


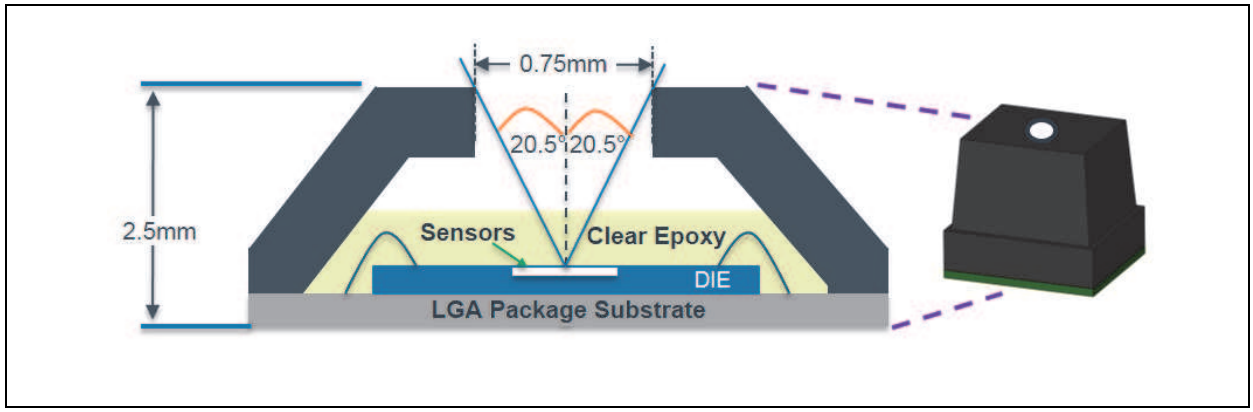
Figure 13:
AS7261 Optical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
Color_m(2)	Color measurement accuracy	White Light CCT = 2700K, 3500K, 4500K and 5700K		0.002		du'v'
Z_count	Z channel count accuracy	White Light CCT = 5700K	3.375	4.5	5.625	counts/ ($\mu W/cm^2$)

Note(s):

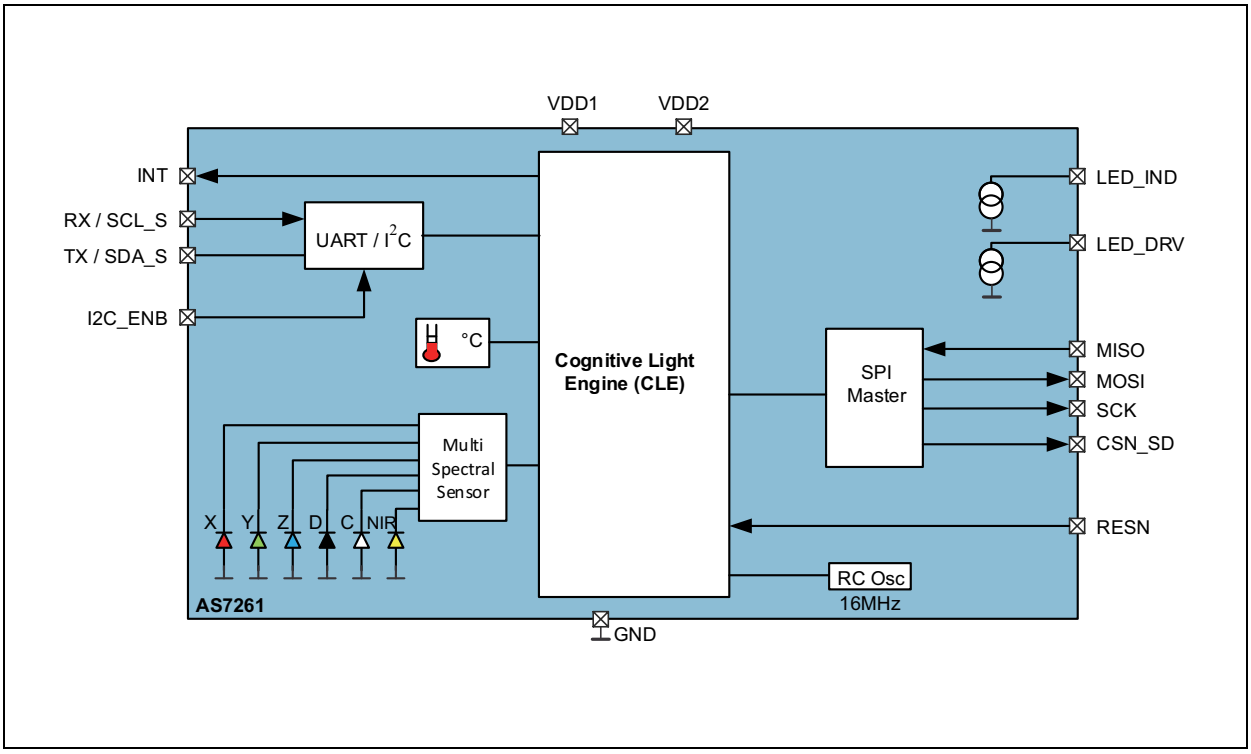
1. Typical values at Lux ≥50, Integration time=400.4ms, Gain=1x, T_{AMB} = 25°C.
2. Calibration and measurements are made using diffused light.

Figure 14:
AS7261 LGA Package Field of View



Detailed Descriptions

Figure 15:
Internal Block Diagram



XYZ Chromatic White Color Sensor

The XYZ Chromatic White Color sensor is a next-generation digital color sensor device. Each channel is a designed to meet the X, Y, Z standard observer filter characteristics compliant with the CIE 1931 standard or an NIR spectrum.

The sensor contains analog-to-digital converters (16-bit resolution ADC), which integrate the current from each channel's photodiode. Upon completion of the conversion cycle, the integrated result is transferred to the corresponding data registers. The transfers are double-buffered to ensure that the integrity of the data is maintained.

Standard observer interference filters realize the XYZ response, which enables minimal life-time drift and very high temperature stability. Filter accuracy will be affected by the angle of incidence which itself is limited by an integrated aperture and an internal micro-lens structure. The aperture-limited field of view is ±20.5° to deliver specified accuracy.

Data Conversion Description

AS7261 Spectral Conversion is implemented via two photodiode banks. The First Bank, Bank1 consists of data from the X, Y, Z and NIR (near-IR) photodiodes. Bank2 provides data from the same X and Y photodiodes as well as the D (dark) and C (Clear) photodiodes. Spectral conversion requires the integration time (IT in ms) set to complete. If both photodiode banks are required to complete the conversion, the 2nd bank requires an additional IT ms. Minimum IT for a single bank conversion is 2.8 ms. If data is required from all 6 photodiodes then the device must perform 2 full conversions (2 x Integration Time).

The spectral conversion process is controlled with four BANK Mode settings as follows:

BANK Mode 0:
Conversions will occur continuously and data will be available in I^2C registers X, Y, Z, and NIR or via the ATDATA command when using the UART device interface.

BANK Mode 1:
Conversions will occur continuously and data will be available in I^2C registers X, Y, D, and C or via the ATDATA command.

BANK Mode 2:
Conversions occur continuously and data will be available in registers X, Y, Z, NIR, D and C or via the ATDATA command after two integration periods. In this Mode 2 the calibrated, corrected values may also be obtained from the appropriate I^2C registers or using the ATXYZC command.

When the bank setting is Mode 0, Mode 1, or Mode 2, the spectral data conversion process operates continuously, with new data available after each IT ms period. In the continuous modes, care should be taken to assure prompt interrupt servicing so that integration values from both banks are all derived from the same spectral conversion cycle.

BANK Mode 3:
Data will be available in registers X, Y, Z, NIR, D and C in One-Shot mode. And in this Mode 3 the calibrated, corrected values may also be obtained from the appropriate I^2C registers or using the ATXYZC command.

When the bank setting is set to Mode 3 the device initiates One-Shot operation. The DATA_RDY bit is set to 1 once data is available, indicating spectral conversion is complete. One-Shot mode is intended for use when it is critical to ensure spectral conversion results are obtained contemporaneously.

Figure 16:
Photo Diode Array

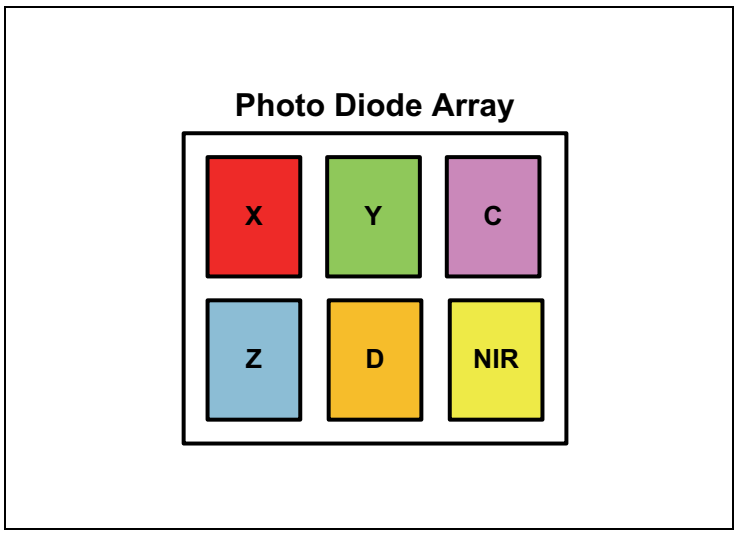
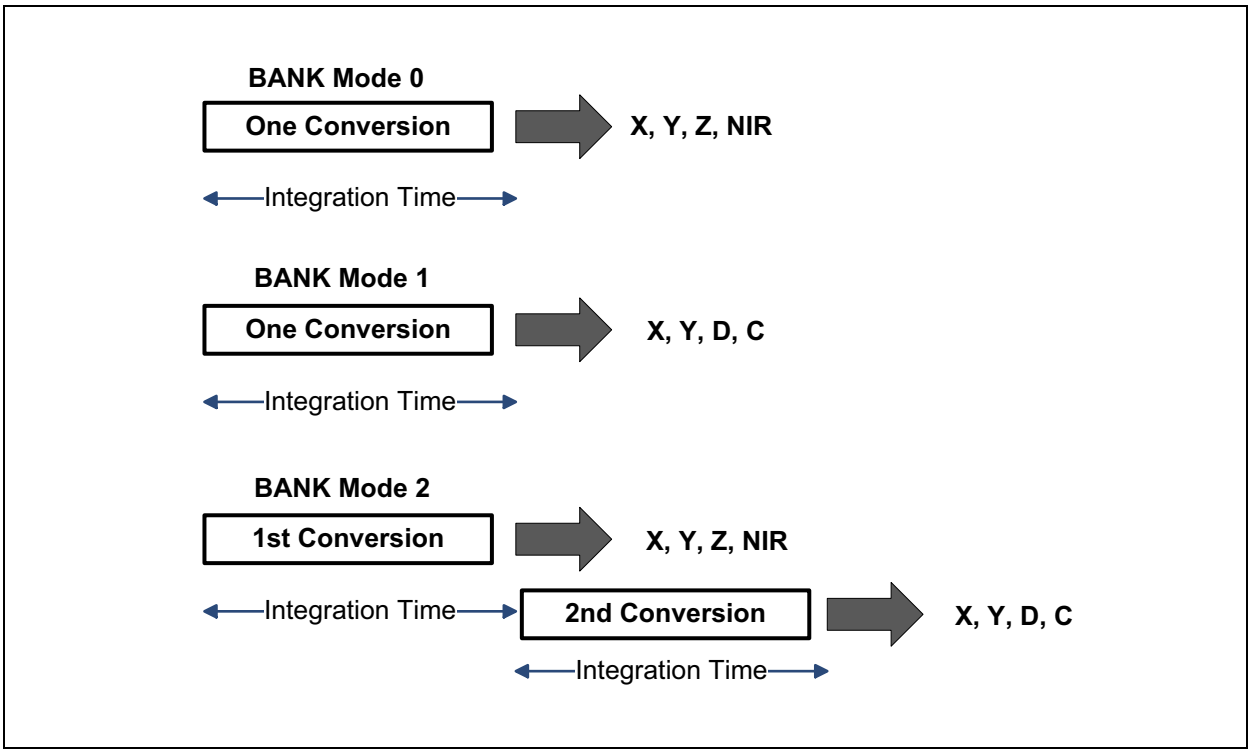


Figure 17:
Bank Mode and Data Conversion



RC Oscillator

The timing generation circuit consists of an on-chip 16MHz, temperature compensated oscillator which provides the master clock for the AS7261.

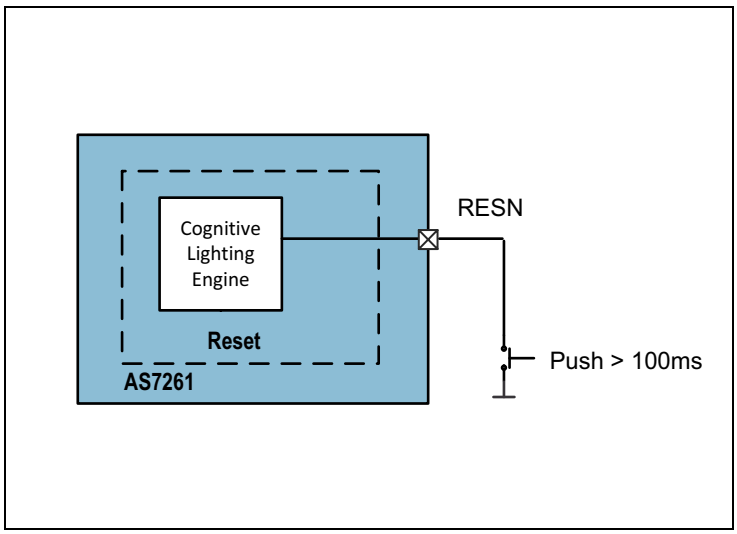
Temperature Sensor

The internal temperature sensor is constantly measuring the on-chip temperature and enables temperature compensation procedures. It can be read via I^2C or AT Command.

Reset

Pulling down the RESN pin for longer than 100ms resets the AS7261.

Figure 18:
Reset Circuit



Indicator LED for Flash Memory Programming Progress

The LED, connected to pin LED_IND, can be used to indicate Flash memory programming progress of the device. While programming the AS7261 via the external SD card the indicator LED automatically starts flashing. When programming is completed the indicator LED is automatically switched off. The Flash Memory Programming is initiated by the user as needed, but once started the LED flashing is not under user control.

Electronic Shutter with LED_IND or LED_DRV Driver Control

Under user control there are two LED driver outputs that can be used to control LEDs on each driver pin. This allows different wavelength light sources to be used in the same system. The LED output sink currents are programmable and can drive external LED sources: LED_IND for 1mA, 2mA, 4mA or 8mA and LED_DRV for 12.5mA, 25mA, 50mA or 100mA. After programming for current the sources can be turned off and on via I^2C registers or AT commands to provide the AS7261 with an electronic shutter capability.

Interrupt Operation

If BANK is set to Mode 0 or Mode 1 then the data is ready after the 1st integration time. If BANK is set to Mode 2 or Mode 3 then the data is ready after two integration times. If the interrupt is enabled (INT = 1) then when the data is ready, the INT line is pulled low and DATA_RDY is set to 1. The INT line is released (returns high) when the control register is read.

DATA_RDY is cleared to 0 when any of the sensor registers X, Y, Z, NIR, D and C are read. For multi-byte sensor data (2 or 4 bytes), after the 1st byte is read the remaining bytes are shadow protected in case an integration cycle completes just after the 1st byte is read.

In continuous spectral conversion mode (BANK setting of Mode 0, 1, or 2), the sensors continue to gather information at the rate of the integration time, hence if the sensor registers are not read when the interrupt line goes low, it will stay low and the next cycle's sensor data will be available in the registers at the end of the next integration cycle.

When the control register BANK bits are written with a value of Mode 3, One-Shot Spectral Conversion mode is entered. When a single set of contemporaneous sensor readings is desired, writing BANK Mode 3 to the control register immediately triggers exactly two spectral data conversion cycles. At the end of these two conversion cycles, the DATA_RDY bit is set as for the other BANK modes. To perform a new One-Shot sequence, the control register BANK bits should be written with a value of Mode 3 again. This process may continue until the user writes a different value into the BANK bits.

I^2C Slave Interface

If selected by the I2C_ENB pin setting, interface and control can be accomplished through an I^2C compatible slave interface to a set of registers that provide access to device control functions and output data. These registers on the AS7261 are, in reality, implemented as virtual registers in software. The actual I^2C slave hardware registers number only three and are described in the table below. The steps necessary to access the virtual registers defined in the following are explained in pseudocode for external I^2C master writes and reads below.

I²C Feature List

- Fast mode (400kHz) and standard mode (100kHz) support
- 7+1-bit addressing mode
- Write format: Byte
- Read format: Byte

Figure 19:
I²C Slave Device Address and Physical Registers

Entity	Description	Note
Device Slave Address	8-bit Slave Address	Byte = 1001001x (device address = 49 hex) x= 1 for Master Read (byte = 93 hex) x= 0 for Master Write (byte = 92 hex)
STATUS Register	I²C slave interface STATUS register Read-only	Register Address = 0x00 Bit 1: TX_VALID 0 → New data may be written to WRITE register 1 → WRITE register occupied. Do NOT write. Bit 0: RX_VALID 0 → No data is ready to be read in READ register. 1 → Data byte available in READ register.
WRITE Register	I²C slave interface WRITE register Write-only	Register Address = 0x01 8-Bits of data written by the I²C Master intended for receipt by the I²C slave. Used for both virtual register addresses and write data.
READ Register	I²C slave interface READ register Read-only	Register Address = 0x02 8-Bits of data to be read by the I²C Master.

I²C Virtual Register Write Access

I²C Virtual Resister Byte Write, detailed below, shows the pseudocode necessary to write virtual registers on the AS7261. Note that, because the actual registers of interest are realized as virtual registers, a means of indicating whether there is a pending read or write operation of a given virtual register is needed. To convey this information, the most significant bit of the virtual register address is used as a marker. If it is 1, then a write is pending, otherwise the slave is expecting a virtual read operation. The pseudocode illustrates the proper technique for polling of the I²C slave status register to ensure the slave is ready for each transaction.

I²C Virtual Register Byte Write

Pseudocode

Poll I²C slave STATUS register;
If TX_VALID bit is 0, a write can be performed on the interface;
Send a virtual register address and set the MSB of the register address to 1 to indicate the pending write;
Poll I²C slave STATUS register;
If TX_VALID bit is 0, the virtual register address for the write has been received and the data may now be written;
Write the data.

Sample Code:

```
#define I2C_AS72XX_SLAVE_STATUS_REG     0x00
#define I2C_AS72XX_SLAVE_WRITE_REG      0x01
#define I2C_AS72XX_SLAVE_READ_REG       0x02
#define I2C_AS72XX_SLAVE_TX_VALID       0x02
#define I2C_AS72XX_SLAVE_RX_VALID       0x01

void i2cm_AS72xx_write(uint8_t virtualReg, uint8_t d)
{
volatile uint8_t status;

while (1)
{
      // Read slave I²C status to see if the write buffer is ready.
      status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG);

      if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
      // No inbound TX pending at slave. Okay to write now.
      break,
}
// Send the virtual register address (setting bit 7 to indicate a pending write).
i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, (virtualReg | 0x80)) ;
while (1)
{
      // Read the slave I²C status to see if the write buffer is ready.
      status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;
      if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
            // No inbound TX pending at slave. Okay to write data now.
      break;
}
//Send the data to complete the operation.
i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, d) ;
}
```

I²C Virtual Register Read Access

I²C Virtual Register Byte Read, detailed below, shows the pseudocode necessary to read virtual registers on the AS7261. Note that in this case, reading a virtual register, the register address is not modified.

I²C Virtual Register Byte Read

Pseudocode

Poll I²C slave STATUS register;
If TX_VALID bit is 0, the virtual register address for the read may be written;
Send a virtual register address;
Poll I²C slave STATUS register;
If RX_VALID bit is 1, the read data is ready;
Read the data.

Sample Code:

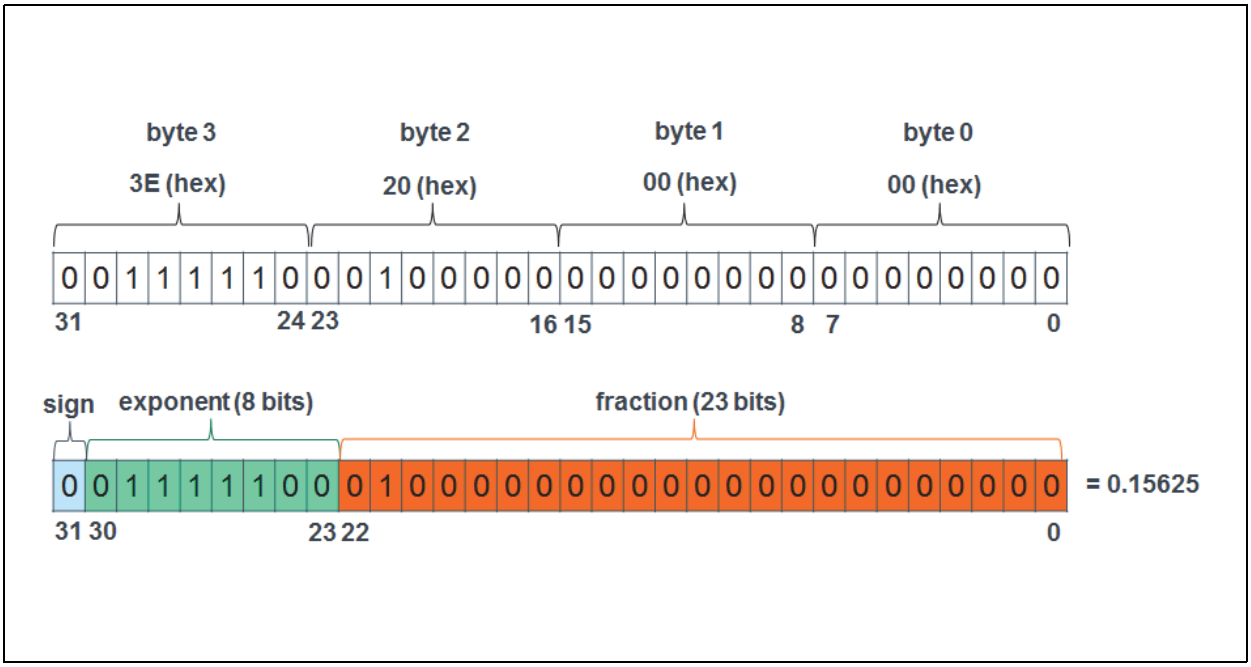
```
uint8_t i2cm_AS72xx_read(uint8_t virtualReg)
{
    volatile uint8_t status, d ;
    while (1)
    {
            // Read slave I2C status to see if the read buffer is ready.
            status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG);

            if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                // No inbound TX pending at slave. Okay to write now.
                break;
    }
    // Send the virtual register address (setting bit 7 to indicate a pending write).
    i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, virtualReg);
    while (1)
    {
            // Read the slave I2C status to see if our read data is available.
            status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

            if ((status & I2C_AS72XX_SLAVE_RX_VALID) != 0)
                // Read data is ready.
                break ;
    }
    // Read the data to complete the operation.
    d = i2cm_read(I2C_AS72XX_SLAVE_READ_REG) ;
    return d ;s
}
```

The details of the *i2cm_read()* and *i2cm_write()* functions in previous Figures are dependent upon the nature and implementation of the external I²C master device.

4-Btye Floating-Point (FP) Registers

Several 4 byte registers (hex) are used by the AS7261. Here is an example of how these registers are used to represent floating point data (based on the IEEE 754 standard):

Figure 20:
Example of the IEEE 754 Standard



The floating point (FP) value assumed by 32 bit **binary32 data** with a biased exponent **e** (the 8 bit unsigned integer) and a **23 bit fraction** is (for the above example):

(EQ1) $$FPvalue = (-1)^{sign}\left(1 + \sum_{i=1}^{23} b_{23-i}2^{-i}\right) \times 2^{(e-127)}$$

(EQ2) $$FPvalue = (-1)^{0}\left(1 + \sum_{i=1}^{23} b_{23-i}2^{-i}\right) \times 2^{(124-127)}$$

(EQ3) $$FPvalue = 1 \times (1 + 2^{-2}) \times 2^{(-3)} = 0.15625$$

I²C Virtual Register Set

The figure below provides a summary of the AS7261 I²C register set. Figures after that provide additional register details. All register data is hex, and all multi-byte entities are Big Endian (most significant byte is situated at the lowest register address).

Multiple byte registers (2 byte integer, or, 4 byte floating point) must be read in the order of ascending register addresses (low to high). And if capable of being written to, must also be written in the order ascending register addresses.

Figure 21:
I²C Virtual Register Set Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Version Registers									
0x00:0x01	HW_Version	Hardware Version							
0x02:0x03	FW_Version	Firmware Version							
Control Registers									
0x04	Control_Setup	RST	INT	GAIN		Bank		DATA_RDY	RSVD
0x05	INT_T	Integration Time							
0x06	Device_Temp	Device Temperature							
0x07	LED_Control	RSVD		ICL_DRV		LED_DRV	ICL_IND		LED_IND
Sensor Raw Data Registers									
0x08	X_High	Channel X High Data Byte							
0x09	X_Low	Channel X Low Data Byte							
0x0A	Y_High	Channel Y High Data Byte							
0x0B	Y_Low	Channel Y Low Data Byte							
0x0C	Z_High	Channel Z High Data Byte							
0x0D	Z_Low	Channel Z Low Data Byte							
0x0E	NIR_High	Channel NIR High Data Byte							
0x0F	NIR_Low	Channel NIR Low Data Byte							
0x10	Dark_High	Channel Dark High Data Byte							
0x11	Dark_Low	Channel Dark Low Data Byte							
0x12	Clear_High	Channel Clear High Data Byte							
0x13	Clear_Low	Channel Clear Low Data Byte							

Sensor Calibrated Data Registers		
0x14:0x17	Cal_X	Cal-X data (4-byte floating-point)
0x18:0x1B	Cal_Y	Cal-Y data (4-byte floating-point)
0x1C:0x1F	Cal_Z	Cal-Z data (4-byte floating-point)
0x20:0x23	Cal_x_1931	Cal-x (CIE 1931) (4-byte floating-point)
0x24:0x27	Cal_y_1931	Cal-y (CIE 1931) (4-byte floating-point)
0x28:0x2B	Cal_upri	Cal_u' (CIE 1976) (4-byte floating-point)
0x2C:0x2F	Cal_vpri	Cal_v' (CIE 1976) (4-byte floating-point)
0x30:0x33	Cal_u	Cal_u (CIE 1976) (4-byte floating-point)
0x34:0x37	Cal_v	Cal_y (CIE 1976) (4-byte floating-point)
0x38:0x3B	Cal_DUV	Cal_DUV (CIE 1976) (4-byte floating-point)
0x3C:0x3F	Cal_LUX	Calibrated LUX (4-byte)
0x40:0x4F	Cal_CCT	Calibrated CCT (4-byte)

Detailed Register Description

Figure 22:
HW Version Registers

Addr: 0x00		HW_Version		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device Type	01000000	R	Device type number
Addr: 0x01		**HW_Version**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	HW Version	00111101	R	Hardware version

Figure 23:
FW Version Registers

Addr: 0x02		FW_Version		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Minor version		R	Minor version [1:0]
5:0	Sub version		R	Sub version
Addr: 0x03		**FW_Version**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Major version		R	Major version
3:0	Minor version		R	Minor version [5:2]

Figure 24:
Control Setup Register

Addr: 0x04/0x84		Control_Setup		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	RST	0	R/W	Soft Reset, Set to 1 for soft reset, goes to 0 automatically after the reset
6	INT	0	R/W	Enable interrupt pin output (INT), 1: Enable, 0: Disable
5:4	GAIN	10	R/W	Sensor Channel Gain Setting (all channels) 'b00=1x; 'b01=3.7x; 'b10=16x; 'b11=64x;
3:2	BANK	10	R/W	Data Conversion Type (continuous) 'b00=Mode 0: X, Y, Z and NIR 'b01=Mode 1: X, Y, D and C 'b10=Mode 2: X, Y, Z, NIR, D and C 'b11=Mode 3: One-Shot operation
1	DATA_RDY	0	R/W	1: Data Ready to Read, sets INT active if interrupt is enabled. Can be polled if not using INT.
0	RSVD	0	R	Reserved; Unused

Figure 25:
Integration Time Register

Addr: 0x05/0x85		INT_T		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	INT_T	0xFF	R/W	Integration time = <value> * 2.8ms

Figure 26:
Device Temperature Register

Addr: 0x06		Device_Temp		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device_Temp	0xFF	R/W	Internal device temperature data byte (°C)

Figure 27:
LED Control Register

Addr: 0x07/0x87		LED Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	RSVD	0	R	Reserved
5:4	ICL_DRV	00	R/W	LED_DRV current limit 'b00=12.5mA; 'b01=25mA; 'b10=50mA; 'b11=100mA;
3	LED_DRV	0	R/W	Enable LED_DRV 1: Enabled; 0: Disabled
2:1	ICL_IND	00	R/W	LED_IND current limit 'b00=1mA; 'b01=2mA; 'b10=4mA; 'b11=8mA;
0	LED_IND	0	R/W	Enable LED_IND 1: Enabled; 0: Disabled

Figure 28:
Sensor Raw Data Registers

Addr: 0x08		X_High		
Bit	Bit Name	Default	Access	Bit Description
7:0	X_High		R	Channel X High Data Byte
Addr: 0x09		**X_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	X_Low		R	Channel X Low Data Byte
Addr: 0x0A		**Y_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	Y_High		R	Channel Y High Data Byte
Addr: 0x0B		**Y_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	Y_Low		R	Channel Y Low Data Byte
Addr: 0x0C		**Z_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	Z_High		R	Channel Z High Data Byte
Addr: 0x0D		**Z_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	Z_Low		R	Channel Z Low Data Byte
Addr: 0x0E		**NIR_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	NIR_High		R	Channel NIR High Data Byte
Addr: 0x0F		**NIR_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	NIR_Low		R	Channel NIR Low Data Byte
Addr: 0x10		**Dark_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	Dark_High		R	Channel Dark High Data Byte