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AS7263

6-Channel NIR *Spectral_ID* Device with Electronic Shutter and Smart Interface

General Description

The AS7263 is a digital 6-channel spectrometer for spectral identification in the near IR (NIR) light wavelengths. AS7263 consists of 6 independent optical filters whose spectral response is defined in the NIR wavelengths from approximately 600nm to 870nm with full-width half-max (FWHM) of 20nm. An integrated LED driver with programmable current is provided for electronic shutter applications.

The AS7263 integrates Gaussian filters into standard CMOS silicon via Nano-optic deposited interference filter technology and is packaged an LGA package that provides a built in aperture to control the light entering the sensor array.

Control and Spectral data access is implemented through either the I^2C register set, or with a high level AT Spectral Command set via a serial UART.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS7263, 6-Channel NIR *Spectral_ID* Device with Electronic Shutter and Smart Interface are listed below:

Figure 1:
Added Value of Using AS7263

Benefits	Features
• Compact 6-channel spectrometry solution	• 6 near-IR channels: 610nm, 680nm, 730nm, 760nm, 810nm and 860nm, each with 20nm FWHM
• Simple text-based command interface via UART, or direct register read and write with interrupt on sensor ready option on I^2C	• UART or I^2C slave digital Interface
• Lifetime-calibrated sensing with no drift over time or temperature	• NIR filter set realized by silicon interference filters
• No additional signal conditioning required	• 16-bit ADC with digital access
• Electronic shutter control/synchronization	• Programmable LED drivers
• Low voltage operation	• 2.7V to 3.6V with I^2C interface
• Small, robust package, with built-in aperture	• 20-pin LGA package 4.5mm x 4.7mm x 2.5mm, -40°C to 85°C temperature range

Applications

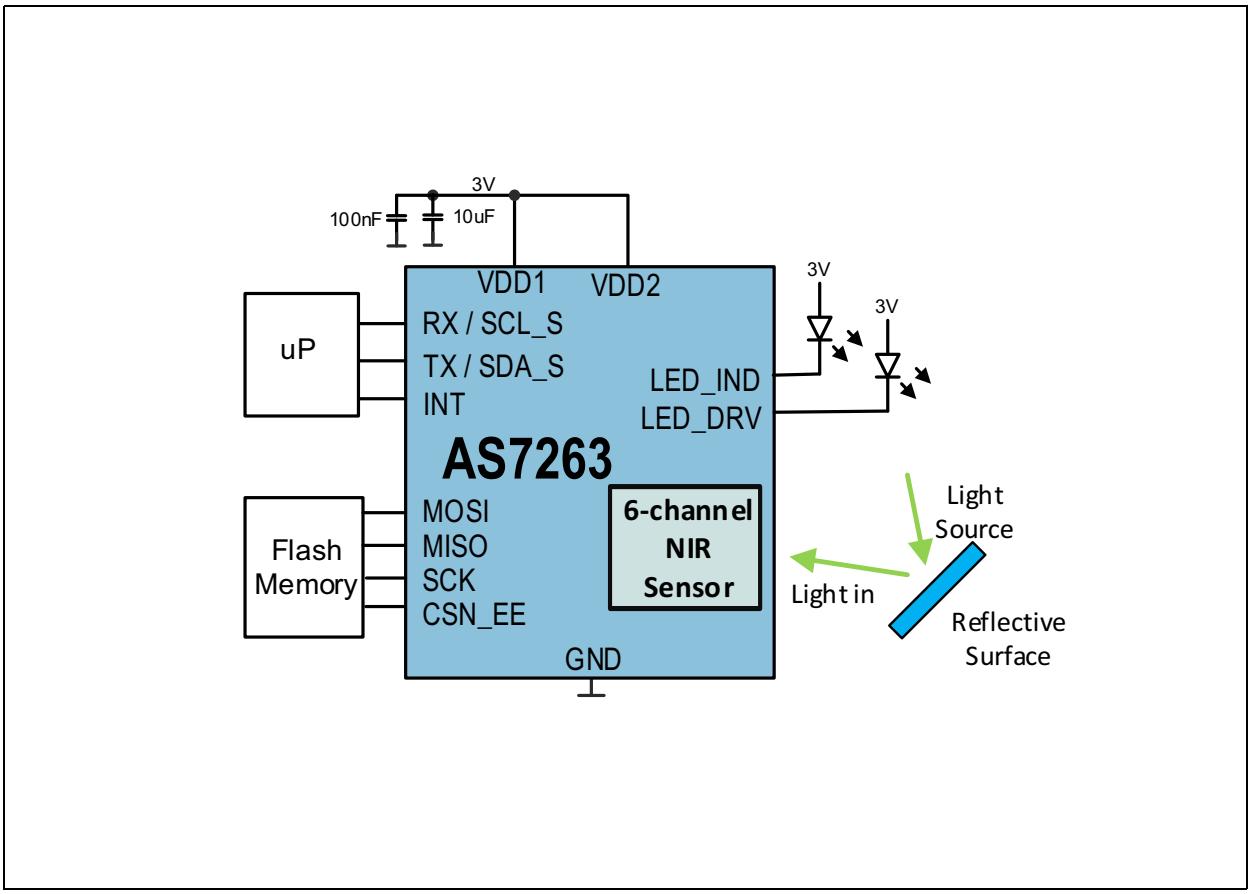
The AS7263 applications include:

- Product authentication
- Bank note/document validation
- Chemical analysis
- Food/beverage safety

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS7263 NIR *Spectral_ID* System



Pin Assignment

The device pin assignments are described below.

Figure 3:
Pin Diagram (Top View)

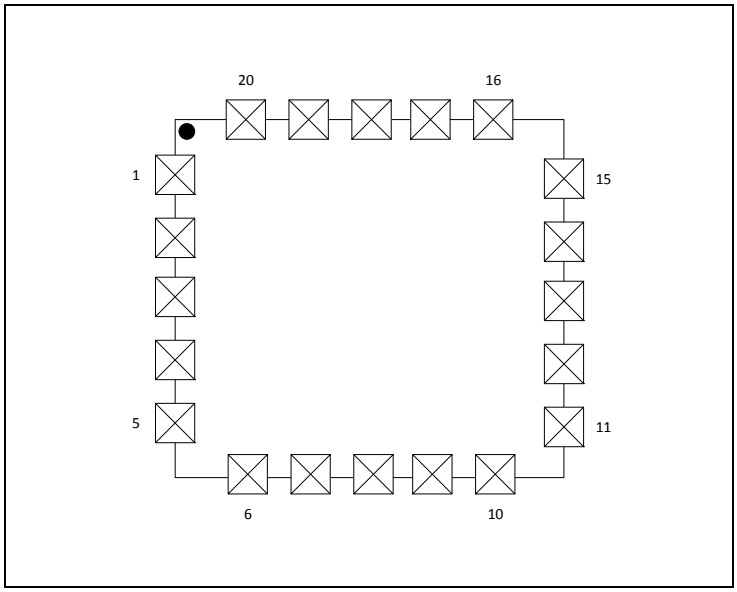


Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	NF	Not Functional. Do not connect.
2	RESN	Reset, Active LOW
3	SCK	SPI Serial Clock
4	MOSI	SPI Master Out Slave In
5	MISO	SPI Master In Slave Out
6	CSN_EE	Chip Select for External Serial Flash Memory, Active LOW
7	CSN_SD	Chip Select for SD Card Interface, Active LOW
8	I2C_ENB	Select UART (Low) or I^2C (High) Operation
9	NF	Not Functional. Do not connect.
10	NF	Not Functional. Do not connect.
11	RX/SCL_S	RX (UART) or SCL_S (I^2C Slave) Depending on I^2C_ENB
12	TX/SDA_S	TX (UART) or SDA_S (I^2C Slave) Depending on I^2C_ENB
13	INT	Interrupt, Active LOW
14	VDD2	Voltage Supply

Pin Number	Pin Name	Description
15	LED_DRV	LED Driver Output for Driving LED, Current Sink
16	GND	Ground
17	VDD1	Voltage Supply
18	LED_IND	LED Driver Output for Indicator LED, Current Sink
19	NF	Not Functional. Do not connect.
20	NF	Not Functional. Do not connect.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device is not designed for high energy UV (ultraviolet) environments, including upward looking outdoor applications, which could affect long term optical performance.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD1_MAX}	Supply Voltage VDD1	-0.3	5	V	Pin VDD1 to GND
V_{DD2_MAX}	Supply Voltage VDD2	-0.3	5	V	Pin VDD2 to GND
V_{DD_IO}	Input/Output Pin Voltage	-0.3	VDD+0.3	V	Input/Output Pin to GND
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JESD78D
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 1000		V	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM	± 500		V	JSD22-C101F
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices."
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Maximum floor life time of 168 hours

Electrical Characteristics

All limits are guaranteed with VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics of AS7263

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General Operating Conditions						
VDD1 /VDD2	Voltage Operating Supply	UART Interface	2.97	3.3	3.6	V
VDD1 /VDD2	Voltage Operating Supply	I^2C Interface	2.7	3.3	3.6	V
T_{AMB}	Operating Temperature		-40	25	85	°C
I_{VDD}	Operating Current				5	mA
$I_{STANDBY}$ (1)	Standby Current			12		µA
Internal RC Oscillator						
F_{OSC}	Internal RC Oscillator Frequency		15.7	16	16.3	MHz
t_{JITTER} (2)	Internal Clock Jitter	@25°C			1.2	ns
Temperature Sensor						
D_{TEMP}	Absolute Accuracy of the Temperature Measurement		-8.5		8.5	°C
Indicator LED						
I_{IND}	LED Current		1	4	8	mA
I_{ACC}	Accuracy of Current		-30		30	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V
LED_DRV						
I_{LED1}	LED Current	12.5, 25, 50 or 100	12.5		100	mA
I_{ACC}	Accuracy of Current		-10		10	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital Inputs and Outputs						
I_{IH}, I_{IL}	Logic Input Current	Vin=0V or VDD	-1		1	µA
I_{ILRESN}	Logic Input Current (RESN pin)	Vin=0V	-1		-0.2	mA
V_{IH}	CMOS Logic High Input		0.7* VDD		VDD	V
V_{IL}	CMOS Logic Low Input		0		0.3* VDD	V
V_{OH}	CMOS Logic High Output	I=1mA			VDD - 0.4	V
V_{OL}	CMOS Logic Low Output	I=1mA			0.4	V
t_{RISE} (2)	Current Rise Time	C(Pad)=30pF			5	ns
t_{FALL} (2)	Current Fall Time	C(Pad)=30pF			5	ns

Note(s):

1. 15µA over temperature
2. Guaranteed, not tested in production

Timing Characteristics

Figure 7:
AS7263 I²C Slave Timing Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I²C Interface						
f_{SCLK}	SCL Clock Frequency		0		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HS:STA}$	Hold Time (Repeated) START		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HS:DAT}$	Data Hold Time		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	CB — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

Figure 8:
I²C Slave Timing Diagram

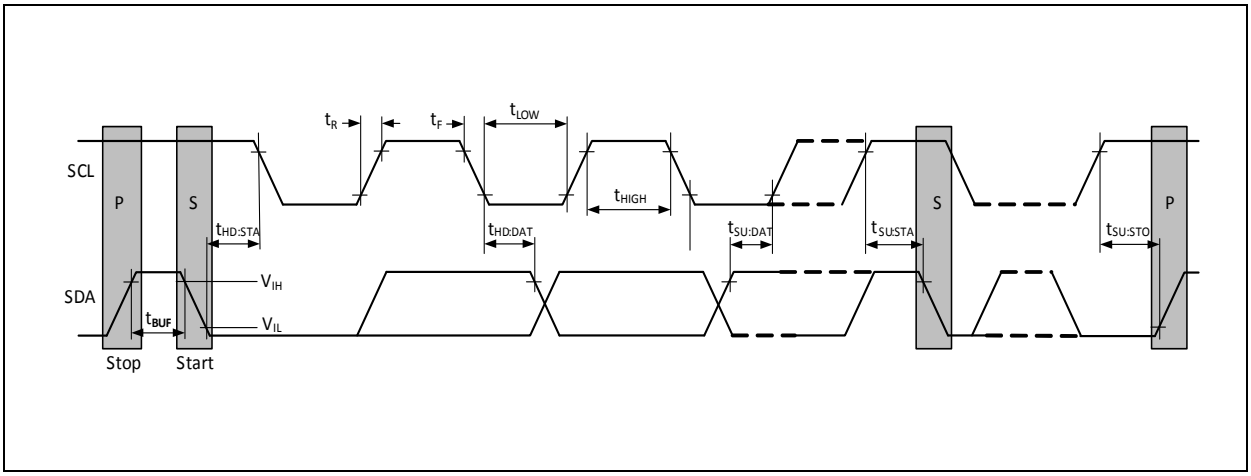


Figure 9:
AS7263 SPI Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI Interface						
f_{SCK}	Clock Frequency		0		16	MHz
t_{SCK_H}	Clock High Time		40			ns
t_{SCK_L}	Clock Low Time		40			ns
t_{SCK_RISE}	SCK Rise Time		5			ns
t_{SCK_FALL}	SCK Fall Time		5			ns
t_{CSN_S}	CSN Setup Time	Time between CSN high-low transition to first SCK high transition	50			ns
t_{CSN_H}	CSN Hold Time	Time between last SCK falling edge and CSN low-high transition	100			ns
t_{CSN_DIS}	CSN Disable Time		100			ns
t_{DO_S}	Data-Out Setup Time		5			ns
t_{DO_H}	Data-Out Hold Time		5			ns
t_{DI_V}	Data-In Valid		10			ns

Note(s):

1. Guaranteed, not tested in production

Figure 10:
SPI Master Write Timing Diagram

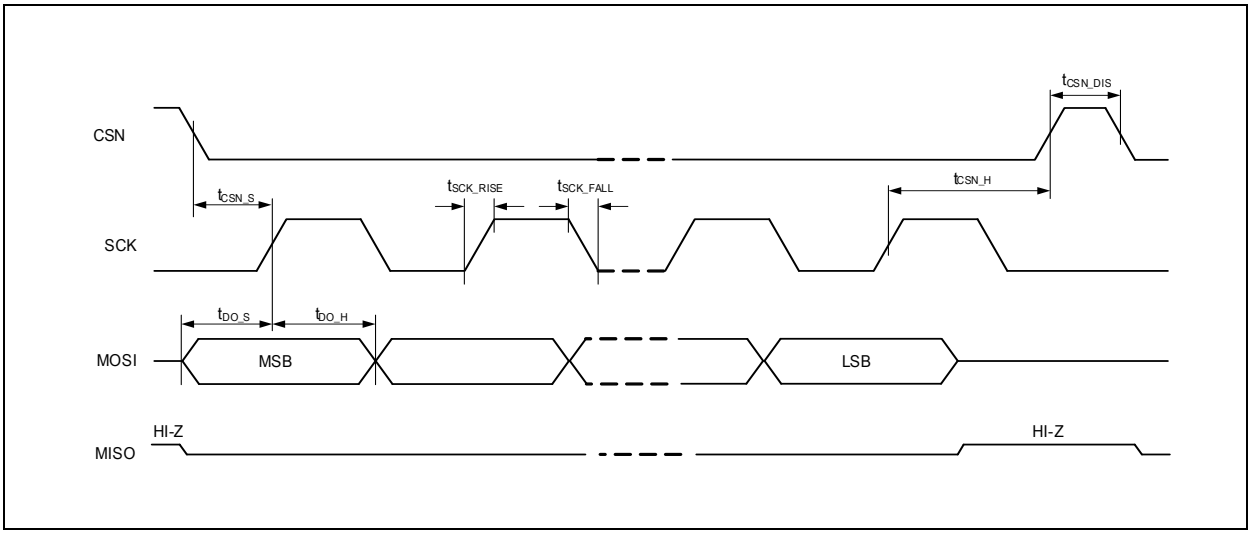
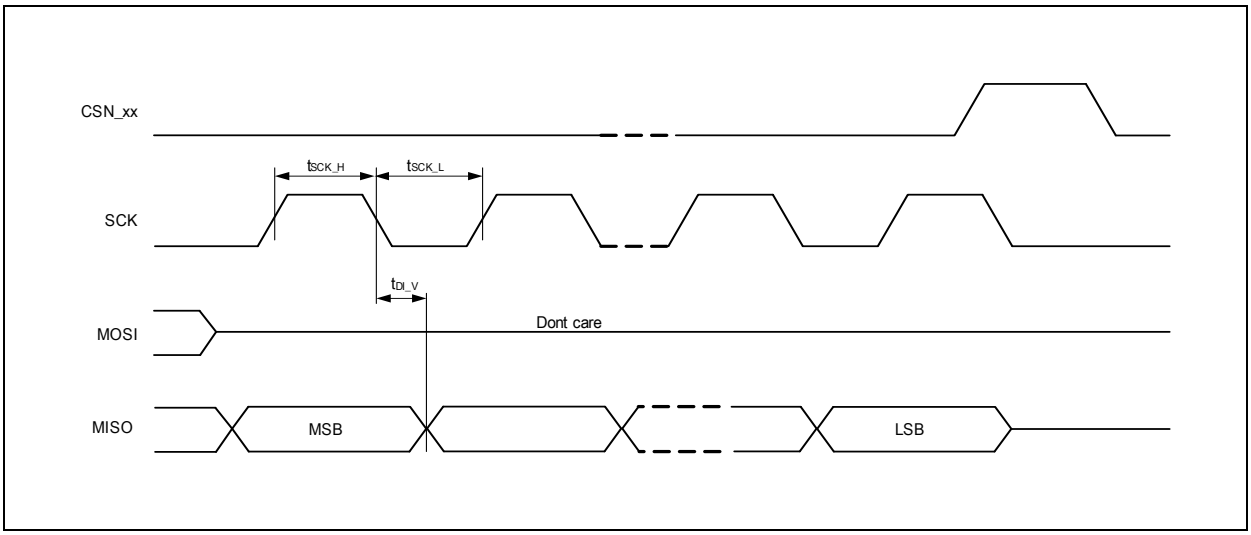


Figure 11:
SPI Master Read Timing Diagram



Optical Characteristics

Figure 12:
Optical Characteristics of AS7263 (Pass Band)(1)

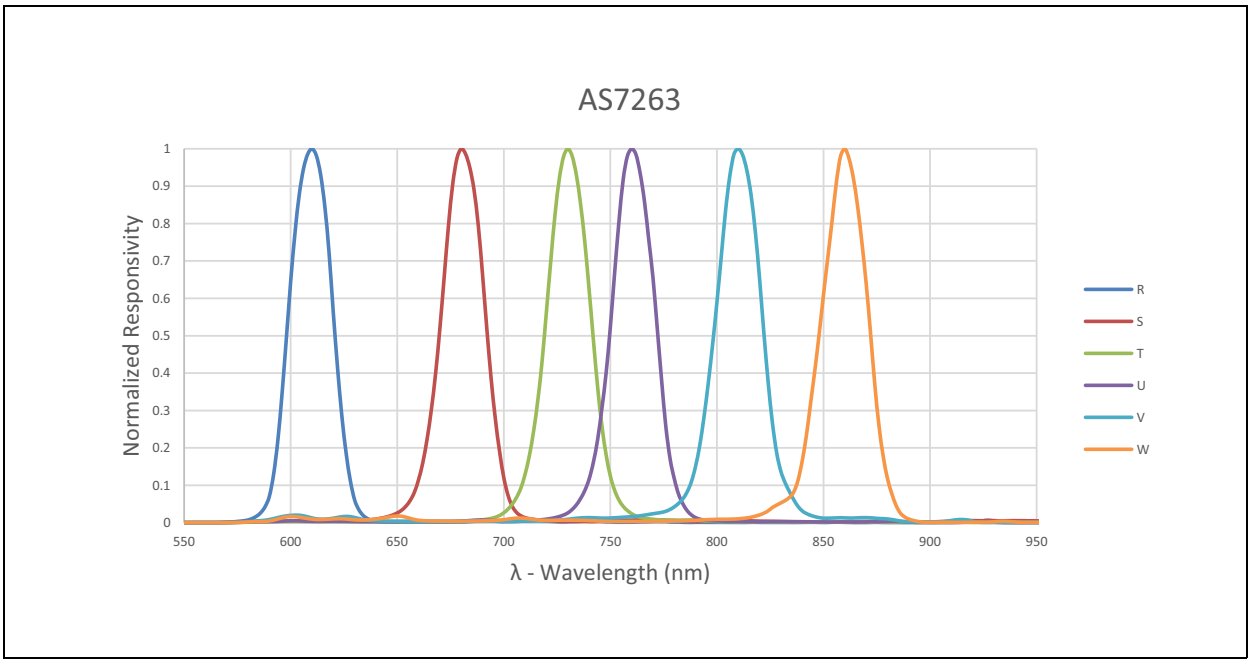
Symbol	Parameter	Test Conditions	Channel (nm)	Min	Typ	Max	Unit
R	Channel R	Incandescent (2), (4)	610		35 (3),(4)		counts/ (µW/cm^2)
S	Channel S	Incandescent (2), (4)	680		35 (3),(4)		counts/ (µW/cm^2)
T	Channel T	Incandescent (2), (4)	730		35 (3),(4)		counts/ (µW/cm^2)
U	Channel U	Incandescent (2), (4)	760		35 (3),(4)		counts/ (µW/cm^2)
V	Channel V	Incandescent (2), (4)	810		35 (3),(4)		counts/ (µW/cm^2)
W	Channel W	Incandescent (2), (4)	860		35 (3),(4)		counts/ (µW/cm^2)
FWHM	Full Width Half Max		20		20		nm
Wacc	Wavelength Accuracy				±5		nm
dark	Dark Channel Counts	GAIN=64, T_{AMB}=25°C				5	counts
f	Angle of Incidence	On the sensors			±20.0		deg

Note(s):

1. Calibration & measurements are made using diffused light.
2. Each channel is tested with GAIN = 16x, Integration Time (INT_T) = 166ms and VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C.
3. The accuracy of the channel counts/µW/cm^2 is ±12%.
4. The light source is an incandescent light with an irradiance of ~1500µW/cm^2 (300-1000nm). The energy at each channel (R, S, T, U, V, W) is calculated with a ±33nm bandwidth around the center wavelengths (610, 680, 730, 760, 810, 860nm).

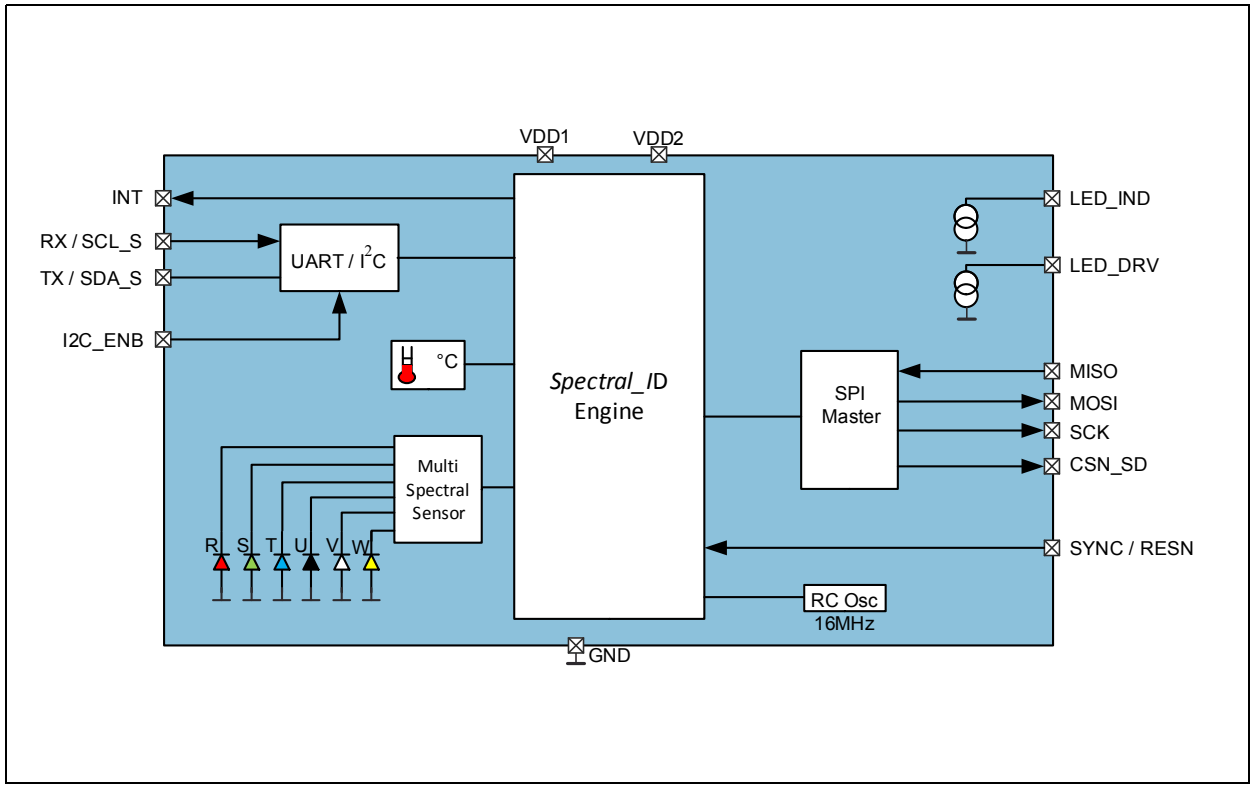
Typical Operating Characteristics

Figure 13:
Spectral Responsivity



Detailed Description

Figure 14:
Internal Block Diagram



6-Channel NIR *Spectral_ID* Detector

The AS7263 6-channel Spectral_ID is a next-generation digital spectral sensor device. Each channel has a Gaussian filter characteristic with a full width half maximum (FWHM) bandwidth of 20nm. The channels are spaced roughly at 50nm intervals in the NIR spectrum: R, S, T, U, V, W. The sensor contains analog-to-digital converters (16-bit resolution ADC), which integrate the current from each channel's photodiode. Upon completion of the conversion cycle, the integrated result is transferred to the corresponding data registers. The transfers are double-buffered to ensure that the integrity of the data is maintained.

Interference filters enable high temperature stability and eliminate lifetime drift. Filter accuracy will be affected by the angle of incidence, and require 0° angle of incidence ±20.0° for specified accuracy. Angles of light beyond this will shift the spectral response of the filters. The LGA package aperture assists in the control of the light input, helping to maintain the proper angle of incidence at the sensors.

Data Conversion Description

AS7263 spectral conversion is implemented via two photodiode banks per device. Bank 1 consists of data from the S, T, U, V photodiodes. Bank 2 consists of data from the R, T, U, W photodiodes. Spectral conversion requires the integration time (IT in ms) set to complete. If both photodiode banks are required to complete the conversion, the 2nd bank requires an additional IT ms. Minimum IT for a single bank conversion is 2.8 ms. If data is required from all 6 photodiodes then the device must perform 2 full conversions (2 x Integration Time).

The spectral conversion process is controlled with BANK Mode settings as follows:

BANK Mode 0: Data will be available in registers S, T, U & V (R and W registers will be zero)

BANK Mode 1: Data will be available in registers R, T, U & W (V and W registers will be zero)

BANK Mode 2: Data will be available in registers R, S, T, U, V & W

When the bank setting is Mode 0, Mode 1, or Mode 2, the spectral data conversion process operates continuously, with new data available after each IT ms period. In the continuous modes, care should be taken to assure prompt interrupt servicing so that integration values from both banks are all derived from the same spectral conversion cycle.

BANK Mode 3: Data will be available in registers R, S, T, U, V & W in One-Shot mode

When the bank setting is Mode 3, the device operates in One-Shot mode. Spectral conversion occurs only when bit 0 of the control register (1SHOT) is set to 1. The 1SHOT bit in the control register is subsequently cleared by hardware at the same time the DATA_RDY bit is set to 1 indicating the availability of spectral conversion result data. The One-Shot mode is intended for use when it is critical to ensure that spectral conversion results are obtained contemporaneously.

Figure 15:
Photo Diode Array

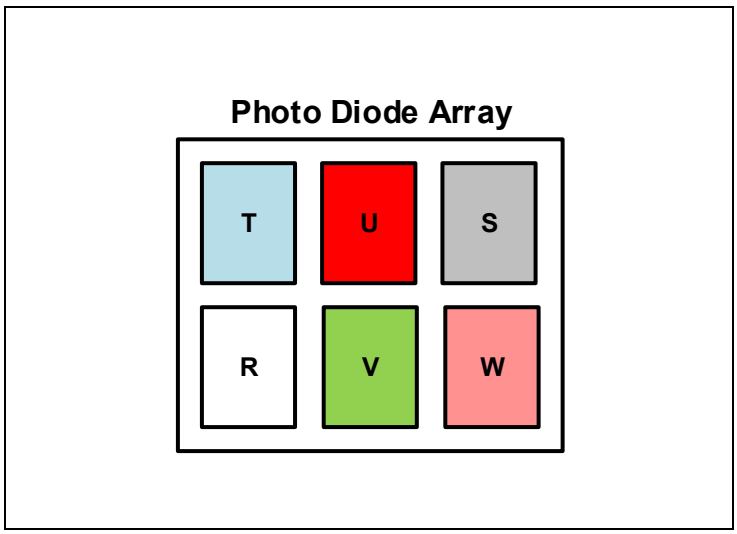
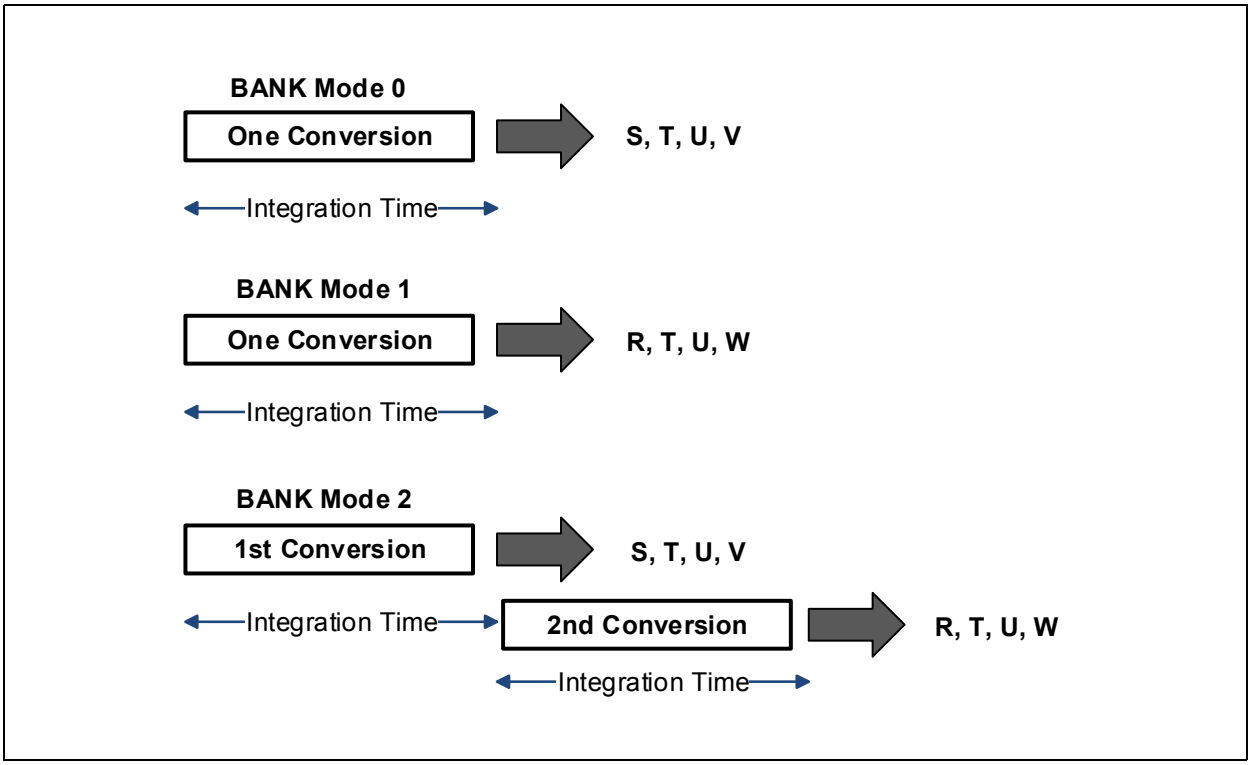


Figure 16:
Bank Mode and Data Conversion



RC Oscillator

The timing generation circuit consists of an on-chip 16MHz, temperature compensated oscillator, which provides the master clock for the AS7263.

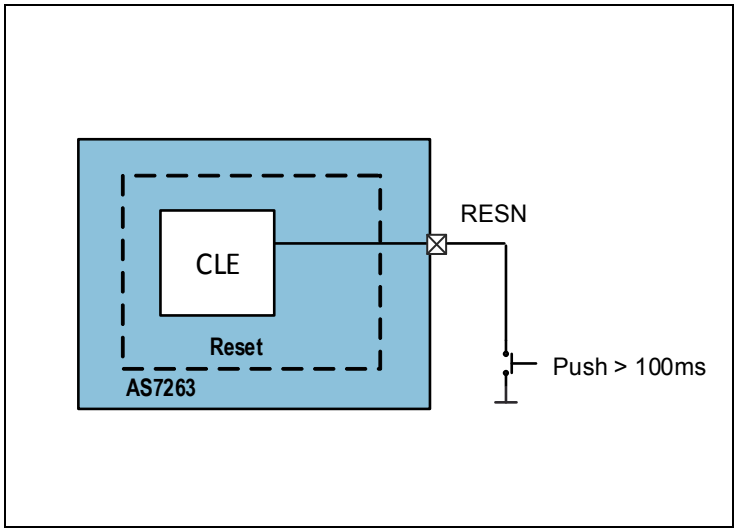
Temperature Sensor

The Temperature Sensor is constantly measuring the on-chip temperature and enables temperature compensation procedures.

Reset

Pulling down the RESN pin for longer than 100ms resets the AS7263.

Figure 17:
Reset Circuit



Indicator LED

The LED, connected to pin LED_IND, can be used to indicate programming progress of the device.

While programming the AS7263 via the external SD card the indicator LED starts flashing (500ms pulses). When programming is completed the indicator LED is switched off. The LED (LED0) can be turned ON/OFF via AT commands or via I^2C register control. The LED sink current is programmable from 1mA, 2mA, 4mA and 8mA.

Electronic Shutter with LED_DRV Driver Control

There are two LED driver outputs that can be used to control up to 2 LEDs. This will allow different wavelength light sources to be used in the same system. The LED output sink currents are programmable and can drive external LED sources: LED_IND from 1mA, 2mA, 4mA and 8mA and LED_DRV from 12.5mA, 25mA, 50mA and 100mA. The sources can be turned off and on via I^2C registers control or AT commands and provides the device with an electronic shutter.

Interrupt Operation

If BANK is set to Mode 0 or Mode 1 then the data is ready after the 1st integration time. If BANK is set to Mode 2 or Mode 3 then the data is ready after two integration times. If the interrupt is enabled (INT = 1) then when the data is ready, the INT line is pulled low and DATA_RDY is set to 1. The INT line is released (returns high) when the control register is read. DATA_RDY is cleared to 0 when any of the sensor registers R, S, T, U, V, W are read. Since each sensor value is 2 bytes, after the 1st byte is read the 2nd byte is shadow-protected in case an integration cycle completes just after the 1st byte is read.

In continuous spectral conversion mode (BANK setting of Mode 0, Mode 1, or Mode 2), the sensors continue to gather information at the rate of the integration time, hence if the sensor registers are not read when the interrupt line goes low, it will stay low and the next cycle's sensor data will be available in the registers at the end of the next integration cycle. When the control register BANK bits are written with a value of Mode 3, One-Shot Spectral Conversion mode is entered. When a single set of contemporaneous sensor readings is desired, writing BANK Mode 3 to the control register immediately triggers exactly two spectral data conversion cycles. At the end of these two conversion cycles, the DATA_RDY bit is set as for the other BANK modes. To perform a new One-Shot sequence, the control register BANK bits should be written with a value of Mode 3 again. This process may continue until the user writes a different value into the BANK bits.

I²C Slave Interface

If selected by the I2C_ENB pin setting, interface and control can be accomplished through an I²C compatible slave interface to a set of registers that provide access to device control functions and output data. These registers on the AS7263 are, in reality, implemented as *virtual* registers in software. The actual I²C slave hardware registers number only three and are described in the table below. The steps necessary to access the virtual registers defined in the following are explained in pseudocode for external I²C master writes and reads below.

I²C Feature List

- Fast mode (400kHz) and standard mode (100kHz) support.
- 7+1-bit addressing mode.
- Write format: Byte.
- Read format: Byte.
- SDA input delay and SCL spike filtering by integrated RC-components.

Figure 18:
I²C Slave Device Address and Physical Registers

Entity	Description	Note
Device Slave Address	8-bit Slave Address	Byte = 1001 001*x* x= 1 for Master Read (byte = 93 hex) x= 0 for Master Write (byte = 92 hex)
STATUS Register	I²C slave interface STATUS register. Read-only.	Register Address = 0x00 Bit 1: TX_VALID 0 -> New data may be written to WRITE register 1 -> WRITE register occupied. Do NOT write. Bit 0: RX_VALID 0 -> No data is ready to be read in READ register. 1 -> Data byte available in READ register.
WRITE Register	I²C slave interface WRITE register. Write-only.	Register Address = 0x01 8-Bits of data written by the I²C Master intended for receipt by the I²C slave. Used for both *virtual* register addresses and write data.
READ Register	I²C slave interface READ register. Read-only.	Register Address = 0x02 8-Bits of data to be read by the I²C Master.

I²C Virtual Register Write Access

Figure 19 shows the pseudocode necessary to write virtual registers on the AS7263. Note that, because the actual registers of interest are realized as virtual registers, a means of indicating whether there is a pending read or write operation of a given virtual register is needed. To convey this information, the most significant bit of the virtual register address is used as a marker. If it is 1, then a write is pending, otherwise the slave is expecting a virtual read operation. The pseudocode illustrates the proper technique for polling of the I²C slave status register to ensure the slave is ready for each transaction.

Figure 19:
I²C Virtual Register Byte Write

Pseudocode

Poll I²C slave STATUS register;
If TX_VALID bit is 0, a write can be performed on the interface;
Send a virtual register address and set the MSB of the register address to 1 to indicate the pending write;
Poll I²C slave STATUS register;
If TX_VALID bit is 0, the virtual register address for the write has been received and the data may now be written;
Write the data.

Sample Code:

```
#define I2C_AS72XX_SLAVE_STATUS_REG0x00
#define I2C_AS72XX_SLAVE_WRITE_REG0x01
#define I2C_AS72XX_SLAVE_READ_REG0x02
#define I2C_AS72XX_SLAVE_TX_VALID0x02
#define I2C_AS72XX_SLAVE_RX_VALID0x01

void i2cm_AS72xx_write(uint8_t virtualReg, uint8_t d)
{
        volatile uint8_tstatus;

        while (1)
        {
        // Read slave I²C status to see if the write buffer is ready.
        status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG);

        if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                // No inbound TX pending at slave.  Okay to write now.
                break ;
        }
        // Send the virtual register address (setting bit 7 to indicate a pending write).
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, (virtualReg | 0x80)) ;

        while (1)
        {
        // Read the slave I2C status to see if the write buffer is ready.
        status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

        if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                // No inbound TX pending at slave.  Okay to write data now.
                break;
        }
        // Send the data to complete the operation.
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, d);
}
```

I²C Virtual Register Read Access

Figure 20 shows the pseudocode necessary to read virtual registers on the AS7263. Note that in this case, reading a virtual register, the register address is not modified.

Figure 20:
I²C Virtual Register Byte Read

Pseudocode

```
Poll I²C slave STATUS register;
If TX_VALID bit is 0, the virtual register address for the read may be written;
Send a virtual register address;
Poll I²C slave STATUS register;
If RX_VALID bit is 1, the read data is ready;
Read the data.
```

Sample Code:

```
uint8_t i2cm_AS72xx_read(uint8_t virtualReg)
{
        volatile uint8_t status, d ;

        while (1)
        {
        // Read slave I2C status to see if the read buffer is ready.
        status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

        if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                // No inbound TX pending at slave.  Okay to write now.
                break ;
        }
        // Send the virtual register address (setting bit 7 to indicate a pending write).
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, virtualReg) ;

        while (1)
        {
        // Read the slave I²C status to see if our read data is available.
        status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

        if ((status & I2C_AS72XX_SLAVE_RX_VALID) != 0)
                // Read data is ready.
                break ;
        }
        // Read the data to complete the operation.
        d = i2cm_read(I2C_AS72XX_SLAVE_READ_REG) ;
        return d ;s
}
```

The details of the i2cm_read() and i2cm_write() functions in previous Figures are dependent upon the nature and implementation of the external I²C master device.

I²C Virtual Register Set

The figure below provides a summary of the AS7263 I²C register set. Figures after that provide additional details. All register data is hex or, where noted, 32-bit floating point, and all multi-byte entities are Big Endian (most significant byte is situated at the lowest register address).

Figure 21:
I²C Register Set Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Version Registers									
0x00: 0x01	HW_Version	Hardware Version							
0x02: 0x03	FW_Version	Firmware Version							
Control Registers									
0x04	Control_Setup	RST	INT	GAIN		Bank		DATA_ RDY	RSVD
0x05	INT_T	Integration Time							
0x06	Device_Temp	Device Temperature							
0x07	LED_Control	RSVD		ICL_DRV		LED_ DRV	ICL_IND		LED_IND
Sensor Raw Data Registers									
0x08	R_High	Channel R High Data Byte							
0x09	R_Low	Channel R Low Data Byte							
0x0A	S_High	Channel S High Data Byte							
0x0B	S_Low	Channel S Low Data Byte							
0x0C	T_High	Channel T High Data Byte							
0x0D	T_Low	Channel T Low Data Byte							
0x0E	U_High	Channel U High Data Byte							
0x0F	U_Low	Channel U Low Data Byte							
0x10	V_High	Channel V High Data Byte							
0x11	V_Low	Channel V Low Data Byte							
0x12	W_High	Channel W High Data Byte							
0x13	W_Low	Channel W Low Data Byte							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Sensor Calibrated Data Registers									
0x14: 0x17	R_Cal	Channel R Calibrated Data (float)							
0x18: 0x1B	S_Cal	Channel S Calibrated Data (float)							
0x1C: 0x1F	T_Cal	Channel T Calibrated Data (float)							
0x20: 0x23	U_Cal	Channel U Calibrated Data (float)							
0x24: 0x27	V_Cal	Channel V Calibrated Data (float)							
0x28: 0x2B	W_Cal	Channel W Calibrated Data (float)							

Detailed Register Description

Figure 22:
HW Version Registers

Addr: 0x00		HW_Version		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device Type	0100000	R	Device type number
Addr: 0x01		**HW_Version**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	HW Version	00111111	R	Hardware version

Figure 23:
FW Version Registers

Addr: 0x02		FW_Version		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Minor Version		R	Minor Version [1:0]
5:0	Sub Version		R	Sub Version
Addr: 0x03		**FW_Version**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Major Version		R	Major Version
3:0	Minor Version		R	Minor Version [5:2]

Figure 24:
Control Setup Register

Addr: 0x04/0x84		Control_Setup		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	RST	0	R/W	Soft Reset, Set to 1 for soft reset, goes to 0 automatically after the reset
6	INT	0	R/W	Enable interrupt pin output (INT), 1: Enable, 0: Disable
5:4	GAIN	0	R/W	Sensor Channel Gain Setting (all channels) 'b00=1x; 'b01=3.7x; 'b10=16x; 'b11=64x
3:2	BANK	10	R/W	Data Conversion Type (continuous) 'b00=Mode 0; 'b01=Mode 1; 'b10=Mode 2; 'b11=Mode 3 One-Shot
1	DATA_RDY	0	R/W	1: Data Ready to Read, sets INT active if interrupt is enabled. Can be polled if not using INT.
0	RSVD	0	R	Reserved; Unused

Figure 25:
Integration Time Register

Addr: 0x05/0x85		INT_T		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	INT_T	0xFF	R/W	Integration time = <value> * 2.8ms

Figure 26:
Device Temperature Register

Addr: 0x06		Device_Temp		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Device_Temp		R	Device temperature data byte (°C)

Figure 27:
LED Control Register

Addr: 0x07/0x87		LED Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	RSVD	0	R	Reserved
5:4	ICL_DRV	00	R/W	LED_DRV current limit 'b00=12.5mA; 'b01=25mA; 'b10=50mA; 'b11=100mA
3	LED_DRV	0	R/W	Enable LED_DRV 1: Enabled; 0: Disabled
2:1	ICL_IND	00	R/W	LED_IND current limit 'b00=1mA; 'b01=2mA; 'b10=4mA; 'b11=8mA
0	LED_IND	0	R/W	Enable LED_IND 1: Enabled; 0: Disabled

Figure 28:
Sensor Raw Data Registers

Addr: 0x08		R_High		
Bit	Bit Name	Default	Access	Bit Description
7:0	R_High		R	Channel R High Data Byte
Addr: 0x09		**R_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	R_Low		R	Channel R Low Data Byte
Addr: 0x0A		**S_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	S_High		R	Channel S High Data Byte
Addr: 0x0B		**S_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	S_Low		R	Channel S Low Data Byte
Addr: 0x0C		**T_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	T_High		R	Channel T High Data Byte
Addr: 0x0D		**T_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	T_Low		R	Channel T Low Data Byte
Addr: 0x0E		**U_High**		
Bit	Bit Name	Default	Access	Bit Description
7:0	U_High		R	Channel U High Data Byte
Addr: 0x0F		**U_Low**		
Bit	Bit Name	Default	Access	Bit Description
7:0	U_Low		R	Channel U Low Data Byte