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AS7264N

XYZ Chromatic Color and 440/490nm Blue Sensor with Electronic Shutter

General Description

The AS7264N provides direct XYZ sensor data which conforms to the tri-stimulus standard observer color response of the human eye. In addition, two channels added for measurement of blue spectrum light, plus a near-IR channel enables additional application flexibility. LED drivers with programmable currents are provided for electronic shutter applications.

The AS7264N integrates Gaussian filters into standard CMOS silicon via nano-optic deposited interference filter technology and is packaged in an LGA package that provides a built in aperture to control the light entering the sensor array.

Control and spectral data access is implemented through an I²C register set.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS7264N, XYZ Chromatic Color and 440/490nm Blue Sensor with Electronic Shutter are listed below:

Figure 1:
AS7264N Benefits and Features

Benefits	Features
<ul style="list-style-type: none"> XYZ channel data conforming to human eye response to color information 	<ul style="list-style-type: none"> XYZ tri-stimulus standard observer filter set
<ul style="list-style-type: none"> Additional specific blue light sensing in ranges associated with eye health and other biological light effects 	<ul style="list-style-type: none"> Two added blue channels at 440nm and 490nm
<ul style="list-style-type: none"> High accuracy ambient light measurements 	<ul style="list-style-type: none"> Ambient light sensing (photopic response)
<ul style="list-style-type: none"> Direct register read and write with interrupt on sensor ready 	<ul style="list-style-type: none"> I²C slave digital Interface with optional interrupt operation
<ul style="list-style-type: none"> High stability over lifetime with minimal drift over temperature 	<ul style="list-style-type: none"> Filter set realized by silicon interference filters
<ul style="list-style-type: none"> No additional signal conditioning required 	<ul style="list-style-type: none"> 16-bit ADC with digital access
<ul style="list-style-type: none"> Direct register read and write with interrupt on sensor ready 	<ul style="list-style-type: none"> I²C slave digital Interface with optional interrupt operation

Benefits	Features
<ul style="list-style-type: none"> • Electronic shutter control/synchronization 	<ul style="list-style-type: none"> • Programmable LED drivers
<ul style="list-style-type: none"> • Low voltage operation 	<ul style="list-style-type: none"> • 2.7V to 3.6V with I²C interface
<ul style="list-style-type: none"> • Small, robust package, with built-in aperture 	<ul style="list-style-type: none"> • 20-pin LGA package 4.5mm x 4.7mm x 2.5mm • -40°C to 85°C temperature range

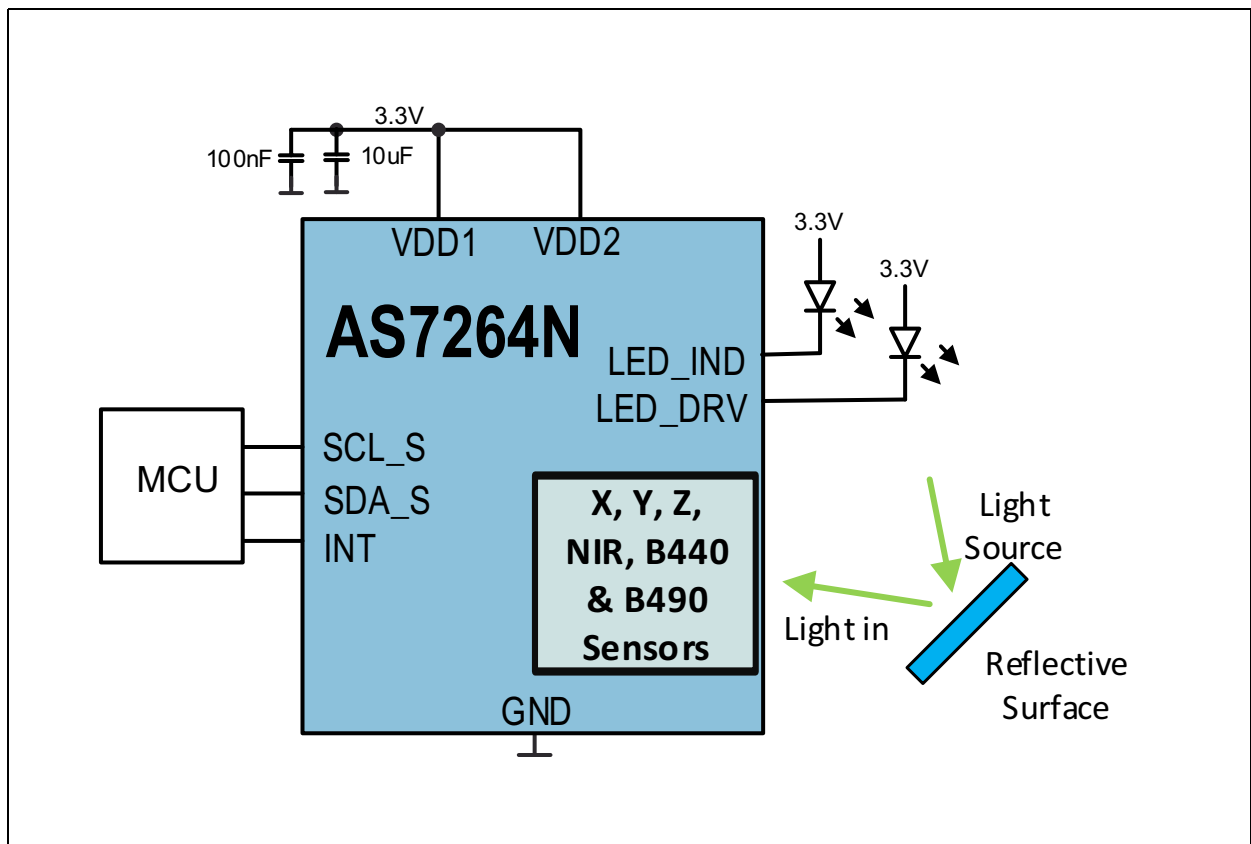
Application

The AS7264N applications include:

- Ambient light spectral exposure
- Biological lighting measurements
- Color measurement and absorbance
- Color matching and identification
- Precision color tuning/calibration

System Block Diagram

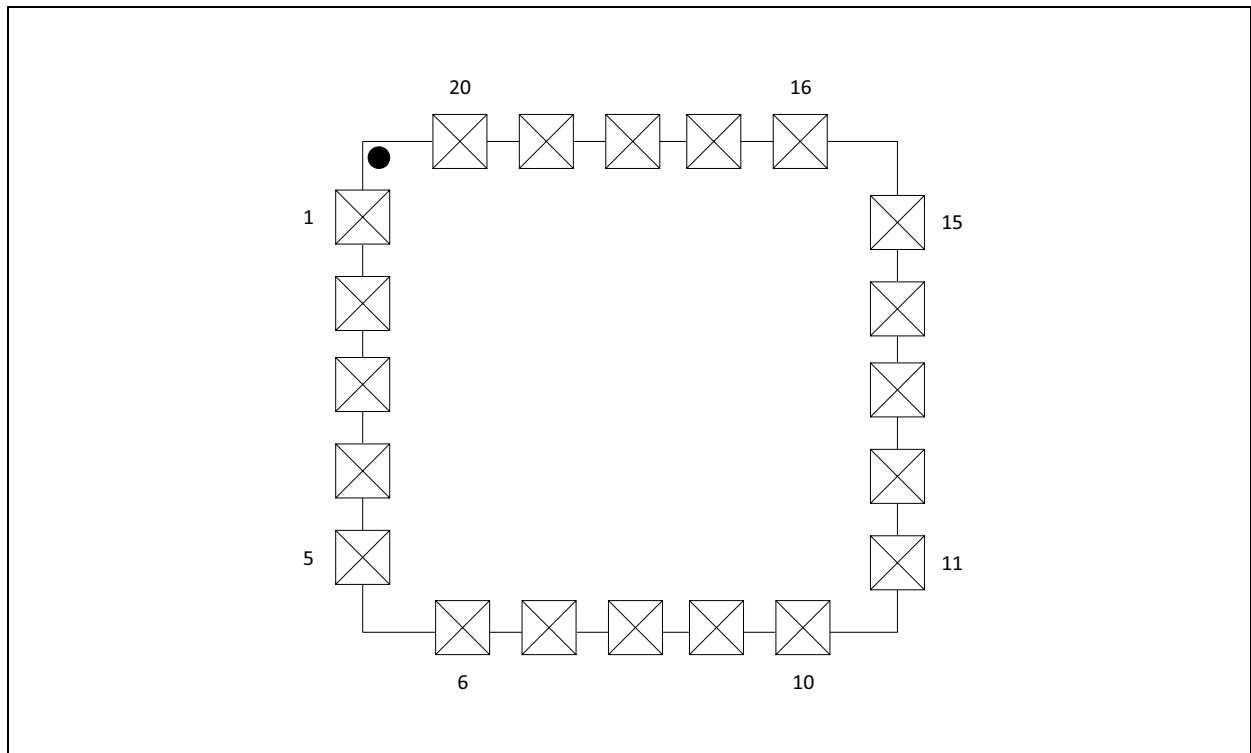
Figure 2:
AS7264N Sensor System



Pin Assignments

The device pin assignments are described below.

Figure 3:
Pin Diagram of AS7264N (Top View)



Pin Description

Figure 4:
Pin Description of AS7264N

Pin Number	Pin Name	Description
1	NF	Not functional. Do not connect.
2	RESN	Reset, active LOW
3	NF	Not functional. Do not connect.
4	NF	Not functional. Do not connect.
5	NF	Not functional. Do not connect.
6	NF	Not functional. Do not connect.
7	NF	Not functional. Do not connect.
8	NF	Not functional. Do not connect.
9	SCL_S	I ² C slave clock pin
10	SDA_S	I ² C slave data pin
11	NF	Not functional. Do not connect.

Pin Number	Pin Name	Description
12	NF	Not functional. Do not connect.
13	INT	Interrupt, active HIGH
14	VDD2	Voltage supply
15	LED_DRV	LED driver output for driving LED current sink
16	GND	Ground
17	VDD1	Voltage supply
18	LED_IND	LED driver output for indicator LED current sink
19	NF	Not functional. Do not connect.
20	NF	Not functional. Do not connect.

Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device is not designed for high energy UV (ultraviolet) environments, including upward looking outdoor applications, which could affect long term optical performance.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD_MAX}	Supply Voltages VDD1, VDD2	-0.3	5	V	Pins VDD1 & VDD2 must be sourced from the same supply voltage
V_{DD_IO}	Input/Output Pin Voltage	-0.3	VDD+0.3	V	Input/Output pin to GND
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JESD78D
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 1000		V	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM	± 500		V	JSD22-C101F
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices"
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Maximum floor life time of 168 hours

Electrical Characteristics

All limits are guaranteed with $V_{DD} = V_{DD1} = V_{DD2} = 3.3V$, $T_{AMB} = 25^{\circ}C$. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. V_{DD1} and V_{DD2} must be sourced from the same power supply.

Figure 6:
Electrical Characteristics of AS7264N

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General Operating Conditions						
V_{DD}	Voltage Operating Supply	I ² C Interface	2.7	3.3	3.6	V
T_{AMB}	Operating Temperature		-40	25	85	°C
I_{VDD}	Operating Current				5	mA
$I_{STANDBY}^{(1)}$	Standby Current			12		μA
Internal RC Oscillator						
F_{OSC}	Internal RC Oscillator Frequency		15.7	16	16.3	MHz
$t_{JITTER}^{(2)}$	Internal Clock Jitter	@25°C			1.2	ns
Temperature Sensor						
D_{TEMP}	Absolute Accuracy of the Internal Temperature Measurement		-8.5		8.5	°C
Indicator LED						
I_{IND}	LED Current	Available current steps: 1, 2, 4, or 8mA	1		8	mA
I_{ACC}	Accuracy of Current		-30		30	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V
LED_DRV						
I_{LED1}	LED Current	Available current steps: 12.5, 25, 50, or 100mA	12.5		100	mA
I_{ACC}	Accuracy of Current		-10		10	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital Inputs and Outputs						
I_{IH}, I_{IL}	Logic Input Current	$V_{in}=0V$ or VDD	-1		1	μA
$I_{IL RESN}$	Logic Input Current (RESN pin)	$V_{in}=0V$	-1		-0.2	mA
V_{IH}	CMOS Logic High Input		$0.7 * V_{DD}$		VDD	V
V_{IL}	CMOS Logic Low Input		0		$0.3 * V_{DD}$	V
V_{OH}	CMOS Logic High Output	$I=1mA$			VDD - 0.4	V
V_{OL}	CMOS Logic Low Output	$I=1mA$			0.4	V
$t_{RISE}^{(2)}$	Current Rise Time	$C(Pad)=30pF$			5	ns
$t_{FALL}^{(2)}$	Current Fall Time	$C(Pad)=30pF$			5	ns

Note(s):

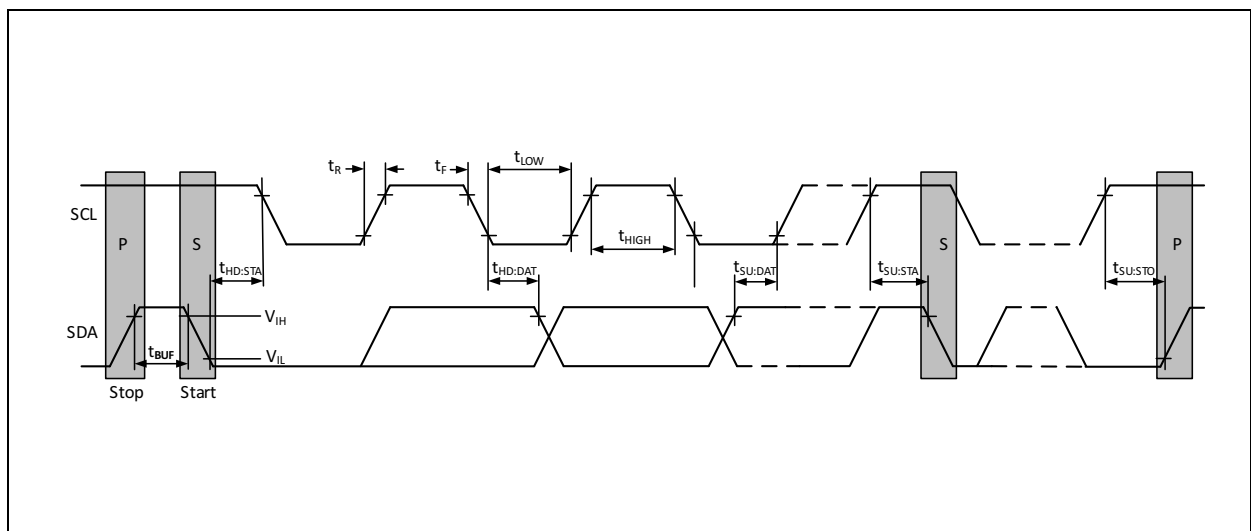
1. $15\mu A$ over temperature
2. Guaranteed, not tested in production

Timing Characteristics

Figure 7:
AS7264N I²C Slave Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C Interface						
f _{SCLK}	SCL Clock Frequency		0		400	kHz
t _{BUF}	Bus Free Time Between a STOP and START		1.3			μs
t _{HS:STA}	Hold Time (Repeated) START		0.6			μs
t _{LOW}	LOW Period of SCL Clock		1.3			μs
t _{HIGH}	HIGH Period of SCL Clock		0.6			μs
t _{SU:STA}	Setup Time for a Repeated START		0.6			μs
t _{HS:DAT}	Data Hold Time		0		0.9	μs
t _{SU:DAT}	Data Setup Time		100			ns
t _R	Rise Time of Both SDA and SCL		20		300	ns
t _F	Fall Time of Both SDA and SCL		20		300	ns
t _{SU:STO}	Setup Time for STOP Condition		0.6			μs
C _B	Capacitive Load for Each Bus Line	Total capacitance of one bus line in pF			400	pF
C _{I/O}	I/O Capacitance (SDA, SCL)				10	pF

Figure 8:
I²C Slave Timing Diagram



Operation Characteristics

Figure 9:
Spectral Responsivity

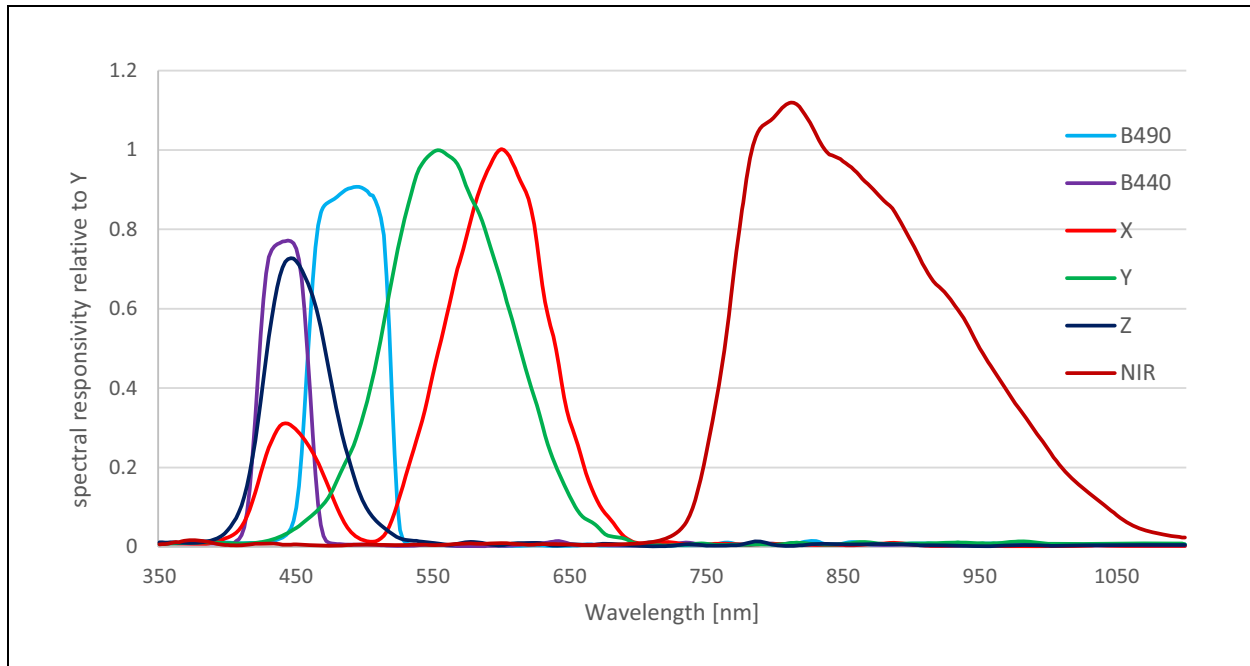


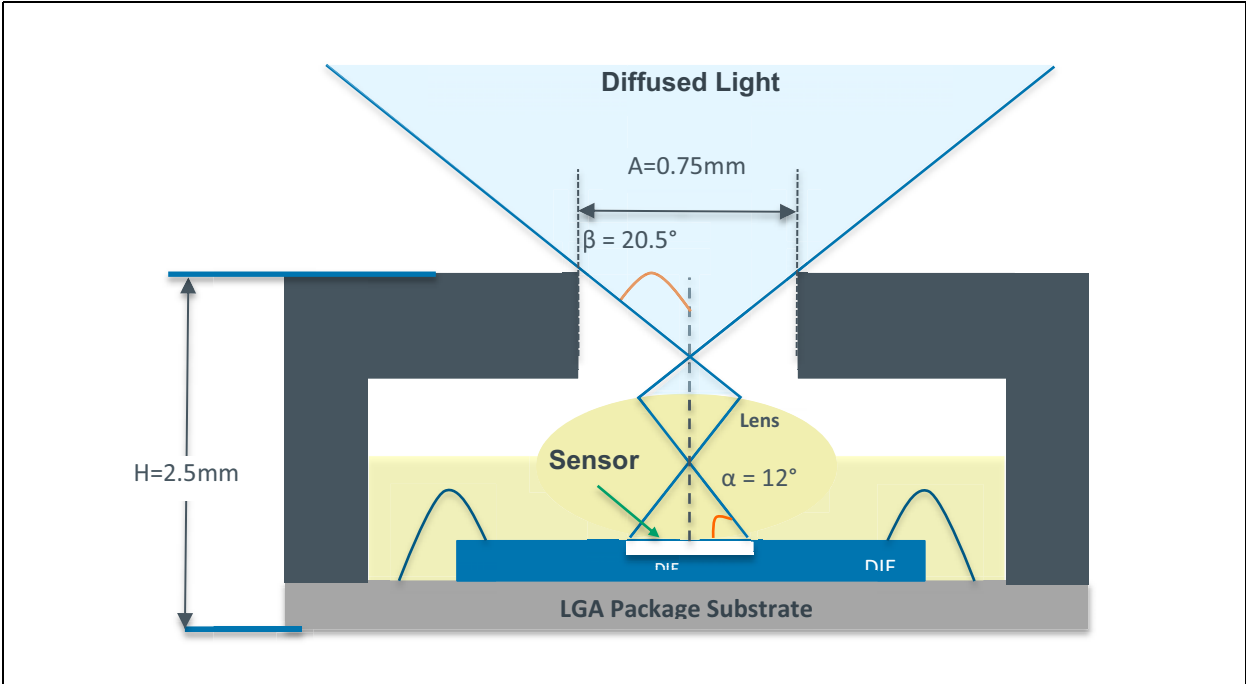
Figure 10:
AS7264N Optical Characteristics (Pass Band)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
X	Channel X	White LED 5700K source, Ee=116μW/cm ²		7.7		counts/ (μW/cm ²)
Y	Channel Y	White LED 5700K source, Ee=116μW/cm ²		8.6		counts/ (μW/cm ²)
Z	Channel Z	White LED 5700K source, Ee=116μW/cm ²		4.7		counts/ (μW/cm ²)
NIR	Channel NIR	Incandescent light source, Ee=465μW/cm ²		14.0		counts/ (μW/cm ²)
B ₄₉₀	Channel Blue490	White LED 5700K source, Ee=116μW/cm ²		9.4		counts/ (μW/cm ²)
B ₄₄₀	Channel Blue440	White LED 5700K source, Ee=116μW/cm ²		10.9		counts/ (μW/cm ²)
PFOV	Package Field of View			±20.5		deg

Note(s):

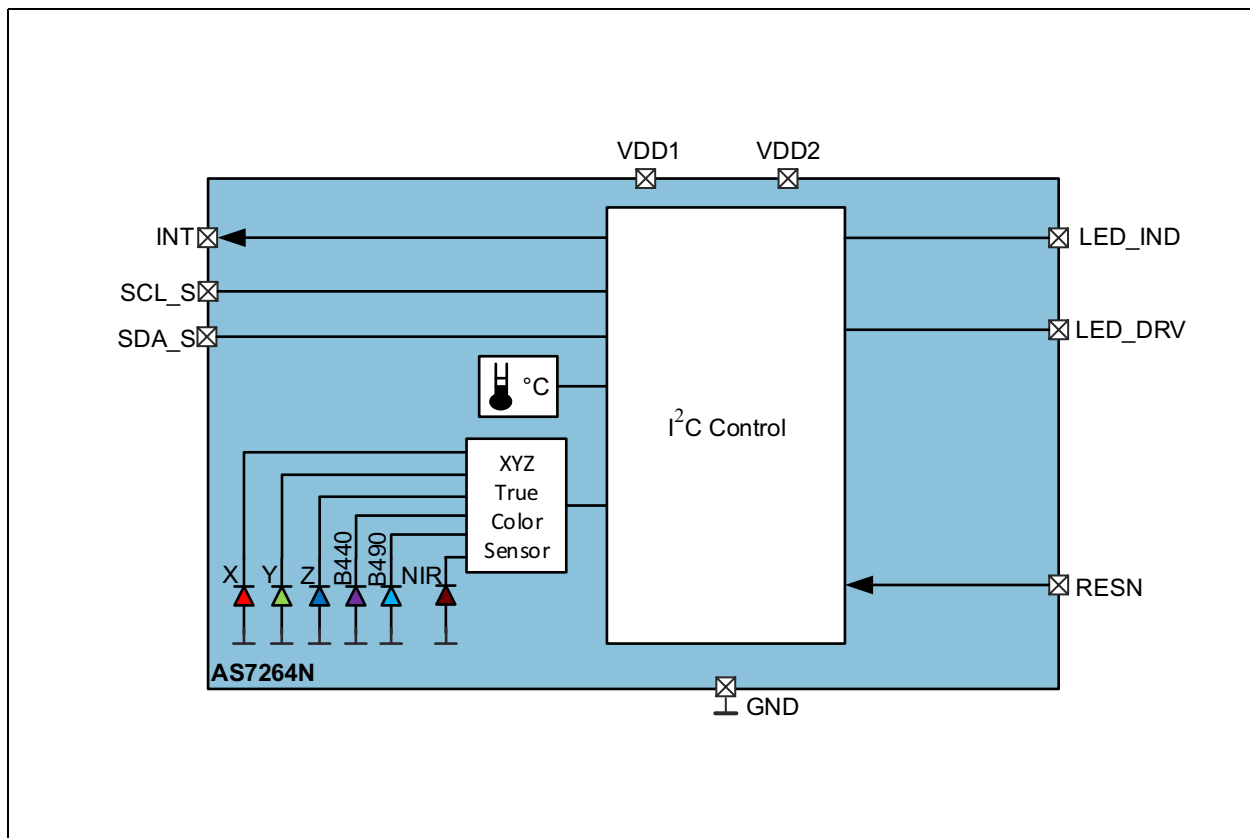
- Each channel is tested with GAIN = 3.7x, Integration Time (INT_T) = 166ms and T_{AMB}=25°C
- The accuracy of each channel count is ±25%

Figure 11:
AS7264N LGA Package Field of View



Detailed Descriptions

Figure 12:
Internal Block Diagram



XYZ Sensor

The AS7264N XYZ sensor is a next-generation digital color sensor device. It senses X, Y, Z standard observer filters compliant with the CIE 1931 standard observer color response in addition to near IR (NIR), long wavelength blue (490nm) and short wavelength blue (440nm) spectrum filters.

The sensor contains analog-to-digital converters (16-bit resolution ADC), which integrate current from each channel's photodiode. Upon completion of conversion cycle, the integrated result is transferred to the corresponding data register. Transfers are double-buffered to ensure integrity of the data is maintained.

Interference filters realize all filter responses and enable minimal life-time drift and very high temperature stability. Filter accuracy is affected by the optical angle of incidence which itself is limited by an integrated aperture and an internal micro-lens structure in the AS7264N. The package field of view (PFOV) is $\pm 20.5^\circ$ to deliver the specified accuracy. External optics can be used as needed to expand or reduce this built in PFOV.

Data Conversion

AS7264N spectral conversion is implemented via two photodiode banks. The first bank provides data from the X, Y, Z and NIR (near-IR) photodiodes. The second bank provides data from the same X and Y photodiodes as well as blue 440nm and blue 490nm photodiodes.

The spectral conversion process is controlled with two BANK Mode settings. Bank Mode 0 uses I²C registers for X, Y, B440 and B490 data. Bank Mode 1 uses I²C registers for X, Y, Z and NIR data. Sensor data is available in four I²C registers (NDATAL/NDATAH, XDATAL/XDATAH, YDATAL/YDATAH and ZDATAL/ZDATAH) as shown in the figures below.

Figure 13: Bank Modes

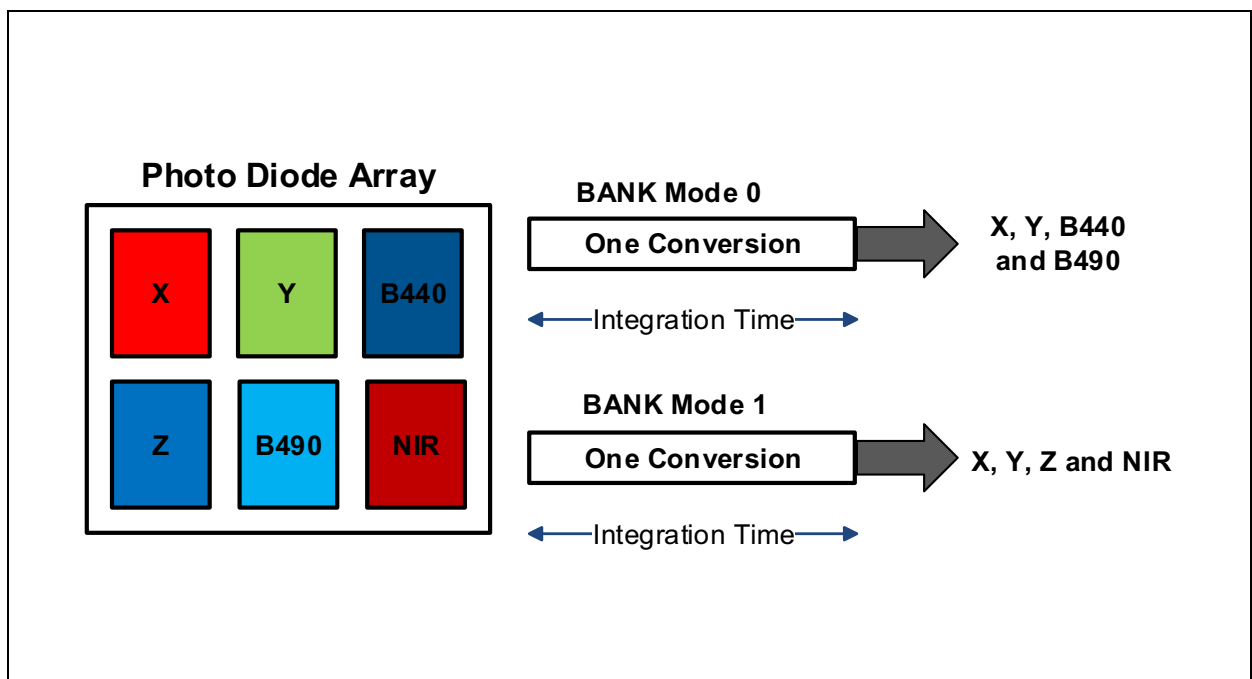


Figure 14: AS7264N Sensor Data I²C Registers

I ² C Register	Bank Mode 0	Bank Mode 1
NDATAL/NDATAH	B490	NIR
XDATAL/XDATAH	X	X
YDATAL/YDATAH	Y	Y
ZDATAL/ZDATAH	B440	Z

Spectral Conversion and Data Acquisition

Spectral conversion uses a register set for integration time (register INT_T). If both photodiode banks are required to complete the conversion, the second bank requires an additional integration time. Minimum conversion time for a single bank is 2.8 milliseconds. If data is required from all 6 photodiodes the device must perform 2 full conversions (2x integration time). The user has control of gain for the photodiode current, programmed into bits 0 and 1 of the GAIN_IDRV register where gain can be set to 1x, 3.7x, 16x or 64x. A wait time between integration cycles can be programmed into register WTIME using the same units as the INT_T register.

An auto zero function is automatically performed before the first data conversion after a power-on or reset, in order to achieve the best data quality. Auto zero corrects for internal device temperature. But since it's automatically done only once, it can also be manually run. Typically, if the temperature changes by 15 °C or more the auto zero should be manually run by writing to the Auto_Zero register (temperature is user calculated based on TMPL & TMPH registers values). But auto zero can also be manually done before every conversion. When auto zero function is complete the DONE bit (bit7) of Auto_Zero register will be set to 1.

The BANK bit (bit7) in the BANK register can be changed as needed before data conversion to acquire the desired channels. While conversion is continuous, timing is done using registers. Both polling and interrupt operation are then supported for "conversion complete" timing. Both require programming the INTR_POLL_EN register bit 2 to a 1. The conversion process is started by writing a 0x01 to the DATA_EN register followed by clearing any previous Data Valid bit in the INTR_POLL_CLR register. This is followed by a separate write of 0x03 to the DATA_EN register.

If the AS7264N interrupt output is to be used for data conversion timing the INTR_PIN_Config register should be programmed to 0xCA. The INT pin will then be asserted high at the completion of the conversion cycle. A 0x04 should be written to the INTR_POLL_CLR register to clear this interrupt which also clears polling bit 2 in the register.

If only polling is to be used for conversion timing, an external interrupt is not required and the INTR_PIN_Config register should be programmed to 0x00. Polling of bit 2 in the INTR_POLL_CLR register will return 0x00 if the conversion is not complete, and 0x04 if complete. Once complete a 0x04 should be written to the INTR_POLL_CLR register to clear bit 2, the polled bit.

For acquisition, done after conversion, data needs to be latched by writing 0x83 to the DATA_EN register. The purpose of latching the data by the user is to provide a mechanism for data to be coherent and under user control. Now, the data bank register can be read (one bank per single conversion-acquisition cycle). The CLR bit (bit2) should be

cleared by writing a 1 to the CLR bit (bit2) of the INTR_POLL_CLR register (0xF8) after each conversion-acquisition cycle is completed.

Temperature Sensor

The Temperature Sensor measures on-chip temperature on demand, and enables temperature compensation procedures. The basic equation for calculating the internal temperature of the device is:

$$(EQ1) \quad \frac{0.7604 - \frac{TMP_VALUE \cdot 2.048}{1024}}{2.046 \cdot 10^{-3}} - 40$$

TMP_VALUE is the derived from TMPL & TMPH (0xD2 [1:0] and 0xD1 [7:0]) register data. Temperature conversions are performed by writing 0x24 to the TMP_Config register. Polling the TMP_Config register will indicate data acquisition is complete upon reading 0x84. After reading 0x84 the TMP_Config register should be written to either 0x00 for idle or 0x24 to perform another temperature measurement. The result of the calculation is the device temperature in degree Celsius (°C).

Electronic Shutter with LED_IND or LED_DRV Driver Control

Under user control there are two LED driver outputs that can be used to control LEDs on the two driver pins. This allows different wavelength light sources to be used in the same system. The LED output sink currents are programmable and can drive external LED sources. After programming for current the sources can be turned off and on via registers to provide the AS7264N with an electronic shutter capability. If turning LEDs on, they should be fully on optically before a conversion begins and not shut off until after the conversion-acquisition cycle completes

The LED_IND pin can be turned on/off via the LED_IND register with values 0x01, 0x05, 0x09 and 0x0D for sink currents of 1mA, 2mA, 4mA and 8mA respectively.

For the LED_DRV pin, the GAIN_IDRV Register (0xB9) bits 7 and 6 control the drive strength of the pin for current values 12.5mA, 25mA, 50mA and 100mA. This register also controls the gain of all light acquisitions so care should be taken when writing to it. The LED_DRV pin can be turned on/off via the LED_DRV register bit 2.

Low Power Mode

AS7264N can be put into the low power mode by writing 0x02 to the POWER MODE Register (0x73). Write 0x00 to set it back to normal mode. Wait at least 50µs before doing further AS7264N operations after powering back to normal.

The sequence to configure AS7264N into low power mode:

- Write 0x00 to Register 0xFA
- Write 0x02 to Register 0x73
- AS7264N is in low power mode

The sequence to configure AS7264N out of low power mode:

- Write 0x00 to Register 0x73
- Wait for at least 50µs
- Write 0x03 to Register 0xFA
- AS7264N is in normal mode

Device Initialization and Pin Assignment

On power up device needs to be initialized as follows before programming registers to do data conversion and acquisition:

- Device Config 1 register: 0x70 written to 0x8A
- Device Config 2 register: 0x71 written to 0x02
- Device Config 3 register: 0xB0 written to 0x02
- Device Config 4 register: 0x88 written to 0x00
- Device Config 5 register: 0x9A written to 0x02
- Interrupt Operation: The only user defined pin functionality is whether to use pin 13 as an interrupt signal at the completion of data conversion. This is done by programming the INTR_PIN_Config register (0x22) to 0xCA. To disable interrupt function the INTR_PIN_Config register should be programmed to 0x00, which is the power-on and reset default.

RC Oscillator

An internal on-chip timing generation circuit provides a 16MHz temperature compensated oscillator for the AS7264N master clock.

Reset

Pulling down the RESN pin for longer than 100ms resets the AS7264N.

Figure 15:
Reset Circuit

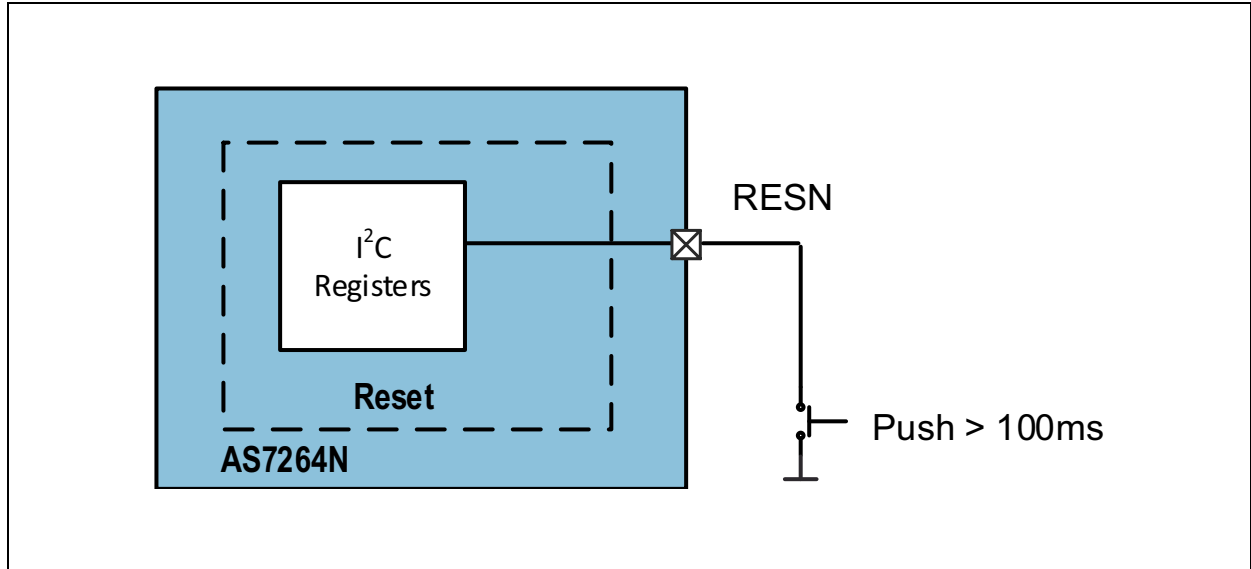
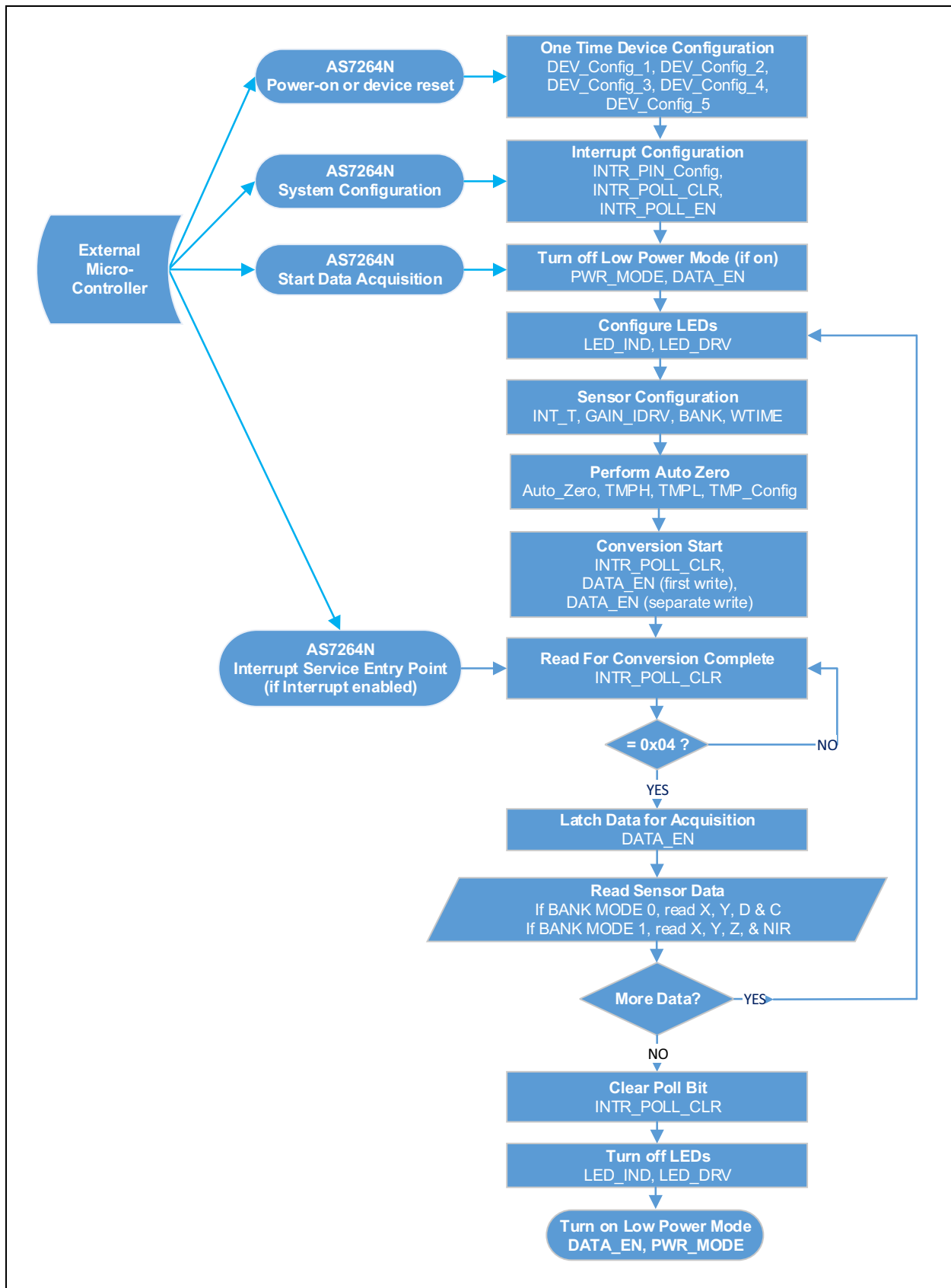


Figure 16:
I²C Register Programming Flow Chart



Note(s):

1. When using shuttered LEDs, the LED source(s) should be at desired brightness before conversion starts.

I²C Slave Interface

Interface, control and reading sensor data is accomplished through an I²C compatible slave interface via a set of registers.

I²C Feature List

- Fast mode (400 kHz) and standard mode (100 kHz) support
- 7+1-bit addressing mode
- Write format: Byte
- Read format: Byte

I²C Register Set

The 7-bit I²C slave address of AS7264N is 0x49 plus one bit for read/write. When reading from I²C registers, the 7 + 1-bit address should be 0x93. When writing to I²C registers, the 7+1-bit address should be 0x92.

The figure below provides a summary of the AS7264N I²C register set. Figures after that provide additional details. All register data is hex, and all multi-byte entities are Big Endian (most significant byte is situated at the lower register address).

I²C register addresses not listed should be treated as reserved and not used.

Figure 17:
I²C Register Set Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	
Device Version Registers										
0x10	DEV_ID	Device Identification								
0x11	DEV_VER	Device Version								
Device Configuration Registers										
0x70	DEV_Config_1	Device Configuration 1								
0x71	DEV_Config_2	Device Configuration 2								
0xB0	DEV_Config_3	Device Configuration 3								
0x88	DEV_Config_4	Device Configuration 4								
0x9A	DEV_Config_5	Device Configuration 5								
Power Mode Register										
0x73	PWR_MODE	RESV						PM	RESV	

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	
Interrupt and Polling Control Registers										
0x22	INTR_PIN_Config	OPIN		FUNCT						
0xF8	INTR_POLL_CLR	RESV					CLR	RESV		
0xF9	INTR_POLL_EN	RESV					EN	RESV		
LED Control Registers										
0xEA	LED_DRV	RESV					ON_OFF	RESV		
0x84	LED_IND	RESV				CURRENT		RESV	ON_OFF	
Auto Zero and Temperature Control Registers										
0xBA	Auto_Zero	RESV				C_EN	X_EN	Y_EN	Z_EN	
0xD1	TMPH	Most Significant bits (9:2) of Temperature Measurement								
0xD2	TMPL	RESV						TMPL		
0xD3	TMP_Config	ISTAT	RESVSTRT		RESV	SRC				
Sensor Control Registers										
0xDB	BANK	BANK	RESV							
0xB9	GAIN_IDRV	IDRV		RESV				GAIN		
0xD9	INT_T	Integration Time								
0xDA	WTIME	Wait Time								
0xFA	DATA_EN	DL	RESV			WAIT	RESV	CON	PON	
Sensor Data Registers										
0xDC	NDATA_L	N Channel Low Byte								
0xDD	NDATA_H	N Channel High Byte								
0xDE	YDATA_L	Y Channel Low Byte								
0xDF	YDATA_H	Y Channel High Byte								
0xEC	ZDATA_L	Z Channel Low Byte								
0xED	ZDATA_H	Z Channel High Byte								
0xEE	XDATA_L	X Channel Low Byte								
0xEF	XDATA_H	X Channel High Byte								

Detailed Register Description

Figure 18:
Device ID and Version Registers

Addr: 0x01		Device Identification		
Bit	Bit Name	Default	Access	Bit Description
7:0	DEV_ID	01110010	R	Device identification number
Addr: 0x11		Device Version		
Bit	Bit Name	Default	Access	Bit Description
7:0	DEV_VER		R	Device version number

Figure 19:
Device Configuration Registers

Addr: 0x70		Device Configuration 1		
Bit	Bit Name	Default	Access	Bit Description
7:0	DEV_Config_1		R/W	Device Configuration 1, must be initialized to 0x8A by external MCU
Addr: 0x71		Device Configuration 2		
Bit	Bit Name	Default	Access	Bit Description
7:0	DEV_Config_2		R/W	Device Configuration 1, must be initialized to 0x02 by external MCU
Addr: 0xB0		Device Configuration 3		
Bit	Bit Name	Default	Access	Bit Description
7:0	DEV_Config_3		R/W	Device Configuration 1, must be initialized to 0x02 by external MCU
Addr: 0x88		Device Configuration 4		
Bit	Bit Name	Default	Access	Bit Description
7:0	DEV_Config_4		R/W	Device Configuration 1, must be initialized to 0x00 by external MCU
Addr: 0x9A		Device Configuration 5		
Bit	Bit Name	Default	Access	Bit Description
7:0	DEV_Config_5		R/W	Device Configuration 1, must be initialized to 0x02 by external MCU

Figure 20:
Power Mode Register

Addr: 0x04/0x84		PWR_MODE		
Bit	Bit Name	Default	Access	Bit Description
7:2	RESV	0	R/W	Reserved, set to 000000 if writing the register
1	PM	1	R/W	1= Normal Operation Power Mode 0= Low Power Mode
0	RSVD	0	R/W	Reserved, set to 0 if writing the register

Figure 21:
Interrupt Pin Configuration Register

Addr: 0x22		INTR_PIN_Config		
Bit	Bit Name	Default	Access	Bit Description
7:0	INTR_PIN_Config	0x00	R/W	0x00 = INT pin disabled 0xCA = INT pin enabled

Figure 22:
Interrupt and Polling Clear Register

Addr: 0xF8		INTR_POLL_CLR		
Bit	Bit Name	Default	Access	Bit Description
7:3	RESV	00000	R/W	Reserved, set to 00000 if writing the register
2	CLR	0	R/W	Set to 1 to clear any asserted interrupt pin INT (the interrupt channel ready must be enabled). If the interrupt channel ready is enabled this bit will read a 1.
1:0	RSVD	00	R/W	Reserved, set to 00 if writing the register

Figure 23:
Interrupt and Polling Enable Register

Addr: 0xF9		INT_POLL_EN		
Bit	Bit Name	Default	Access	Bit Description
7:3	RESV	0	R/W	Reserved, set to 00000 if writing the register
2:1	EN	0	R/W	Set to 1 to enable the channel data ready for polling or interrupt.
0	RSVD	0	R/W	Reserved, set to 0 if writing the register

Figure 24:
LED Driver Register

Addr: 0xEA		LED_DRV		
Bit	Bit Name	Default	Access	Bit Description
7:3	RESV	0	R/W	Reserved, set to 00000 if writing the register
2	ON_OFF	0	R/W	Set to 1 to enable the LED_DRV pin to the current level specified by the register GAIN_IDRV (0xB9). Set to 0 to turn off.
0:1	RSVD	0	R/W	Reserved, set to 00 if writing the register

Figure 25:
LED Indicator Register

Addr: 0x84		LED_IND		
Bit	Bit Name	Default	Access	Bit Description
7:4	RESV	0	R/W	Reserved, set to 0 if writing the register
3:2	CURRENT	00	R/W	For LED_IND pin current value (when on). Set to: 'b00=1mA; 'b01=2mA; 'b10=4mA; 'b11=8mA;
1	RSVD	0	R/W	Reserved, set to 0 if writing the register
0	ON_OFF	0	R/W	Set to 1 to enable the LED_DRV pin to the current level specified by the CURRENT bits. Set to 0 to turn off.

Figure 26:
Auto Zero Register

Addr: 0xBA		Auto_Zero		
Bit	Bit Name	Default	Access	Bit Description
7	DONE	0	R/W	Will be set to 1 when any auto zero function is completed. Set to 0 if writing to the register.
6:4	RESV	0	R/W	Reserved, set to 000 if writing the register
3	B440_EN	0	R/W	Set to 1 to manually run auto zero on the B440 channel. Will be automatically set to 0 when DONE bit is set.
2	X_EN	0	R/W	Set to 1 to manually run auto zero on the X channel. Will be automatically set to 0 when DONE bit is set.
1	Y_EN	0	R/W	Set to 1 to manually run auto zero on the Y channel. Will be automatically set to 0 when DONE bit is set.
0	Z_EN	0	R/W	Set to 1 to manually run auto zero on the Z/B490 channel. Will be automatically set to 0 when DONE bit is set.

Temperature Measurement High Register (bits 9:2)

TMP_VALUE is the value from TMPL & TMPH (0xD2 [1:0] and 0xD1 [7:0]) registers (see the Temperature Sensor section of this datasheet). Temperature conversion controlled by the TEMP_Config register.

Figure 27:
Temperature Measurement High Register

Addr: 0xD1		TMPH		
Bit	Bit Name	Default	Access	Bit Description
7:0	TMPH		R	Most significant 8 bits (9:2) of the temperature measurement.

Temperature Measurement Low Register (bits 1:0)

TMP_VALUE is the value from TMPL & TMPH (0xD2 [1:0] and 0xD1 [7:0]) registers (see the Temperature Sensor section of this datasheet). Temperature conversion controlled by the TEMP_Config register.

Figure 28:
Temperature Measurement Low Register

Addr: 0xD2		TMPL		
Bit	Bit Name	Default	Access	Bit Description
7:0	TMPL		R	Least significant 2 bits (1:0) of the temperature measurement.

Figure 29:
Temperature Configure Register

Addr: 0xD3		TEMP_Config		
Bit	Bit Name	Default	Access	Bit Description
7	ISTAT	0	R/W	Will be set to 1 when internal temperature measurement is complete. Set to 0 if writing to the register.
6	RESV	0	R/W	Reserved, set to 0 if writing the register
5	START	0	R/W	Set to 1 to start a temperature conversion cycle. Set to 0 for IDLE state.
4	RESV	0	R/W	Reserved, set to 0 if writing the register
3:0	SRC	0	R/W	Set to 0100 to start a temperature conversion cycle. Set to 0000 for IDLE state.

Figure 30:
Bank Register

Addr: 0xDB		BANK		
Bit	Bit Name	Default	Access	Bit Description
7	BANK	0	R/W	Sets Bank mode for sensor channel selection: 0= Mode 0 for X, Y, D and D sensor data 1= Mode 1 for X, Y, Z and NIR sensor data
6:0	RESV	0	R/W	Reserved, set to 0000000 if writing the register

Figure 31:
Sensor Gain and LED_DRV Current Drive Register

Addr: 0xB9		GAIN_IDRV		
Bit	Bit Name	Default	Access	Bit Description
7:6	IDRV	0	R/W	For LED_DRV pin current limit (when on). Set to: 'b00=100mA; 'b01=50mA; 'b10=25mA; 'b11=12.5mA;
5:2	RESV	0	R/W	Reserved, set to 0000 if writing the register
1:0	GAIN	0	R/W	Sensor channel gain setting (all channels) 'b00=1x; 'b01=3.7x; 'b10=16x; 'b11=64x;

Figure 32:
Integration Time Register

Addr: 0xD9		INT_T		
Bit	Bit Name	Default	Access	Bit Description
7:0	INT_T	0xFF	R/W	Sets sensor integration time Integration time = (256 - value) * 2.8ms