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AS7265x

Smart 18-Channel VIS to NIR Spectral_ID 3-Sensor Chipset with Electronic Shutter

General Description

The AS7265x chipset consists of three sensor devices AS72651 with master capability, AS72652 and AS72653. The multispectral sensors can be used for spectral identification in a range from visible to NIR. Every of the three sensor devices has 6 independent on-device optical filters whose spectral response is defined in a range from 410nm to 940nm with FWHM of 20nm. The AS72651, combined with the AS72652 (spectral response from 560nm to 940nm) and the AS72653 (spectral response from 410nm to 535nm) form an AS7265x 18-channel multi-spectral sensor chip-set. Using the AS7265x chipset requires the use of firmware. It must be loaded into a serial flash via a UART interface. The list of **ams** tested serial flash memories can be found in Figure 56. The components AS72651, AS72652 and AS72653 are pre-calibrated with a specific light source. The information about the conditions of the performed calibration (for example light source, gain, integration time) can be found in the table of optical characteristics of the respective component. Any operation other than these conditions might require a new calibration in the application.

Each AS7265x device has two integrated LED drivers with programmable current and can be timed for electronic shutter applications.

The device family integrates Gaussian filters into standard CMOS silicon via nano-optic deposited interference filter technology in LGA packages that also provide built-in apertures to control the light entering the sensor array.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS7265x, Smart 18-Channel VIS to NIR Spectral_ID 3-Sensor Chipset with Electronic Shutter are listed below:

Figure 1:
AS7265x Chip-Set Benefits and Features

Benefits	Features
• Compact 18-channel spectrometry chip-set solution	• 3 chip set including master device delivering 18 visible and NIR channels from 410nm to 940nm each with 20nm FWHM
	• UART or I^2C slave digital Interface
	• Visible filter set realized by silicon interference filters
• No additional signal conditioning required	• 16-bit ADC with digital access
	• Programmable LED drivers
	• 2.7V to 3.6V with I^2C interface
• Small, robust package, with built-in aperture	• 20-pin LGA package 4.5mm x 4.7mm x 2.5mm -40°C to 85°C temperature range

Applications

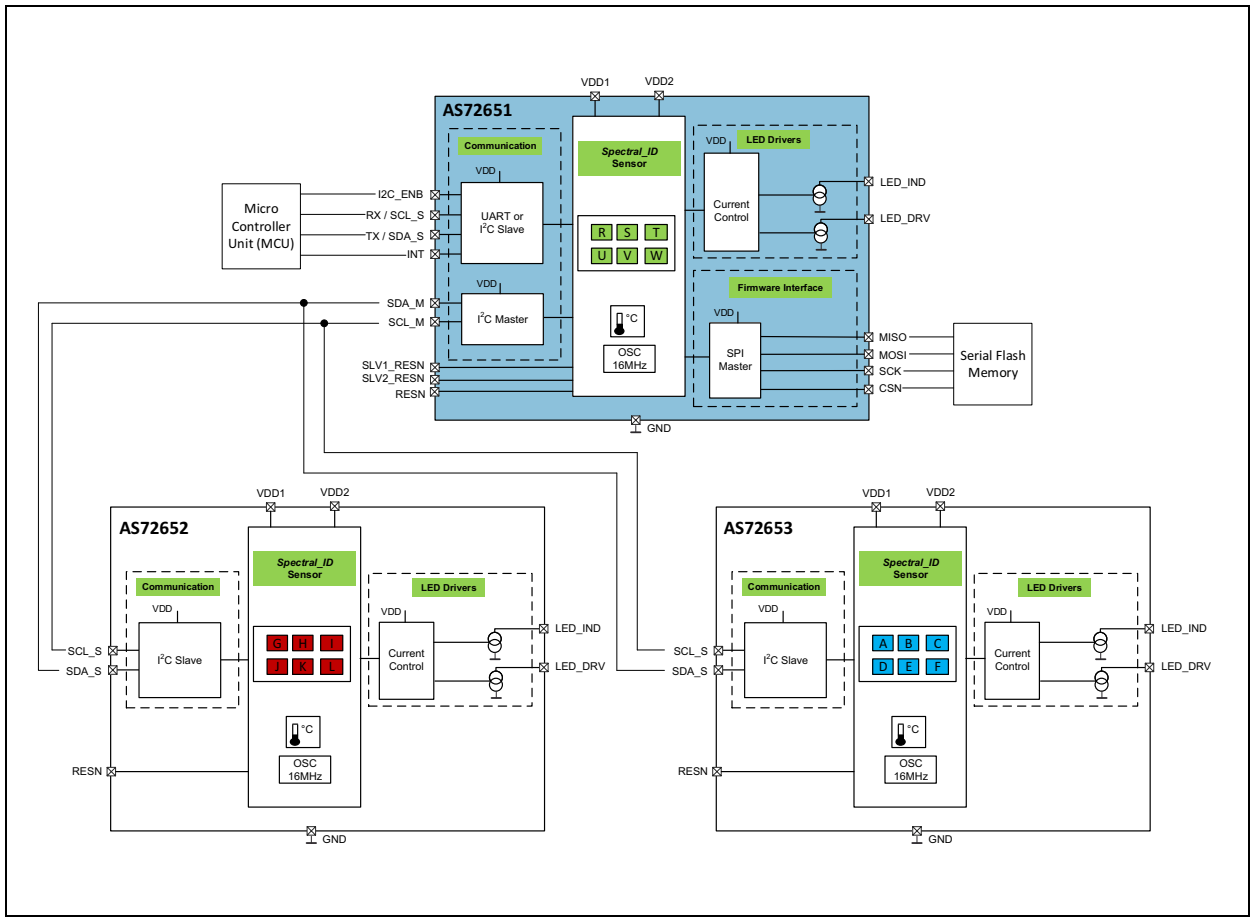
The AS7265x applications include:

- Product/Brand authentication
- Anti-counterfeiting
- Portable spectroscopy
- Product safety/adulteration detection
- Horticultural and specialty lighting
- Material analysis

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS7265x Chip-Set Block Diagram



Note(s):

1. Refer to the Application Diagram in Figure 60.

Pin Assignments

The device pin assignments are described below.

Figure 3:
Pin Diagram of AS7265x (Top View)

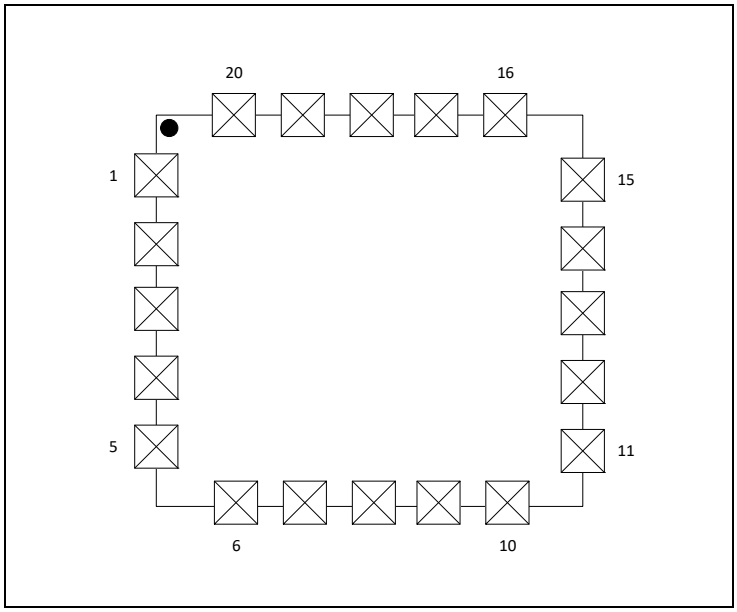


Figure 4:
AS72651 Pin Description

Pin No.	Pin Name	Pin Type	Description
1	SLV1_RESN	Digital Input and Output	Reset pin for Slave 1 e.g. AS72652, active low
2	RESN	Digital Input	Reset pin, active low (with internal pull-up to VDD)
3	SCK	Digital Output	SPI serial clock
4	MOSI	Digital Input and Output	SPI MOSI
5	MISO	Digital Input and Output	SPI MISO
6	CSN	Digital Output	Chip select for external flash
7	NC		Not functional, no connect
8	I2C_ENB	Digital Input	Selects UART (low) or I^2C (high) operation
9	SCL_M	Digital Output	I^2C master clock for communication with AS72652 and AS72653
10	SDA_M	Digital Input and Output	I^2C master data for communication with AS72652 and AS72653

Pin No.	Pin Name	Pin Type	Description
11	RX / SCL_S	Digital Input and Output	RX (UART) or SCL_S (I^2C slave) depending on I2C_ENB setting
12	TX / SDA_S	Digital Input and Output	TX (UART) or SDA_S (I^2C slave) depending on I2C_ENB setting
13	INT	Digital Output	INT is active low
14	VDD2	Voltage Supply	Voltage supply
15	LED_DRV	Analog Output	LED driver output for driver LED, current sink
16	GND	Supply	Ground
17	VDD1	Voltage Supply	Voltage supply
18	LED_IND	Analog Output	LED driver output for indicator LED, current sink
19	NC		Not functional, no connect
20	SLV2_RESN	Digital Output	Reset pin for slave 2 e.g. AS72653, active low

Note(s):

1. Pin out is valid for firmware versions from 11 and later.

Figure 5:
AS72652 and AS72653 Pin Description

Pin No.	Pin Name	Pin Type	Description
1	NC		Not functional, no connect
2	RESN	Digital Input	Reset pin, active low (with internal pull-up to VDD)
3	NC		Not functional, no connect
4	NC		Not functional, no connect
5	NC		Not functional, no connect
6	NC		Not functional, no connect
7	NC		Not functional, no connect
8	NC		Not functional, no connect
9	SCL_S	Digital Input and Output	I^2C slave clock for communication with master AS72651
10	SDA_S	Digital Input and Output	I^2C slave data for communication with master AS72651

Pin No.	Pin Name	Pin Type	Description
11	NC		Not functional, no connect
12	NC		Not functional, no connect
13	INT	Digital Output	INT is active low
14	VDD2	Voltage Supply	Voltage supply
15	LED_DRV	Analog Output	LED driver output for driver LED, current sink
16	GND	Supply	Ground
17	VDD1	Voltage Supply	Voltage supply
18	LED_IND	Analog Output	LED driver output for indicator LED, current sink
19	NC		Not functional, no connect
20	NC		Not functional, no connect

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings of AS7265x may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device is not designed for high energy UV (ultraviolet) environments, including upward looking outdoor applications, which could affect long term optical performance.

Figure 6:
Absolute Maximum Ratings of AS7265x

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{DD1_MAX}	Supply Voltage VDD1	-0.3	5	V	Pin VDD1 to GND
V_{DD2_MAX}	Supply Voltage VDD2	-0.3	5	V	Pin VDD2 to GND
V_{DD_IO}	Input/Output Pin Voltage	-0.3	VDD+0.3	V	Input/Output Pin to GND
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JESD78D
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±1000		V	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM	±500		V	JESD22-C101F
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a 168 hour max. floor lifetime

Electrical Characteristics

All limits are guaranteed with VDD = VDD1 = VDD2 = 3.3V, T_{AMB} = 25°C. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

VDD1 and VDD2 should be sourced from the same power supply output.

Figure 7:
Electrical Characteristics of AS7265x

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General Operating Conditions						
VDD1 /VDD2	Voltage Operating Supply	UART Interface	2.97	3.3	3.6	V
VDD1 /VDD2	Voltage Operating Supply	I^2C Interface	2.7	3.3	3.6	V
T_{AMB}	Operating Temperature		-40	25	85	°C
I_{VDD}	Operating Current				5	mA
Internal RC Oscillator						
F_{OSC}	Internal RC Oscillator Frequency		15.7	16	16.3	MHz
t_{JITTER} (1)	Internal Clock Jitter	@25°C			1.2	ns
Temperature Sensor						
D_{TEMP}	Absolute Accuracy of the Internal Temperature Measurement		-8.5		8.5	°C
Indicator LED						
I_{IND}	LED Current		1		8	mA
I_{ACC}	Accuracy of Current		-30		30	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V
LED_DRV						
I_{LED1}	LED Current		12.5		100	mA
I_{ACC}	Accuracy of Current		-10		10	%
V_{LED}	Voltage Range of Connected LED	Vds of current sink	0.3		VDD	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital Inputs and Outputs						
I_{IH}, I_{IL}	Logic Input Current	Vin=0V or VDD	-1		1	µA
V_{IH}	CMOS Logic High Input		0.7* VDD		VDD	V
V_{IL}	CMOS Logic Low Input		0		0.3* VDD	V
V_{OH}	CMOS Logic High Output	I=1mA			VDD-0.4	V
V_{OL}	CMOS Logic Low Output	I=1mA			0.4	V
t_{RISE} (1)	Current Rise Time	C(Pad)=30pF			5	ns
t_{FALL} (1)	Current Fall Time	C(Pad)=30pF			5	ns

Note(s):

1. Guaranteed by design, not tested in production.

Timing Characteristics

Figure 8:
AS7265x I²C Slave Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C Interface						
f_{SCLK}	SCL Clock Frequency		0		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START		1.3			µs
$t_{HS:STA}$	Hold Time (Repeated) START		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START		0.6			µs
$t_{HS:DAT}$	Data Hold Time		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time		100			ns
t_R	Rise Time of Both SDA and SCL		20		300	ns
t_F	Fall Time of Both SDA and SCL		20		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	CB - total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

Figure 9:
I²C Slave Timing Diagram

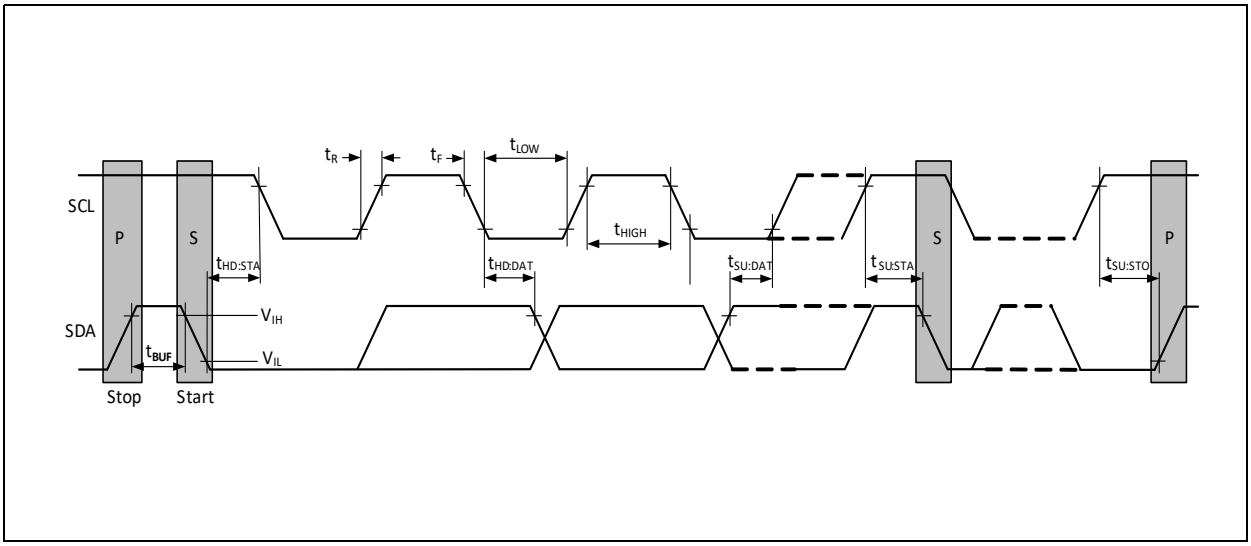


Figure 10:
AS72651 SPI Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI Interface						
f_{SCK}	Clock Frequency		0		16	MHz
t_{SCK_H}	Clock High Time		40			ns
t_{SCK_L}	Clock Low Time		40			ns
t_{SCK_RISE}	SCK Rise Time		5			ns
t_{SCK_FALL}	SCK Fall Time		5			ns
t_{CSN_S}	CSN Setup Time	Time between CSN high-low transition to first SCK high transition	50			ns
t_{CSN_H}	CSN Hold Time	Time between last SCK falling edge and CSN low-high transition	100			ns
t_{CSN_DIS}	CSN Disable Time		100			ns
t_{DO_S}	Data-Out Setup Time		5			ns
t_{DO_H}	Data-Out Hold Time		5			ns
t_{DI_V}	Data-In Valid		10			ns

Figure 11:
SPI Master Write Timing Diagram

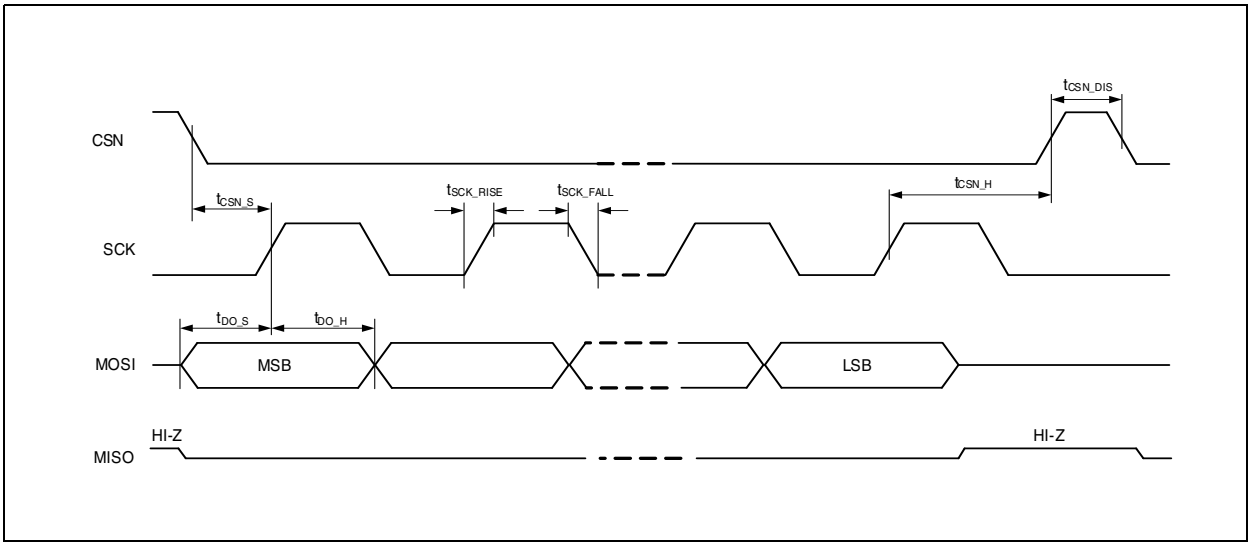
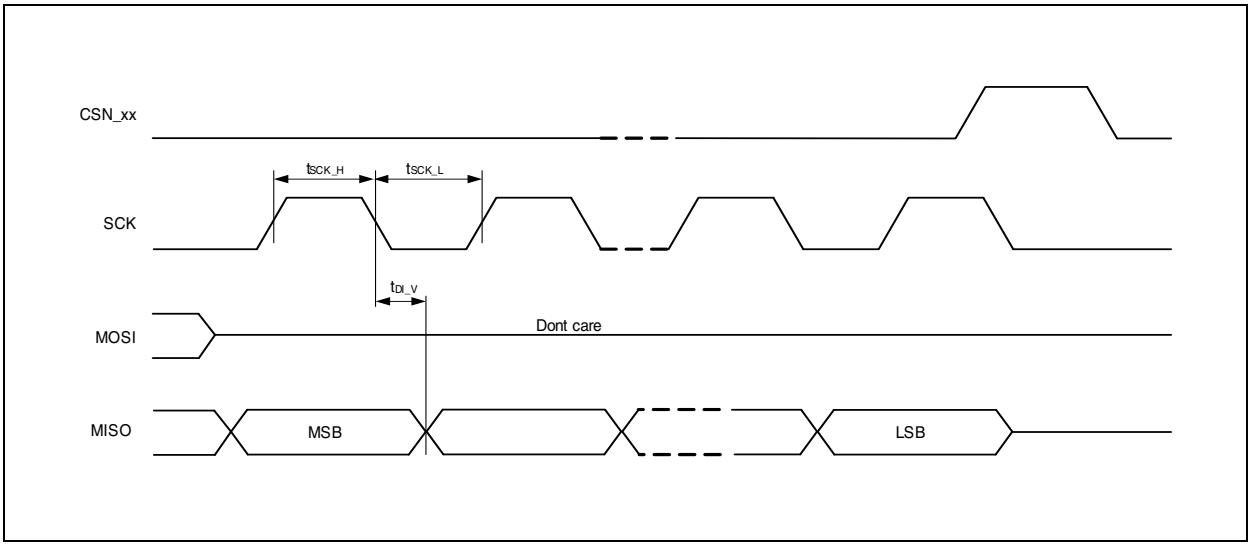


Figure 12:
SPI Master Read Timing Diagram



Typical Operating Characteristics

Optical Characteristics

All optical characteristics are optimized for diffused light. When using a point light source or collimated light on the sensor, the sensor opening must be covered by a lambertian diffuser with achromatic characteristics. Diffusor of Tsujiden like D121UP have been successfully tested at **ams**. If in the application diffused light, e.g. used by a reflective surface, no additional diffuser is required.

Figure 13:
AS7265x LGA Average Field of View

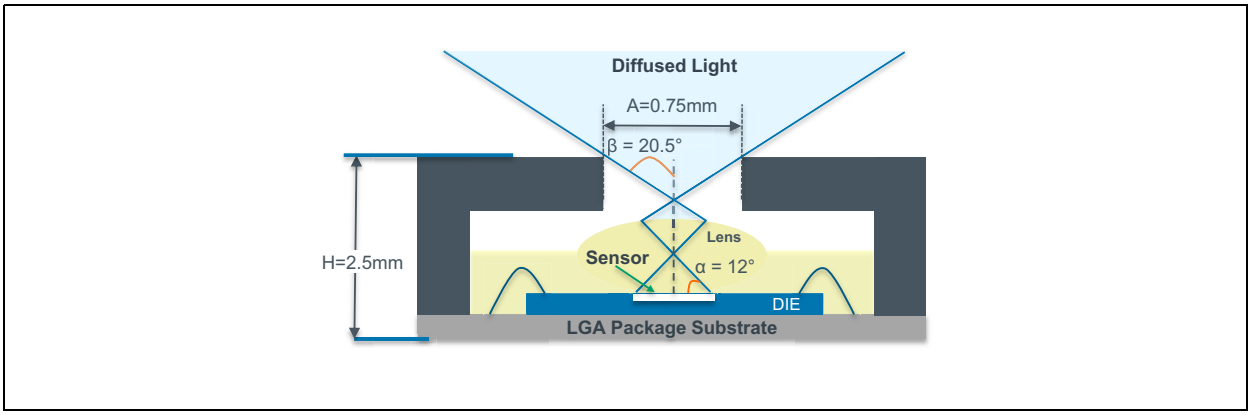


Figure 14:
AS7265x 18-Channel Spectral Responsivity

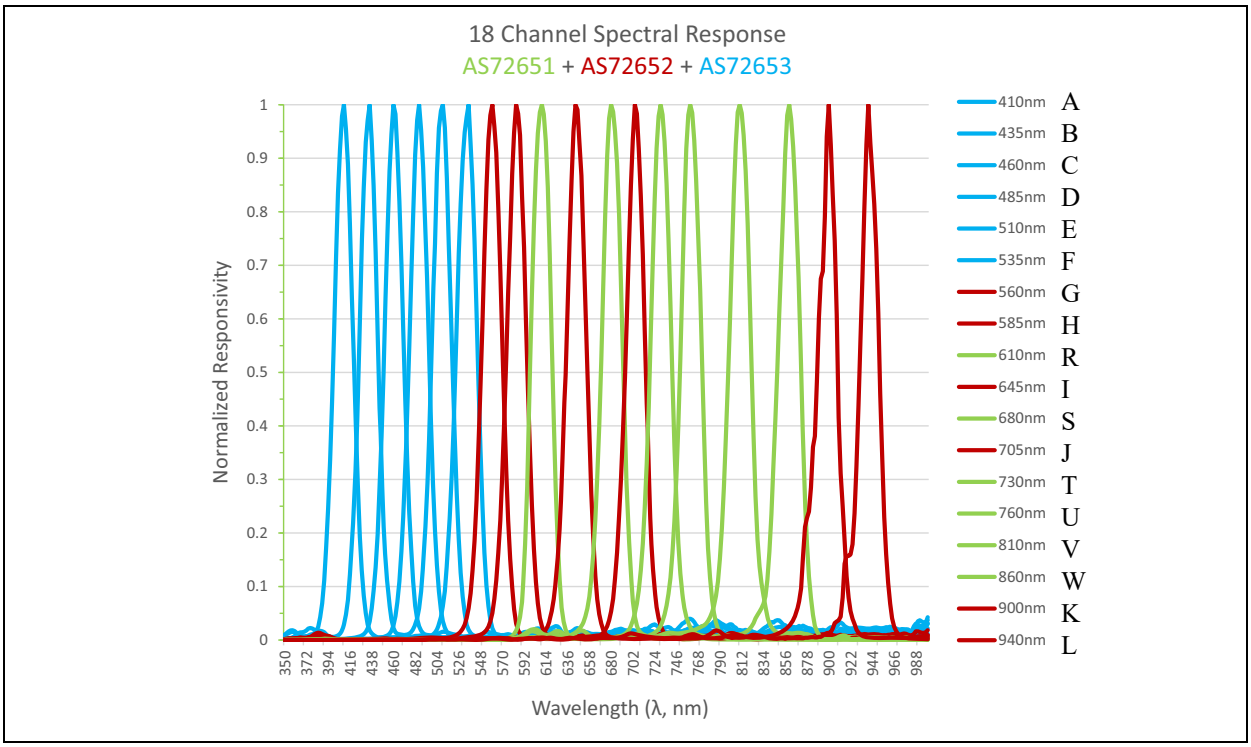


Figure 15:
AS72651 Spectral Responsivity

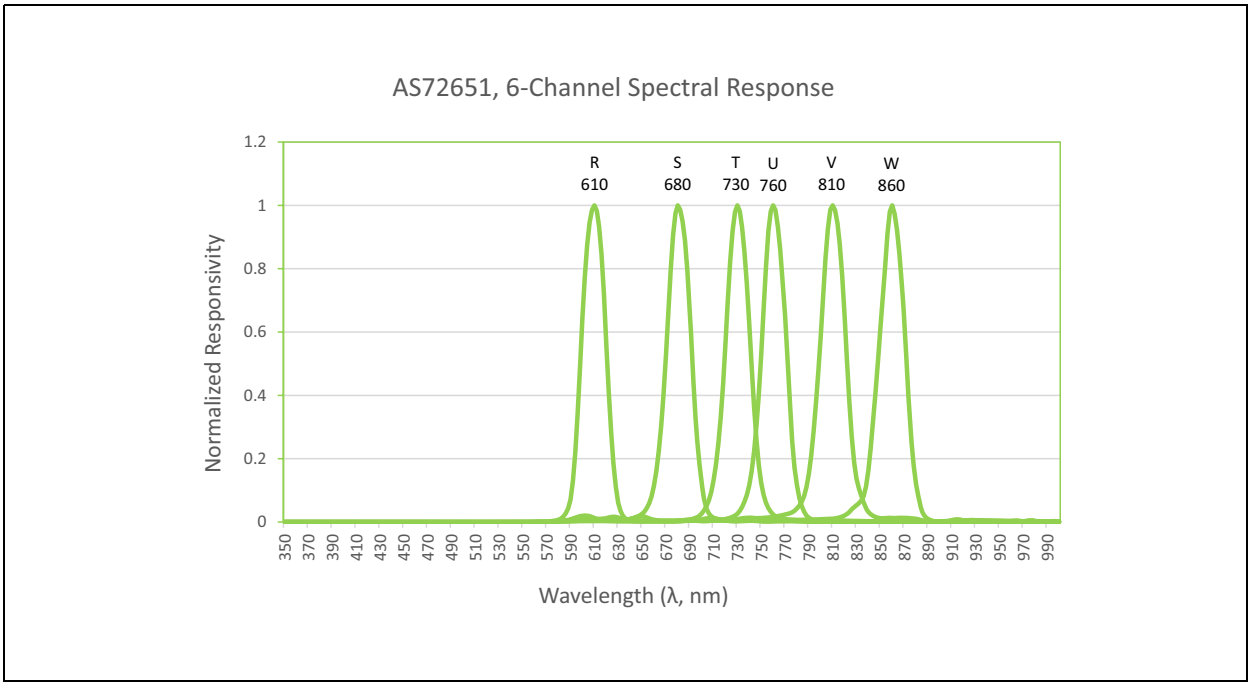


Figure 16:
Optical Characteristics of AS72651 (Pass Band) (1)

Symbol	Parameter	Test Conditions	Channel (nm)	Min	Typ	Max	Unit
R	Channel R	Incandescent(2),(4)	610		35(3),(4)		counts/ (µW/cm^2)
S	Channel S	Incandescent(2),(4)	680		35(3),(4)		counts/ (µW/cm^2)
T	Channel T	Incandescent(2),(4)	730		35(3),(4)		counts/ (µW/cm^2)
U	Channel U	Incandescent(2),(4)	760		35(3),(4)		counts/ (µW/cm^2)
V	Channel V	Incandescent(2),(4)	810		35(3),(4)		counts/ (µW/cm^2)
W	Channel W	Incandescent(2),(4)	860		35(3),(4)		counts/ (µW/cm^2)
FWHM	Full Width Half Max				20		nm
Wacc	Wavelength Accuracy			+10		-10	nm

Symbol	Parameter	Test Conditions	Channel (nm)	Min	Typ	Max	Unit
dark	Dark Channel Counts	GAIN=64, T_{AMB}=25°C t_{int}=165ms				5	counts
AFOV	Average Field of View				±20.5		deg

Note(s):

1. Calibration and measurements are made using diffused light.
2. Each channel is tested with GAIN = 16x, Integration Time (INT_T) = 166ms and VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C.
3. The accuracy of the channel counts/µW/cm^2 is ±12%.
4. The light source is an incandescent light with an irradiance of ~1500µW/cm^2 (300-1000nm).

Figure 17:
AS72652 Spectral Responsivity

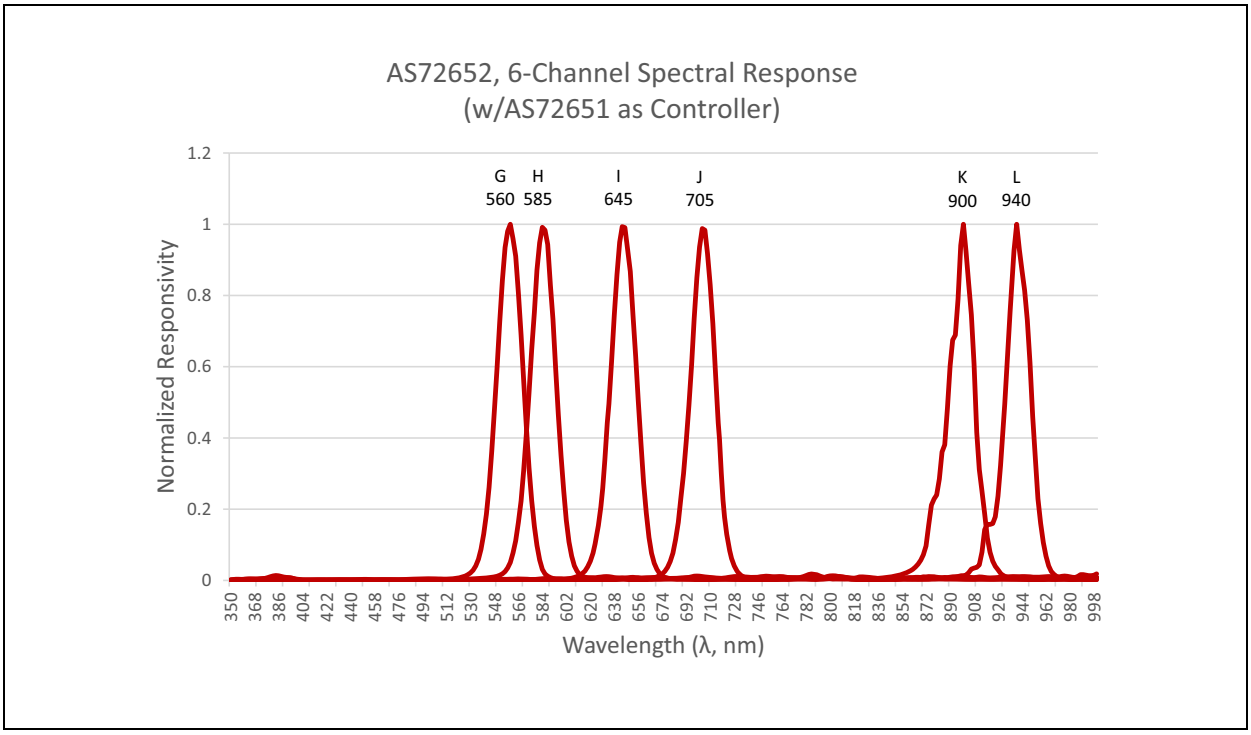


Figure 18:
Optical Characteristics of AS72652 (Pass Band) (1)

Symbol	Parameter	Conditions	Channel (nm)	Min	Typ	Max	Unit
G	Channel G	3300K White LED(2)	560		35(3)		counts/ ($\mu W/cm^2$)
H	Channel H	3300K White LED(2)	585		35(3)		counts/ ($\mu W/cm^2$)
I	Channel I	3300K White LED(2)	645		35(3)		counts/ ($\mu W/cm^2$)
J	Channel J	3300K White LED(2)	705		35(3)		counts/ ($\mu W/cm^2$)
K	Channel K	Incandescent(2)	900		35(3)		counts/ ($\mu W/cm^2$)
L	Channel L	940nm LED(2)	940		35(3)		counts/ ($\mu W/cm^2$)
FWHM	Full Width Half Max				20		nm
Wacc	Wavelength Accuracy			-10		+10	nm
dark	Dark Channel Counts	GAIN=64, T_{AMB}=25°C t_{int} = 165ms				5	counts
AFOV	Average Field of View				±20.5		deg

Note(s):

1. Calibration and measurements are made using diffused light.
2. Each channel is tested with GAIN = 16x, Integration Time (INT_T) = 166ms and VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C.
3. The accuracy of the channel counts/$\mu W/cm^2$ is ±12%.

Figure 19:
AS72653 Spectral Responsivity

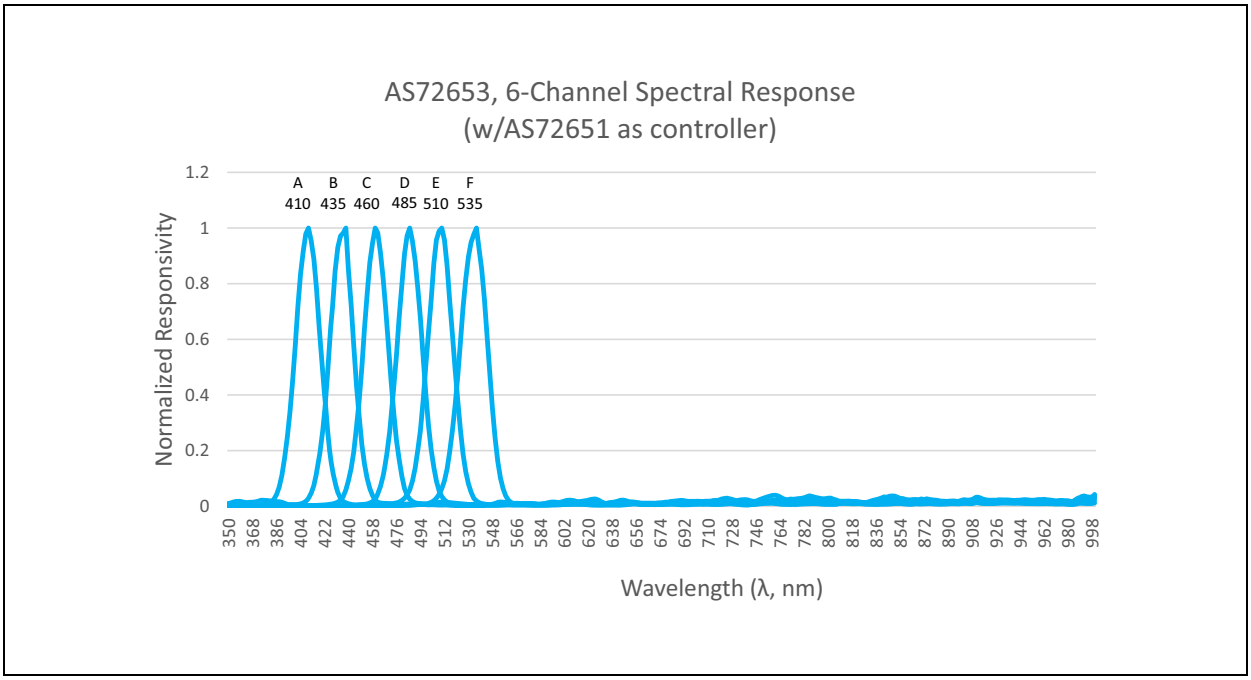


Figure 20:
Optical Characteristics of AS72653 (Pass Band)(1)

Symbol	Parameter	Conditions	Channel (nm)	Min	Typ	Max	Unit
A	Channel A	LED:(2) 395nm 415nm 428nm 5600K white	410		35(3)		counts/ (µW/cm^2)
B	Channel B		435		35(3)		counts/ (µW/cm^2)
C	Channel C		460		35(3)		counts/ (µW/cm^2)
D	Channel D		485		35(3)		counts/ (µW/cm^2)
E	Channel E		510		35(3)		counts/ (µW/cm^2)
F	Channel F		535		35(3)		counts/ (µW/cm^2)
FWHM	Full Width Half Max				20		nm
Wacc	Wavelength Accuracy			-10		+10	nm
dark	Dark Channel Counts	GAIN=64, T_{AMB}=25°C t_{int} = 165ms				5	counts
AFOV	Average Field of View				±20.5		deg

Note(s):

1. Calibration and measurements are made using diffused light.
2. Each channel is tested with GAIN = 16x, Integration Time (INT_T) = 166ms and VDD = VDD1 = VDD2 = 3.3V, T_{AMB}=25°C.
3. The accuracy of the channel counts/µW/cm^2 is ±12%.

Detailed Description

AS7265x 18-Channel *Spectral_ID* Detector Overview

Each of the three AS7265x *Spectral_ID* devices are next-generation digital 6-channel spectral sensor devices. Each of the 6 channels has a Gaussian filter characteristic with a full width half maximum (FWHM) bandwidth of 20nm. The filters use an interference topology design providing high stability in terms of drift in time and temperature. The drifts are so small that it is undetectable in the measurement. The temperature drift of the device is largely determined by the drift of the sensor and the electronics. To compensate for the temperature drift in the application, every device of the AS7265x chipset includes an integrated temperature sensor.

Filter accuracy will be affected by the angle of incidence which itself is limited by integrated aperture and internal micro-lens structure. The aperture-limited average field of view is ±20.5° to deliver specified accuracy. All optical characteristics are optimized for using diffused light.

Each device contains an analog-to-digital converter (16-bit resolution ADC) which integrates the current from each channel's photodiode. Upon completion of the conversion cycle, the integrated result is transferred to the corresponding data registers. The transfers are double-buffered to ensure data integrity is maintained.

The external MCU interface control via I^2C registers or AT commands, transparently controls the AS72652 and/or AS72653.

A serial flash is a required operating companion for this device and enables factory calibration/normalization of the filters. Supported device types are noted in Ordering & Contact Information at the end of this document. Required operating code can be downloaded at download.ams.com.

Channel Data Conversion of the AS7265x Devices

All three of these 6 channel devices use conversion implemented via two photodiode banks in each device. Refer to Figure 21and Figure 22. Bank 1 consists of register data from 4 of the 6 photodiodes, with 2 registers zeroed and Bank 2 consists of data from a different set of 4 of the 6 photodiodes, with 2 different registers zeroed. Spectral conversion requires the integration time (IT in ms) set to complete. If both photodiode banks are required to complete the conversion, the 2^{nd} bank requires an additional IT ms. Minimum IT for a single bank conversion is 2.8 ms. If data is required from all 6 photodiodes then the device must perform 2 full conversions (2 x Integration Time).

This spectral data conversion process operates continuously, new data is available after each IT ms period.

The conversion process is controlled with BANK Mode settings in the AS72651 as follows:

BANK Mode 0 Registers:

AS72651 data will be in S, T, U & V registers (R & W will be zero)

AS72652 data will be in G, H, K & I registers (J & L will be zero)

AS72653 data will be in A, B, E & C registers (D & F will be zero)

BANK Mode 1 Registers:

AS72651 data will be in R, T, U & W registers (S & V will be zero)

AS72652 data will be in G, H, J & L registers (I & K will be zero)

AS72653 data will be in F, A, B & D registers (C & E will be zero)

BANK Mode 2 Registers:

AS72651 data will be in S, T, U, V, R & W registers

AS72652 data will be in G, H, K, I, J & L registers

AS72653 data will be in A, B, C, D, E & F registers

For BANK Mode 2, care should be taken to assure prompt interrupt servicing so integration values from both banks are all derived from the same spectral conversion cycle.

Figure 21:
AS7265x Photo Diode Arrays

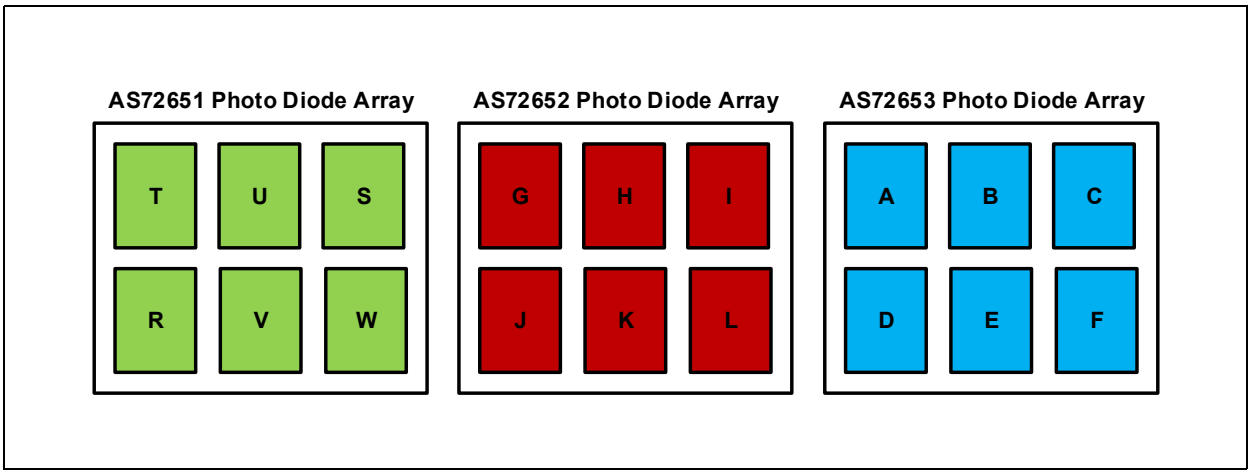
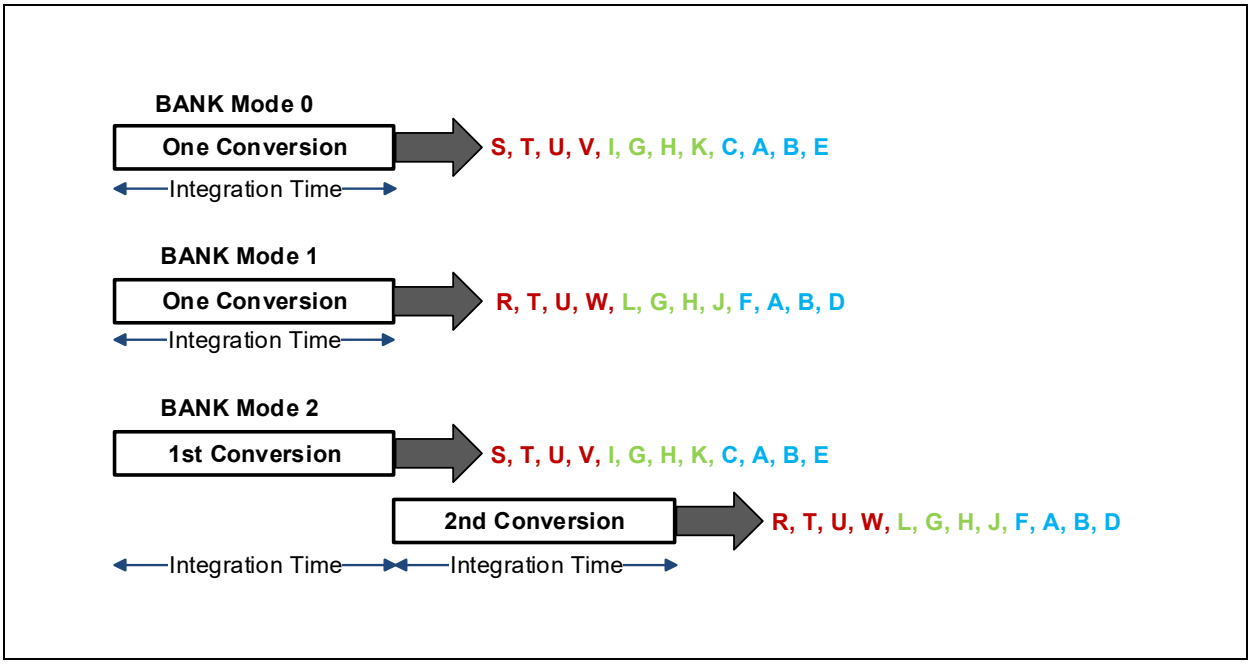


Figure 22:
Bank Mode and Data Conversion



RC Oscillator

The timing generation circuit consists of on-chip 16MHz, temperature compensated oscillators, which provide the individual master clocks of the AS7625x devices

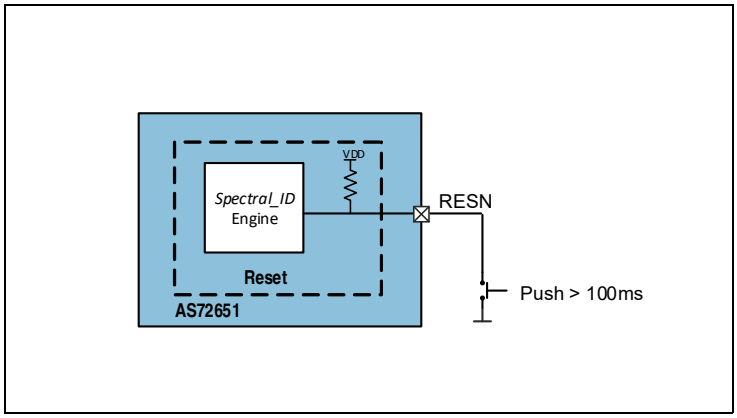
Temperature Sensor

The AS7265x internal temperature sensors are constantly measuring on-chip temperature to enable temperature compensation procedures, and can be read via I^2C registers or AT commands in the AS72651.

Reset

Pulling down the RESN pin for longer than 100ms resets the AS72651 which proceed to reset the AS72562 and the same RESN signal shown below can be used directly to reset the AS72653.

Figure 23:
Reset Circuit



AS7265x LED_IND Controls

There are LED_IND pins on all AS7265x devices. An LED connected to LED_IND can be used as a general power indicator and will automatically be used to indicate a Flash firmware update is occurring.

The LED_IND can then be setup as needed. Each AS7265x LED_IND source can be turned on/off via AT commands or I^2C register control, and LED_IND sink current is programmable to 1mA, 2mA, 4mA or 8mA. This LED_IND control can also be used in applications just like the LED_DRV control (described below), if the lower current sink of the LED_IND control is appropriate.

Electronic Shutter with AS7265x LED_DRV Driver Control

There are LED_DRV pins on all AS7265x devices. The LED_DRV pin can be used to control external LED sources as needed for sensor applications. LED_DRV can sink a programmable current of 12.5mA, 25mA, 50mA or 100mA. The control can be turned on/off via I^2C registers or AT commands, and as such it provides the AS7265x device with an electronic shutter.

Interrupt Operation

Interrupt operation is only needed for AS72651 as it transparently controls data collection from the AS72652 (if used) or AS72653 (if used).

If BANK is set in the AS72651 to Mode 0 or Mode 1, data is ready after the 1st integration time. If BANK is set to Mode 2, data is ready after two integration times.

For interrupt operation using I²C registers, if interrupts are enabled and data is ready, the INT pin is set low and DATA_RDY is set to 1. Reading the raw or calibration data releases (returns high) the interrupt. For multi-byte sensor data (2 or 4 bytes), after the 1st byte is read the remaining bytes are shadow protected in case an integration cycle completes just after the 1st byte is read. The sensors continue to gather information at the rate of the integration time, hence if the sensor registers are not read when the interrupt line goes low, it will stay low and the next cycle's sensor data will be available in the registers at the end of the next integration cycle.

For interrupt operation using AT Commands, if interrupts are enabled and data is ready the INT pin is set low and is released (returns high) after any sensor data is read.

Required Flash Memory

Serial flash is a required operating companion for this device, and enables the I²C and UART interfaces, as well as enabling calibrated data results. Supported device types are noted in Ordering & Contact Information at the end of this document. Required operating code can be downloaded at download.ams.com.

I²C Slave Interface

If selected by the I2C_ENB pin setting, interface and control can be accomplished through an I²C compatible slave interface to a set of registers that provide access to device control functions and output data. These registers on the AS72651 are, in reality, implemented as *virtual* registers in software. The actual I²C slave hardware registers number only three and are described in the table below. The steps necessary to access the virtual registers defined in the following are explained in pseudocode for external I²C master writes and reads below.

I²C Feature List

- Fast mode (400kHz).
- 7+1-bit addressing mode.
- Write format: Byte.
- Read format: Byte.
- SDA input delay and SCL spike filtering by integrated RC-components.

Figure 24:
I²C Slave Device Address and Physical Registers

Entity	Description	Note
Device Slave Address	8-bit slave address	Byte = 1001001x (device address = 49 hex) • x= 1 for Master Read (byte = 93 hex) • x= 0 for Master Write (byte = 92 hex)
STATUS Register	I²C slave interface STATUS register. Read-only.	Register Address = 0x00 Bit 1: TX_VALID • 0 - New data may be written to WRITE register • 1 -WRITE register occupied. Do NOT write. Bit 0: RX_VALID • 0 -No data is ready to be read in READ register. • 1 -Data byte available in READ register.
WRITE Register	I²C slave interface WRITE register. Write-only.	Register Address = 0x01 • 8-Bits of data written by the I²C Master intended for receipt by the I²C slave. Used for both *virtual* register addresses and write data.
READ Register	I²C slave interface READ register. Read-only.	Register Address = 0x02 • 8-Bits of data to be read by the I²C Master.

I²C Virtual Register Write Access

I²C Virtual Resister Byte Write, detailed below, shows the pseudocode necessary to write virtual registers on the AS72651. Note that, because the actual registers of interest are realized as virtual registers, a means of indicating whether there is a pending read or write operation of a given virtual register is needed. To convey this information, the most significant bit of the virtual register address is used as a marker. If it is 1, then a write is pending, otherwise the slave is expecting a virtual read operation. The pseudocode illustrates the proper technique for polling of the I²C slave status register to ensure the slave is ready for each transaction.

I²C Virtual Register Byte Write

Pseudocode

Poll I²C slave STATUS register;

If TX_VALID bit is 0, a write can be performed on the interface;

Send a virtual register address and set the MSB of the register address to 1 to indicate the pending write;

Poll I²C slave STATUS register;

If TX_VALID bit is 0, the virtual register address for the write has been received and the data may now be written;

Write the data.

Sample Code:

```
#define I2C_AS72XX_SLAVE_STATUS_REG     0x00
#define I2C_AS72XX_SLAVE_WRITE_REG      0x01
#define I2C_AS72XX_SLAVE_READ_REG       0x02
#define I2C_AS72XX_SLAVE_TX_VALID       0x02
#define I2C_AS72XX_SLAVE_RX_VALID       0x01

void i2cm_AS72xx_write(uint8_t virtualReg, uint8_t d)
{
        volatile uint8_tstatus;

        while (1)
        {
                // Read slave I2C status to see if the write buffer is ready.
                status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG);

                if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                        // No inbound TX pending at slave.  Okay to write now.
                        break ;
        }
        // Send the virtual register address (enabling bit 7 to indicate a write).
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, (virtualReg | 0x80)) ;

        while (1)
        {
                // Read the slave I2C status to see if the write buffer is ready.
                status = i2cm_read(I2C_AS72XX_SLAVE_STATUS_REG) ;

                if ((status & I2C_AS72XX_SLAVE_TX_VALID) == 0)
                        // No inbound TX pending at slave.  Okay to write data now.
                        break ;
        }
        // Send the data to complete the operation.
        i2cm_write(I2C_AS72XX_SLAVE_WRITE_REG, d) ;
}
```

I²C Virtual Register Read access