

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China









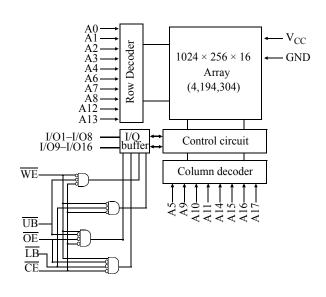
5.0 V 256 K × 16 CMOS SRAM

Features

- Pin compatible with AS7C4098
- Industrial and commercial temperature
- Organization: 262,144 words × 16 bits
- Center power and ground pins
- High speed
 - 10/12/15/20 ns address access time
 - 5/6 ns output enable access time
- Low power consumption: ACTIVE
 - 990mW/max @ 10 ns
- Low power consumption: STANDBY
- 55mW/max CMOS
- Individual byte read/write controls

- Easy memory expansion with \overline{CE} , \overline{OE} inputs
- TTL- and CMOS-compatible, three-state I/O
- 44-pin JEDEC standard packages
- 400-mil SOJ
- TSOP 2
- ESD protection \geq 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement for SOJ and TSOP 2

44-pin (400 mil) SOJ TSOP2

| A0 | 44 A17 43 A16 42 A15 41 OE 40 UB 39 LB 38 I/O16 37 I/O15 36 I/O15 36 I/O14 35 I/O13 34 GND 33 VCC 32 I/O12 31 I/O10 29 I/O9 28 NC 27 A14 26 A13 25 A12 24 A11 23 A10 |
|----|--|
|----|--|

Selection guide

| | -10 | -12 | -15 | -20 | Unit |
|-----------------------------------|-----|-----|-----|-----|------|
| Maximum address access time | 10 | 12 | 15 | 20 | ns |
| Maximum output enable access time | 5 | 6 | 6 | 6 | ns |
| Maximum operating current | 180 | 160 | 140 | 120 | mA |
| Maximum CMOS standby current | 10 | 10 | 10 | 10 | mA |



Functional description

The AS7C4098A is a high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 262,144 words × 16 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5/6 ns are ideal for high-performance applications. The chip enable input \overline{CE} permits easy memory expansion with multiple-bank memory systems.

When \overline{CE} is high the device enters standby mode. The device is guaranteed not to exceed 55mW power consumption in CMOS standby mode. A write cycle is accomplished by asserting write enable (\overline{WE}) and chip enable (\overline{CE}). Data on the input pins I/O1–I/O16 is written on the rising edge of \overline{WE} (write cycle 1) or \overline{CE} (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable (\overline{OE}) or write enable (\overline{WE}).

A read cycle is accomplished by asserting output enable (\overline{OE}) and chip enable (\overline{CE}) , with write enable (\overline{WE}) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

The device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. \overline{LB} controls the lower bits, I/O1–I/O8, and \overline{UB} controls the higher bits, I/O9–I/O16.

All chip inputs and outputs are TTL- and CMOS-compatible, and operation is for 5.0V (AS7C4098A) supply. The device is available in the JEDEC standard 400-mL, 44-pin SOJ, TSOP 2 packages.

Absolute maximum ratings

| Parameter | Symbol | Min | Max | Unit |
|--|-------------------|-------|-----------------------|------|
| Voltage on V _{CC} relative to GND | V _{t1} | -0.50 | +7.0 | V |
| Voltage on any pin relative to GND | V _{t2} | -0.50 | V _{CC} +0.50 | V |
| Power dissipation | P_{D} | _ | 1.5 | W |
| Storage temperature (plastic) | T _{stg} | -65 | +150 | °C |
| Ambient temperature with V _{CC} applied | T _{bias} | -55 | +125 | °C |
| DC current into outputs (low) | I _{OUT} | - | ±20 | mA |

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

| Truth table | | | | | | | |
|-------------|----|---------------|----|---------------|------------------|------------------|---|
| CE | WE | OE | LB | UB | I/O1–I/O8 | I/O9–I/O16 | Mode |
| Н | X | X | X | X | High Z | High Z | Standby (I _{SB} , I _{SB1}) |
| L | Н | Н | X | X | High Z | High 7 | Outmut disable (I) |
| L | X | X | Н | Н | rigii Z | High Z | Output disable (I _{CC}) |
| | | | L | Н | D _{OUT} | High Z | |
| L | Н | L | Н | L | High Z | D _{OUT} | Read (I _{CC}) |
| | | | L | L | D _{OUT} | D _{OUT} | |
| | | | L | Н | D_{IN} | High Z | |
| L | L | X | Н | L | High Z | D _{IN} | |
| | | | L | L | D _{IN} | D _{IN} | Write (I _{CC}) |

Key: X = Don't care, L = Low, H = High.



Recommended operating conditions

| Parameter | Symbol | Min | Typical | Max | Unit | |
|-------------------------------|-------------------------------|------------------|---------|----------------|------|----|
| Supply voltage | V _{CC} (10/12/15/20) | 4.5 | 5.0 | 5.5 | V | |
| Input voltage | V _{IH} * | 2.2 | _ | $V_{CC} + 0.5$ | V | |
| input voltage | Input voltage | | | _ | 0.8 | V |
| Ambient operating temperature | commercial | $T_{\mathbf{A}}$ | 0 | _ | 70 | °C |
| Ambient operating temperature | industrial | $T_{\mathbf{A}}$ | -40 | _ | 85 | °C |

 $V_{IH} = V_{CC} + 1.5V$ for pulse width less than 5 nS.

DC operating characteristics (over the operating range)¹

| | | | -1 | -10 | | -12 | | 15 | -20 | | | |
|--------------------------------|-----------------|---|-----|-----|-----|-----|-----|-----|-----|-----|------|-------|
| Parameter | Symbol | Test conditions | Min | Max | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Input leakage current | $ I_{LI} $ | $V_{CC} = Max$ $V_{IN} = GND \text{ to } V_{CC}$ | _ | 1 | _ | 1 | 1 | 1 | _ | 1 | μА | |
| Output leakage current | $ I_{LO} $ | $V_{CC} = Max$ $\overline{CE} = V_{\underline{IH}} \text{ or } \overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = GND \text{ to } V_{CC}$ | _ | 1 | _ | 1 | ı | 1 | _ | 1 | μΑ | |
| Operating power supply current | I _{CC} | $\begin{aligned} V_{CC} &= Max \\ \overline{CE} &\leq V_{IL}, \ f = fmax, \ I_{OUT} = 0 \ mA \end{aligned}$ | - | 180 | - | 160 | - | 140 | - | 120 | mA | |
| Standby | I_{SB} | $\frac{V_{CC} = Max}{CE \ge V_{IH}, f = Max}$ | - | 60 | - | 55 | i | 50 | - | 45 | mA | |
| power supply current | I_{SB1} | $\begin{aligned} \mathbf{V}_{CC} &= \mathbf{Max} \\ \overline{CE} &\geq \mathbf{V}_{CC} - 0.2\mathbf{V}, \mathbf{V}_{IN} \geq \mathbf{V}_{CC} \\ &- 0.2\mathbf{V} \text{ or } \mathbf{V}_{IN} \leq 0.2\mathbf{V}, \mathbf{f} = 0 \end{aligned}$ | - | 10 | - | 10 | - | 10 | - | 10 | mA | |
| Output | V _{OL} | $I_{OL} = 6 \text{ mA}, V_{CC} = \text{Min}$ | _ | 0.4 | _ | 0.4 | | 0.4 | _ | 0.4 | V | 4 |
| Output voltage | * OL | $I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$ | _ | 0.5 | | 0.5 | _ | 0.5 | _ | 0.5 | • | |
| | V_{OH} | $I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$ | 2.4 | _ | 2.4 | _ | 2.4 | _ | 2.4 | _ | V | 4 |

Capacitance (f = 1MHz, $T_a = 25^{\circ} C$, $V_{CC} = NOMINAL)^4$

| Parameter | Symbol | Signals | Test conditions | Max | Unit |
|-------------------|------------------|--|-------------------------|-----|------|
| Input capacitance | C_{IN} | $A, \overline{CE}, \overline{WE}, \overline{OE}, \overline{UB}, \overline{LB}$ | $V_{IN} = 0V$ | 6 | pF |
| I/O capacitance | C _{I/O} | I/O | $V_{IN} = V_{OUT} = 0V$ | 8 | pF |

^{**} $V_{\rm IL}$ min = -1.0V for pulse width less than 5 nS.



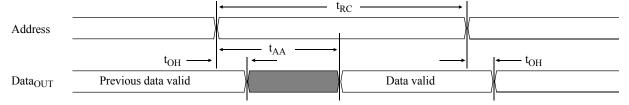
Read cycle (over the operating range)^{2,8}

| | | - | 10 | -1 | 12 | -1 | 15 | -2 | 20 | | |
|---|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|------|-------|
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Read cycle time | t_{RC} | 10 | _ | 12 | _ | 15 | _ | 20 | _ | ns | |
| Address access time | t_{AA} | _ | 10 | _ | 12 | _ | 15 | _ | 20 | ns | |
| Chip enable (\overline{CE}) access time | t _{ACE} | _ | 10 | _ | 12 | _ | 15 | _ | 20 | ns | |
| Output enable (OE) access time | t _{OE} | _ | 5 | _ | 6 | _ | 6 | _ | 6 | ns | |
| Output hold from address change | t _{OH} | 3 | _ | 3 | _ | 3 | _ | 3 | _ | ns | 4 |
| CE Low to output in low Z | t _{CLZ} | 3 | _ | 3 | _ | 3 | _ | 3 | _ | ns | 3, 4 |
| CE High to output in high Z | t _{CHZ} | _ | 5 | _ | 6 | _ | 7 | _ | 9 | ns | 3, 4 |
| OE Low to output in low Z | t _{OLZ} | 0 | _ | 0 | _ | 0 | _ | 0 | _ | ns | 3, 4 |
| OE High to output in high Z | t _{OHZ} | _ | 5 | _ | 6 | _ | 7 | _ | 9 | ns | 3, 4 |
| LB, UB access time | t_{BA} | _ | 5 | _ | 6 | _ | 7 | _ | 8 | ns | |
| LB, UB Low to output in low Z | $t_{ m BLZ}$ | 0 | _ | 0 | _ | 0 | _ | 0 | _ | ns | |
| LB, UB High to output in high Z | t _{BHZ} | _ | 5 | _ | 6 | _ | 7 | _ | 9 | ns | |
| Power up time | t_{PU} | 0 | _ | 0 | _ | 0 | _ | 0 | _ | ns | 4 |
| Power down time | t _{PD} | _ | 10 | _ | 12 | | 15 | | 20 | ns | 4 |

Key to switching waveforms

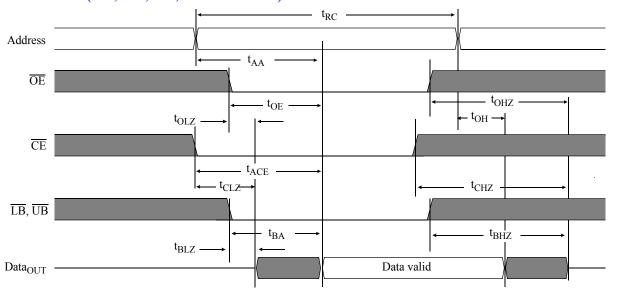
Rising input
Falling input
Undefined/don't care

Read waveform 1 (address controlled)^{5,6,8}





Read waveform 2 (CE, OE, UB, LB controlled)^{5,7,8}

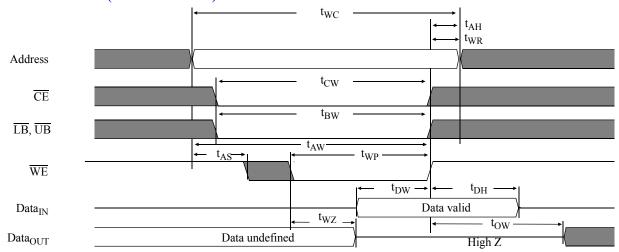


Write cycle (over the operating range)⁹

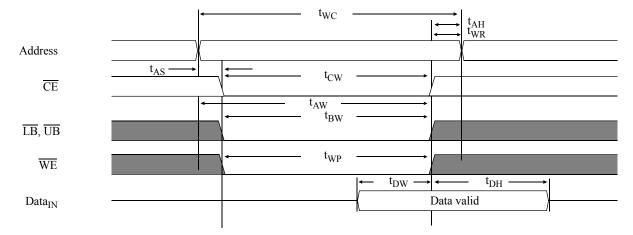
| | | - | 10 | _ | 12 | _ | 15 | _ | 20 | | |
|---|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|------|------|
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Unit | Note |
| Write cycle time | t_{WC} | 10 | _ | 12 | _ | 15 | _ | 20 | _ | ns | |
| Chip enable $\overline{\text{(CE)}}$ to write end | t_{CW} | 7 | _ | 8 | _ | 10 | _ | 12 | _ | ns | |
| Address setup to write end | t _{AW} | 7 | _ | 8 | _ | 10 | - | 12 | - | ns | |
| Address setup time | t _{AS} | 0 | _ | 0 | _ | 0 | - | 0 | - | ns | |
| Write pulse width $(\overline{OE} = High)$ | t _{WP1} | 7 | _ | 8 | _ | 10 | _ | 12 | _ | ns | |
| Write pulse width $(\overline{OE} = Low)$ | t _{WP2} | 10 | _ | 12 | _ | 15 | - | 20 | - | ns | |
| Write recovery time | t_{WR} | 0 | _ | 0 | _ | 0 | _ | 0 | _ | ns | |
| Address hold from end of write | t _{AH} | 0 | _ | 0 | _ | 0 | - | 0 | - | ns | |
| Data valid to write end | t_{DW} | 5 | _ | 6 | | 7 | _ | 9 | _ | ns | |
| Data hold time | t _{DH} | 0 | _ | 0 | _ | 0 | _ | 0 | _ | ns | 3, 4 |
| Write enable to output in High-Z | t_{WZ} | 2 | 5 | 2 | 6 | 2 | 7 | 2 | 9 | ns | 3, 4 |
| Output active from write end | t_{OW} | 3 | _ | 3 | _ | 3 | _ | 3 | _ | ns | 3, 4 |
| Byte enable Low to write end | t_{BW} | 7 | _ | 8 | _ | 10 | _ | 12 | _ | ns | 3, 4 |



Write waveform 1(WE controlled)9

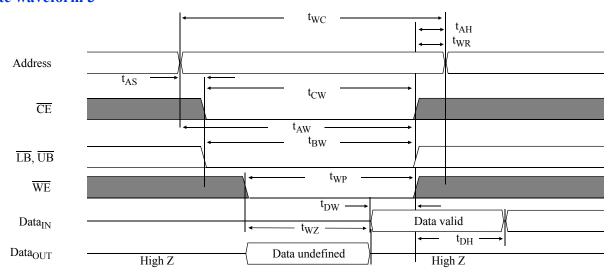


Write waveform 2 (CE controlled)9





Write waveform 3 9



AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to $V_{\mbox{\footnotesize CC}}$ 0.5V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

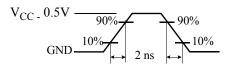


Figure A: Input pulse

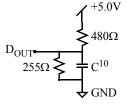
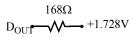


Figure B:5.0V Output load

Thevenin equivalent:

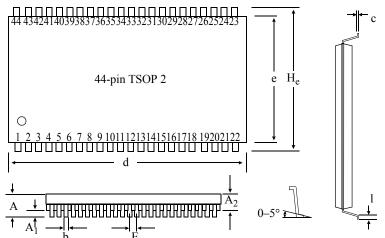


Notes

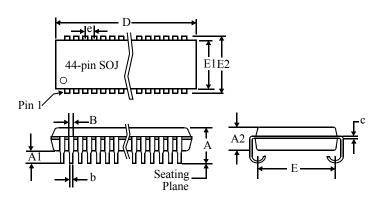
- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CE} is required to meet I_{SB} specification.
- 2 For test conditions, see AC Test Conditions, Figures A and B.
- 3 t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure B. Transition is measured ± 500 mV from steady-state voltage.
- 4 This parameter is guaranteed, but not tested.
- $\overline{\text{WE}}$ is High for read cycle.
- 6 $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are Low for read cycle.
- 7 Address valid prior to or coincident with \overline{CE} transition Low.
- 8 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 9 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 10 C = 30 pF, except on High Z and Low Z parameters, where C = 5 pF.



Package dimensions



| | 44-pin ' | TSOP 2 | | | | | |
|----------------|----------------|----------|--|--|--|--|--|
| | Min (mm) | Max (mm) | | | | | |
| A | | 1.2 | | | | | |
| $\mathbf{A_1}$ | 0.05 | 0.15 | | | | | |
| A ₂ | 0.95 | 1.05 | | | | | |
| b | 0.30 | 0.45 | | | | | |
| c | 0.12 | 0.21 | | | | | |
| d | 18.31 | 18.52 | | | | | |
| e | 10.06 | 10.26 | | | | | |
| H _e | 11.68 | 11.94 | | | | | |
| E | 0.80 (typical) | | | | | | |
| 1 | 0.40 | 0.60 | | | | | |



| | 44-pin SO | J 400 mils |
|------------|-----------|------------|
| | Min(mils) | Max(mils) |
| A | 0.128 | 0.148 |
| A1 | 0.025 | - |
| A2 | 0.105 | 0.115 |
| В | 0.026 | 0.032 |
| b | 0.015 | 0.020 |
| c | 0.007 | 0.013 |
| D | 1.120 | 1.130 |
| E | 0.370 | NOM |
| E 1 | 0.395 | 0.405 |
| E2 | 0.435 | 0.445 |
| e | 0.050 | NOM |

P. 9 of 11



Ordering Codes

| Package | Version | 10 ns | 12 ns | 15 ns | 20 ns |
|---------|-----------------|----------------|----------------|----------------|----------------|
| SOJ | 5.0V commercial | AS7C4098A-10JC | AS7C4098A-12JC | AS7C4098A-15JC | AS7C4098A-20JC |
| | 5.0V industrial | AS7C4098A-10JI | AS7C4098A-12JI | AS7C4098A-15JI | AS7C4098A-20JI |
| TSOP 2 | 5.0V commercial | AS7C4098A-10TC | AS7C4098A-12TC | AS7C4098A-15TC | AS7C4098A-20TC |
| 1501 2 | 5.0V industrial | AS7C4098A-10TI | AS7C4098A-12TI | AS7C4098A-15TI | AS7C4098A-20TI |

Note: Add suffix 'N' to the above part numbers for Lead Free Parts. (Ex: AS7C4098A - 10TCN)

Part numbering system

| AS7C | 4098A | -XX | J or T | X | X |
|-------------|------------------|----------------|--|---|---------------------|
| SRAM prefix | Device number | Access time | Packages: J: SOJ 400 mil T: TSOP 2 | Temperature ranges: C: Commercial, 0°C to 70°C I: Industrial, –40°C to 85°C | N = Lead Free Parts |



Revision History

| Rev. No. | History | Revised Date |
|----------|--|--------------|
| v1.0 | Initial release | 11/08/04 |
| v1.1 | Included I _{CC} , I _{SB} & I _{SB1} parameters | 05/27/05 |
| | Corrected the following: T _{OE} , V _{IH} , V _{OL} & t _{WZ} | |
| v1.2 | Removed the title "PRELIMINARY INFORMATION" | 02/21/06 |





Alliance Semiconductor Corporation 2575, Augustine Drive, Santa Clara, CA 95054 Tel: 408 - 855 - 4900

Fax: 408 - 855 - 4999

www.alsc.com

Copyright © Alliance Semiconductor All Rights Reserved Part Number: AS7C4098A Document Version: v 1.2

© Copyright 2003 Alliance Semiconductor Corporation. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems