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high performance needs great design.

Datasheet: AS8222 Enhanced FlexRay Standard Transceiver

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AS8222
Enhanced FlexRay Standard Transceiver

1 General Description

The AS8222 is a high-speed fault tolerant device operating as interface between a generic FlexRay Communication Controller and the copper wiring.

This device is the first FlexRay certified Transceiver for temperature ranges up to 150°C ambient temperature. For bare-die deliveries please contact ams for more information.

The AS8222 is designed to extend the application range for high speed and safety critical time triggered bus systems in an automotive environment. The bus driver is protected against short circuits to the supply and GND. The AS8222 operates at baudrates up to 10 Mbps and is fully conforming to the FlexRay Electrical Physical Layer Specification V2.1 Rev B.

The AS8222 provides a host controller interface consisting of Enable (EN) and Standby (STBN) input pins for mode handling by the microcontroller and the Error (ERRN) output pin, signalling failures and status information.

The device supports the NORMAL mode with activated FlexRay bus transmitter and receiver, the RECEIVE_ONLY mode with activated receiver only to avoid unwanted disturbances while listening to the communication and the low-power modes STANDBY and SLEEP with very low power consumption.

In case of undervoltage at one of the supply voltages (V_{BAT}, V_{CC}, and V_{IO}) the device will change its mode to a low-power mode (either STANDBY or SLEEP mode) and the device will signal an error accordingly. In case of low voltage is detected on both V_{BAT} and V_{CC} the device will enter the POWER-OFF mode.

Ensuring application in safety critical environments a two wire bus-guardian interface is implemented where additional redundant circuitries on the electronic-control-unit can monitor the communication on the receive enable output (RxEN) and can activate and deactivate through the bus guardian enable input (BGE) the transmitter. Additionally in low-power modes the wake conditions at the RxEN pin can be monitored.

A thermal sensor circuit with an integral shutdown mechanism prevents damage to the device in extreme temperature conditions.

2 Key Features

- Data transfer up to 10 Mbps
- Compliant with FlexRay Electrical Physical Layer Specification V2.1 Rev. B
- **Wide operating ambient temperature range -40°C to +150°C**
- Excellent EMC performance
- High common mode range insures excellent EMI immunity

- Interface with optional bus guardian for bus supervision
- Automatic thermal shutdown protection
- Supports 12, 24V systems with low sleep current consumption
- Integrated power management system
- Two INH pins for the external voltage regulators control
- Local wake-up input
- Remote wake-up capability via FlexRay bus in sleep mode
- Supports 2.5, 3, 3.3, 5 V microcontrollers and automatically adapts to interface levels
- Does not disturb the bus line if not powered
- Protected against damage due to short circuit conditions on the bus (positive and negative battery voltage)
- Small Pb-free package: SSOP-20
- Automotive qualified to AEC-Q100, grade 0
- For bare-die deliveries please contact us.
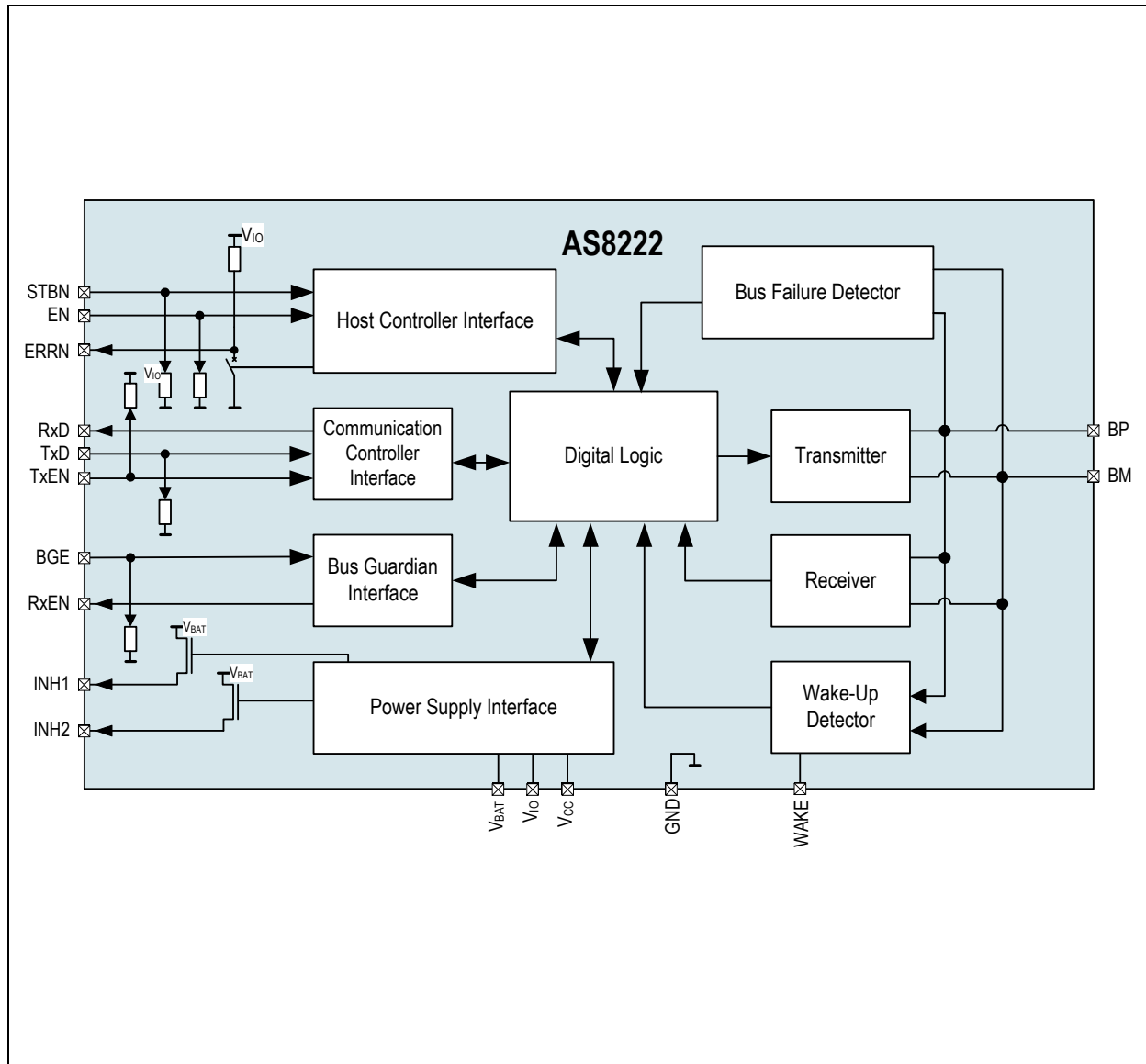
3 Applications

The AS8222 FlexRay Standard Transceiver is best fitting for automotive FlexRay nodes where bus wake-up and voltage regulator control for voltage supplies is needed.

The device addresses all ECUs connected to the permanent battery supply (terminal 30).

The device is best suited for high temperature applications with up to 150°C.

Figure 1. AS8222 Enhanced FlexRay Standard Transceiver Block Diagram

Contents

4 Pin Assignments

The AS8222 is available in SSOP-20 5.3mm.

Figure 2. Pin Assignments (Top View)
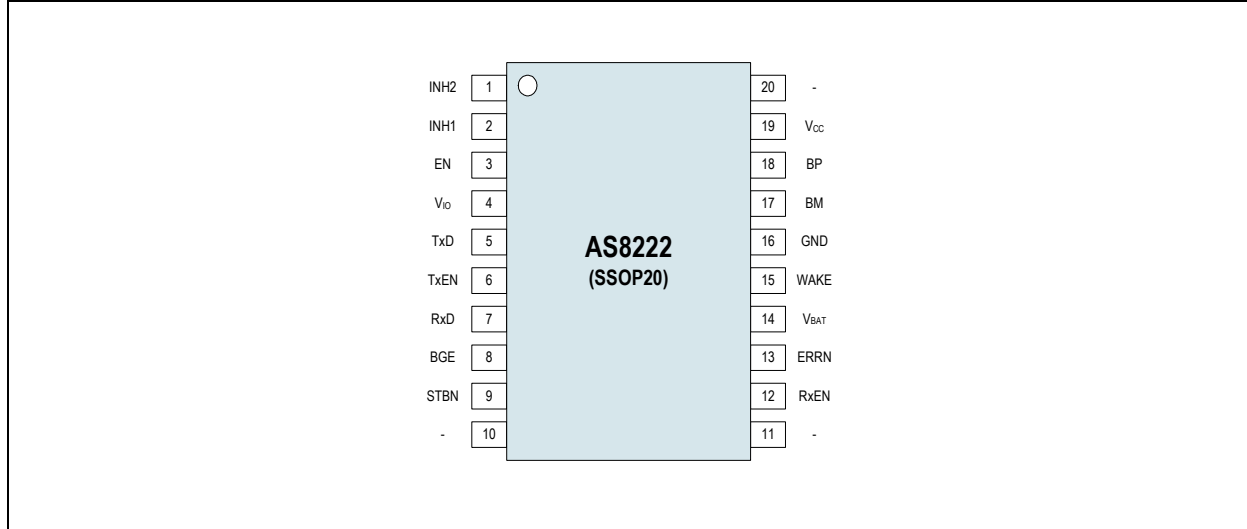
4.1 Pin Descriptions

Table 1. SSOP-20 Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
INH2	1	Analog I/O	Analog Output. Inhibit 2 output for switching external voltage regulator
INH1	2		Analog Output. Inhibit 1 output for switching external voltage regulator
EN	3	Digital Input with Pull-down	Digital Input. Enable input
V_{IO}	4	Supply	Supply Voltage. I/O supply voltage
TxD	5	Digital Input with Pull-down	Digital Input. Transmit data input
TxEN	6	Digital Input with Pull-up	Digital Input. Transmitter enable input
RxD	7	Digital Output	Digital Output. Receive data output
BGE	8	Digital Input with Pull-down	Digital Input. Bus guardian enable input
STBN	9		Digital Input. Standby input
Reserved	10	Analog/digital Input/output with Pull-down	To be connected to GND or to be unconnected
Not used	11	-	-
RxEN	12	Digital Output	Digital Output. Receive data enable output
ERRN	13		Digital Output. Error diagnosis output and wake status output
V_{BAT}	14	Supply	Supply Voltage. Battery supply voltage
WAKE	15	Analog I/O	Analog Input. Local wake-up input
GND	16	Supply	Ground
BM	17	Analog I/O	Analog Input/Output. Bus line Minus
BP	18		Analog Input/Output. Bus line Plus
V_{CC}	19	Supply	Supply voltage.
Not used	20	-	-

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Absolute Maximum Ratings is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: All voltages are referred to pin GND.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
Electrical Parameters					
V_{BAT}	Battery Supply Voltage	-0.3	+50	V	
V_{CC}	Supply Voltage	-0.3	+7.0	V	
V_{IO}		-0.3	+7.0	V	$V_{IO} < V_{CC}$
	DC Voltage at EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN	-0.3	V_{IO} +0.3	V	
	DC Voltage on pin WAKE, INH1, INH2	-0.3	V_{BAT} +0.3		
	DC Voltage at BP and BM	-40	+40	V	
	Input current (latchup immunity)	-100	100	mA	According to JEDEC 78
Electrostatic Discharge					
ESD	Electrostatic Discharge	±2		kV	All pins AEC-Q100-002 (HBM)
	uESDInt	2		kV	ESD on all other pins
	Electrostatic Discharge	±4		kV	For V_{BAT}, GND, WAKE AEC-Q100-002 (HBM)
	uESD$_{Ext}$	4		kV	ESD protection on pins that lead to ECU external terminals
	Electrostatic Discharge	±6		kV	BP, BM AEC-Q100-002 (HBM)
	uESD$_{Ext}$	4		kV	ESD protection on pins that lead to ECU external terminals
	Electrostatic Discharge	±6		kV	BP, BM FlexRay Physical Layer EMC Measurement Specification Version 3.0
	Electrostatic Discharge	±500		V	On all pins AEC-Q100-011 (Charge Device Model)
		±750		V	At the corner pins AEC-Q100-011 (Charge Device Model)
		±100		V	On all pins AEC-Q100-003 (Machine Model)

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
Damage Tests					
U_s	Transient voltage on V_{BAT}, Bus and Wake pins (damage tests)	-100		V	ISO7637-2 test pulse 1; class D (see Figure 14)
			+75	V	ISO7637-2 test pulses 2a; class D (see Figure 14)
		-150		V	ISO7637-2 test pulses 3a; class D (see Figure 14)
			+100	V	ISO7637-2 test pulses 3b; class D (see Figure 14)
Power Dissipation					
P_t	Total power dissipation (all supplies and outputs)		150	mW	
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-55	+150	ºC	
T_{BODY}	Package body temperature [1]		260	ºC	
H	Humidity non-condensing	5	85	%	
MSL	Moisture Sensitivity Level [2]	3			

1. The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices". The lead finish for Pb-free leaded packages is matte tin (100% Sn).
2. Represents a maximum floor life time of 168h.

6 Electrical Characteristics

In this specification, all the defined tolerances for external components are assured over the whole operation conditions range as well as over lifetime.

Operation Range:

T_{AMB}=-40ºC to +150ºC, V_{CC}=+4.75V to +5.25V, V_{BAT}=5.5V to +40V, V_{IO}=+2.2 to V_{CC}, R_L=40Ω, C_L= 100pF unless otherwise specified.

6.1 Supply Voltage

Table 3. Supply Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{AMB}	Ambient temperature		-40	+25	+150	ºC
T	Ambient temperature		-40		+125	ºC
V_{CC}-V_{IO}	Difference of supplies		-0.1		3.05	V
I_{BAT}	V_{BAT} current consumption (standard transceiver only)	V_{BAT}=12V; SLEEP mode; T_{AMB}<125ºC [1]	0	30	50	µA
		V_{BAT}=12V; SLEEP mode [1]	0	80	170	µA
		Non-low-power modes	0	0.24	1	mA
I_{CC}	V_{CC} current consumption	Low-power modes; V_{CC} = 0 V to +5.25V [1]	-5	10	20	µA
		Non-low-power mode: NORMAL, driver enabled	15	25	45	mA
		Non-low-power mode: NORMAL, driver enabled; R_{BUS}= ∞Ω	3	7	15	mA
		Non-low-power mode: RECEIVE-ONLY	1	2	10	mA
I_{IO}	V_{IO} current consumption	Low-power Modes; V_{IO} = 0 V to +5.25V [1]	-5	2	20	µA
		Non-low-power Modes	0	0.02	1	mA

1. EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN, WAKE, INH1, INH2: open.

6.2 State Transitions

Table 4. State Transitions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{STBN_RXD}	Delay STBN high to RxD high with wake flag set		1	10	50	µs
t_{STBN_RXEN}	Delay STBN high to RxEN high with wake flag set		1	10	50	µs
t_{SLEEP_INH1}	Delay STBN high to INH1 high	INH1 high = 80 % V_{BAT}	1	10	50	µs
$t_{STANDBY\_INH2}$	Delay STBN high to INH2 high	INH2 high = 80 % V_{BAT}	1	10	50	µs
t_{SLEEP}	go-to-sleep hold time	INH1 low = 20 % V_{BAT}	10	25	70	µs

6.3 Transmitter

The following parameters are applicable to all the branch transmitters.

Table 5. Transmitter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{BUS\_DIFF\_D0}$	Differential bus voltage low in NORMAL mode (Data_0)	$V_{BPdata0} - V_{BMdata0}$; $40\ \Omega < R_L < 55\ \Omega$	-2	-1	-0.6	V
uBDTx$_{active}$	Absolute value of uBus, while sending	Load on BP/BM: 40Ω || 100pF	|2000|		|600|	mV
$V_{BUS\_DIFF\_D1}$	Differential bus voltage high in NORMAL mode (Data_1)	$V_{BPdata1} - V_{BMdata1}$; $40\ \Omega < R_L < 55\ \Omega$	0.6	1	2	V
uBDTx$_{active}$	Absolute value of uBus, while sending	Load on BP/BM: 40Ω || 100pF	|600|		|2000|	mV
ΔV_{BUS_DIFF}	Matching between Data_0 and Data_1 differential bus voltage in NORMAL mode	$V_{BUS\_DIFF\_D0}$ - $V_{BUS\_DIFF\_D1}$ $40\ \Omega < R_L < 55\ \Omega$	-200	0	200	mV
$V_{BUS\_COM\_D0}$	Common mode bus voltage in case of Data_0 in non-low-power mode	$V_{BPdata0}/2 + V_{BMdata0}/2$ $40\ \Omega < R_L < 55\ \Omega$	0.4 * V_{CC}	0.5 * V_{CC}	0.6 * V_{CC}	V
$V_{BUS\_COM\_D1}$	Common mode bus voltage in case of Data_1 in non-low-power mode	$V_{BPdata1}/2 + V_{BMdata1}/2$ $40\ \Omega < R_L < 55\ \Omega$	0.4 * V_{CC}	0.5 * V_{CC}	0.6 * V_{CC}	V
ΔV_{BUS_COM}	Matching between Data_0 and Data_1 common mode voltage	$V_{BUS\_COM\_D0}$ - $V_{BUS\_COM\_D1}$ $40\ \Omega < R_L < 55\ \Omega$	-200	0	200	mV
$V_{BUS\_DIFF\_Idle}$	Absolute differential bus voltage in idle mode	$40\ \Omega < R_L < 55\ \Omega$		0	30	mV
uBDTxidle	Absolute value of uBus, while Idle		0		30	mV
IBP$_{BMShortMax}$ IBM$_{BPShortMax}$	Absolute max current when BP shorted to BM	$V_{BP} = V_{BM}$		25	+100	mA
IBP$_{BMShortMax}$ IBM$_{BPShortMax}$	Absolute maximum output current when BP shorted to BM				100	mA
IBP$_{GNDShortMax}$	Absolute max current when BP is shorted to GND	$V_{BP} = 0\ V$		50	+100	mA
IBP$_{GNDShortMax}$	Absolute maximum output current when shorted to GND				100	mA

Table 5. Transmitter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IBM$_{GNDShortMax}$	Absolute max current when BM is shorted to GND	V$_{BM}$=0 V		50	+100	mA
IBM$_{GNDShortMax}$	Absolute maximum output current when shorted to GND				100	mA
IBP$_{-5VShortMax}$	Absolute max current when BP is shorted to -5 V	V$_{BP}$=-5 V		50	+100	mA
IBP$_{-5VShortMax}$	Absolute maximum output current when shorted to –5V				100	mA
IBM$_{-5VShortMax}$	Absolute max current when BM is shorted to -5 V	V$_{BM}$=-5 V		50	+100	mA
IBM$_{-5VShortMax}$	Absolute maximum output current when shorted to –5V				100	mA
IBP$_{27VShortMax}$	Absolute max current when BP is shorted to 27 V	V$_{BP}$=27 V		60	+100	mA
IBP$_{BAT27ShortMax}$	Absolute maximum output current when shorted to 27V				100	mA
IBM$_{27VShortMax}$	Absolute max current when BM is shorted to 27 V	V$_{BM}$=27 V		60	+100	mA
IBM$_{BAT27ShortMax}$	Absolute maximum output current when shorted to 27V				100	mA
IBP$_{40VShortMax}$	Absolute max current when BP is shorted to 40 V	V$_{BP}$=40 V		75	+100	mA
IBM$_{40VShortMax}$	Absolute max current when BM is shorted to 40 V	V$_{BM}$=40 V		75	+100	mA
t$_{TXD\_BUS01}$	Delay time from TxD to BUS positive edge	t$_{riseTxD}$ = 5 ns		25	50	ns
dBDTx01	Transmitter delay, positive edge				100	ns
t$_{TXD\_BUS10}$	Delay time from TxD to BUS negative edge	t$_{fall\,TxD}$ = 5 ns		25	50	ns
dBDTx10	Transmitter delay, negative edge				100	ns
t$_{TXD\_MISMATCH}$	Delay time from TxD to BUS mismatch	t$_{TxD\_BUS10}$ – t$_{TxD\_BUS01}$	-4	0	4	ns
dTxAsym	Transmitter delay mismatch | dBDTx10 - dBDTx01 |				4	ns
t$_{BUS\_TX10}$	Fall time differential bus voltage	80 % - 20 % of V$_{BUS}$; R$_L$=45 Ω; C$_L$= 100 pF	3.75	13	18.75	ns
dBusTx10	Fall time differential bus voltage (80% → 20%)		3.75		18.75	ns
t$_{BUS\_TX01}$	Rise time differential bus voltage	20 % - 80 % of V$_{BUS}$; R$_L$=45 Ω; C$_L$= 100 pF	3.75	13	18.75	ns
dBusTx01	Rise time differential bus voltage (20% → 80%)		3.75		18.75	ns
t$_{TXEN\_BUS\_Idle\_Active}$	Delay time from TxEN to bus active	R$_L$=45 Ω; C$_L$= 100 pF		18	50	ns
dBDTxia	Propagation delay idle → active				100	ns

Table 5. Transmitter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{TXEN\_BUS\_Active\_Idle}$ dBDTxai	Delay time from TxEN to bus idle Propagation delay active → idle	R_L=45 Ω; C_L= 100 pF		18	50 100	ns ns
$t_{TXEN\_MISMATCH}$ dBDTxDM	Delay time from TxEN to BUS mismatch | dBDTxia - dBDTxai |	| $t_{TXEN\_BUS\_Idle\_Active}$ - $t_{TXEN\_BUS\_Active\_Idle}$ |; R_L=45 Ω; C_L= 100 pF	0		50 50	ns ns
$t_{BGE\_BUS\_IdleActive}$ dBDTxia	Delay time from BGE to bus active Propagation delay idle → active			18	50 100	ns ns
$t_{BGE\_BUS\_Active\_Idle}$ dBDTxai	Delay time from BGE to bus idle Propagation delay active → idle			18	50 100	ns ns
$t_{BUS\_Idle\_Active}$ dBusTxia	Differential bus voltage transition time: idle to active Transition time idle → active	R_L=45 Ω; C_L= 100 pF		5	30 30	ns ns
$t_{BUS\_Active\_Idle}$ dBusTxai	Differential bus voltage transition time: active to idle Transition time active → idle	R_L=45 Ω; C_L= 100 pF		2	30 30	ns ns
$t_{TxEN\_timeout}$	TxEN timeout		3	5	10	ms

6.4 Receiver

The following parameters are applicable to all the branch receivers.

Table 6. Receiver

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{BP}, R_{BM} RCM1, RCM2	BP, BM input resistance Receiver common mode input resistance	Idle mode; R_{BUS}= ∞	10 10	25	40 40	kΩ kΩ
R_{DIFF}	BP, BM differential input resistance	Idle mode; R_{BUS}= ∞	20	50	80	kΩ
V_{BP}, V_{BM} uCM	Common mode voltage range Common mode voltage range (with respect to GND) that does not disturb the receive function		-10 -10		+15 +15	V V
V_{BPidle}, V_{BMidle} uBias	Idle voltage in non-low-power modes on pin BP, BM Bus bias voltage during BD_Normal mode	Non-low-power modes; V_{TXEN}=V_{IO} 40 Ω < R_L < 55 Ω	0.4*V_{CC} 1800	0.5*V_{CC}	0.6*V_{CC} 3200	V mV

Table 6. Receiver

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{BPidle_low}, V_{BMidle_low}	Idle voltage in low-power modes on pin BP, BM	Low-power modes $40\ \Omega < R_L < 55\ \Omega$	-0.2	0	+0.2	V
uBias	Bus bias voltage during low-power modes		-200		+200	mV
I_{BPidle}	Absolute idle output current on pin BP	$-40\ V < V_{BP} < 40\ V$	0	2	7.5	mA
I_{BMidle}	Absolute idle output current on pin BM	$-40\ V < V_{BM} < 40\ V$	0	2	7.5	mA
I_{BPleak_ST}, I_{BMleak_ST}	Absolute leakage current, when not powered	$V_{BP}=V_{BM}=5\ V$, $V_{DD}=0\ V$, $V_{BAT}=0\ V$; $V_{IO}=0\ V$; $T_{amb} < 125°C$		6	25	μA
iBPLeak, iBMLeak	Absolute leakage current, when not powered				25	μA
I_{BPleak_HT}, I_{BMleak_HT}	Absolute leakage current, when not powered	$V_{BP}=V_{BM}=5\ V$, $V_{DD}=0\ V$, $V_{BAT}=0\ V$; $V_{IO}=0\ V$; $125°C < T_{amb} < 150°C$		35	150	μA
$V_{BUSActiveHigh}$	Activity detection differential input voltage high	Normal power modes $-10\ V < (V_{BP}, V_{BM}) < 15\ V$	150	260	400	mV
uBusActiveHigh	Upper receiver threshold for detecting activity		150		425	mV
$V_{BUSActiveLow}$	Activity detection differential input voltage low	Normal power modes $-10\ V < (V_{BP}, V_{BM}) < 15\ V$	-400	-260	-150	mV
uBusActiveLow	Lower receiver threshold for detecting activity		-425		-150	mV
V_{Data1}	Data1 detection differential input voltage	Pre-condition: activity already detected. Normal power mode. $-10\ V < (V_{BP}, V_{BM}) < 15\ V$	150	225	300	mV
uData1	Receiver threshold for detecting Data_1		150		300	mV
V_{Data0}	Data0 detection differential input voltage	Pre-condition: activity already detected. Normal power mode. $-10\ V < (V_{BP}, V_{BM}) < 15\ V$	-300	225	-150	mV
uData0	Receiver threshold for detecting Data_0		-300		-150	mV
$V_{DataErr}$	Mismatch between Data0 and Data1 differential input voltage	$2 \times (||V_{Data0}| - |V_{Data1}||)\ /$ $(|V_{Data0}| + |V_{Data1}|)$ [1]		0	10	%
ΔuData	Mismatch of receiver thresholds				10	%
t_{BUS_RxD10}	Delay from BUS to RxD negative edge	$C_{RXD}=15\ pF$ [2]		34	80	ns
dBDRx10	Receiver delay, negative edge				100	ns
t_{BUS_RxD01}	Delay from BUS to RxD positive edge	$C_{RXD}=15\ pF$ [2]		34	80	ns
dBDRx01	Receiver delay, positive edge				100	ns

Table 6. Receiver

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{bit}	Bit time	C_{RXD}=15 pF [2]	60			ns
t_{RxD_ASYM}	Delay time from BUS to RxD mismatch	C_{RXD}=15 pF, $\mid t_{BUS\_RxD10}$- $t_{BUS\_RxD01}\mid$ [2]		0	5	ns
dRxAsym	Receiver delay mismatch $\mid$ dBDRx10 – dBDRx01 $\mid$				5	ns
$t_{RXDfall}$	Fall time RxD voltage	80 % - 20 % of V_{RXDL};C_{RXD}=15 pF [2]		2	5	ns
dRxSlope	Fall and rise time 20%-80%, 15pF load				5	ns
$t_{RXDrise}$	Rise time RxD voltage	20 % - 80 % of V_{RXDL};C_{RXD}=15 pF [2]		2	5	ns
dRxSlope	Fall and rise time 20%-80%, 15pF load				5	ns
$t_{BUSIdleDetection}$	Idle detection time	V_{BUS}: 400mV $\rightarrow$ 0	50	150	250	ns
dIdleDetection	Filter-time for idle detection		50		250	ns
$t_{BUSActivityDetection}$	Activity detection time	V_{BUS}: 0 V $\rightarrow$ 400 mV	100	200	300	ns
dActivityDetection	Filter-time for activity detection		100		300	ns
$t_{BUSIdleReaction}$	Idle reaction time	V_{BUS}: 400mV $\rightarrow$ 0	50	160	300	ns
dBDRxai	Idle reaction time		50		400	ns
$t_{BUSActivityReaction}$	Activity reaction time	V_{BUS}: 0 V $\rightarrow$ 400 mV	100	210	350	ns
dBDRxia	Activity reaction time		100		450	ns

1. Test condition: (VBP + VBM) / 2 = 2,5V ± 5%
2. For test signal see Figure 13

6.5 Wake-up Detector

The following parameters are applicable to all the branch wake-up detectors.

Table 7. Wake-up Detector

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{BAT_BW}	VBAT voltage supply for bus wake-up		6.5		40	V
		In case a VBAT supply voltage input is implemented, the wake-up detector shall be operable when uVBAT is equal to or greater than 7V even if other supplies are not present.				
t_{BWU0}	Data_0 detection time in remote wake-up pattern	-10V<(V_{BP}, V_{BM})<15V	1	2	4	µs
dWU0Detect	Acceptance timeout for detection of a Data_0 phase in wake-up pattern		1		4	µs

Table 7. Wake-up Detector

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{BWUIdle}$	Idle or Data_1 detection time in remote wake-up pattern	-10V<(V_{BP}, V_{BM})<15V	1	2	4	µs
dWUIdleDetect	Acceptance timeout for detection of a Idle phase in wake-up pattern		1		4	µs
$t_{BWUDetect}$	Total remote wake-up detection time	-10V<(V_{BP}, V_{BM})<15V	48	75	140	µs
dWUTimeout	Acceptance timeout for wake-up pattern recognition		48		140	µs
V_{BWU0}	Remote wake-up detector threshold	-10V<(V_{BP}, V_{BM})<15V	-300	-250	-150	mV
V_{LWUTH}	Wake-up detection threshold		2	2.8	4	V
I_{LWUL}	Low level input current on WAKE pin	V_{BAT}=12V; V_{LWAKE}=2V for t<$t_{LWUFilter}$	-20	-10	-5	µA
I_{LWUH}	High level input current on WAKE pin	V_{BAT}=12V; V_{LWAKE}=4V for t<$t_{LWUFilter}$	5	10	20	µA
$t_{LWUFilter}$	Local wake filter time		1	20	40	µs
dWakePulseFilter	Wake pulse filter time (spike rejection)		1		500	µs

6.6 Supply Voltage Monitor

Table 8. Supply Voltage Monitor

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$VBAT_{THH}$	VBAT undervoltage recovery threshold		3.5	4	4.5	V
$VBAT_{THL}$	VBAT undervoltage detection threshold		2.5	3	3.5	V
uUV$_{BAT}$	Undervoltage detection threshold		2		5.5	V
VCC_{THH}	VCC undervoltage recovery threshold		3.5	4	4.5	V
VCC_{THL}	VCC undervoltage detection threshold		2.5	3	3.5	V
uUV$_{CC}$	Undervoltage detection threshold		2			V
VIO_{THH}	VIO undervoltage recovery threshold		1.25	1.6	2.0	V
VIO_{THL}	VIO undervoltage detection threshold		0.75	1.1	1.5	V
uUV$_{IO}$	Undervoltage detection threshold		0.75			V
t_{UV_DETECT}	Undervoltage detection time		100	300	700	ms
dUV$_{BAT}$, dUV$_{CC}$, dUV$_{IO}$	Undervoltage reaction time				1000	ms
t_{UV_REC}	Undervoltage recovery time		0.7	2	5	ms

6.7 Bus Error Detection

The following parameters are applicable to all the branch error detectors.

Table 9. Bus Error Detection

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{THL}	Absolute bus current for low current detection	NORMAL mode, Transmitter enabled not production tested		5	20	mA
I_{THH}	Absolute bus current for high current detection	NORMAL mode, Transmitter enabled not production tested	20	40		mA
V_{SHORT}	Differential voltage on BP and BM for detecting short circuit between bus lines	NORMAL mode, Transmitter enabled	150	260	400	mV
t_{BUS_ERROR}	Bus error detection time	Normal mode, Transmitter enabled (**) detection only required while actively transmitting a data frame, error indication to host latest when transmission stops.			500	ns
t_{BUS_INHIB}	Bus short detection inhibit time	Normal mode, Transmitter enabled	0.5	2	4	µs

6.8 Over Temperature

Table 10. Over Temperature

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OT_{TH}	Over temperature threshold high		175	190	205	ºC
OT_{TL}	Over temperature hysteresis low		165	180	195	ºC

6.9 Power Supply Interface

Table 11. Power Supply Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ΔV_{OINH}	High level voltage drop on INH1, INH2	I_{INH}=0.2mA; V_{BAT}=5.5V	0	0.2	0.8	V
$\lvert I_{IL} \rvert$	Leakage current	Sleep mode, V_{INH}=0V	-5	0	5	µA

6.10 Communication Controller Interface

Table 12. Communication Controller Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TxDIH} uVDIG-IN-HIGH	Threshold for detecting TxD as on logical high Threshold for detecting a digital input as on logical high			0.48 * V_{IO}	0.7 * V_{IO} 0.7 × uVDIG	V
V_{TxDIL} uVDIG-IN-LOW	Threshold for detecting TxD as on logical low Threshold for detecting a digital input as on logical low		0.3 * V_{IO} 0.3 × uVDIG			V
I_{TxDIH}	TxD high level input current		20	50	100	µA
I_{TxDIL}	TxD low level input current		-5	0	5	µA
V_{TxENIH} uVDIG-IN-HIGH	Threshold for detecting TxEN as on logical high Threshold for detecting a digital input as on logical high				0.7 * V_{IO} 0.7 × uVDIG	V

Table 12. Communication Controller Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TxENIL} uVDIG-IN-LOW	Threshold for detecting TxEN as on logical low Threshold for detecting a digital input as on logical low		$0.3 * V_{IO}$ $0.3 \times$ uVDIG			V
I_{TxENIH}	TxEN high level input current		-5	0	5	µA
I_{TxENIL}	TxEN low level input current		-100	-50	-20	µA
V_{RxDOH} uVDIG-OUT-HIGH	RxD high level output voltage Output voltage on a digital output, when in logical high state	I_{RxD}=-4mA, V_{IO}=5V	$0.8 * V_{IO}$ $0.8 \times$ uVDIG	$0.9 * V_{IO}$	$1.0 * V_{IO}$ $1.0 \times$ uVDIG	V
V_{RxDOL} uVDIG-OUT-LOW	RxD low level output voltage Output voltage on a digital output, when in logical low state	I_{RxD}=4mA, V_{IO}=5V	0	$0.1 * V_{IO}$	$0.2 * V_{IO}$ $0.2 \times$ uVDIG	V

6.11 Host Interface

Table 13. Host Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{STBNIH}	Threshold for detecting STBN as on logical high			0.48 * V_{IO}	0.7 * V_{IO}	V
uVDIG-IN-HIGH	Threshold for detecting a digital input as on logical high				0.7 × uVDIG	
V_{STBNIL}	Threshold for detecting STBN as on logical low		0.3 * V_{IO}	0.48 * V_{IO}		V
uVDIG-IN-LOW	Threshold for detecting a digital input as on logical low		0.3 × uVDIG			
I_{STBNIH}	STBN high level input current		20	50	100	µA
I_{STBNIL}	STBN low level input current		-5	0	5	µA
$t_{STBN\_DEB\_LP}$	STBN de-bouncing time low-power modes		0.1	1	40	µs
$t_{STBN\_DEB\_NLP}$	STBN de-bouncing time non-low-power modes		0.1	1	2	µs
V_{ENIH}	Threshold for detecting EN as on logical high			0.48 * V_{IO}	0.7 * V_{IO}	V
uVDIG-IN-HIGH	Threshold for detecting a digital input as on logical high				0.7 × uVDIG	
V_{ENIL}	Threshold for detecting EN as on logical low		0.3 * V_{IO}	0.48 * V_{IO}		V
uVDIG-IN-LOW	Threshold for detecting a digital input as on logical low		0.3 × uVDIG			
I_{ENIH}	EN high level input current		20	50	100	µA
I_{ENIL}	EN low level input current		-5	0	5	µA
$t_{EN\_DEB\_LP}$	EN de-bouncing time low-power modes		0.1	1	40	µs
$t_{EN\_DEB\_NLP}$	EN de-bouncing time non-low-power modes		0.1	1	2	µs
V_{ERRNOH}	ERRN high level output voltage	I_{ERRN} =-4mA, V_{IO}=5V	0.8 * V_{IO}	0.9 * V_{IO}	1.0 * V_{IO}	V
uVDIG-OUT-HIGH	Output voltage on a digital output, when in logical high state		0.8 × uVDIG		1.0 × uVDIG	
V_{ERRNOL}	ERRN low level output voltage	I_{ERRN} =4mA, V_{IO}=5V	0	0.1 * V_{IO}	0.2 * V_{IO}	V
uVDIG-OUT-LOW	Output voltage on a digital output, when in logical low state				0.2 × uVDIG	

6.12 Bus Guardian Interface

Table 14. Bus Guardian Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{BGEIH} uVDIG-IN-HIGH	Threshold for detecting BGE as on logical high Threshold for detecting a digital input as on logical high			$0.48 * V_{IO}$	$0.7 * V_{IO}$ $0.7 \times$ uVDIG	V
V_{BGEIL} uVDIG-IN-LOW	Threshold for detecting BGE as on logical low Threshold for detecting a digital input as on logical low		$0.3 * V_{IO}$ $0.3 \times$ uVDIG	$0.48 * V_{IO}$		V
I_{BGEIH}	BGE high level input current		20	50	100	µA
I_{BGEIL}	BGE low level input current		-5	0	5	µA
V_{RxENOH} uVDIG-OUT-HIGH	RxEN high level output voltage Output voltage on a digital output, when in logical high state	I_{RxEN}=-4mA, V_{IO}=5V	$0.8 * V_{IO}$ $0.8 \times$ uVDIG	$0.9 * V_{IO}$	$1.0 * V_{IO}$ $1.0 \times$ uVDIG	V
V_{RxENOL} uVDIG-OUT-LOW	RxEN low level output voltage Output voltage on a digital output, when in logical low state	I_{RxEN}=4mA, V_{IO}=5V	0	$0.1 * V_{IO}$	$0.2 * V_{IO}$ $0.2 \times$ uVDIG	V

6.13 Read Out Interface

Table 15. Read Out Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{RO\_PROP\_ERRN}$	Propagation delay falling edge EN to ERRN			2	4.5	µs
$t_{RO\_EN\_TIMEOUT}$	Error read out time out		25	50	100	µs

7 Detailed Description

The AS8222 is a FlexRay Transceiver operating as an interface between the Communication Controller and the wired bus lines. The AS8222 is designed to extend the application range for high speed and safety critical time triggered bus systems in an automotive environment. The drivers are short circuit protected against the positive and negative supply voltage to increase the robustness and reliability of automotive systems. The AS8222 operates at baudrates up to 10 Mbps.

7.1 Block Description

The AS8222 consists of 9 functional blocks Figure 1.

Table 16. Functional Blocks

Symbol	Parameter
Host Controller Interface (HCI)	Digital interface between the Transceiver and the host controller (HC) The host interface comprises the read-out handler, which delivers failure and status information via the ERRN pin to the host controller.
Communication Controller Interface (CCI)	Digital interface between the Transceiver and the FlexRay communication controller (CC)
Bus Guarding Interface (BGI)	Digital interface between the Transceiver and the FlexRay bus guardian (BG) or monitoring circuitry.
Power Supply Interface (PSI)	The power supply interface consists of the voltage monitor (VM) with two analog inhibit outputs switching external voltage supplies.
Internal Logic (IL)	The digital signals from the functional blocks of the device are fed into the internal logic where the forwarding of FlexRay messages from analog side to digital interfaces and vice versa is done. The state machine is embedded in the Internal Logic and the handling of error, wake, and power-on flags is executed herein.
Bus Failure Detector (BFD) Temperature Protection (TP)	The bus failure detector is directly connected to the bus pins, in order to detect several external failure conditions which may occur on the bus. The temperature protection turns off the output driver when reaching the specified internal temperature in order to protect the device.
Transmitter	The transmitter provides the differential signaling according the FlexRay standard on the bus pins.
Receiver	The Receiver captures FlexRay valid signals at the bus pins and provides the received data streams to the Internal Logic.
Wake-Up Detector (WUD)	The wake-up detector recognizes valid wake-up frames on the bus, recognizes a wake signal on the local WAKE pin and signals valid wake-up events to the Internal Logic.

7.2 Events

Transitions in order to change between the operation modes are possible only if events are detected. The device supports three types of events:

- Events on the host controller interface (STBN, EN),
- Detection of undervoltage or supply voltage recovery and
- Wake events.

Mode changes are only performed upon detected events.

7.3 Operating Modes

The AS8222 provides the following operating modes:

- NORMAL: Non-low-power mode
- RECEIVE-ONLY: Non-low-power mode
- STANDBY: Low-power mode
- GO-TO-SLEEP: Low-power mode
- SLEEP: Low-power mode

7.3.1 NORMAL Mode

In this mode the transceiver is able to send and receive data signals on the bus. TxEN and BGE control the state of the transmitter. INH1 and INH2 outputs are set high. RxD shows the bus data and RxEN the bus state. The error read out mechanism is enabled. In this mode the transmitter state can be selected as shown in Table 17. In case the over-temperature flag is set the transmitter is disabled. The bus wires are terminated to $V_{CC}/2$ via receiver input resistances.

Table 17. Transmitter States

BGE	TxEN	TxD	Transmitter State	Bus state
H	L	H	Enabled	Data_1 (BP is driven high, BM is driven low)
H	L	L	Enabled	Data_0 (BP is driven low, BM is driven high)
X	H	X	Disabled	Idle (BP and BM are not driven)
L	X	X	Disabled	Idle (BP and BM are not driven)

- If the differential bus voltage is higher than $V_{BUSActivehigh}$ or lower than $V_{BUSActivelow}$ for a time longer than $t_{BUSActiveDetection}$, then activity is detected on the bus (Bus = active), RxEN is switched to logical "low" and RxD is released.

- If after the activity detection, the differential bus voltage is higher than V_{Data1}, RxD is high.

- If after the activity detection, the differential bus voltage is lower than V_{Data0}, RxD is low.

- If the absolute differential bus voltage is lower than $V_{BUSActivehigh}$ and higher than $V_{BUSActivelow}$ for a time longer than $t_{BUSIdleDetection}$, then idle is detected on the bus (Bus = idle), RxEN and RxD are switched to logical "high".

7.3.2 RECIEVE-ONLY Mode

In this mode the transceiver has the same behavior as in NORMAL mode but the transmitter is disabled.

7.3.3 STANDBY Mode

In this mode the transceiver is not able to send and receive data signals to and from the bus, but the wake up detector is active. The power consumption is significantly reduced with respect to the non-low-power operation modes. RxD, RxEN signals the negation of the wake-up flag. INH1 is set to high. If wake-up flag is set then INH2 is high, otherwise it is floating. The error read out mechanism is not enabled. The bus wires are terminated to GND (bus state: Idle_LP).

7.3.4 GO-TO-SLEEP Mode

In this mode the transceiver has the same behavior as in STANDBY mode but if this mode is selected for a time longer than t_{SLEEP} and the wake flag is cleared the device enters into the SLEEP mode.

7.3.5 SLEEP Mode

In this mode the transceiver has the same behavior as in standby mode but INH1 and INH2 are floating.

7.4 Non-Operating Modes

The AS8222 provides the following non-operating mode:

- POWER-OFF

7.4.1 POWER-OFF Mode

In this mode the transceiver is not able to operate. RxD, RxEN are set to high and ERRN is set to low. INH1 and INH2 are floating. The bus wires are not connected to GND (bus state: Idle_HZ).

7.5 Undervoltage Events

The device monitors the following three voltage supplies:

- **V$_{BAT}$**: Battery supply voltage

- **V$_{IO}$**: Supply voltage for I/O digital level adaptation

- **V$_{CC}$**: Supply voltage (+5V)

7.5.1 Undervoltage / Voltage Recovery V_{BAT}

If V_{BAT} voltage falls below VCC_{THL} for a time longer than t_{UV_DETECT} then an undervoltage V_{BAT} event is detected. Undervoltage recovery is detected if V_{BAT} exceeds the voltage threshold V_{BATTHH} for a time longer than t_{UV_REC}.

7.5.2 Undervoltage / Voltage Recovery V_{IO}

If V_{IO} voltage falls below VIO_{THL} for a time longer than t_{UV_DETECT} then an undervoltage V_{IO} event is detected. Undervoltage recovery is detected if V_{IO} exceeds the voltage threshold VIO_{THH} for a time longer than t_{UV_REC}.

7.5.3 Undervoltage / Voltage Recovery V_{CC}

If V_{CC} voltage falls below VCC_{THL} for a time longer than t_{UV_DETECT} then an undervoltage V_{CC} event is detected. Undervoltage recovery is detected if V_{CC} exceeds the voltage threshold VCC_{THH} for a time longer than t_{UV_REC}.

7.6 Power On/Off Events

- Starting from POWER-OFF mode a power-on event occurs in case V_{BAT} undervoltage recovery is detected.

- Starting from every operation mode a POWER-OFF event occurs in case V_{BAT} and V_{CC} undervoltage flags are set.
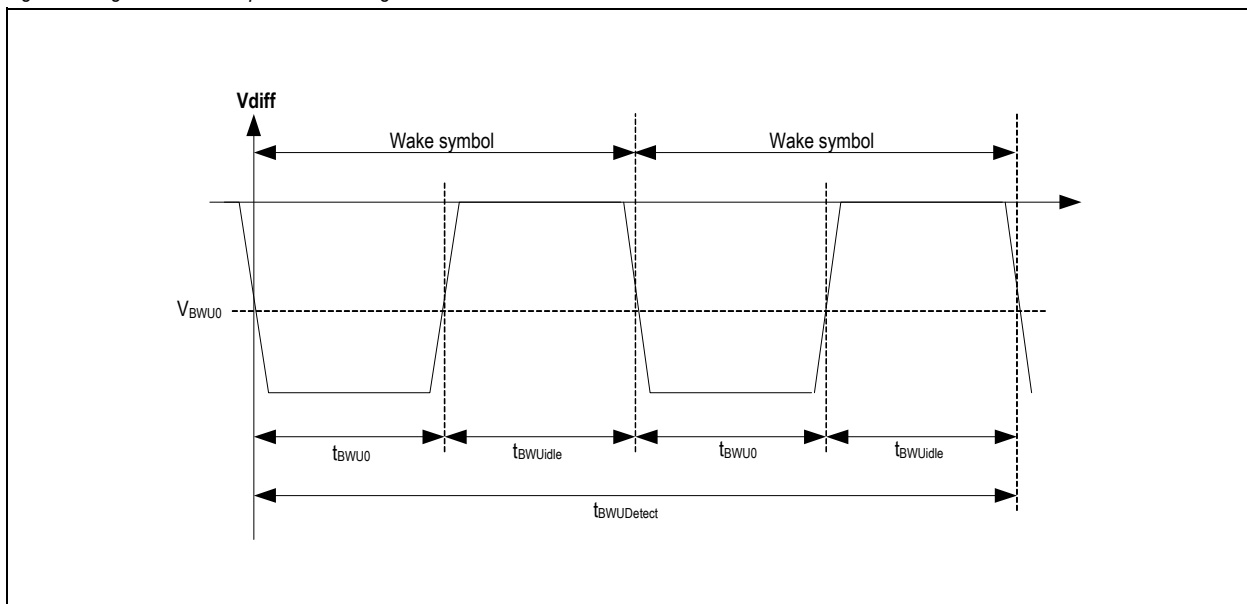
7.7 Wake-Up Events

A wake-up event is only detected in low-power modes.

7.7.1 Remote Wake-Up Event

A remote wake-up event, only possible in low-power modes, is detected if at least two consecutive wake-up symbols via the FlexRay bus within $t_{BWUDetect}$ are received. The wake-up symbol is defined as Data0 longer than t_{BWU0} followed by idle or Data1 longer than $t_{BWUIdle}$ shown in Figure 3.

Figure 3. Signal for Wake-up Pattern Recognition

7.7.2 Remote Wake-up with Frames

A valid wake-up event can be generated out of the standard FlexRay communication in 5 Mbps and 10 Mbps network configurations, while the data bits of the FlexRay Frame are set to "low" for a time longer than t_{BWU0} and set to "high" for time longer than $t_{BWUIdle}$ represent one wake symbol. A valid wake-up pattern consists of two wake symbols as shown in Figure 3.

In a 10Mbps speed configuration of the network, the payload of the frame is configured as follows:

- 1st wake symbol :   0x00 0x00 0x00 0x00 0x00 0xFF 0xFF 0xFF 0xFF 0xFF

- 2nd wake symbol :   0x00 0x00 0x00 0x00 0x00 0xFF 0xFF 0xFF 0xFF 0xFF

Repetitions of wake symbols might be required if network components are shortening valid Wake symbols (e.g. the time until the device is able to re-send wake symbols after wake-up).
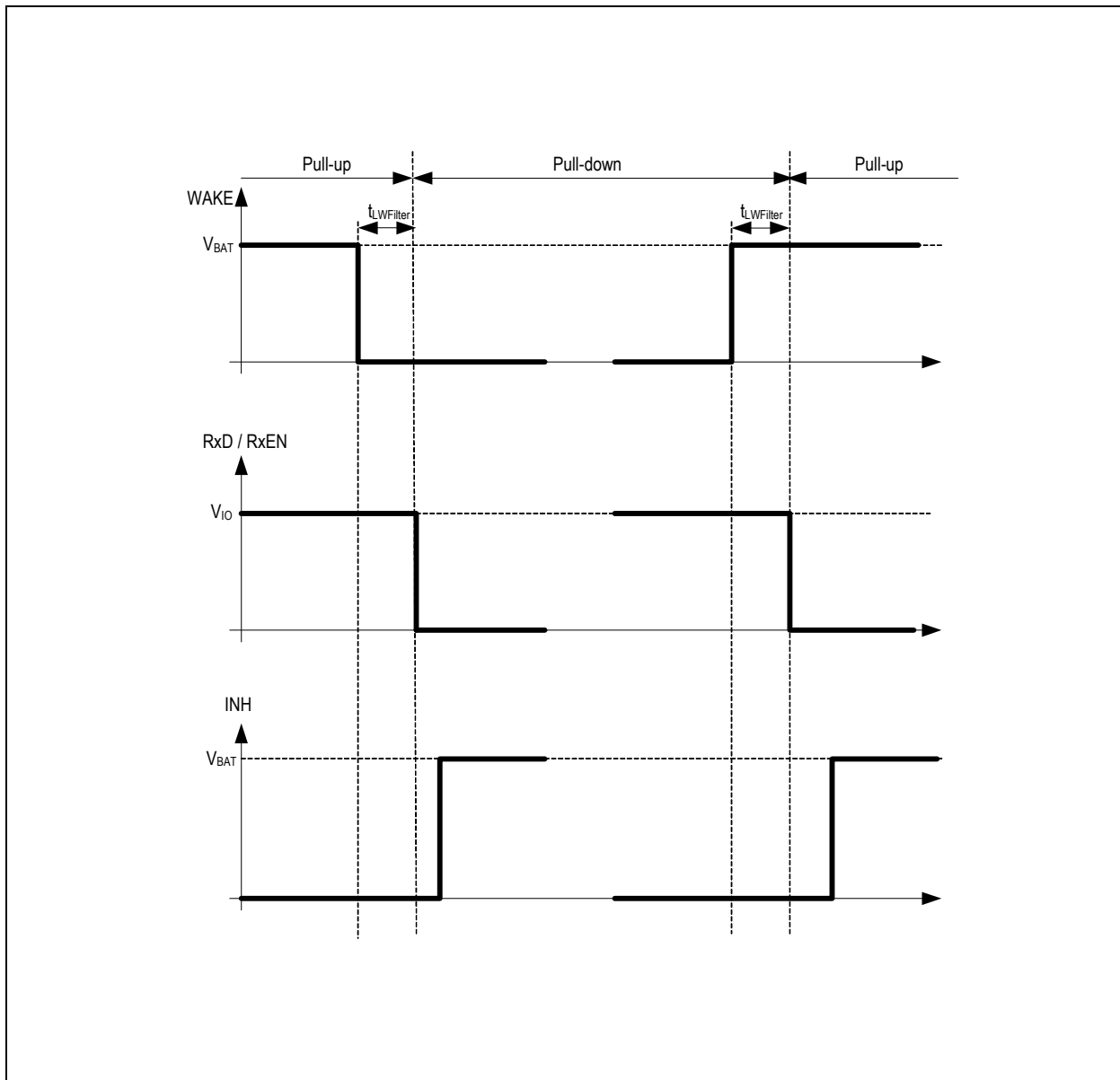
7.7.3 Local Wake-Up Event

In all low-power modes, if the voltage on the WAKE pin falls below V_{LWUTH} for longer than $t_{LWUFilter}$, a local wake-up event is detected. At the same time the biasing of the pin is switched to pull-down. As well a local wake up event is detected if the voltage on the WAKE pin rises above V_{LWUTH} for longer than $t_{LWUFilter}$, then biasing of the pin is switched to pull-up. The pull-up and -down mechanism is activated in low- and non-low-power modes.

7.8 Over-temperature Events

In NORMAL mode if the temperature exceeds OT_{TH}, the transmitter is deactivated. During this condition the device will remain in NORMAL mode.

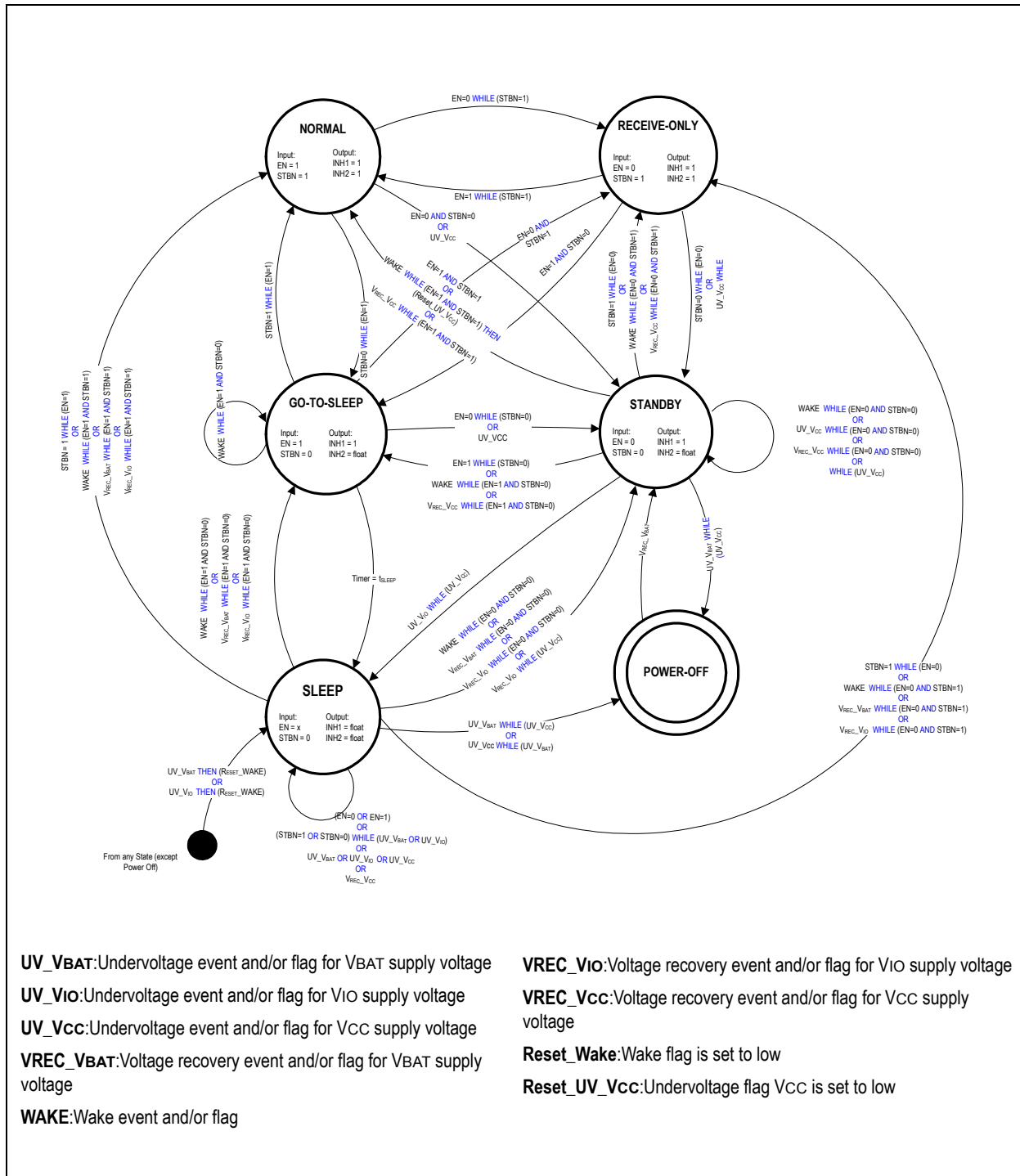The transmitter is activated again, if the temperature falls below OT_{TL}.

Figure 4. Wake Input Pin Behaviour

7.9 System Description

Figure 5. State Machine Diagram

UV_V$_{BAT}$:Undervoltage event and/or flag for V$_{BAT}$ supply voltage

UV_V$_{IO}$:Undervoltage event and/or flag for V$_{IO}$ supply voltage

UV_V$_{CC}$:Undervoltage event and/or flag for V$_{CC}$ supply voltage

VREC_V$_{BAT}$:Voltage recovery event and/or flag for V$_{BAT}$ supply voltage

WAKE:Wake event and/or flag

VREC_V$_{IO}$:Voltage recovery event and/or flag for V$_{IO}$ supply voltage

VREC_V$_{CC}$:Voltage recovery event and/or flag for V$_{CC}$ supply voltage

Reset_Wake:Wake flag is set to low

Reset_UV_V$_{CC}$:Undervoltage flag V$_{CC}$ is set to low

Notes:

1. This state diagram does not include all transitions, which are shown in Table 19.

2. Prefix of "WHILE" is an event and suffix in brackets checks the flags or in case of EN and STBN the input condition.
   - **For example:** V$_{REC\_VBAT}$ WHILE (EN=0 AND STBN=0)
   - After the event V$_{BAT}$ supply voltage recovery is detected, the transition is performed if EN and STBN are "low".

7.10 Fail Silent Behaviour

7.10.1 RxEN / BGE Timeout

In case no edges on RxEN and BGE are detected within $t_{TxEN\_timeout}$, the transmitter will stop transmitting the signals on RxD to the bus pins.

Transmission is only possible in case the BGE (Bus Guardian Enable) pin is set to high and if TxEN (Transmit Enable Not) is set to low (see Table 17).

7.10.2 State Transitions due to Undervoltage Detection

■ In case of V_{BAT} or V_{IO} undervoltage is detected, SLEEP mode will be entered regardless the status of EN and STBN.

■ In case V_{CC} undervoltage is detected, STANDBY mode will be entered regardless the status of EN and STBN.

■ V_{BAT} and V_{IO} undervoltage detection have higher priority than V_{CC} undervoltage detection.

■ In case undervoltage at V_{BAT} and V_{CC} is detected, POWER-OFF mode is entered (bus state: Idle_HZ).

7.10.3 State Transitions due to Voltage Recovery Detection

■ If the voltage recovers the device will enter the mode selected by the EN and STBN pins, in case no undervoltage is present at the other supply pins.

■ Starting from the POWER-OFF, the device enters the state selected by the host input pins (EN, STBN) only if V_{BAT} or V_{CC} recovers (V_{BAT} ≥ V_{BATTHH} or V_{CC} ≥ V_{CCTHH}) while V_{IO} is available (undervoltage flag of V_{IO} flag not set). If the V_{IO} undervoltage flag is set, the STANDBY mode will be entered. In both cases the Power-On flag is set.

■ If V_{BAT} ≤ V_{BATTHL} and V_{CC} ≤ V_{CCTHL} the device will be in POWER-OFF state, thus the bus wires are not terminated (bus state: Idle_HZ).

7.11 Mode Transitions

■ Starting from every operation mode the device enters POWER-OFF in case a power-off event occurs regardless the V_{IO} undervoltage flag, the wake-up flag and the host input pins (EN, STBN).

■ Starting from the POWER-OFF the device enters STANDBY only in case a power-on event occurs.

■ Starting from every operation mode the device enters SLEEP in case V_{BAT} or V_{IO} undervoltage flag is set regardless the V_{CC} undervoltage flag, the wake-up flag and the host input pins (EN, STBN).

■ Starting from every operation mode except SLEEP the device enters STANDBY in case V_{CC} undervoltage flag is set and V_{BAT} and V_{IO} undervoltage flags are not set, regardless the wake-up flag indication and the host input pins state.

■ Starting from a low-power mode the device enters the operation mode indicated by the host input pins if a wake-up event occurs.

■ In case all the undervoltage flags are reset the operation mode is selected by the wake-up flag and the host pins according to Table 18