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AS8506C

Battery Cell Monitor and Balancer IC

General Description

The AS8506C is a battery management IC dedicated to support cell voltage measurement, monitoring, cell balancing and temperature measurement functions in Li-Ion battery stacks for industrial/consumer/PV battery applications.

Ambient temperature range is from -40°C to +85°C.

It features cell voltage diagnosis with externally adjustable upper and lower cell voltage limits, fast cell voltage capture on request through 12-bit SAR ADC, passive cell balancing by simultaneous comparison of actual cell voltages with a reference cell voltage and temperature measurement on two external NTC sensors through 12-bit ADC.

Cells that are above reference will sequentially be discharged through integrated switches and one external resistor.

There is also an active balancing option AS8506C A through factory setting to sequentially charge cells which are below reference from an external DC-DC Flyback converter and an integrated low side driver.

The device can be used flexibly for battery stacks up to 7 cells with a minimum stack voltage of 6V and a maximum stack voltage of 32V.

It can be chained to support battery packs of virtually any number of cells in synchronized mode through chained clock and trigger signal.

The status of the battery stack is communicated to outside world through OR'd voltage_ok signal and balance ready signal.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS8506C, Battery Cell Monitor and Balancer IC are listed below:

Figure 1:
Added Value of using AS8506C

Benefits	Features
Reduce filter / synchronization effort. Acquired data have same time stamp to inherently generate accurate comparison results independent from load transients.	Simultaneous cell voltage capture for safe operating area (SOA) monitoring and balancing.
Strongly reduces data communication and data processing and thereby improves EMC robustness.	Autonomous balancing and SOA monitoring.
To compensate accumulative charge differences only. This mitigates cases of occasional wrong balance decisions due to flat OCV characteristic or mismatch in cell temperature	Autonomous passive balancing in the 100 mA range
Intrinsic inter module balancing through charge redistribution, efficiency improvement in case of leakage path due to defect induced leakage in particular cells.	Option for active charge balancing with very few external components.
For OCV capture, cell impedance calculation, diagnosis	Absolute cell voltage read out, read out of two temperature sensors.
Small form factor, low BOM	40-pin MLF (6x6) package, very low number of external components.

Applications

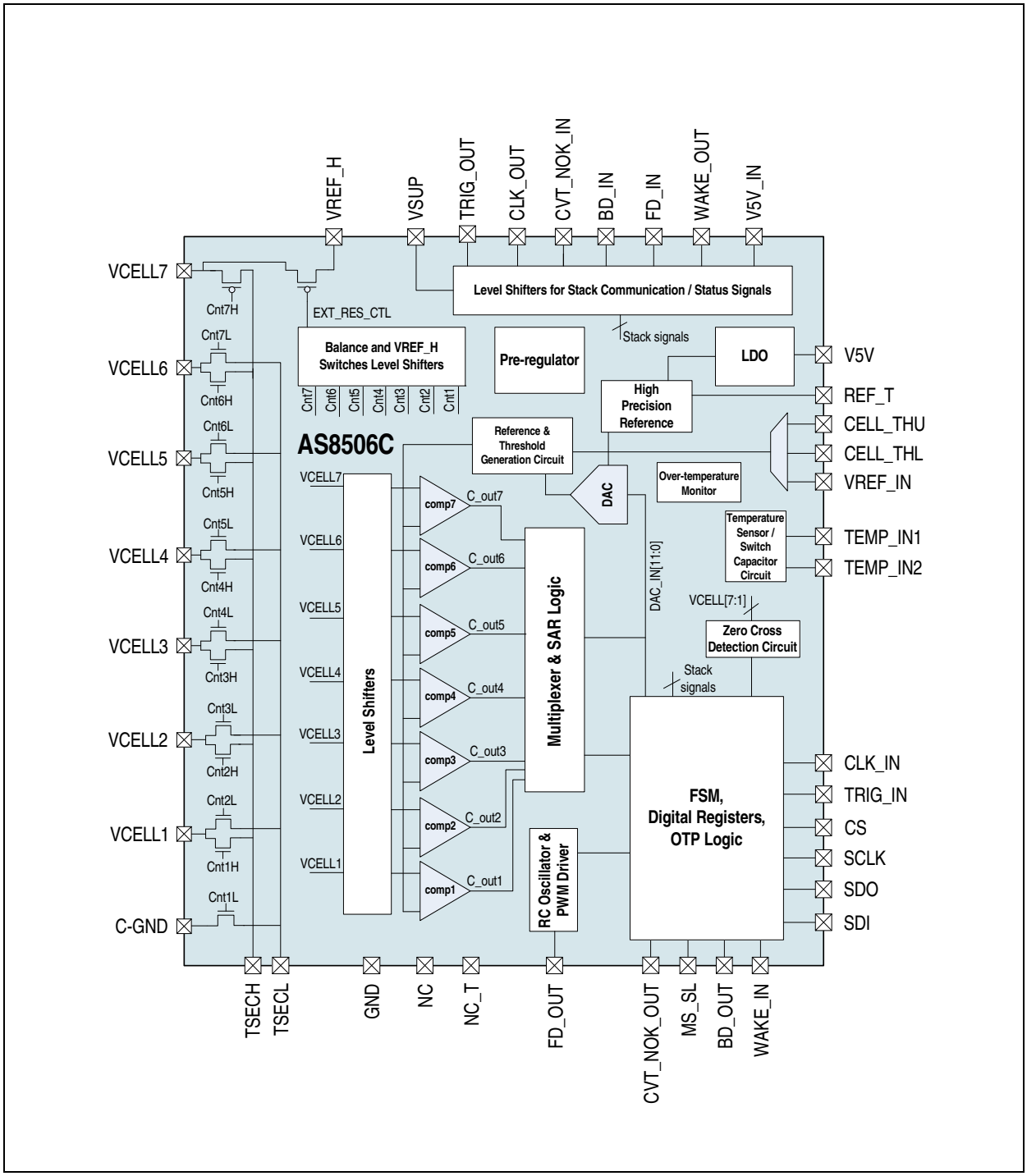
The applications of AS8506C include:

- The AS8506C is ideal for simultaneous cell monitoring and cell balancing in stacked energy storage systems. Current levels in the 100 mA range enables to compensate accumulative SOC mismatch over the entire cell pack.
- Typical applications are
  - Li-Ion batteries up to 200 cells,
  - Energy storage systems to buffer energy from PV panels or for emergency power supplies,
  - Battery management for e-scooters and e-bikes,

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
AS8506C Block Diagram



Pin Assignment

Figure 3:
Pin Diagram of AS8506C

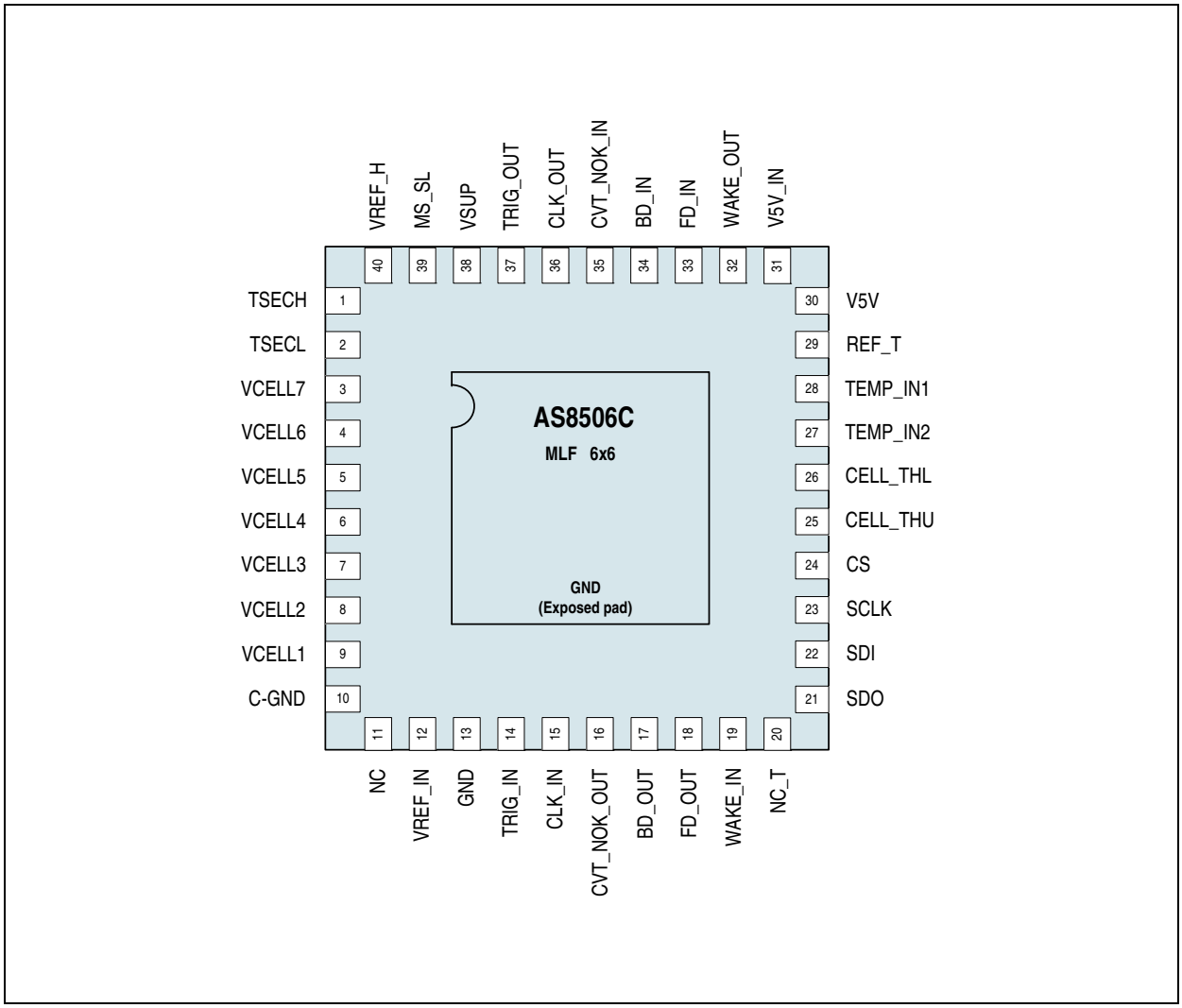


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	TSECH	Analog input / output	Flyback converter transformer secondary high side
2	TSECL		Flyback converter transformer secondary low side
3	VCELL7		Battery cell 7 high level pin
4	VCELL6		Battery cell 6 high level pin
5	VCELL5		Battery cell 5 high level pin
6	VCELL4		Battery cell 4 high level pin
7	VCELL3		Battery cell 3 high level pin
8	VCELL2		Battery cell 2 high level pin
9	VCELL1		Battery cell 1 high level pin
10	C-GND	Power supply input	Battery cell 1 low level pin
11	NC		Not connected
12	VREF_IN	Analog input / output	Cell voltage reference value (cell target voltage of battery)
13	GND	Power supply input	Ground to the IC
14	TRIG_IN	Digital input	This pin triggers the cell balancing in the device. Short pulse is for receiving status and continuous 'High' for cell balancing. It also acts as a data line during 3-wire communication.
15	CLK_IN		Clock input pin in the Slave device. This pin also acts as a clock during 3-wire communication. Scan clock in scan mode.
16	CVT_NOK_OUT	Digital output	This pin alerts when the cell voltage or the device/cell temperature is not within limits. During 3-wire communication, the CRC error is indicated on this pin. The internal device cell voltage or temperature status is ORed with CVT_NOK_IN on this pin.
17	BD_OUT		The 'device internal balance done' and 'balance done from above device' are ANDed on this pin. This pin in Master device indicates the complete system balance done. During address allocation process, this pin will be 'High' if BD_IN is 'High'.
18	FD_OUT		Flyback converter gate/opto coupler drive (pad is push-pull type) can drive up to 12mA.

Pin Number	Pin Name	Pin Type	Description
19	WAKE_IN	Digital input with pull-up	The wake pulse on this pin brings the IC into *NORMAL* mode. This pin has a pull-up resistor to the internal regulator. Should be driven with an open drain or external NMOS.
20	NC_T	Analog input / output	Not connected. Only used in Test mode.
21	SDO	Digital output	SPI data out
22	SDI	Digital input	SPI data in
23	SCLK		SPI clock
24	CS	Digital input with pull-up	SPI chip select
25	CELL_THU	Analog input / output	Cell voltage upper threshold
26	CELL_THL		Cell voltage lower threshold
27	TEMP_IN2		Temperature input2 to the IC (NTC input; if NTC is not connected, then should be connected to GND with 1K resistor).
28	TEMP_IN1		Temperature input1 to the IC (NTC input; if NTC is not connected, then should be connected to GND with 1K resistor).
29	REF_T		Supply to temperature sensor (Reference voltage to DAC and ADC).
30	V5V	Power supply input	LDO 5V output.
31	V5V_IN		Supply to the bottom IC from the cascaded top IC.
32	WAKE_OUT	Digital output open drain	Open drain o/p on the VSUP+5V domain. WAKE_IN information will be transmitted to top device.
33	FD_IN	Digital input	Flyback converter gate drive input in daisy chain connection. (If FD_IN is 'high' then FD_OUT will be PWM o/p in balance mode).
34	BD_IN	Digital input with pull-down	In cell stack system, the device gets balance done status of above device. During address allocation process if this pin is 'High', then the device address is decremented by '1'.
35	CVT_NOK_IN		Indicates cell voltage or temperature status of above device.

Pin Number	Pin Name	Pin Type	Description
36	CLK_OUT	Digital output	This pin propagates the clock to next device in the stack system. In case of Master device internal RC clock is transmitted on this pin to Slave device.
37	TRIG_OUT		This pin transmits the data fromTRIG_IN for balance and measurement phase. This pin is also used for propagating the data information to next device in stack system in SPI3.
38	VSUP	Power supply input	Supply to the IC.
39	MS_SL	Digital input	This pin informs the device whether it should act as the Master or Slave. If this pin is connected to GND, then device will act as Master. If this pin is connected to VSUP then device will act as Slave.
40	VREF_H	Analog input / output	High sides PMOS switch for external resistive divider. Input to VREF_IN can be taken from external resistive divider in one of the options.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units	Comments
Electrical Parameters						
V_{VSUP}	Voltage at positive supply pin	-0.3		42	V	VSUP pin
V_{GND}	Voltage at negative supply pin	-0.3		0	V	GND, C-GND; Reference potential
V_{V5V_IN}	Voltage at high side supply	-0.3		VSUP + 0.3	V	MS_SL,VREF_H, TSECH and TSECL
VSUP + V5V_IN	High side supply from top device	VSUP - 0.3		VSUP + 5.5	V	TRIG_OUT, CLK_OUT, CVT_NOK_IN, FD_IN, BD_IN, WAKE_OUT
V_{V5V}	Voltage at on LDO o/p pins	-0.3		7	V	**V5V** pin
V_{ESD}	Voltage on 5V pins	-0.3		V5V+0.3	V	All pins expect VSUP, VCELL1, VCELL2, VCELL3, VCELL4, VCELL5, VCELL6, VCELL7, MS_SL, WAKE_IN
VCELL1 to VCELL7	Voltage on pins VCELL1, VCELL2, VCELL3, VCELL4, VCELL5, VCELL6, VCELL7	-0.3		7	V	Applied cell voltages
I_{SCR}	Latch-up Immunity	-100		+100	mA	

Symbol	Parameter	Min	Typ	Max	Units	Comments
Electrostatic Discharge						
ESD	Electrostatic discharge voltage HBM standard (1)	±2			kV	VSUP, VREF_IN, SDI, SDO, CS, SCLK, CELL_THU, CELL_THL, TEMP_IN1, TEMP_IN2, REF_T, V5V, V5V_IN, MS_SL, VREF_H, NC_T
		±4				GND, C-GND, CELL1 – CELL7 (Cell-voltage pins,), TSECH, TSECL, TRIG_IN, TRIG_OUT, CLK_IN, CLK_OUT, CVT_NOK_IN, CVT_NOK_OUT, WAKE_IN, WAKE_OUT, FD_IN, FD_OUT, BD_IN and BD_OUT
Continuous Power Dissipation						
P_{tot}	Maximum power dissipation			1	W	
Temperature Ranges and Storage Conditions						
T_{stg}	Storage temperature	-55		150	°C	
R_{thj_36}	Thermal resistance package		30		°C/W	
T_{BODY}	Package body temperature			260	°C	Norm: IPC/JEDEC J-STD-020 (2)
MSL	Moisture Sensitive Level	3				

Note(s) and/or Footnote(s):

1. Human body model: R = 1.5kΩ; C = 100pF.
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices".

Typical Operating Characteristics

All defined tolerances for external components in this specification need to be assured over the whole operation conditions range and also over lifetime.

Figure 6:
Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
VSUP	Positive supply voltage	6		32	V	Normal operating condition
VSS	Negative supply voltage	-0.3		0	V	With reference to all the voltages
T_{AMB}	Ambient temperature	-40		85	°C	Maximum junction temperature (T_J) 115°C
$I_{SUPP, nom}$	Supply current, *NORMAL* mode	2	3	6	mA	VSUP=32V, in *NORMAL* mode
	Supply current, *NORMAL* mode, With External Components	15	20	40	mA	VSUP=32V, in the balancing phase with stack connection (50% PWM duty cycle)
$I_{SUPP, sleep}$	Supply current, *SLEEP* mode	10	17	35	µA	

Electrical Characteristics

Device Level Specifications

-40°C < Tj < 115°C.

Figure 7:
Device Level Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
Vcell_in	Cell Input voltage measurement	1.8		4.5	V	
ADC/DAC	ADC/DAC Reference		±7	±15	mV	0 hour, specification does not include solder stress / board stress effects
DAC_error	Error of the DAC		2		mV	0.1% error because of the DAC/Guaranteed by design
Com_off	Error because of the comparator resolution		1		mV	Guaranteed by design
Sign_path_accuracy	Signal path accuracy		±5	±15	mV	Typical value is from the lab evaluation data. Maximum value is from the test data. 0 hour accuracy, specification does not include solder stress / board stress effects.
$T_{INITIALIZATION}$	Initialization time			50	ms	After Initialization, the system will go to sleep mode and waits for wake signal.
$T_{WAKE-UP}$	Wake up time from the Wake signal to system wait mode			75	ms	After wake signal, device enters into wait mode and stays for two seconds for TRIG_IN signal, if no TRIG_IN event occurs, device goes to sleep mode.
Tmeas	Cell voltage and Temperature measurement time		16		ms	At10KHz clock time
Tspi3_read5k	SPI3 read time for single channel measurement		13.6		ms	At 5KHz clock time
Tspi3_read20k			3.4			At 20KHz clock time
Tspi3_read40k			1.7			At 40KHz clock time

Low Dropout Regulator (5V Output LDO)

-40°C < T_J < 115°C; all voltages are with respect to ground (GND); positive current flows into the pin, *NORMAL* operating mode, if not otherwise mentioned. The LDO block is a linear voltage regulator, which provides a regulated 5V.

Figure 8:
LDO Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{SUP}	Input supply voltage	6	12	32	V	
V5V	Output voltage range	4.75	5.0	5.25	V	
I_{LOAD}	Load Current			50	mA	
ICC_SH	Output short circuit current		85	250	mA	*NORMAL* mode
PSRR	PSRR		60		dB	f=1kHz / No production test
			35			f=1MHz / No production test
CL1	LDO output Capacitor 1	2.2		10	µF	Electrolytic
ESR1		1		10	Ω	
CL2	LDO output Capacitor 2	100		220	nF	Ceramic
ESR2		0.02		1	Ω	

Note(s) and/or Footnote(s):

1. In *NORMAL* mode, maximum load current will be 50mA. After internal thermal shutdown, current limit is 20mA.
2. The LDO is disabled in *SLEEP* mode.

High-precision Bandgap Reference

-40ºC < T_J < 115ºC; all voltages are with respect to ground (GND).

Figure 9:
Bandgap Reference Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
BG_Out	Reference output after trim	1.2	1.235	1.27	V	After temperature trim
BG_out_T_{var}	Reference variation with respect to Temperature		±2.5	±4	mV	After trim on the absolute
PSRR1K	PSRR at 1KHz	20			dB	No production test
PSRRDC	PSRR at DC	80			dB	

Note(s) and/or Footnote(s):

1. This bandgap output is the reference for the V5V (LDO) regulator.

Digital to Analog Converter

-40ºC < T_J < 115ºC; all voltages are with respect to ground (GND).

Figure 10:
Digital to Analog Converter

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{SUP_DAC}	Input supply voltage	4.75	5	5.25	V	LDO output as supply
V_{INREF}	Input reference voltage	4.485	4.5	4.515	V	After absolute trim at 0 hours, specification does not include solder stress/board stress effects
D_{IN}	Resolution		12		bits	Guaranteed by design
F_{DAC}	Update rate		10		KHz	No production test
T_{SETT_DAC}	Settling time		50		µs	
DAC_{INL}	INL		±4		LSB	
DAC_{DNL}	DNL		±0.5		LSB	

Analog to Digital Converter

-40ºC < T_J < 115ºC; all voltages are with respect to ground (GND).

Figure 11:
Analog to Digital Converter

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{SUP}	Input supply voltage	4.75	5	5.25	V	LDO output as supply
V_{INREF}	Input reference voltage	4.485	4.5	4.515	V	After absolute trim at 0 hours, specification does not include solder stress/board stress effects
D_{OUT}	Resolution		12		bits	
T_{MEAS_ADC}	Measurement time per channel		1.4		ms	
ADC_{INL}	INL		±4		LSB	No production test.
ADC_{DNL}	DNL		±2		LSB	No production test.

Pre-Regulator

This Pre_reg is an internal regulator which provides supply to digital and a few analog blocks..

-40ºC < T_J < 115ºC; all voltages are with respect to ground (GND).

Figure 12:
Pre-reg Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{SUP}	Input supply voltage	6	12	32	V	
P5V	Prereg_output voltage range	4.3	5.0	5.5	V	
3V3	3.3V_output voltage range	2.8	3.3	3.6	V	

PWM Driver

40°C < T_J < 115°C; all voltages are with respect to ground (GND).

Figure 13:
PWM Driver

Symbol	Parameter	Min	Typ	Max	Unit	Note
V5V	Output voltage	4.5	5	5.5	V	
F_{PWM}	Frequency of PWM	25	100	200	KHz	CMOS load mode, Optocoupler load mode
F_{Duty}	Duty cycle	22	25	28	%	
		12	15	18	%	
		17	20	23	%	
		27	30	33	%	
		30	35	38	%	
		37	40	43	%	
		42	45	48	%	
		47	50	53	%	
F_{duty_error}	Duty cycle error	7	12	20	%	
tr_{pwm}	Rise time	30	50	80	ns	CMOS load mode, Optocoupler load mode Guaranteed by design
tf_{pwm}	Fall time	30	50	80	ns	
$Idrive_{opto}$	Driver strength		10	12	mA	Optocoupler load mode
$Cload_{fd\_out}$	Driver switch load capacitance		60	100	pF	

PWM Oscillator

-40°C < T_J < 115°C; all voltages are with respect to ground (GND).

Figure 14:
PWM Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{OSC}	Frequency	90	100	110	kHz	• After the frequency trim. • Programmable frequency options for 25KHz, 50KHz and 200KHz are available.
f_{OSC_ACC}	Accuracy		±15		%	

Oscillator for Digital Circuit

-40°C < T_J < 115°C; all voltages are with respect to ground (GND).

Figure 15:
Oscillator for Digital Circuit

Symbol	Parameter	Min	Typ	Max	Unit	Note
$f_{OSC-DIG}$	Frequency	9	10	11	kHz	Oscillator for Digital circuit
f_{OSC_ACC}	Accuracy		±15		%	

External Temperature Thresholds

-40°C < T_J < 115°C; all voltages are with respect to ground (GND).

Figure 16:
External Temperature Thresholds

Symbol	Parameter	Min	Typ	Max	Unit	Note
Ref_ext_warn/sutdown	Code 0000	3.084	3.165	3.238	V	16 reference thresholds are with a step of 66mV.
	Code 0001	3.148	3.231	3.306		
	Code 0010	3.213	3.297	3.373		
	Code 0011	3.277	3.363	3.441		
	Code 0100	3.341	3.429	3.508		
	Code 0101	3.406	3.495	3.576		
	Code 0110	3.470	3.561	3.643		
	Code 0111	3.534	3.627	3.711		
	Code 1000	3.599	3.693	3.779		
	Code 1001	3.663	3.759	3.846		
	Code 1010	3.727	3.825	3.914		
	Code 0011	3.792	3.891	3.981		
	Code 0100	3.856	3.957	4.049		
	Code 0101	3.920	4.023	4.116		
	Code 0110	3.984	4.089	4.184		
	Code 0111	4.049	4.155	4.25		

Ron of the Shuttle Switches (Internal Switch for Charging/Discharging)

-40°C < T_J < 115°C.

Figure 17:
Ron of the Shuttle Switches

Symbol	Parameter	Min	Typ	Max	Unit	Note
Ron_shut	Shuttle switch ON resistance		5	20	Ω	The maximum charging/discharging current limit through shuttle switch is 100mA. Only for Cell1 maximum charging/discharging current is limited to 30mA less than 2V of cell voltage at 115 junction of cell voltage.

Over-Temperature Measurement

Figure 18:
OTM Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{jshut}	Shut down temperature	115	135	145	°C	Junction temperature for Shutdown
T_{jwarn}	Warning temperature	100	125	140	°C	Junction temperature for Warning
T_{jrecv}	Recovery temperature	100	115	130	°C	Junction temperature for Recovery

Weak Cell Detection (Voltage Comparator)

Figure 19:
Weak Cell Detection

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CELL}	Supply voltage	-0.3	3.6	4.5	V	
V_{LOW}	Low voltage detection	-100		100	mV	
Tl_spike	Minimum input spike filter		2		µs	No production test. Programmable option.
			4			
			6			
			8			

Power on Voltage Detection

Figure 20:
Power on Voltage Detection

Symbol	Parameter	Min	Typ	Max	Unit	Note
VSUP_POR	VSUP Power-on-Reset threshold ON	5.2	5.5	5.8	V	Rising edge of VSUP
VSUP_RESET	VSUP Power-on-Reset threshold OFF	4.6	4.85	5.1	V	Master reset for device
V5V_IN_POR	V5V_IN Power-on-Reset threshold ON	3.8	4.45	4.8	V	Voltages are with respect to VSUP measure as pass fail test
V5V_IN_RESET	V5V_IN Power-on-Reset threshold OFF	3.6	4.1	4.5	V	
V5V_POR	V5V Power-on-Reset threshold ON	4.1	4.5	4.7	V	Rising edge of V5V
V5V_RESET	V5V Power-on-Reset threshold OFF	3.8	4.1	4.3	V	Falling edge of V5V

Electrical Characteristics for Digital Inputs and Outputs

All pull-up, pull-downs have been implemented with active devices.

Figure 21:
Digital Inputs and Outputs

Port Type	Symbol	Parameter	Min	Typ	Max	Unit	Note
CS							
INPUT Schmitt Trigger	Vt-	Negative-going threshold	1.62		2.22	V	V5V=5V
	Vt+	Positive-going threshold	2.27		3.42	V	
	I_{lil_cs}	Pull-up current	-100		-30	µA	In CS pad, Pulled up to V5V. (ISUP_HV)
SDO							
OUTPUT Tristate	V_{OH}	High level output voltage	2.5			V	
	V_{OL}	Low level output voltage			0.4	V	VSUP ≥ 6V
	V_{IH}	High level input voltage	0.7*V5V			V	
	V_{IL}	Low level input voltage			0.3*V5V	V	
	I_O	Output drive current			4	mA	
SCLK, SDI							
IO Buffer	V_{IH}	High level input voltage	0.7*V5V			V	
	V_{IL}	Low level input voltage			0.3*V5V	V	

Port Type	Symbol	Parameter	Min	Typ	Max	Unit	Note
CVT_NOK_OUT							
OUTPUT Buffer	V_{OH}	High level output voltage	2.4			V	
	V_{OL}	Low level output voltage			0.4	V	VSUP ≥ 6V
	I_O	Output drive current			2	mA	
BD_OUT							
OUTPUT Buffer	V_{OH}	High level output voltage	2.4			V	
	V_{OL}	Low level output voltage			0.4	V	VSUP ≥ 6V
	I_O	Output drive current			1	mA	
TRIG_OUT, CLK_OUT							
OUTPUT Buffer	V_{OH}	High level output voltage	2.4			V	
	V_{OL}	Low level output voltage			0.4	V	VSUP ≥ 6V
	I_O	Output drive current			4	mA	
FD_OUT							
OUTPUT Buffer	V_{OH}	High level input voltage	2.4			V	
	V_{OL}	Low level input voltage			0.4	V	VSUP ≥ 6V
	I_O	Output drive current			24	mA	
MS_SL							
INPUT Buffer	V_{IH}	High level input voltage			VSUP	V	High voltage input pad
	V_{IL}	Low level input voltage			0.3*V5V	V	
CLK_IN, TRIG_IN							
INPUT Schmitt Trigger	Vt-	High level input voltage	1.62		2.22	V	
	Vt+	Low level input voltage	2.27		0.3*V5V	V	

Port Type	Symbol	Parameter	Min	Typ	Max	Unit	Note
FD_IN,BD_IN, CVT_NOK_IN							
INPUT Buffer	V_{IH}	High level input voltage	0.7*V5V			V	
	V_{IL}	Low level input voltage			3.42	V	
WAKE_IN Pull up current	Ipull_up	Pull-up current	-100		-30	µA	Internal pull

Note(s) and/or Footnote(s):

1. Test limits for Iih and Iil are 1.0uA and -1.0uA for input pads.

Detailed Description

The device consists of the following blocks:

- PWM driver
- LDO_5V with 5V / 50mA output
- Temperature monitor block
- High precision bandgap reference
- DAC for the reference voltage generation
- SAR ADC for cell voltage and external temperature measurement
- Oscillators for PWM drive and for the digital logic
- Pre-Regulator
- SC Comparator
- Weak cell detection logic
- PORs on different supplies

Voltage Regulator (LDO_5V)

Power input to the LDO is VSUP pin. It is switched ON when the device is in *NORMAL* mode and switched OFF in *SLEEP* mode. The LDO takes the input from Bandgap and scales it up to the required voltage. It starts charging only after entering *NORMAL* mode. This LDO is the supply for DAC, the PWM driver and Cell voltage comparators.It's additional features are as follows:

- Stability is better than ±2.5% over input range.
- Load current up to 50mA.

High Precision Bandgap (HPBG)

AS8506C has a high precision bandgap to generate accurate reference. This reference voltage is used to generate reference for DAC and ADC.

HPBG is trimmed with respect to temperature. Variation of the bandgap with temperature is ±4mV in the temperature range from -40ºC to 115ºC.

External Temperature Monitor and Measurement

Two sensor inputs TEMP_IN1 and TEMP_IN2 with a comparator on each pin, are available. If the temperature sensor connected to TEMP_IN1 crosses its threshold, then a warning flag is set in the device (status can be read through SPI) and the device will continue balancing.

If the temperature sensor connected to TEMP_IN2 crosses its threshold, then a flag is set in the device and balancing is stopped; but the device continues to stay in *NORMAL* mode for maintaining synchronism. In both the cases, the microcontroller will be interrupted by a pulse on CVT_NOK_OUT pin.

In case the external temperature sensors are not being used, then both the inputs must be connected to GND pin through 1k resistor. In the measurement phase, external temperature is measured through the SAR ADC. Both channels of temperature will be measured and stored in temp_in1_lsb_reg to temp_in2_msb_reg.

Internal Temperature Monitor

The internal temperature monitor has two thresholds at T_{jwarn} 125°C and T_{jshut} 135°C. If the internal temperature exceeds 125°C, then a warning flag is set in the device (status can be read through SPI) and the device will continue balancing.

If the internal temperature exceeds 135°C, then a flag is set in the device and balancing is stopped; but the device continues to stay in *NORMAL* mode for maintaining synchronism. In both the cases, the microcontroller will be interrupted by a pulse on CVT_NOK_OUT pin. The balance recovery temperature is 115°C.

PWM Generator

In the Balance phase of the AS8506C, based on the decision made during the Compare phase, some part of the cell is charged with the Flyback converter. To drive the external Flyback converter, AS8506C generates a PWM signal to drive external FET or Optocoupler or Isolation device.

The frequency and of the PWM generator can be controlled by timer_cntl_reg register.

PWM frequency is not used for the passive balancing.

RC Oscillator

The AS8506C has a trimable RC oscillator. It is designed to generate $f_{osc\text{-}dig}$ clock for the digital circuit and for the clocking of the IC. Each oscillator will be trimmed with the process to get the accuracy to $f_{osc\text{-}accy}$ with 5-bit OTP Factory trim code.

DAC for the Reference Generation

AS8506C has a 12-bit DAC to generate the cell reference voltage, cell threshold low and high voltage. The DAC code is written into AS8506C with SPI interface from microcontroller. The output of the DAC is given to one of the inputs of the comparators, to compare the cell voltages synchronously. Reference for the DAC is 4.5V, which is internally generated and is available as reference for temperature inputs on REF_T.

SAR ADC

AS8506C has a 12-bit SAR ADC to measure the cell voltage and external temperature. The SAR ADC uses the 12-bit DAC to generate the digital code. The SAR ADC range is 1.8V to 4.5V for cell voltage measurement and 0.2V to 4.5V for the temperature measurement.

Cell voltage and temperature is measured in the short trigger phase. After the trigger goes 'high', compare phase starts and then all the cell voltages and external temperature are measured and stored in the digital registers.

Pre-Regulator

AS8506C has an internal pre-regulator, which generates supply voltages for the internal blocks. Pre-Regulator output is used as a supply for the oscillators. All the digital logic and the FSM will work on the pre-regulator supply.

In *SLEEP* mode only the pre-regulator will be working along with the WAKE_IN detect circuit.

Cell Threshold

AS8506C has the potential to set the two threshold levels to the cell voltage through pins CELL_THU and CELL_THL. These values can be set externally, (or) through OTP trim bits, (or) from the external microcontroller by writing DAC code into the cell threshold registers in the register space.

Weak Cell Detection

AS8506C has the ability to detect the weak cell. During load conditions, if the cell reaches voltage of about 0.1V to -0.2V, then this variation is detected and stored in the zero cross detection register. This event is indicated to the master device by a pulse on CVT_NOK_OUT pin in Compare and Balance phase. The master device indicates the microcontroller by setting CVT_NOK_OUT 'high'. In *WAIT* mode only this will be stored in the register; there won't be any CVT_NOK_OUT to µC. The register is cleared on µC reading.

External Resister Divider Control

AS8506C has the provision to enable the external divider to give the desired cell voltage to the at VREF_IN pin. External resister divider can be connected between VREF_H pin to ground. Typical internal ON resistance of the VREF_H switch is 30Ω.Calculate the external resister divider values such that the output of the divider will provide the desired reference value. When comparison is not happening, this divider can be disabled using SPI. PORs on Different Supplies