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Datasheet: AS8515 Data Acquisition System with Power Management and LIN Transceiver for 12V Battery Sensor Applications

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AS8515

Data Acquisition System with Power Management and LIN Transceiver for 12V Battery Sensor Applications

1 General Description

The AS8515 is designed for simultaneous measurement of shunt current sensor signal and battery voltage by two independent ADC channels. Both channels can measure small signals up to ±160 mV versus ground through programmable gain amplifier or larger signals in the 1V range without amplifier. After analog to digital conversion and digital filtering, the resulting digital values are accessible through 4-wire serial interface. The device is powered directly from the battery through LDO and provides a 3.3V supply for an external microcontroller. For communication with the next level ECU, the device offers a LIN 2.1 transceiver. Measurement of battery voltage is supported through resistive attenuator with disable for power saving in standby.

The device is a stacked die system providing a high voltage CMOS IC for power management and transceiver functions as a ***Top die*** and low voltage sensor interface functions as a ***Bottom die*** inside a 32-pin MLF (5x5 mm) package.

2 Key Features

- A precision voltage attenuator with power down facility
- LIN 2.1 transceiver
- Power-On Reset with OTP adjustable reset timeout and brown-out detection
- A window Watchdog function in the normal mode and a timeout Watchdog in the device standby mode as a factory option
- Load dump protection (42V) for all battery supplied pins, LIN bus pin, and Enable pin
- Internal reverse polarity protection (up to -27V) for all battery-sensing pins, and LIN bus pin
- Over temperature warning & shutdown functions
- Two independent high resolution A/D converters with programmable over sampling ratio
- Programmable sampling rate up to 4kHz throughput
- Programmable gain, low noise amplifier for current channel with gain stages 5, 25, 40, 100
- Internal temperature sensor
- Synchronous acquisition for both ADC channels
- Reference-voltage source (high precision and high stability)
- Offset auto zero architecture on both channels
- Current monitoring comparator with interrupt signal generation and µC clock enable. Timer with 2 related outputs for single shot sampling of current and voltage channel in low power mode.
- Precision on chip RC oscillator or external clock. Low slew, low EMC clock output which can be used by external microcontroller which is enabled respectively disabled by mode control through SPI and interrupt from current monitor in low power mode.

The integrated circuit can execute measurements with internal and external sensors and sources for the voltage channel and with external sensor for the current channel.

External Sensors:

- Current measurement via Shunt resistor (4 ranges)
- Battery voltage (internal voltage divider to battery)
- ETR and ETS for external temperature sensor (with switchable current source)

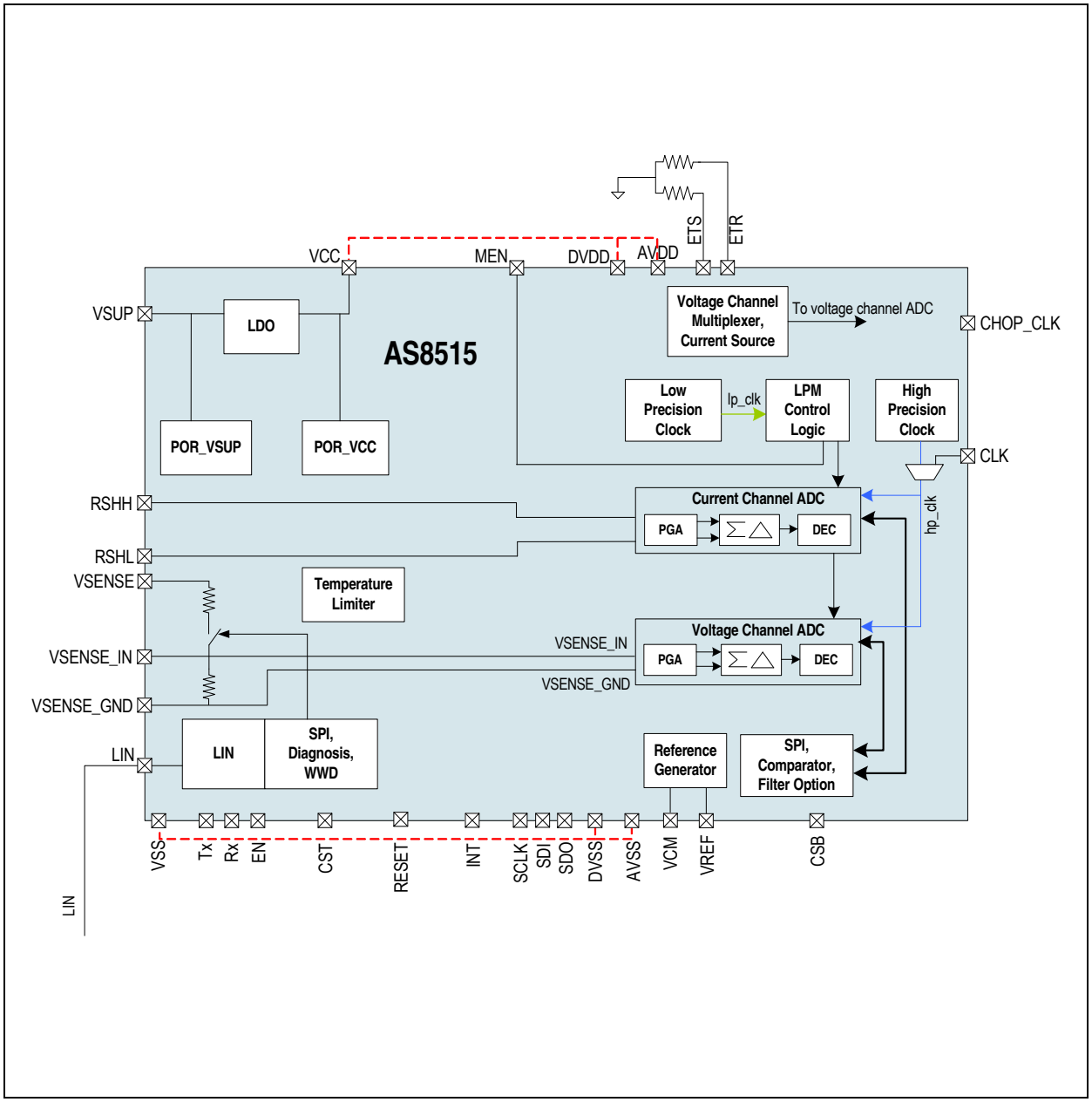
Internal Sensors:

- On chip temperature sensor
- Internal current sources for functional test of measurement path and the connection of shunt resistor

3 Applications

The AS8515 is suitable for battery sensors, having shunt current sensor at minus pole. For lead acid, AGM, Li-Ion batteries up to 18V nominal, 42V over voltage capability.
The device is also ideal as a general purpose sensor interface for automotive LIN slaves.

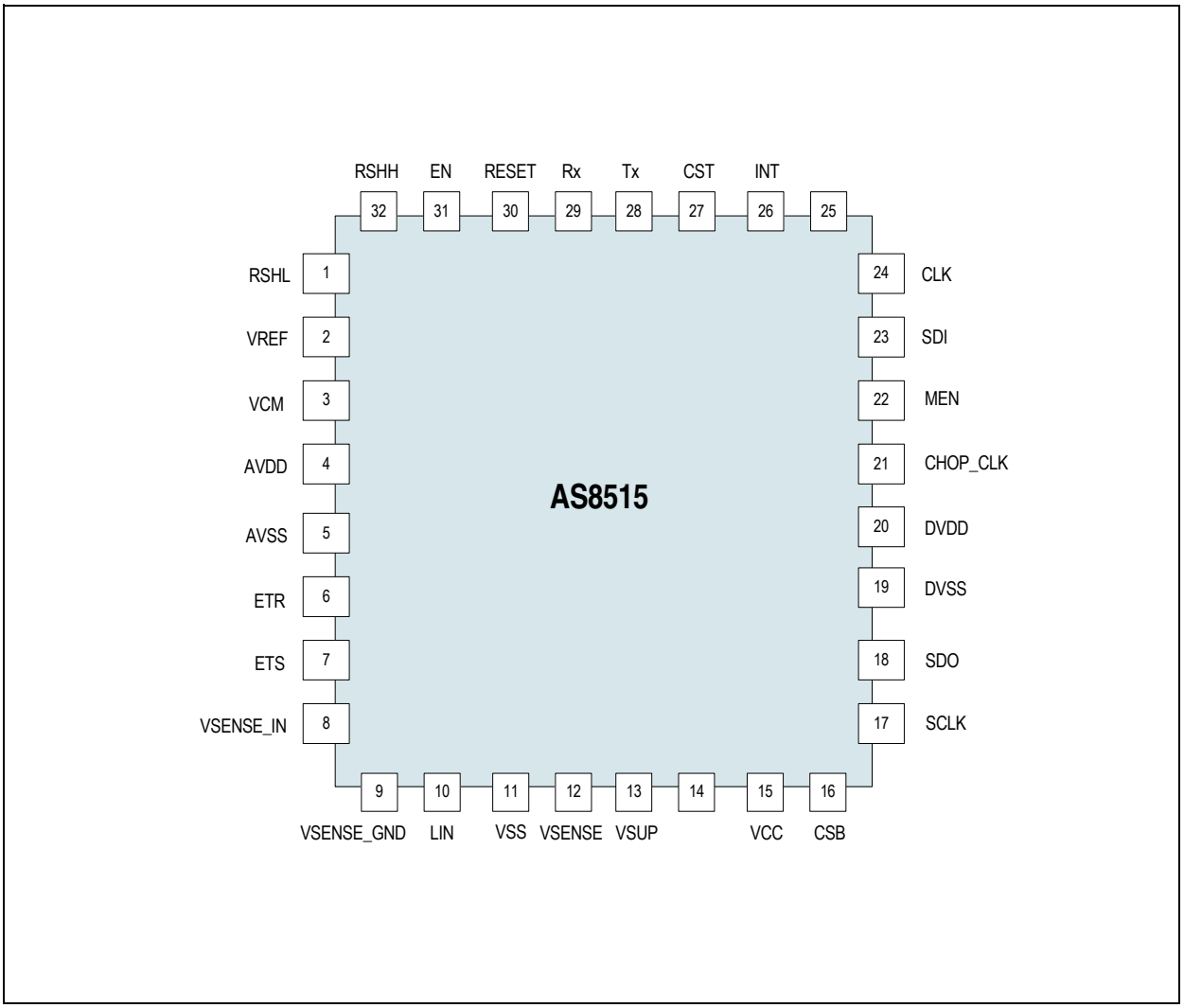
Figure 1. AS8515 Block Diagram



Contents

4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
RSHL	1	Analog input	Negative differential input for current channel
VREF	2	Analog output	Internal reference voltage to Sigma Delta ADC; Connect 100nF to AVSS from this pin.
VCM	3	Analog output	Common mode voltage to the internal measurement path; Connect 100nF to AVSS from this pin.
AVDD [1]	4	Analog input	+3.3V Power-supply; Supplied by LDO output (VCC) in ***Top die***; Should be shorted to pin 21 (VCC) externally.
AVSS [2]	5	Power supply	0V Power-supply Ground analog

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
ETR	6	Analog input	Voltage channel single ended input
ETS	7		
VSENSE_IN	8	Analog I/O	Battery voltage attenuator output and voltage channel input
VSENSE_GND	9	Analog input	Input signal for voltage channel (low)
LIN	10	Analog I/O	LIN BUS
VSS [2]	11	Power supply	0V Power-supply Ground analog
VSENSE	12	Analog input	Battery voltage input Connect 100nF to VSS from this pin.
VSUP	13	Power supply	Supply input from battery (through external reverse polarity protection device)
-	14	-	-
VCC [1]	15	Analog output	Regulated 3.3V output supply for loads up to 50mA
CSB	16	Digital input	Chip select for ***Bottom die***
SCLK	17	Digital input	Clock signal SPI
SDO	18	Digital output	Data signal SDO
DVSS[2]	19	Power supply	0V Power-supply digital
DVDD [1]	20	Analog input	+3.3V Power-supply; Supplied by LDO output (VCC) in ***Top die***; Should be shorted to pin 21(VCC) externally.
CHOP_CLK	21	Digital output	Chopper clock
MEN	22	Digital I/O	Digital output for ***Bottom die*** in SBM mode[3] and input for ***Top die***
SDI	23	Digital I/O	Data signal SDI
CLK	24	Digital I/O	Internal/External digital clock signal
-	25	-	-
INT	26	Digital I/O	Interrupt not: Wake-up, digital interrupt, ready flag 2
CST	27	Digital input	Chip select for ***Top die***
Tx	28	Digital I/O	LIN transceiver transmit pin
Rx	29	Digital I/O	LIN transceiver receive pin
RESET	30	Digital output	Reset output (open drain)
EN	31	Digital input	Enable input
RSHH	32	Analog input	Positive differential input for current channel

1. Pin #4, pin #20 and pin #21 needs to be shorted externally on the board. Pin #21 is the LDO output that supplies pin #4 and pin #20.
2. Pin #5, pin #11 and pin #19 needs to be shorted externally on the board as they are the grounds.
3. Use as output port only.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 8 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units	Comments
Electrical Parameters						
VSUP	Supply voltages	-0.3		42	V	
VSENSE	Battery voltage inputs	-27		42	V	
AVDD, DVDD	DC supply voltage	-0.3		5	V	
EN	Enable input	-0.3		42	V	
VCC	Regulated output supplies	-0.3		5	V	VCC generated by ***Top die*** must not be larger than 5V on board level as it has to be connected with ***Bottom die*** AVDD and AVCC
LIN	LIN bus	-27		40	V	
	Analog & digital inputs and outputs	-0.3		5	V	
	Input current (latch-up immunity)	-100		100	mA	Norm: AEC-Q100 – or Jedec 78
Electrostatic Discharge						
ESD	Electrostatic discharge Norm: AEC-Q100	±6			kV	LIN, VSS
		±4			kV	VSUP, VSENSE
		±2			kV	All other pins
Continuous Power Dissipation						
P_{tot} [1]	Total operating power dissipation (all supplies and outputs)			0.375	W	MLF-32 in still air, soldered on JEDEC standard board @125º ambient, static operation = no time limit
Temperature Ranges and Storage Conditions						
R_{Θ}	Package thermal resistance		34	40	ºC/W	
T_{stg}	Storage temperature	-55		150	ºC	
T_J	Junction temperature			130	ºC	
T_{BODY}	Package body temperature			260	ºC	*The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices". The lead finish for Pb-free leaded packages is matte tin (100% Sn).*
	Soldering conditions			250	ºC	
	Humidity non-condensing	5		85	%	

1. Total power dissipation cannot exceed 0.375W to avoid increase in junction temperature, i.e. greater than 130ºC. VCC LDO can supply current externally, which is not greater than 17mA at 18V VSUP and 20mA at 16V VSUP.

6 Electrical Characteristics

Unless otherwise noted in this specification, all defined tolerances of parameters are assured over the whole operation conditions range and also over lifetime.

6.1 Operating Conditions

Table 3. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{SUP}	Supply voltages	4.3		18	V	
V_{SENSE}	Battery voltage input	4.5		18	V	
AVDD	Positive supply voltage	3.15		3.45	V	
AVSS	Negative supply voltage	0		V		
DVDD	Positive digital supply voltage	3.15		3.45	V	Referring to DVSS, Typical ±10%
DVSS	Negative digital supply voltage	0			V	
LIN	LIN bus	0		18	V	
EN	Enable input	0		18	V	
VCC	Regulated output supply	3.15		3.45	V	
T_{AMB}	Ambient temperature	-40		115	ºC	Maximum junction temperature (T_J) is 130ºC
I_{SUP} [1]	Supply current			27	mA	
f_{CLK}	System clock frequency		8.192		MHz	When external clock is selected, internal clock will be 4.096 MHz

1. Total power dissipation cannot exceed 0.375W to avoid increase in junction temperature, i.e. greater than 130ºC. VCC LDO can supply current externally, which is not greater than 17mA at 18V VSUP and 20mA at 16V VSUP.

6.2 DC/AC Characteristics for Digital Inputs and Outputs

All pull-up, pull-downs have been implemented with active devices. SDO have been measured with 10pF load.

INT Output.

Table 4. INT

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output current				4	mA

CST, CSB, TxD.

Table 5. CST, CSB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		0.8*VCC			V
V_{IL}	Low level input voltage				0.2*VCC	V
I_{LEAK}	Input leakage current		-1		+1	µA
I_{PU}	Pull-up current	Pulled to GND	-150		-10	µA

SDI, SCLK.

Table 6. SDI, SCLK

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	High level input voltage		2.0			V
VIL	Low level input voltage				0.8	V
ILEAK	Input leakage current		-1		+1	µA

SDO Output.

Table 7. SDO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VOH	High level output voltage		2.5			V
VOL	Low level output voltage				0.4	V
IO	Output current				4	mA

CHOP_CLK Output.

Table 8. CHOP_CLK

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOH	High level output voltage		2.5			V
VOL	Low level output voltage				0.4	V
IO	Output current				4	mA

EN Input.

Table 9. EN

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High level input voltage		0.8*VCC			V
V_{IL}	Low level input voltage				0.2*VCC	V
I_{LEAK}	Input leakage current	EN = VSS	-1		+1	µA
I_{pd_en}	Pull-down current	Pulled up to VCC	30		100	µA

CLK I/O.

Table 10. CLK I/O

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	High level input voltage		2.4			V
VIL	Low level input voltage				1	V
ILEAK	Input leakage current		-1		+1	µA
IPD_EN	Pull-down current		10		100	µA
IO	Output current				4	mA
VOH	High level output voltage		2.5			V
VOL	Low level output voltage				0.4	V

MEN Output.

Table 11. MEN

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOH	High level output voltage		2.5			V
VOL	Low level output voltage				0.4	V
IO	Output current				2	mA

Rx Output.

Table 12. Rx

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage		VCC-0.5			V
V_{OL}	Low level output voltage				VSS+0.4	V
I_O	Output Current				1	mA
I_{pu_reset}	Pull-up current	Pulled down to VSS	-30		-100	µA

RESET Output.

Table 13. RESET

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output current	Open Drain Pull-down			8	mA

6.3 System Specifications

Table 14. System Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Ivsupnom	Current consumption in normal mode	No load on VCC, LIN bus in dominant state			7	mA
Ivsupstdby	Current consumption standby	No load on VCC, LIN bus in recessive state		80		µA

Note: Stand by mode power consumption is sum of stop mode power consumption and average of normal mode power consumption over a period of 2s (NOM1 time of device is low in Standby mode).

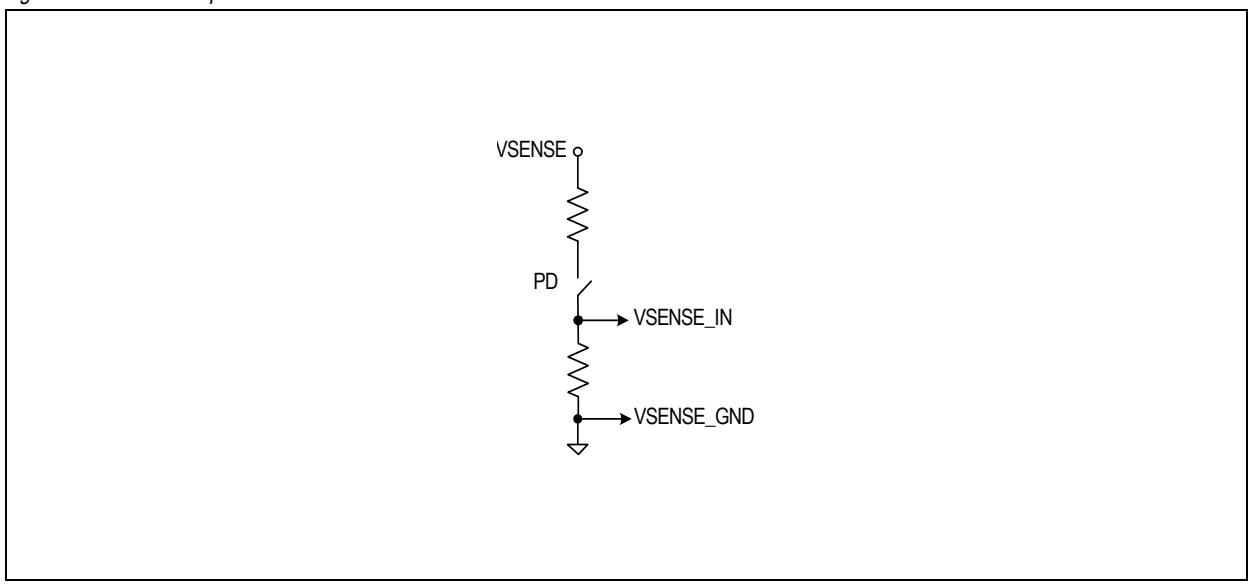
7 AS8515 Top Die Overview

The AS8515 ***Top die*** consists of a resistive divider, a low dropout regulator, and a LIN bus transceiver. Additionally integrated are a RESET unit with a power-on-reset delay, programmable window watchdog and timeout watchdog timers. It also includes a watchdog timeout on LIN Tx node to indicate if the Microcontroller is stuck in a loop and the LIN bus remains in dominant time for more than the necessary time.

7.1 Voltage Attenuator

A resistive divider is used as a battery voltage attenuator. Like the amplifier, the attenuator can be enabled or disabled through SPI, and in the device standby mode, we additionally need logic high on MEN pin for enabling. Internal reverse polarity protection is provided for VSENSE pin.

Figure 3. Attenuator Implementation



7.2 Voltage Regulators (LDO)

The device has a low-dropout voltage regulator named LDO, 3.3V voltage outputs. The output of the LDO is VCC. The regulator is always ON except when the device enters the over-temperature shutdown.

The regulator has in-built short-circuit current limitation feature. The regulator can be temporarily shut down for hard reset of the external circuitry by configuring the device to temporary shutdown mode through SPI.

The LDO power-up happens when the POR-VSUP event occurs (RESET_VSUP_N switching from low to high). The LDO will be switched off if there is an under voltage on VCC, that is, when RESET_VCC_N switches back to low.

7.3 LIN Transceiver

The device has a LIN transceiver with slew-controlled bus driver for controlling the electromagnetic emissions from the LIN bus. Further, the slew rate is independent of the bus load. The transmitter relays the data from the LIN controller (Tx pin) to the bus (LIN pin), and the receiver provides the data on the bus to the controller (Rx pin). The transceiver conforms to the LIN 2.1 standard.

The LIN transceiver has a timeout watchdog for Tx. After the timeout, the LIN bus will be released to the recessive state from the dominant state.

The bus driver has an in-built short-circuit current limitation facility to protect the device from damage when there is a short between the bus and the supply. In addition to the data receiver, there is a low-power receiver active in the device standby mode which received a wake-up event from the LIN bus to bring the device to normal mode.

7.4 Temperature Monitor/Limiter

The temperature limiter circuit powers down the device when the junction temperature exceeds 170°C (nominal). It also issues an over-temperature warning at 160°C (nominal). The device is powered up again when the junction temperature falls below 140°C (nominal). The over-temperature warning flag is also cleared at this temperature.

The temperature limiter circuit can be optionally disabled through SPI.

7.5 VSUP Under-voltage Reset

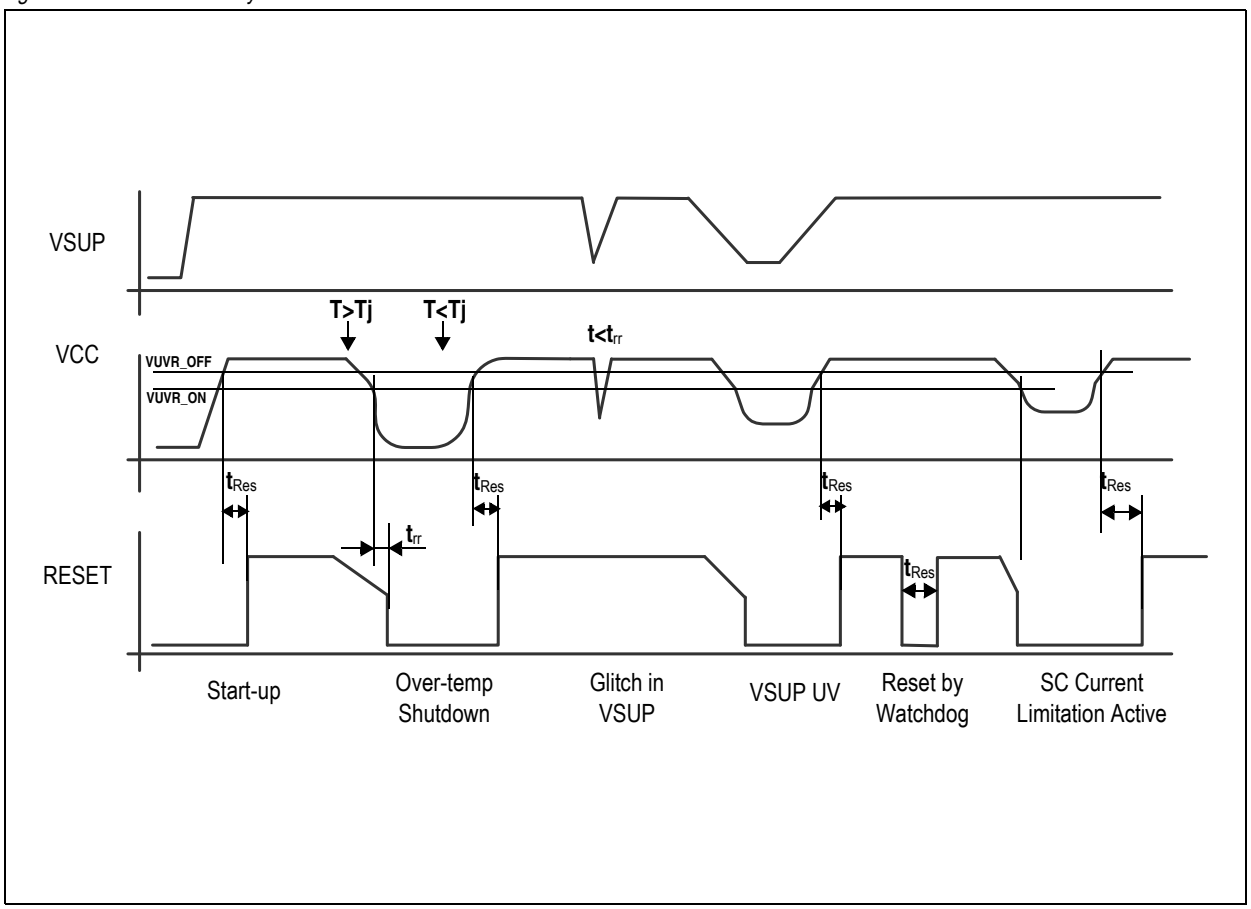
When VSUP drops below VSUVR_ON, the RESET_VSUP_N switches back to low level. This is treated as a master reset and will have the highest priority over all other signals. In this case, the regulators, LIN transceiver, and all other blocks are shut off, and the device comes to a complete stop. The device returns to the normal mode when VSUP rises over VSUVR_OFF again irrespective of the mode it was in prior to this under-voltage condition.

7.6 Reset

RESET module generates an active-low reset signal for the external circuitry supplied by VCC. The behavior of the reset output is depicted in Figure 4 in different cases. As shown, RESET signal is affected by an under-voltage condition on VCC and Watchdogs which are described in detail in the subsequent sections.

The reset period can be one-time programmed to 4, 16 and 32 ms with a default value of 8 ms.

Figure 4. Reset Functionality



7.7 VCC Under-voltage Reset

When VCC drops below VUVR_ON, the RESET_VCC_N switches back to low level. This event generates a reset output. The reset output is released again only a reset period (t_{Res}) later after VCC rises above VUVR_OFF. If the time difference between the VCC falling below VUVR_ON and rising above VUVR_OFF is less than t_{rr}, there will be no reset output. The reset output is affected in the conditions like over-temperature shutdown and temporary shutdown only through VCC under voltage.

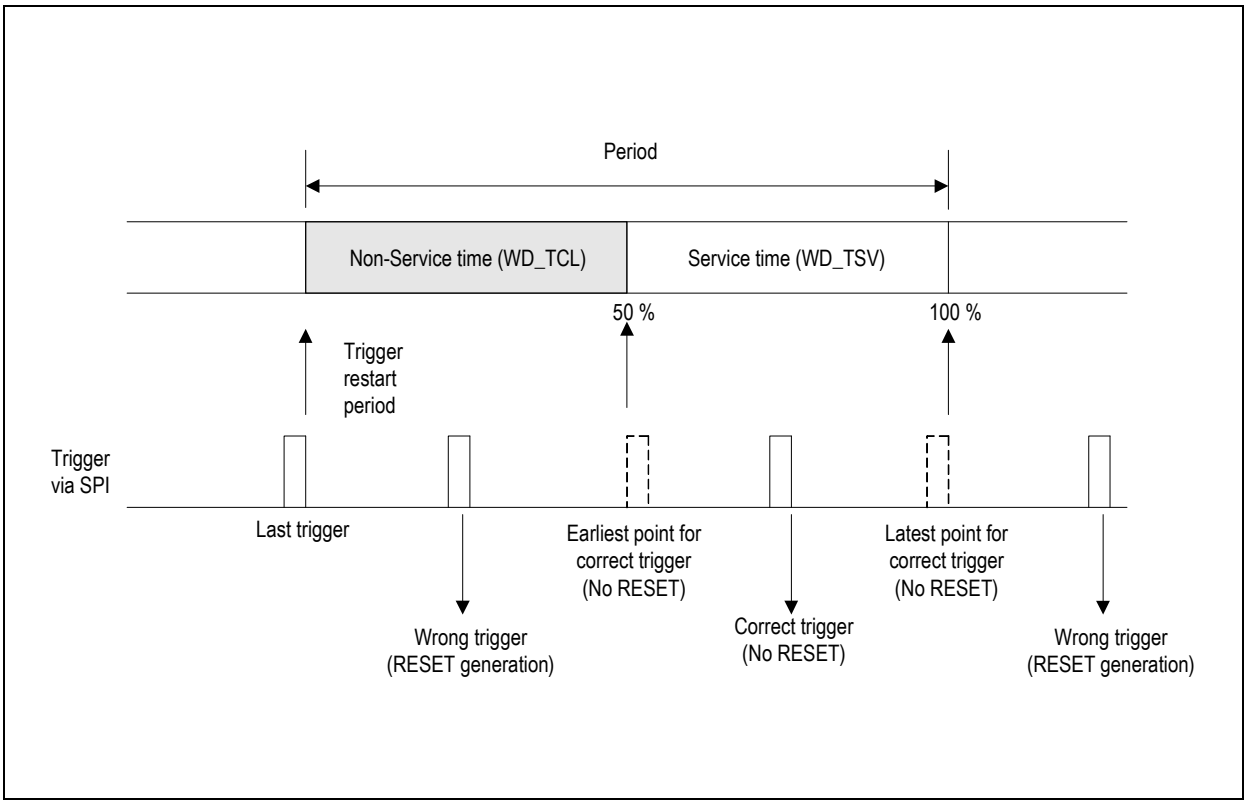
VCC under-voltage reset thresholds (VUVR_ON and VUVR_OFF) can be chosen by OTP.

7.8 Window Watchdog (WWD)

The Window Watchdog ensures that the Microcontroller is properly functioning in the normal mode of the device. The Watchdog is started after a reset and the Microcontroller needs to send a trigger in the window of WD_TSV (service time). If the trigger occurs early, in the period WD_TCL, or after WD_TSV, a reset output is generated.

The Microcontroller can access the trigger bit for the watchdog through SPI. The WWD can be enabled and the window times can be programmed through OTP bits and enabled as a factory option.

Figure 5. Window Watchdog Functionality



7.9 Timeout Watchdog (TWD)

The Timeout Watchdog ensures that the Microcontroller is in proper functional state in the device standby mode. The Watchdog timer will be started upon a rising edge on INT and will generate a reset output if the Microcontroller doesn't send a trigger before the timeout.

The Microcontroller can access the trigger bit for the watchdog through SPI. The TWD can be enabled by OTP and the timeout interval can be programmed through SPI.

7.10 Modes of Operation

The AS8515 ***Top die*** provides the following four main operating modes:

- Normal Mode
- Standby Mode
- Temporary Shutdown Mode
- Thermal Shutdown Mode

The LIN transceiver can be programmed to operate with lower slew in the normal mode. See Figure 6 for a detailed state transition diagram. Soft states like “TxWD Wait”, “Standby Wait”, and other wait states have also been included in the state diagram for completeness.

Figure 6. Finite State Machine Model of AS8515 Top Die

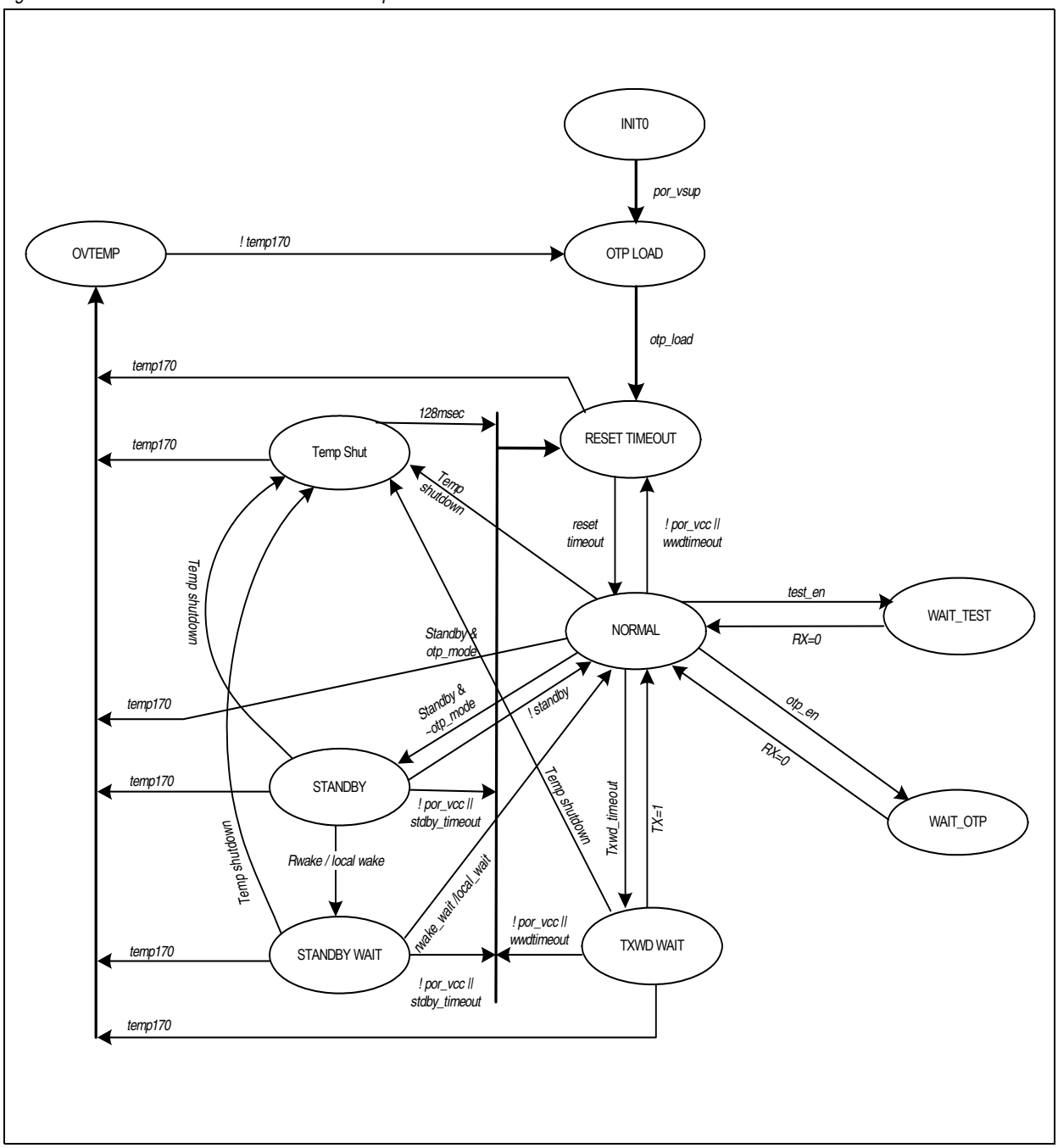


Table 15. Transition Table

Transition		Interface				Reg. 0x05 D0	Flags				Comments
From Mode	To Mode	LIN	Rx	Tx	EN		Rwake	U_{VSENSE}	OT	U_{VCC}	
Normal Mode	Stand-By	X-RS	X-H[1]	H[2]	H-L[2]	L	X	X	inactive	inactive	Tx is high for $T_{STNDY\_trigger}$
	Temporary Shutdown	X-RS	X-H[1]	X	H	H[2]	X	X	inactive	set	The Control Bit is set through the 4-Wire SPI interface
	Over-Temperature	X-RS	X-H[1]	X	X	L	X	X	set	set	Temperature monitor output asserted **(covered by scan)**
Standby Mode	Normal (LW)	X	H-X[1]	X	L-H[2]	L	X	X	inactive	inactive	
	Normal (RW)	X	H-X[1]	H	X	L	set	X	inactive	inactive	Remote Wake up Event occurred on LIN
	Temporary Shutdown	RS	H[1]	H	L	H[2]	X	X	inactive	set	The Control bit is set through the 4-Wire SPI interface
	Over-Temperature	RS	H[1]	H	L	L	X	X	set	set	Temperature monitor output asserted **(covered by scan)**
Temporary Shutdown Mode	Normal	RS-X	H-X[1]	X	X	L	X	X	inactive	clear	Internal 128ms timer expired
Over-temperature Mode	Normal	RS-X	H-X[1]	X	X	L	X	X	clear	clear	Temperature monitor output de-asserted **(covered by scan)**
All States	Power Off	X	X	X	X	X	X	L-H[2]	X	X	

1. Effect of transition
2. Cause for transition

Note: L = Low state, H = High state, OT = Over temperature Reset, U_{VCC} = Under-voltage VCC, U_{VSENSE} = Under-voltage VSENSE, Rwake = Remote wake, X = don't care.

7.10.1 Normal Mode

This is the mode after the power-up. In this mode, voltage regulator, LIN transceiver, window Watchdog is all active. The resistive divider can be enabled through SPI. LIN transceiver is capable of sending the Tx data from microcontroller to the LIN bus at a maximum rate of 20Kbps.

7.10.2 Standby Mode

Standby Mode is a functional low power mode and is entered by pulling EN to ground. The LIN transceiver, resistive divider, window watchdog, and Tx timeout watchdog circuits are disabled. But, it is possible to selectively enable the voltage and current measurement paths in this mode using an externally generated measurement enable (MEN) signal on the MEN pin. The timeout Watchdog can be enabled in this mode to make sure that the Microcontroller is active.

7.10.3 Temporary Shutdown Mode

In this mode, the regulator is powered down and the VCC is pulled down. This provides an alternative way to reset those components powered by AS8515. The feature has to be enabled by an OTP bit (factory programming option) and can be invoked through SPI. The LIN transceiver along with the LIN wake-up circuits are powered down. No remote wake functionality possible. LIN bus enters into recessive state. The system goes out of this mode to normal mode after the timeout of an internal timer.

7.10.4 Thermal Shutdown Mode

If the junction temperature TJ is higher than T_{sd}, the device will be switched into the thermal shutdown mode. The regulator and the transceiver are completely disabled. Only the over-temperature monitor is active. As soon as the temperature returns back to T_{RET}, the system enters normal mode.

7.11 Initialization

When the power supply is switched on, when VSUP > VSUVR_OFF, RESET_VSUP_N becomes high. This starts the regulator LDO with 3.3V and Vuvr_off option of 2.75V. When VCC > Vuvr_off (2.75V), active-low PORN_2_OTP is generated. The rising edge of PORN_2_OTP loads contents of fuse onto the OTP latch after load access time T_{Load}. LOAD_OTP_IN_PREREG signal loads contents of OTP latch onto a register. This register provides the actual settings of LDO, Vuvr_off and Reset Timeout period T_{Res}. This is done as the OTP block is powered by the VCC. If VCC > Vuvr_off (phase 2), Reset timeout is restarted. RESET signal is de-asserted after Reset Timeout period T_{Res} (phase 2) and then device enters into normal mode. The circuit also needs to initialize correctly for very slow ramp rates on VSUP (of the order of 0.5V/min).

Figure 7. Initialization Sequence

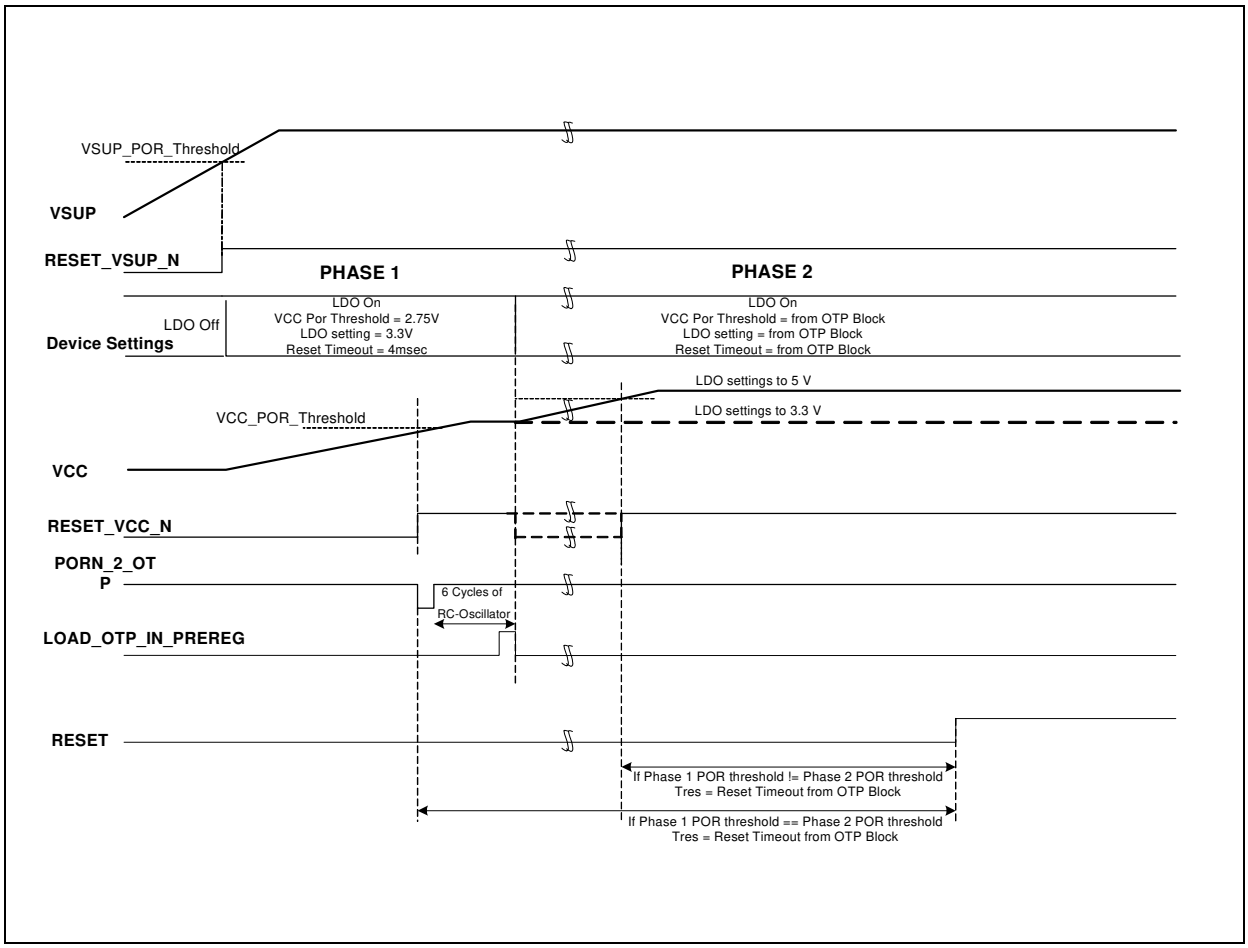


Table 16. VSUP>Vsuvr_on and VCC<Vuvr_on

Block	Output Signal
TRANSCEIVER=Enabled (disabled only during initial VSUP ramp-up)	LIN=high-z, Rx=follows VCC…
LDO=Enabled (disabled only during initial ramp-up)	VCC=low…
RESET BLOCK=Enabled	RESET=high-z…
RESISTIVE DIVIDER=Enabled	VSENSE=high…, VSENSE_DIV=enabled

Table 17. VSUP<Vsuvr_on

Block	Output Signal
TRANSCEIVER=Disabled	LIN=high-z, Rx=high-z…
LDO=Disabled	VCC=low
RESET BLOCK=Disabled	RESET=high-z
RESISTIVE DIVIDER=Disabled	VSENSE=high, VSENSE_DIV=low

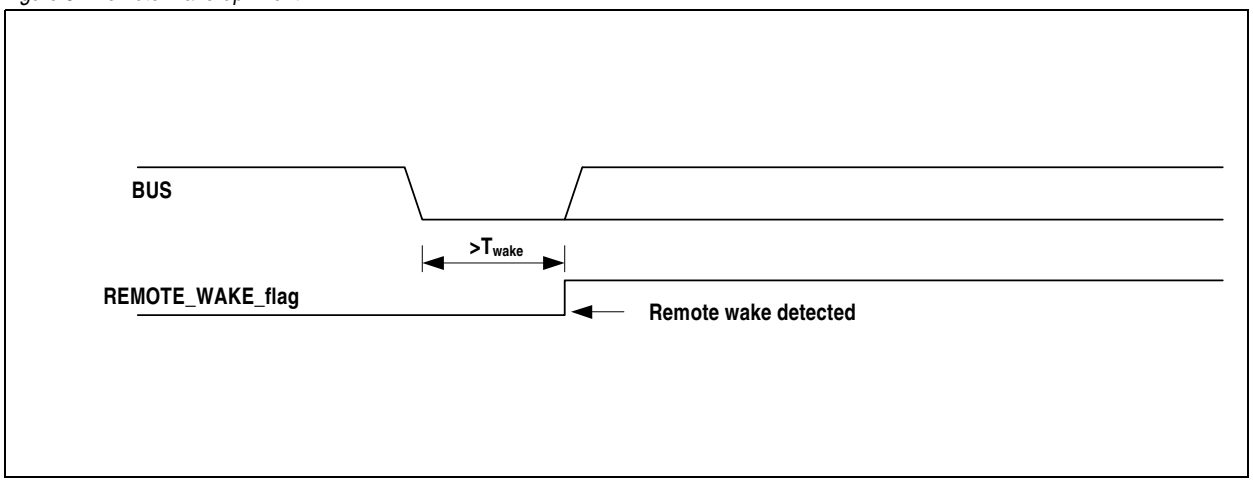
7.12 Wake-up

When the device enters standby mode, it can be brought back to the normal mode. A dominant state on the BUS for duration of t_{WAKE} (see Table 22) will result in the device wake-up which is termed as remote wake.

7.12.1 Remote Wake-up Event

In all low power modes of ***Top die***, low power BUS receiver is ON. If BUS is in dominant state for longer than t_{WAKE} then, remote wake is sensed on the BUS and REMOTE_WAKE_flag is set. Indication of wake-up is given to µC by setting a bit in interrupt register and giving interrupt on INTN pin.

Figure 8. Remote Wake-up Event



7.13 LIN BUS Transceiver

The AS8515 has an integrated bi-directional bus interface device for data transfer between LIN bus and the LIN protocol controller. The transceiver consists of a driver with slew rate control, wave shaping and current limitation and a receiver with high voltage comparator followed by a de-bouncing unit.

7.13.1 Transmit Mode

During transmission the data at the pin Tx will be transferred to the BUS driver to generate a bus signal. To minimize the electromagnetic emission of the bus line, the BUS driver has an integrated slew rate control and wave shaping unit.

Transmitting will be interrupted in the following cases:

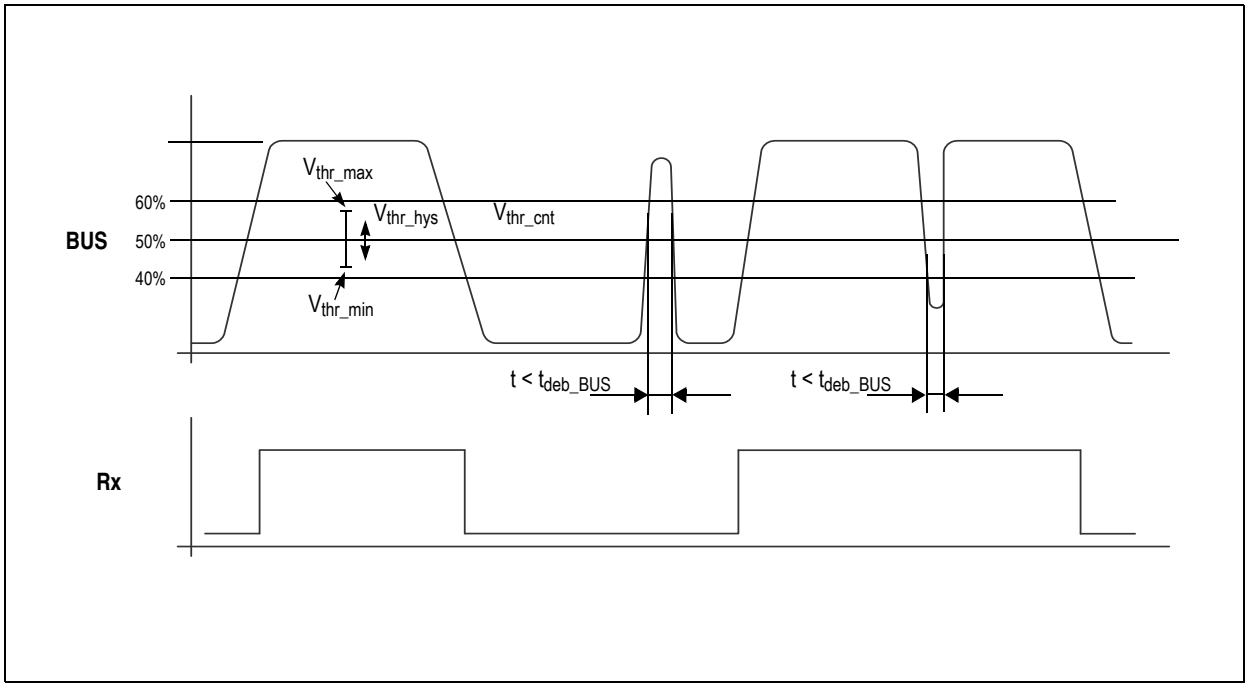
- Thermal Shutdown active
- Master Reset (VSUP < Vsuvr_on)

The recessive BUS level is generated from the integrated 30k pull up resistor in serial with an active diode This diode prevents the reverse current of VBUS during differential voltage between VSUP and BUS (VBUS>VSUP). No additional termination resistor is necessary to use the AS8515 in LIN slave nodes. If this IC is used for LIN master nodes it is necessary that the BUS pin is terminated via an external 1kΩ resistor in series with a diode to VSENSE.

7.13.2 Receive Mode

The data signals from the BUS pin will be transferred continuously to the pin Rx. Short spikes on the bus signal are suppressed by the implemented debouncing circuit. Including all tolerances the LIN specific receive threshold values of 0.4*VSUP and 0.6*VSUP will be securely observed.

Figure 9. Receive Mode Impulse Diagram

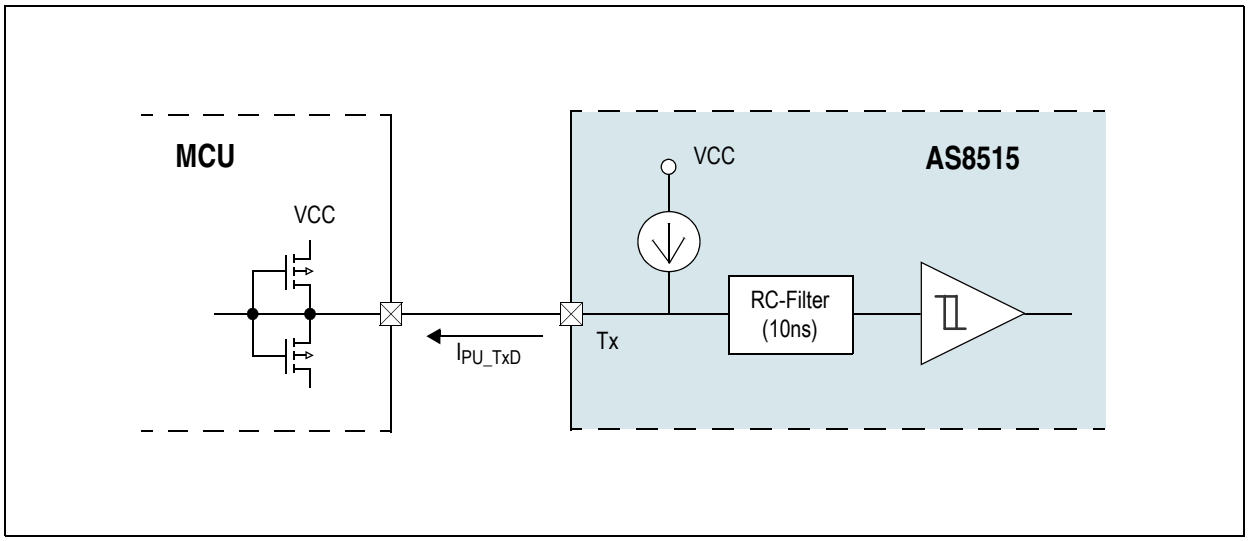


7.14 Rx and Tx Interface

7.14.1 Input Tx

The 3.3V input Tx controls directly the BUS level. LIN Transmitter acts like a slew-controlled level shifter. A dominant state (low) on Tx leads to the LIN bus being pulled low (dominant state) too. The Tx pin has an internal active pull up connected to VCC. This guarantees that an open Tx pin generates a recessive BUS level.

Figure 10. Tx Interface



7.14.2 Output Rx

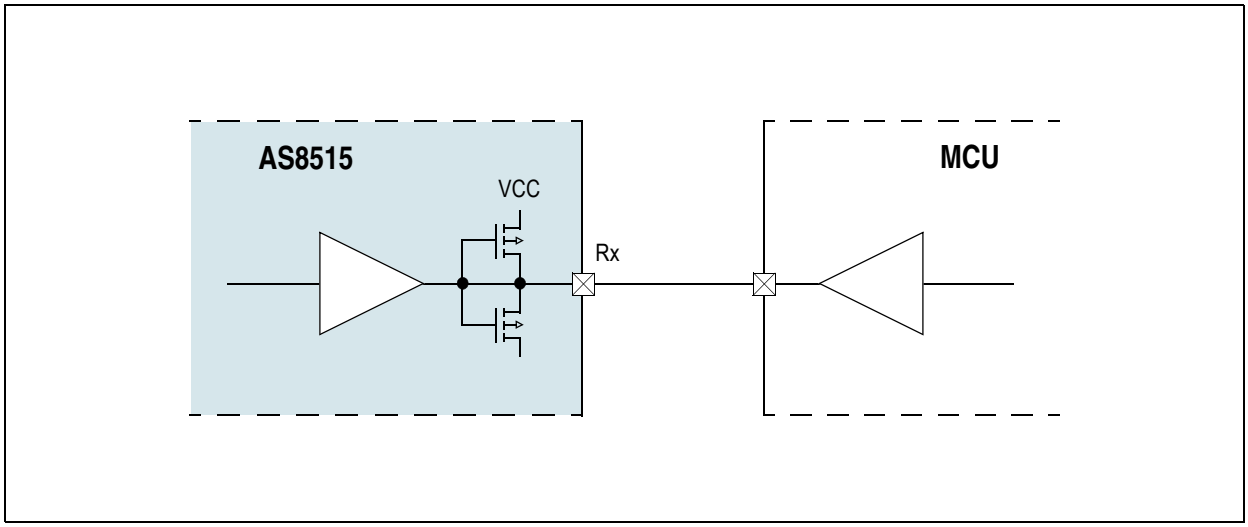
The received BUS signal will be output to the Rx pin:

BUS < Vthr_cnt – 0.5 * Vthr_hys → Rx = low

BUS > Vthr_cnt + 0.5 * Vthr_hys → Rx = high

This output is a push-pull driver between VCC and GND with an output current of 1mA

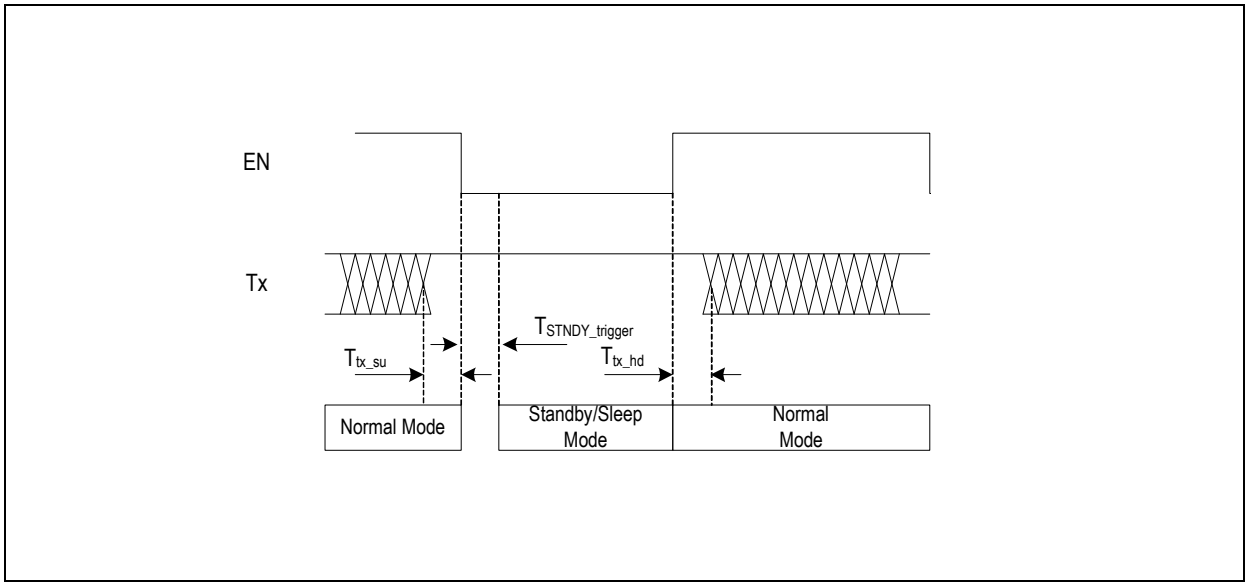
Figure 11. Rx Interface



7.15 MODE Input EN

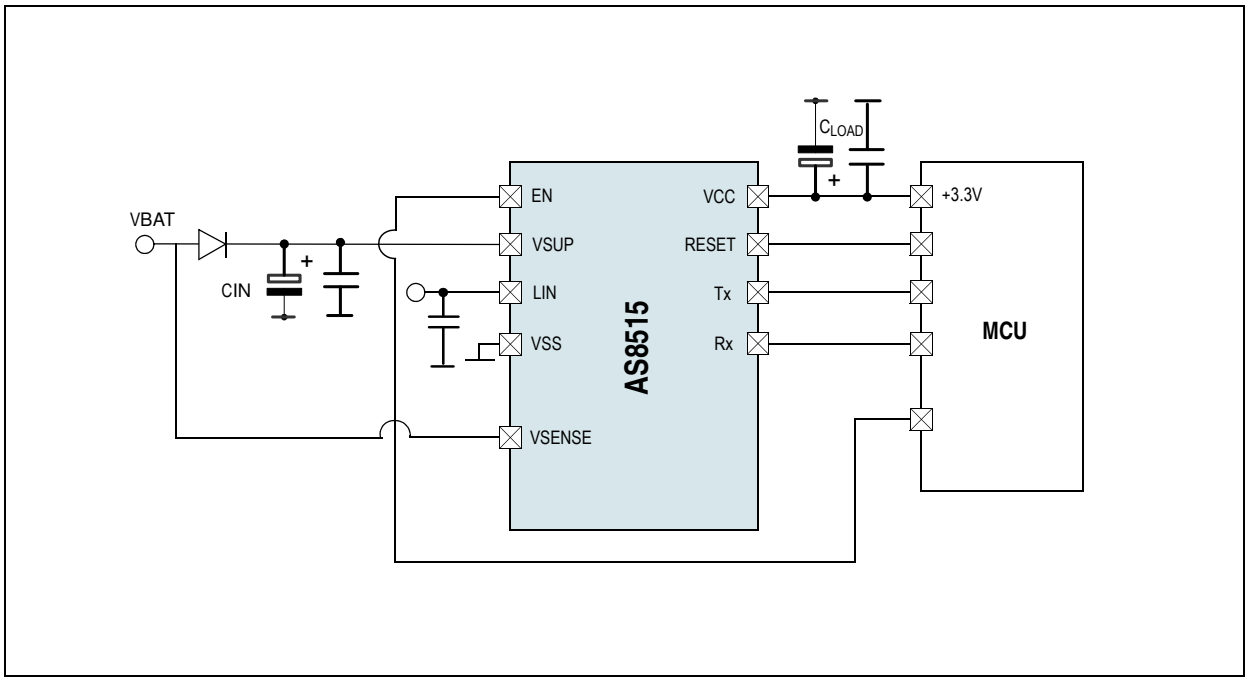
The AS8515 ***Top die*** is switched from normal mode to the standby mode with a falling edge on EN and keeping Tx high for $T_{STNDY\_trigger}$ time. Device is switched from standby mode to normal mode with a rising edge at the EN pin. The mode change for ***Top die*** with a falling edge on EN can be done independently from the state of the transceiver bus. This ensures the direct control of device to enter into standby mode by microcontroller using EN pin.

Figure 12. EN Pin Functionality



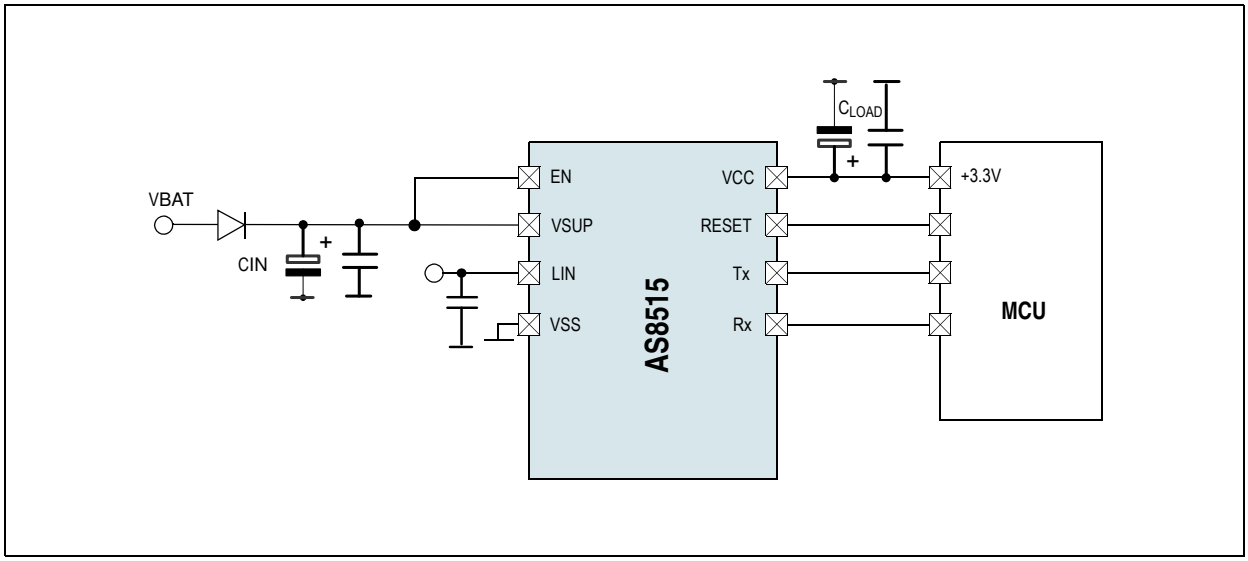
The EN input has an internal active pull down to secure that if this pin is not connected, a low level will be generated.

Figure 13. Enable Interface



If the application doesn't need the low-power modes of the device, a direct connection of EN to VCC is possible. In this case the ***Top die*** operates in permanent normal mode. Also possible is the external (outside of the module) control of the EN line via VSUP signal as shown below.

Figure 14. EN Connection for Permanent Normal Mode



7.16 Top Die Block Specifications

This section provides specification of design related key parameters.

7.16.1 Voltage Attenuator

Table 18. Voltage Attenuator

Symbol	Parameter	Condition	Min	Typ	Max	Unit
RDIV	Division ratio			21		V/V
VSENSE	Input voltage range/ Battery voltage range		4.5	12	18	V
$\varepsilon_{p,RDIV}$	Ratio error	At room temperature, VSENSE=12V			±1	%
$\varepsilon_{dt1,RDIV}$	Ratio drift (with reference to Temperature)	Temperature: -25 to +65° @VSENSE=12V Maximum values will be added after device evaluation (to be guaranteed by evaluation)		±0.05		%
$\varepsilon_{dt2,RDIV}$		Temperature: -40 to +125° @VSENSE=12V Maximum values will be added after device evaluation (to be guaranteed by evaluation)		±0.2		
$\varepsilon_{dv1,RDIV}$	Ratio drift (with reference to VSENSE)	VSENSE: 11V to 13V @Temperature=27° Maximum values will be added after device evaluation (to be guaranteed by evaluation)		±0.05		%
$\varepsilon_{dv2,RDIV}$		VSENSE: 6V to 18V @Temperature=27° Maximum values will be added after device evaluation (to be guaranteed by evaluation)		±0.2		

7.16.2 Voltage Regulator (LDO)

Table 19. Voltage Regulator

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{SUP}	Input Supply Voltage		4.3	12	18	V
VCC	Output Voltage Range		3.15	3.3	3.45	V
I_{LOAD}	LDO Load Current				45	mA
ICC_SH	Output Short Circuit Current	Normal mode			250	mA
dVCC1	Line Regulation	ΔVCC / ΔVSUP for VSUP range			8	mV/V
LOREG	Load Regulation	ΔVCC / ΔICCn (0.5mA < I_{LOAD} < 50mA)			1	mV/mA
CL1	Output Capacitor 1 LDO	Electrolytic	2.2		10	µF
ESR1			1		10	Ω
CL2	Output Capacitor 2 LDO	Ceramic	100		220	nF
ESR2			0.02		1	W
CSUP1E	Input capacitor (Electrolytic)	For EMC suppression	22		100	µF
ESR1_CSUP			1		10	Ω
CSUP2C	Input capacitor (Ceramic)		100		220	nF
ESR2_CSUP			0.02		1	Ω

7.16.3 LIN Transceiver

DC Electrical Characteristics.

Table 20. Driver

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{bus_lim}		Current limitation in dominant state LIN = VSUP_max	40	120	200	mA
LIN_V_{OL}		Output Voltage BUS (dominant state), I_{LIN} = 40mA (short-circuit condition tested at V_{OL}=2.5V)			2	V
Pull-up resistor		Normal mode (recessive BUS level on Tx pin)	20	40	60	KΩ
$I_{bus\_leak\_rec}$		Driver OFF; 7.3V < VSUP < 18; 8V < V_{BAT} < 18, VSUP < VBUS < 1.08 * VSUP (to be tested at VBUS = 18V)			20	µA

Table 21. Receiver

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{bus\_leak\_dom}$		Input Leakage current at receiver Driver OFF; VBUS = 0V; VSUP = 12V; VCC = 3.3V	-1			mA
$I_{bus\_no\_GND}$		VSS = VSUP; VSUP = 12V; 0V < VBUS < 18V, VCC = 3.3V (to be tested at VBUS = 18V)	-1		1	mA
$I_{bus\_no\_bat}$		VSUP = VSS; 0V < VBUS < 18V, VCC = VSS (to be tested at VBUS = 18V)			100	µA
V_{bus_dom}					0.4	VSUP
V_{bus_rec}			0.6			VSUP

Table 21. Receiver

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{bus_cnt}		$V_{bus\_cnt} = (V_{th\_dom} + V_{th\_rec})/2$ [1]	0.475		0.525	VSUP
V_{hys}		$V_{hys} = (V_{th\_dom} - V_{th\_rec})$ [1]	0.05		0.175	VSUP

1. V_{th_dom} : Receiver threshold of the recessive to dominant LIN bus edge
   V_{th_rec} : Receiver threshold of the dominant to recessive LIN bus edge

AC Electrical Characteristics.

LIN Driver, Bus load conditions (C_{BUS} ; R_{BUS}): 1nF; 1kΩ / 6, 8nF; 660Ω / 10nF; 500Ω

Table 22. LIN Driver

Symbol	Parameter	Condition	Min	Typ	Max	Unit
D1	(worst case 20Kbps transmission)	V_{th_rec}(max) = 0.744 x VSUP; V_{th_dom}(max) = 0.581 x VSUP; VSUP = 6.0V...18V; tbit = 50µs; D1 = tbus_rec(min) / (2 x tbit)	0.396			
D2	(worst case 20kbps transmission)	V_{th_rec} (min) = 0.422 x VSUP; V_{th_dom} (min) = 0.284 x VSUP; VSUP = 6V...18V; tbit = 50µs; D2 = tbus_rec(max) / (2 x tbit)			0.581	
D3	(worst case 10.4kbps transmission)	V_{th_rec} (max) = 0.778 x VSUP; V_{th_dom} (max) = 0.616 x VSUP; VSUP = 6.0V...18V; tbit = 96µs; D3 = tbus_rec(min) / (2 x tbit)	0.417			
D4	(worst case 10.4kbps transmission)	V_{th_rec} (min) = 0.389 x VSUP; V_{th_dom} (min) = 0.251 x VSUP; VSUP = 6V...18V; tbit = 96µs; D4 = tbus_rec(max) / (2 x tbit)			0.59	
t_{dLR}		VCC = 3.3V; Propagation delay bus dominant to Rx LOW			6	µs
t_{dHR}		VCC = 3.3V; Propagation delay bus dominant to Rx HIGH			6	µs
t_{RS}		Receiver delay symmetry	-2		2	µs
t_{WAKE}		Dominant time for wake-up via LIN bus	30		150	µs
t_{sln}		Transition from standby mode to normal mode (clock frequency is 128KHz ±25%)		4		Clock cycles
t_{nsl}		Transition from normal mode to standby mode (clock frequency is 128KHz ±25%)		6		Clock cycles
t_{rec_deb}		Receiver de-bounce time	0.6		3	µs
C_{int}		Internal capacitance of the LIN node configured as a slave with a 180pF cap on the LIN bus		220	250	pF

7.17 Timing Diagrams

Figure 15. Timing Diagram for Propagation Delays