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Datasheet: AS8650B High-efficient Power Management Device with High-speed CAN Interface

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AS8650B

High-efficient Power Management Device with High-speed CAN Interface

1 General Description

The AS8650B is a companion IC which combines power management functions and a fully conforming high-speed CAN Transceiver in one high performance analog device for automotive applications. The AS8650B is powered by the battery, provides 4 output voltage levels of which 3 outputs in the range of 1.8V to 3.3V with a maximum current consumption up to 120mA at the LDO voltage regulator outputs. An integrated DCDC converter with a very high efficiency for the 5V output supplies the 3 voltage regulators and ensures a voltage stability of ±2.5%. The combination of DCDC converter with low-drop-out voltage regulators makes the AS8650B suitable for all Automotive Control Units where power efficiency is a must.

The AS8650B provides a high-speed CAN interface up to 1Mbps communication rate conforming to ISO 11898-5. The AS8650B provides wake-up via remote wake-up at CAN bus lines and a local wake pin. The watchdog unit provides three different timing functions: start-up, window- and timeout watchdog; configurable via the SPI and I²C interface.

Voltage monitoring is implemented for the battery supply, DCDC output and the 3 LDO regulator outputs. Undervoltage will be signalled on the INTN pin to the microcontroller. All diagnostics and status flags can be accessed with the SPI interface.

The product is available in a 36-pin QFN (6x6x0.9) package.

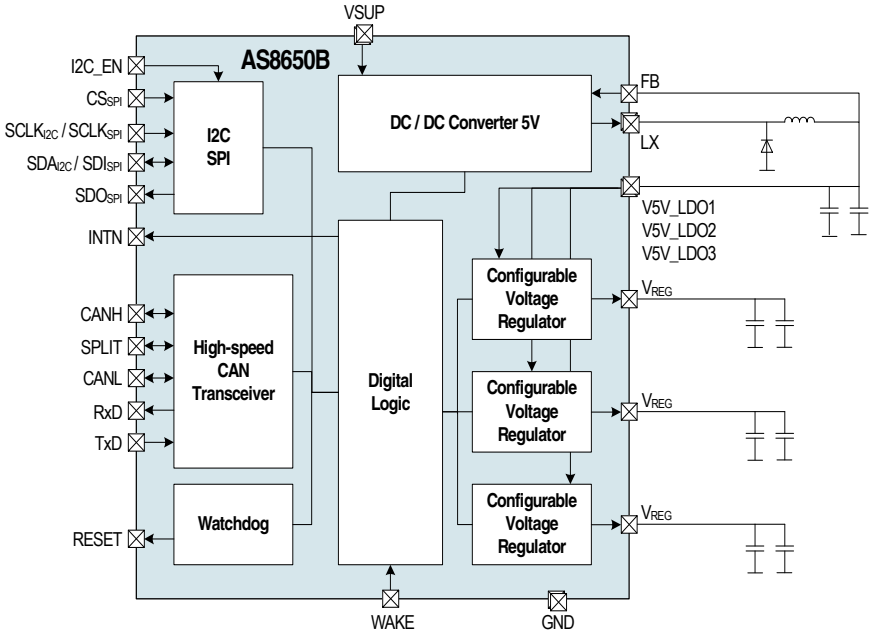
2 Key Features

- DCDC converter for 5V output with very high efficiency
- Three voltage regulators providing 3.3V, 2.8V and 1.8V with accuracy better than 2.5% (Two are adjustable through factory settings).
- High-speed CAN interface (ISO 11898-5) with remote wake-up
- Comprehensive voltage monitoring
- Configurable watchdog functions for start-up, operation, and standby
- Automatic thermal shutdown protection
- Excellent EMC performance with outstanding switching technology for the DCDC converter
- Ambient temperature range from -40°C to +105°C in maximum load conditions
- Lead-free 36-pin QFN (6x6x0.9) package

3 Applications

The AS8650B provides high efficient and flexible power supply together with state-of-the-art high-speed CAN Interface for automotive control units.The device is pin compatible with AS8550 (LIN interface) in order to change from CAN to LIN easy.

Figure 1. AS8650B Block Diagram



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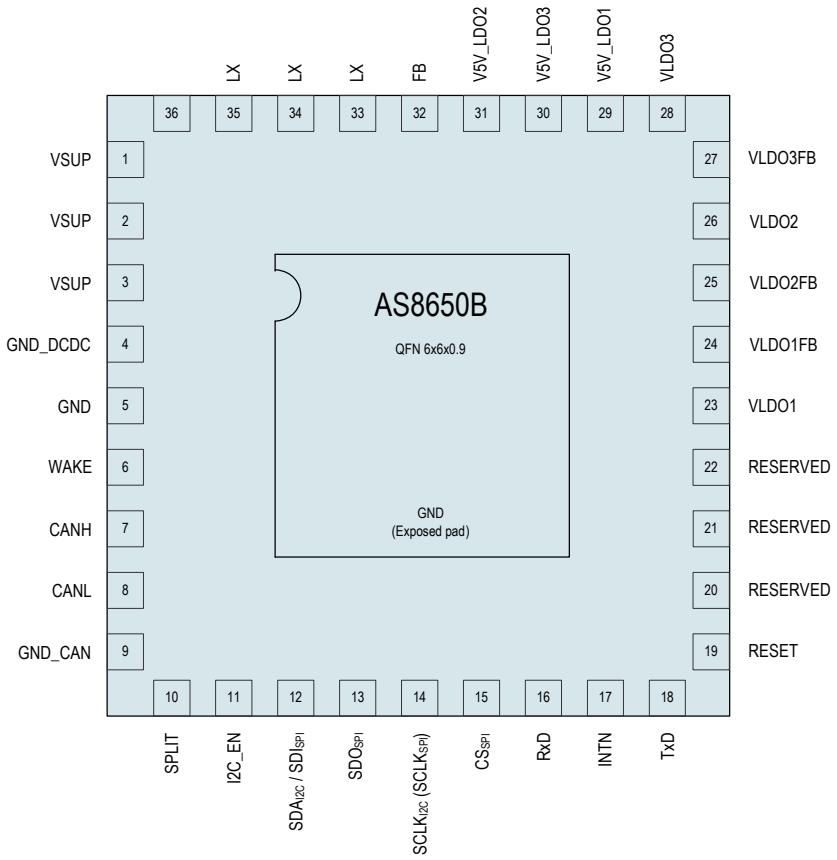
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin	Pin Name	Pin Type	Description
1, 2, 3	VSUP	Power Supply Input	Power Supply
4	GND_DCDC		
5	GND		
6	WAKE	Analog Input / Output high-voltage	Local wake request (high-voltage input)
7	CANH		High level CAN bus line
8	CANL		Low level CAN bus line
9	GND_CAN	Power Supply Input	Power supply
10	SPLIT	Analog Input / Output high-voltage	Common-mode stabilization output

Table 1. Pin Descriptions

Pin	Pin Name	Pin Type	Description
11	I2C_EN	Digital Input	I²C/SPI select signal (High = I²C, Low = SPI)
12	SDA_{I2C} / SDI_{SPI}	Digital Input/Output / Digital Input	Unidirectional for SPI, Bidirectional for I²C
13	SDO_{SPI}	Digital Output	SPI data out
14	$SCLK_{I2C}$ / $SCLK_{SPI}$	Digital Input	Serial clock (Multiplexed for I²C and SPI) unidirectional
15	CS_{SPI}	Digital input with pull-up	SPI chip select
16	RxD	Digital output with pull-up	CAN Transceiver receive signal
17	INTN	Digital Output	Active low interrupt to µC. Generated if status / diagnostic is updated.
18	TxD	Digital input with pull-up	CAN Transceiver transmit signal
19	RESET	Digital Output	Digital Output referenced to VLDO1, active low
20	Reserved	Pin with Digital / Analog Input / Open-Drain-Output	Reserved
21		Analog Input / Output	
22			
23	VLDO1	Power Supply Input	Regulated voltage output
24	VLDO1FB	Pin with Digital / Analog Input / Open-Drain-Output	Regulated voltage feedback
25	VLDO2FB	Pin with Digital / Analog Input / Open-Drain-Output	Regulated voltage feedback
26	VLDO2	Power Supply Input	Regulated voltage output
27	VLDO3FB	Pin with Digital / Analog Input / Open-Drain-Output	Regulated voltage feedback
28	VLDO3	Power Supply Input	Regulated voltage output
29	V5V_LDO1		Step-down converter 5V output, supply for LDO1
30	V5V_LDO3		Step-down converter 5V output, supply for LDO3
31	V5V_LDO2		Step-down converter 5V output, supply for LDO2
32	FB (DCDC)	Analog Input	DCDC output voltage feedback
33, 34, 35	LX (DCDC)	Power Supply Input	DCDC output
0	GND		Exposed pad (GND)

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings[1]

Parameter	Min	Max	Units	Notes
Electrical Parameters				
Voltage at positive supply pin (V_{VSUP})	-0.3	40	V	
Voltage at pin V5V_LDO1, V5V_LDO2, V5V_LDO3, VLDO1, VLDO2, VLDO3, FB, VLDO1FB, VLDO2FB, VLDO3FB	-0.3	7	V	
Voltage at pin CANH, CANL, SPLIT	-40	+40	V	
Voltage at pin LX, WAKE	-0.3	V_{VSUP} + 0.3	V	
Voltage at pin RESET, INTN, RxD, TxD, CS, SCLK, SDO, SDA/SDI, I2C_EN	-0.3	4.5	V	
Input Supply slew-rate (V_{sup_slew})		1	V/µs	Input power supply ramp rate
Electrostatic Discharge				
Electrostatic discharge voltage AEC-Q100-002 human body model standard (ESD)	±2		kV	All pins except VSUP, GND, CANH, CANL, WAKE, SPLIT
	±4			VSUP, GND, WAKE, SPLIT
	±8			CANH, CANL
Latch-Up Immunity	-100	+100	mA	AEC-Q100-004
Continuous Power Dissipation				
Maximum power dissipation (P_{tot})		1.2	W	
Temperature Ranges and Storage Conditions				
Junction temperature (TJ)		170	ºC	
Storage temperature (T_{stg})	-55	+150	ºC	
Thermal resistance MLF package (R_{thj_36})		30	ºC/W	SEMI G42-88
Package body temperature (TBODY)		260	ºC	*The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/ JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h

1. All voltages mentioned above are referred with respect to ground reference voltage V_{GND}.

6 Electrical Characteristics

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Operating Conditions						
V_{SUP}	Positive supply voltage	Normal operating condition	6		18	V
GND	Ground	In reference to all the voltages	0			V
T_{AMB}	Ambient temperature	Junction temperature (T_J) ≤ 150ºC (at full-load)	-40		105	ºC
I_{supp}	Supply current, Normal mode	VSUP = 6V, LDOs at full load, DCDC load = 390mA, CAN dominant		425		mA
		VSUP = 18V, LDOs at full load, DCDC load = 390mA, CAN dominant, not production tested.		150		
		VSUP = 16V, LDOs at full load, CAN dominant		170		
CS						
Vt-	Negative-Going Threshold	VLDO1 = 3.3V	1.12		1.52	V
Vt+	Positive-Going Threshold		1.77		2.23	V
I_{iil_cs}	Pull up current	In CS pad, Pulled up to VLDO1	-60		-15	µA
SDO						
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage	VSUP ≥ 6V			0.4	V
I_O	Output drive current				4	mA
SDA / SDI						
V_{IH}	High level input voltage		0.7* VLDO1			V
V_{IL}	Low level input voltage				0.3* VLDO1	V
V_{OL}	Low level output voltage				0.4	V
SCLK						
V_{IH}	High level input voltage	Open-drain, external 500Ω pull-up	0.7* VLDO1			V
V_{IL}	Low level input voltage				0.3* VLDO1	V
RESET, INTN						
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage	VSUP ≥ 6V			0.4	V
I_O	Output drive current				4	mA
TxD						
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
I_O	Output drive current	VSUP ≥ 6V			1	mA
I_{iil}	Pull-up current	TxD pulled up to VLDO1 with control RxD pulled up to VLDO1	-60		-15	µA

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RxD						
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output drive current	VSUP ≥ 6V			1	mA
I_{lil}	Pull-up current	TxD pulled up to VLDO1 with control RxD pulled up to VLDO1	-60		-15	µA

6.1 Electrical System Specification

-40°C < T_J < 150°C

Table 4. Electrical System Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IDDnom	Current consumption Normal mode	No load, VSUP = 12V, CAN recessive		3.5	6	mA
IDDrecv	Current consumption Receive-only mode	No load, VSUP = 12V, CAN recessive		1	2	mA
IDDstby	Current consumption Standby mode	No load, VSUP = 12V		135	270	µA
IDDsleep	Current consumption Sleep mode	No load, VSUP = 12V		75	150	µA

6.2 DCDC Converter

-40°C < T_J < 150°C; all voltages are with respect to ground, normal operating mode, unless otherwise mentioned.

Table 5. DCDC Converter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VSUP	Battery Voltage Range		6	12	18	V
V5V	Output Voltage	For inductor 22µH and capacitor 100µF	4.75	5	5.25	V
I_{LXS}	LX current limit		0.8	1	1.25	A
I_{V5V}	DCDC output current				500	mA
R_{ON}	LX switch on-resistance	(bondwire resistance included)		0.8	1	Ω
V_{FB}	Reference Voltage for FB		4.75	5	5.25	V
Lireg_dc	Line regulation	Step from V_{IN} = 6V to V_{IN}2 = 18V, I_{LOAD} = 100mA Lireg = 100*(V_{OUT}1-V_{OUT}2) / [V_{OUT}2*(V_{IN}1-V_{IN}2)]	-0.1		+0.1	% / V
Loreg_dc	Load regulation	I_{LOAD} step from 90mA to 10mA VSUP = 12V Loreg = 100*(V_90mA-V_10mA) / V_90mA	-0.9		+0.9	%
LX_ind	Output inductor		10		22	µH
V5V_cer1	Output ceramic capacitor 1		10		100	µF
V5V_esr1	ESR of ceramic capacitor 1		0		0.05	Ω
V5V_cer2	Output ceramic capacitor 2	X7R type	100		220	nF
V5V_esr2	ESR of ceramic capacitor 2				0.01	Ω
Csup	Input capacitor (ceramic)	For EMC suppression	22		100	µF
Csup_esr					1	Ω

6.3 Low Drop Out Regulators

-40°C < Tj < 150°C; all voltages are with respect to ground, normal operating mode, unless otherwise mentioned. The LDO block is a linear voltage regulator, which provides a regulated (band-gap stabilized) output voltage from the DCDC converter output voltage (V5V).

Table 6. VLDO1 Block Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V5V	Input Voltage Range		4.75	5	5.25	V
$I_{OUTLDO1}$	Output current	Guaranteed by design. Not production tested.	0		100	mA
VLDO1	Output Voltage Range		3.217	3.3	3.383	V
ICC_SH	Output Short Circuit Current	Normal mode			300	mA
dVLDO1	Line Regulation	ΔVLDO1 / ΔV5V (static) for the input range, I_{LOAD} = 100mA	-8		8	mV/V
LOREG_NM	Load Regulation	ΔVLDO1 (for 100mA > I_{LOAD} > 1mA), V5V = 5V	-0.15		+0.15	mV/mA
CL2	Output Capacitor (Ceramic)	X7R type	2		5	µF
ESR2			0.02		0.1	Ω
CL1		X7R type	100		220	nF
ESR1					0.01	Ω

Table 7. VLDO2[1] Block Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V5V	Input Voltage Range		4.75	5	5.25	V
IOUTLDO2	Output current	Guaranteed by design. Not production tested.	0		120	mA
VLDO2	Output Voltage Range	V_{OUT} (typ) depends on the trim code as in OTP register mapping. Default code gives 2.8V	0.975* V_{OUT}	V_{OUT}	1.025* V_{OUT}	V
ICC_SH	Output Short Circuit Current	Normal mode			300	mA
dVLDO2	Line Regulation	ΔVLDO2 / ΔV5V (static) for the input range, I_{LOAD} = 100mA	-8		8	mV/V
LOREG_NM	Load Regulation	ΔVLDO2 (for 120mA > I_{LOAD} > 1mA)	-0.15		+0.15	mV/mA
CL2	Output Capacitor (Ceramic)	X7R type	2		5	µF
ESR2			0.02		0.1	Ω
CL1		X7R type	100		220	nF
ESR1					0.01	Ω

1. Factory setting: V_{OUT} = 2.8V.

Table 8. VLDO3[1] Block Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V5V	Input Voltage Range		4.75	5	5.25	V
$I_{OUTLDO3}$	Output current	Guaranteed by design. Not production tested.	0		100	mA
VLDO3	Output Voltage Range	VOUT (typ) depends on the trim code as in OTP register mapping. Default code gives 1.8V	0.975* VOUT	VOUT	1.025* VOUT	V
ICC_SH	Output Short Circuit Current	Normal mode			300	mA
dVLDO3	Line Regulation	ΔVLDO3 / ΔV5V (static) for the input range, ILOAD = 100mA	-8		8	mV/V
LOREG_NM	Load Regulation	ΔVLDO3 (for 100mA > ILOAD > 1mA)	-0.15		+0.15	mV/mA
CL2	Output Capacitor (Ceramic)	X7R type	2		5	µF
ESR2			0.02		0.1	Ω
CL1		X7R type	100		220	nF
ESR1					0.01	Ω

1. Factory setting: VOUT = 1.8V.

6.4 CAN Transceiver

6V < VSUP < 18V; -40°C < Tj < 150°C; all voltages are with respect to ground; 4.75V < V5V_LDO1 < 5.25V; RL=60Ω.

Table 9. DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver						
CANH_dom	Dominant output voltage	V_TxD = 0V	3		4.25	V
CANL_dom			0.5		1.75	V
VO_dom_m	Matching dominant output voltage V5V_LDO1-V_CANH-V_CANL		-0.1		0.15	V
VO_diff	Differential output voltage V_CANH-V_CANL	45Ω < RL < 60Ω, V_TxD = 0V (dominant)	1.5		3	V
		No load; V_TxD = VLDO1 (recessive)	-50		50	mV
VO_rec	Recessive output voltage V_CANH, V_CANL	V_TxD = VLDO1; No bus load, Normal mode	2		3	V
		No bus load, Standby mode	-0.1		0.1	V
IO_short	Short circuit output current	V_TxD = 0V, V_CANH = 0V	-160		-50	mA
		V_TxD = 0V, V_CANL = 40V	+50		+160	mA
IO_rec	Recessive output current	-27V < V_CAN < 40V	-2.5		+2.5	mA
Receiver						
V_RxD_th	Differential receiver threshold voltage	-12V < V_CANH < 12V -12V < V_CANL < 12V Receive-only mode (CAN receiver)	0.5		0.9	V
		-12V < V_CANH < 12V -12V < V_CANL < 12V Standby mode (low-power receiver)	0.4		1.15	V

Table 9. DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_RxD_hys	Differential receiver hysteresis voltage	-12V < V_CANH < 12V -12V < V_CANL < 12V Receive-only mode (CAN receiver)	20		130	mV
I_RxD_LEAK	Input leakage current	V5V_LDO1 = 0V; V_CANH = V_CANL = 5V	100		250	µA
R_IN_cm	Common mode input resistance	Tested in Receive-only mode	15		35	kΩ
R_IN_cm_m	Common mode input resistance matching	V_CANH = V_CANL (Tested in Receive-only mode)	-3		+3	%
R_IN_diff	Differential input resistance	Tested in Receive-only mode	25		75	kΩ
VO_SPLIT	Output voltage on **SPLIT** pin	Normal mode -500µA < I_SPLIT < 500µA	0.3* V5V_LDO1		0.7* V5V_LDO1	V
IL_SPLIT	Leakage current on **SPLIT** pin	Standby mode 0V < V_SPLIT < 35V (Not production tested)	-5		+5	µA
		Standby mode -22V < V_SPLIT < 0 (Not production tested)	-1		+1	mA

Table 10. AC Electrical Characteristics

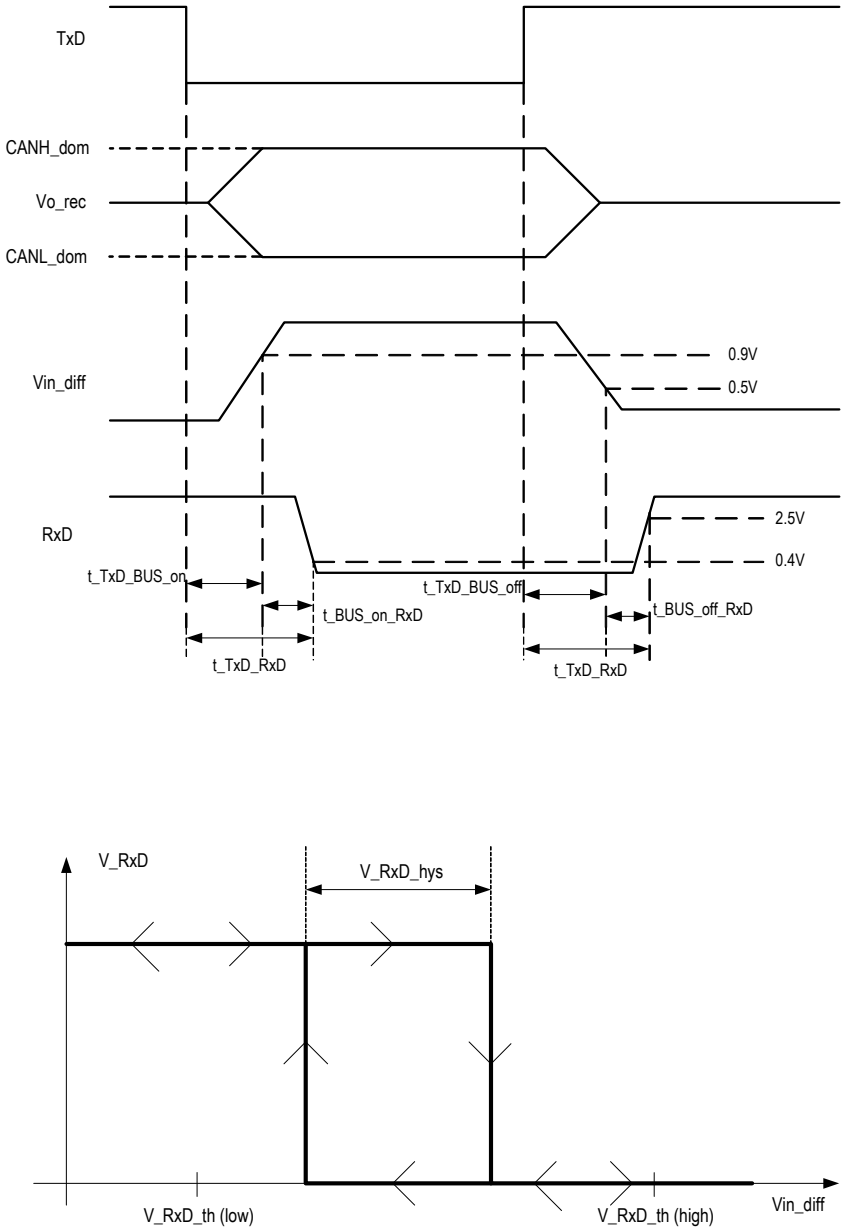
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_TxD_BUS_on	Delay TxD to bus dominant		10		110	ns
t_TxD_BUS_off	Delay TxD to bus recessive		10		140	ns
t_BUS_on_RxD	Delay bus dominant to RxD		15		115	ns
t_BUS_off_RxD	Delay bus recessive to RxD		20		160	ns
t_TxD_RxD	Propagation Delay TxD to RxD		40		255	ns
WAKE UP via BUS						
t_BUS_WR	Dominant time for wake-up detection via bus		0.75		5	µs
BUS Diagnostic						
t_OC_CANH	Time to detect over current CANH	V_TxD = 0V, V_CANH = 0V (Not production tested)	60			µs
t_LC_CANH	Time to detect low current CANH	V_TxD = 0V, V_CANH = 40V (Not production tested)	60			µs
t_OC_CANL	Time to detect over current CANL	V_TxD = 0V, V_CANL = 40V (Not production tested)	60			µs
t_LC_CANL	Time to detect low current CANL	V_TxD = 0V, V_CANL = 0V (Not production tested)	60			µs

Table 11. Temperature Limiter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{jshut}	Shut down temperature	Junction temperature when IC shuts down	150	170	185	ºC
T_{jrecv}	Recovery temperature	Junction temperature below which state machine returns from shutdown / warning	125	140	155	ºC
T_{jwarn}	Over-temperature warning flag set	Junction temperature beyond which the warning flag is set	140	157	175	ºC

6.4.1 Timing Diagrams

Figure 3. Timing Diagram and Hysteresis of CAN Receiver



6.5 Undervoltage Detection

Table 12. Undervoltage Detection

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VSUP_POR	VSUP Power on Reset threshold on	Rising edge of VSUP	5.09	5.5	5.91	V
VSUP_RESET	VSUP Power on Reset threshold off	(Master Reset for Device)	4.49	4.85	5.21	V
VSUP_POKTH	VSUP undervoltage threshold off	VSUP rising edge (Brown out reset threshold)	4.95	5.35	5.75	V
VSUP_UVTH	VSUP undervoltage threshold on (CAN bus in recessive state)	VSUP falling edge (Brown out reset threshold)	4.625	5.0	5.375	V
V5V_POKTH	V5V undervoltage threshold off	Rising edge of V5V	4.16	4.5	4.84	V
V5V_UVTH	V5V undervoltage threshold on	Falling edge of V5V	3.8	4.1	4.4	V
VLDO_POKTH	LDO undervoltage threshold off (VLDO1, VLDO2 and VLDO3)	Percent value is with respect to LDO output. Rising edge of LDO	87	89	91	%
VLDO_UVTH	LDO undervoltage threshold on (VLDO1, VLDO2 and VLDO3)	Percent value is with respect to LDO output. Falling edge of LDO	78	80	82	%
t_{rr}	Spike filter on VLDO1	To remove disturbance	2	4	8	µs
t_{Res}	Reset delay time		4	8	12	ms

6.6 Digital Timing Specification

SPI Protocol.

Table 13. SPI Timing Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
BR_{SPI}	Bit rate				1	Mbps
T_{SCLKH}	Clock high time		500			ns
T_{SCLKL}	Clock low time		500			ns
Write Operation Parameters						
t_{DIS}	Data in setup time		20			ns
t_{DIH}	Data in hold time		10			ns
T_{CSH}	CS hold time		40			ns
Read Operation Parameters						
t_{DOD}	Data out delay				80	ns
t_{DOHZ}	Data out to high impedance delay	Time for the SPI to release the SDO bus			80	ns
Timing Parameters for SCLK Polarity Identification						
t_{CPS}	Clock setup time (CLK polarity)	Setup time of SCLK with respect to CS falling edge	20			ns
t_{CPHD}	Clock hold time (CLK polarity)	Hold time of SCLK with respect to CS falling edge	20			ns

I²C Protocol. Electrical characteristics of SDA & SCLK bus lines for F/S mode

Table 14. I²C Electrical Parameters

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
V_{IL}	Low level input voltage: VLDO1related input levels		0.3V*LDO1		0.3V*LDO1	V
V_{IH}	High level input voltage: VLDO1-related input levels	0.7V*LDO1		0.7V*LDO1		V
V_{hys}	Hysteresis of Schmitt trigger input	n/a	n/a	0.05V*LDO1		V
V_{OL1}	Low level output voltage (open drain or open collector) at 3mA sink current		0.4		0.4	V
t_{of}	Output fall time from VIHmin to VILmax with a bus capacitance from 10pF to 400pF		250 (see Footnote 2)	20 + 0.1Cb (see Footnote 1)	250 (see Footnote 2)	ns (lab tested only)
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	n/a	n/a		50	ns
I_i	Input current of each I/O pin with an input voltage between 0.1VLDO1 and 0.9VLDO1 maximum	-10	10	-10 (see Footnote 3)	10 (see Footnote 3)	µA
C_i	Capacitance for each I/O pin		10		10	pF (guaranteed by design)

1. Cb = capacitance of one bus line in pF.
2. The maximum t_f for the SDA and SCLK bus lines quoted in Table 15 (300ns) is longer than the specified maximum t_{of} for the output stages (250ns). This allows for any series protection resistors to be connected between the SDA/SCLK pins and the SDA/SCLK bus lines without exceeding the maximum specified t_f.
3. I/O pins of Fast-mode devices must not obstruct the SDA and SCLK lines if VLDO1 is switched off.

Characteristics of the SDA and SCLK Bus Lines for F/S Mode I²C Bus.

Table 15. I²C Timing Parameters

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max (see Footnote 1)	
f_{SCLK}	SCLK clock frequency	0	100	0	400	kHz
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4	-	0.6	-	µs
t_{LOW}	Low period of the SCLK clock	4.7	-	1.3	-	µs
t_{HIGH}	High period of the SCLK clock	4.0	-	0.6	-	µs
t_{SU_STA}	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
t_{SU_DAT}	Data set-up time	250	-	100 (see Footnote 2)	-	ns
t_{HD_DAT}	Data hold-time	0 (see Footnote 5)	3450 (see Footnote 3)	0 (see Footnote 5)	900 (see Footnote 3)	ns
t_r	Rise time of SDA and SCLK signals	-	1000	20+ $0.1C_b$ (see Footnote 4)	300	ns
t_f	Fall time of SDA and SCLK signals	-	300	20+ $0.1C_b$ (see Footnote 4)	300	ns
t_{SU_STO}	Set-up time for STOP condition	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF
V_{nL}	Noise margin at the Low level for each connected device (including hysteresis)	0.1V*LDO1	-	0.1V*LDO1	-	
V_{nH}	Noise margin at the High level for each connected device (including hysteresis)	0.2V*LDO1	-	0.2V*LDO1	-	

1. All values referred to V_{IHmin} and V_{Ilmax} levels (see Table 14).
2. A fast mode I²C bus device can be used in Standard mode I²C bus system, but the requirement $t_{SU\_DAT} \geq 250ns$ must then be met. This will automatically be the case if the device do not stretch the low period of the SCLK signal. If such a device does stretch the low period of the SCLK signal, it must output the next data bit to the SDA line t_{rmax}. $T_{SU\_DAT} = 1000 + 250 = 1250ns$ (according to standard mode I²C bus specification) before the SCLK line released.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCLK signal.
4. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table 14 allowed.
5. This device internally provides a hold time of at least 300ns for the SDA signal to bridge the undefined region of the falling edge of the SCLK.

6.6.1 System Specification and Timings

Table 16. System Timing Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Mode Transition Related Timing						
T_{POST}	Power-up to Standby mode	Reset time included, Start-up watchdog not included			70	ms
T_{STNO}	Standby to Normal mode				10	ms
T_{SLST}	Sleep to Standby mode	Reset time included			50	ms
Wake-up Timing						
Tdom(wake)	Minimum dominant pulse for CAN wake-up detection (remote wake)		5			µs
Trec(wake)	Minimum recessive pulse for CAN wake-up detection (remote wake)		5			µs
TL_wake	Time between edge on WAKE pin to local wake detection			32		µs
TLW_filter	Time between edge on WAKE pin to WAKE_LOCAL signal (Filter on WAKE pin)		0.75		5	µs
TR_wake	Remote wake detection time from the valid pattern detection			24		µs
TINTN	INTN pin high time		7			µs
V_LWUTH	Local WAKE threshold input		2		4	V
Local Failure Related Timing						
TTxDC(dom)	TxD dominant timeout period		600	1000	1400	µs
TBUSC(dom)	BUS dominant clamping timeout period		600	1000	1400	µs
Watchdog Timing & Timeouts						
TWD(init)	Start-up Watchdog timeout (initialization time)			300		ms
Twd_trig	Window watchdog Trigger window	Twwd_period is defined in WWD register	0.375	0.5	0.625	Twwd_period

7 Detailed Description

The AS8650B consists of the following components on chip:

- DCDC converter with 5V outputs that supplies the three LDO voltage regulators and the CAN Transceiver
- Three voltage regulators with output voltages 3.3V, 2.8V and 1.8V and output accuracy up to 2.5%
- High-speed CAN bus Transceiver according to ISO 11898-5
- Integrated RESET unit with a power-on-reset delay and a programmable watchdog time

7.1 Operating Modes and States

The AS8650B provides four main operating modes Normal, Receive-only, Standby, and Sleep. In Normal mode, the CAN Transceiver can be disabled in case of over-temperature condition. The detailed transition table for each mode is shown in the subsequent pages.

7.1.1 Normal Mode

In Normal mode DCDC converter, the three voltage regulators, BUS Transceiver, and Window Watchdog are turned on with full functionality. All the LDO regulators are capable of delivering maximum load current possible as per their respective ratings. The BUS Transceiver is capable of sending the TxD data from the microcontroller to the CANH at the maximum rate.

7.1.2 Receive-Only Mode

In this mode, the CAN transmitter is disabled. The CAN receiver, the three voltage regulators, and over-temperature monitor circuit are enabled.

7.1.3 Standby Mode

This is the mode after power up. The Standby mode is a functional low-power mode where the CAN Transceiver is disabled. The bus wake-up (low power receiver) circuit, LDO1, and over-temperature monitor circuit are enabled. Both LDO2 and LDO3 can be enabled or disabled (default state) using the host command. The AS8650B can enter Normal mode, Sleep mode or Receive-only mode through host command.

7.1.4 Sleep Mode

Sleep mode is the current saving mode that is entered by host command or by over-temperature condition. The DCDC converter, the three voltage regulators, CAN Transceiver, the reset, and window watchdog unit are all switched off. The bus wake-up (low power receiver) circuit, oscillator, and over-temperature monitor circuit are active. The bus is in recessive state (high). The only wake-up possible is through remote wake-up (through the bus lines) or local wake up (through the WAKE pin) as described in the WAKE specification. In the case of entering Sleep mode due to over-temperature condition ($T > T_{jshut}$), the device can come out of Sleep only after the temperature falls back below the return temperature T_{jrecv} and any one of the wake up events mentioned above.

7.2 Power Management Strategy

The detailed block diagram and the power management strategy are shown in Figure 4.

Internal Regulator. This module is powered externally by the VSUP. All the critical modules that needs to be kept always on, work on this supply. Some of the important modules among them are Over-temperature monitor, Local Wake block, Internal Power-on Reset module, Internal Oscillator, complete mode-control unit, Undervoltage comparators of three external LDOs.

DCDC Converter. This is the main supply regulator for all the internal blocks. A step-down hysteretic buck converter is used to generate 5V output from VSUP. This 5V output is then used to generate all the three LDOs. This high-efficiency step-down DCDC converter contains the following features:

- Current limited operation
- Thermal shutdown

LDO1. This is the main I/O supply. This is generated internally from the 5V DCDC converter output and gives a regulated 3.3V output to power-up the external micro-controller. All the I/Os that interface with the microcontroller work on this supply.

LDO2. This regulator is generated internally from the 5V DCDC converter output and gives a regulated 2.8V output. The voltage level can be changed through factory settings.

LDO3. This regulator is generated internally from the 5V DCDC converter output and gives a regulated 1.8V output. The voltage level can be changed through factory settings.

Figure 4. Power Management Strategy

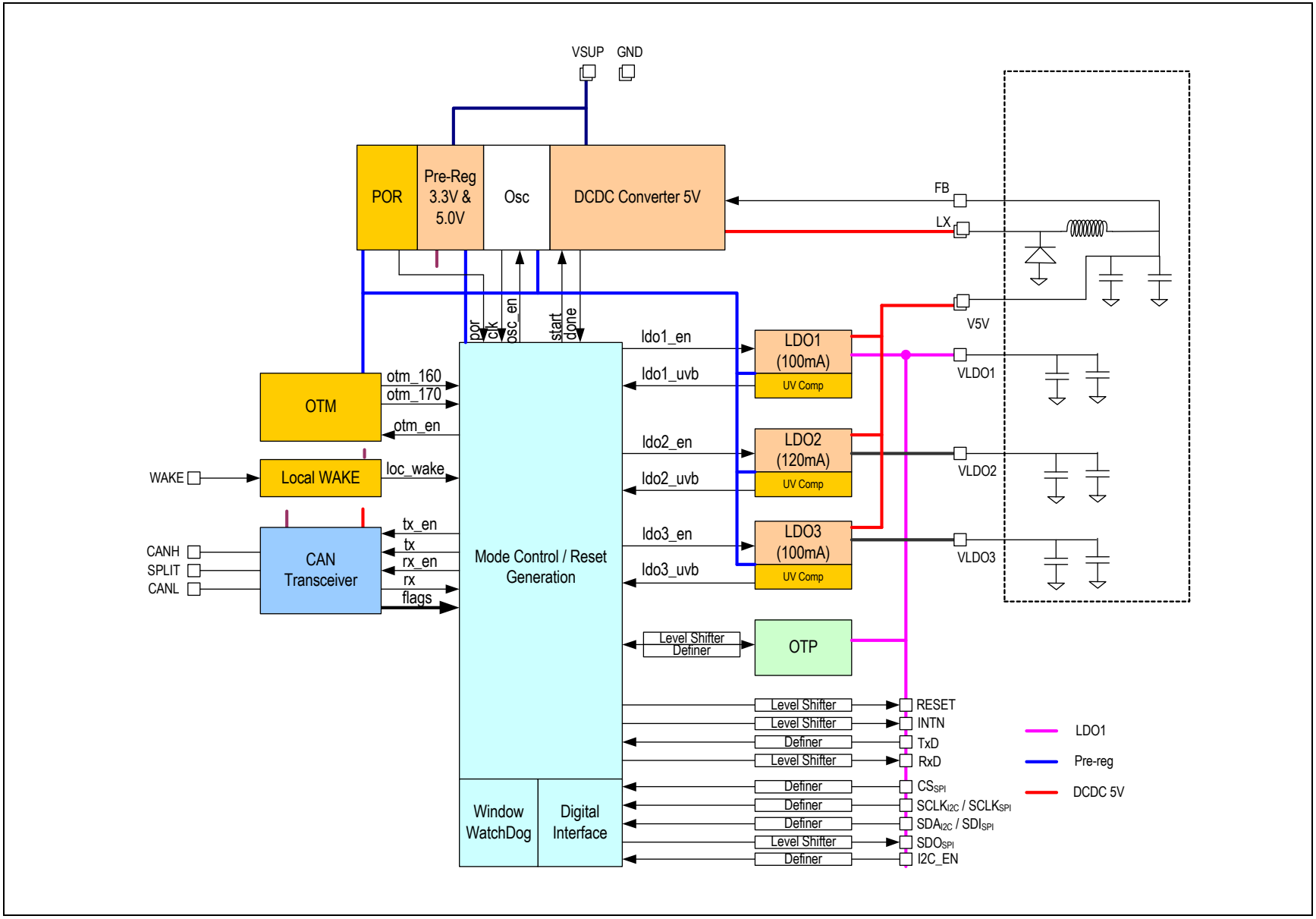


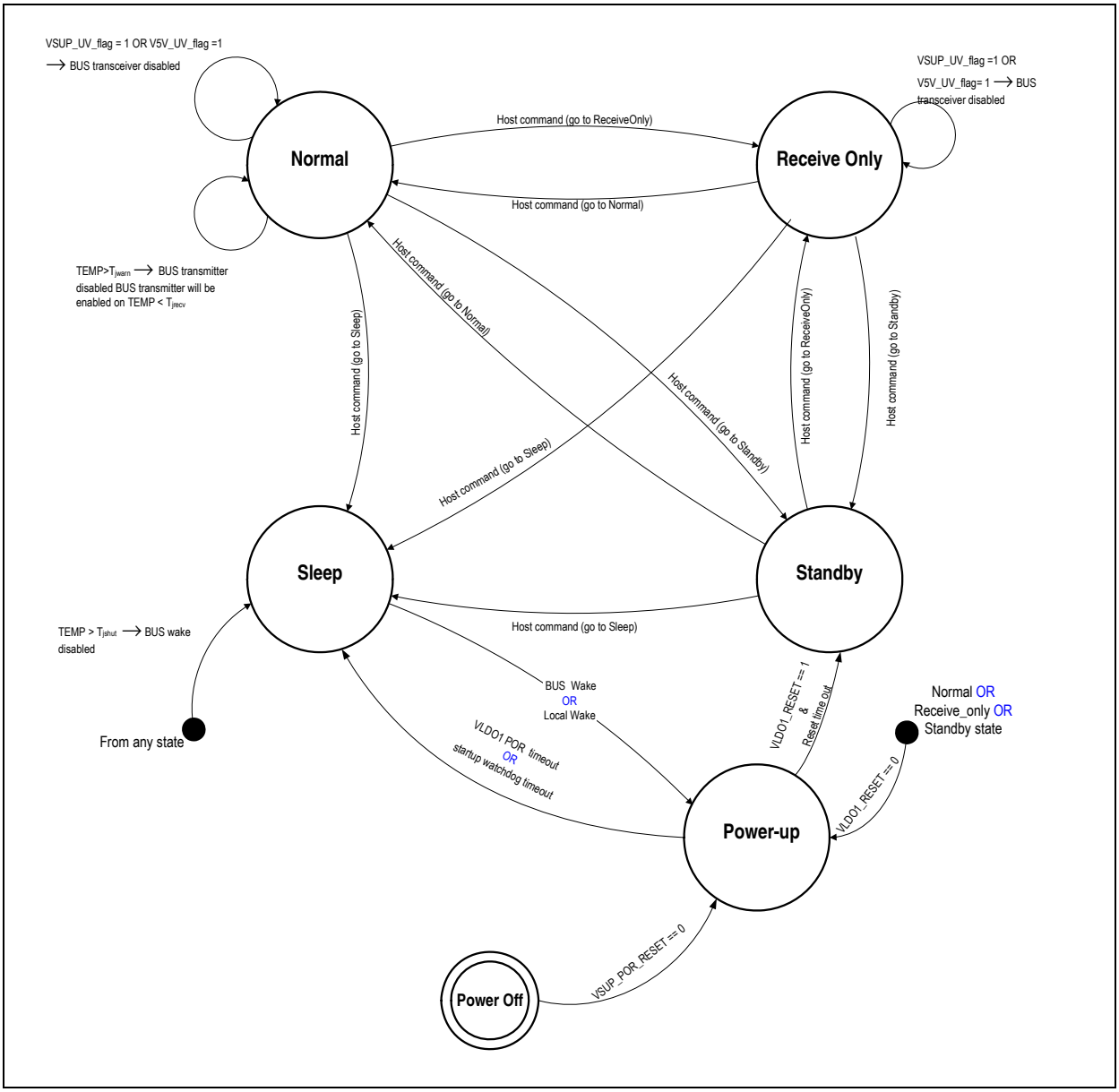
Table 17. Power Management Strategy for AS8650B

Control States	Power-up	Normal	Rx Only	Standby	Sleep
Analog Blocks					
DCDC Converter	ON	ON	ON	ON	OFF [1]
Oscillator	ON	ON	ON	ON	ON
Internal Regulator	ON	ON	ON	ON	ON
OTM	ON	ON	ON	ON	ON
LDO1	ON	ON	ON	ON	OFF
LDO2	OFF	ON [2]	ON [2]	OFF [1]	OFF
LDO3	OFF	ON [2]	ON [2]	OFF [1]	OFF
CAN Tx	OFF	ON	OFF	OFF	OFF
CAN Rx	OFF	ON	ON	OFF	OFF
Low Power Rx	OFF	OFF	OFF	ON	ON
LOCAL WAKE	OFF	OFF	OFF	ON	ON
SPLIT Generation	OFF	ON	ON	ON	ON
Digital Blocks					
WWD	OFF	ON	ON	ON	OFF
Digital Interface	OFF	ON	ON	ON	OFF

1. Can be turned ON using Device Configuration Register
2. Can be turned OFF using Device Configuration Register

7.3 State Diagram

Figure 5. State Machine Model



7.4 Initialization Sequence

The DCDC converter is switched 'ON'. Subsequently, on receiving power-good (PG) signal from the DCDC converter, the LDO1 regulator is switched 'ON'. During the initialization sequence, the VLDO1 is set to 2.5V if VLDO1 > VLDO1_POKTH threshold. VLDO1_RESET is released to 'high'. Then, active-low PORN_2_OTP is generated.

Initially the rising edge of PORN_2_OTP loads contents into the OTP latch. Next the LOAD_OTP_IN_PREREG signal loads the content of OTP latch into the pre-regulator domain register. Once the VLDO1_POKTH threshold is reached, the reset timeout timer also starts.

The RESET signal expires after Reset timeout period T_{Res}. After the RESET signal is 'high', the startup watchdog is launched. If the microcontroller generates a trigger within the startup window, then the device enters into Standby mode.

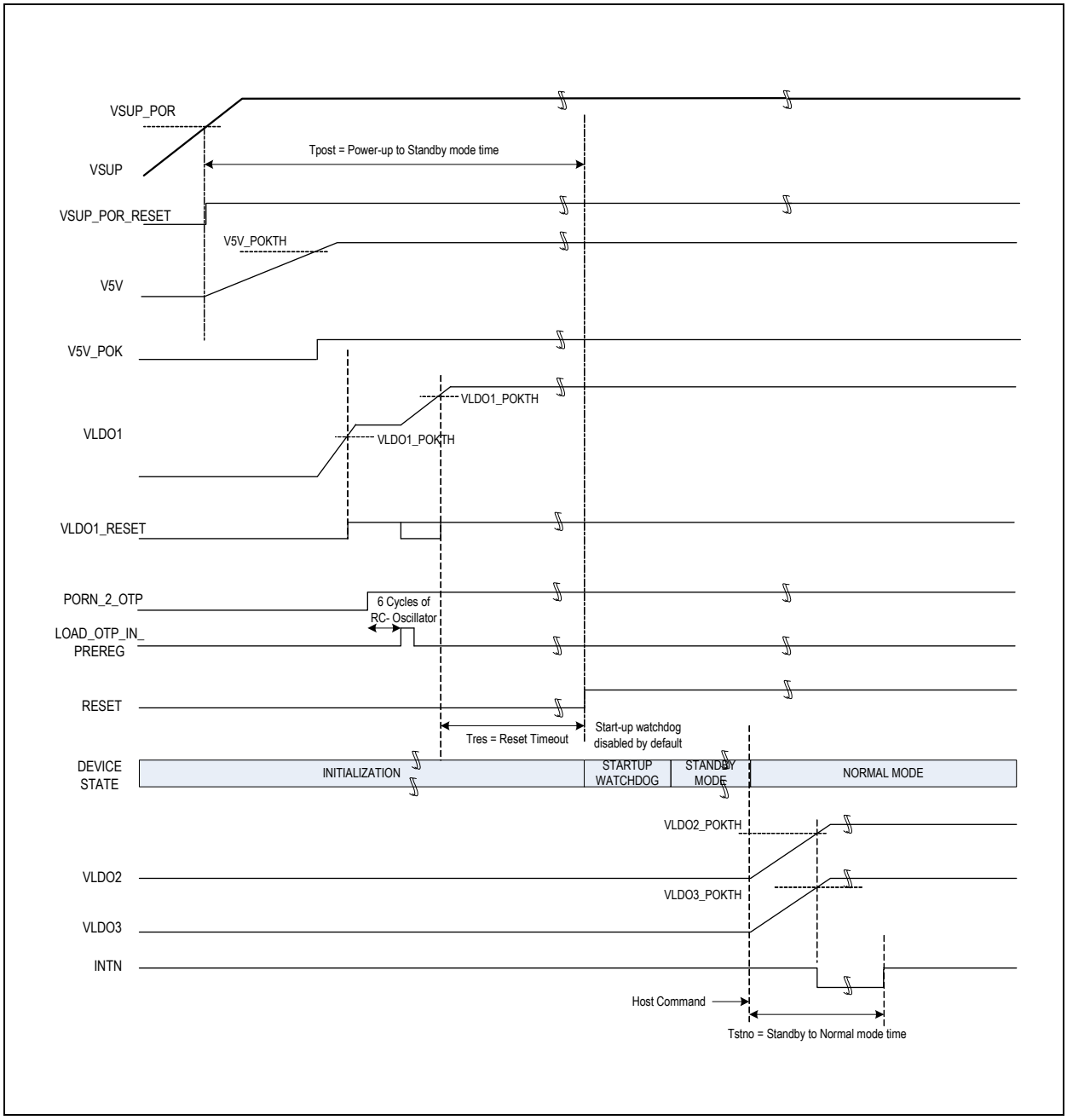
If the microcontroller fails to generate the trigger, then the RESET signal is generated and the Reset timeout will start.

If the microcontroller fails to generate the startup watchdog trigger for 3 consecutive times, then the device enters into Sleep mode. On receiving Normal mode command from the microcontroller, the LDO2 and LDO3 regulators are activated. By the time VLDO2 and VLDO3 reach their respective power-ok (POK) threshold values, an interrupt signal is generated. The AS8650B supports very slow VSUP ramp up of 0.5V/min.

The power initialization sequence diagram is shown in Figure 6.

- After activating the power supply on VSUP pin, the VSUP_POR_RESET flag becomes inactive (high) while the voltage exceeds the VSUP_POR threshold.
- The DCDC output voltage V5V exceeds the V5V_POKTH thresholds after the DCDC settling time and the first voltage regulator (LDO1) will be activated with the V5V_POK set.
- If the voltage output at LDO1 (set to 2.5V on power-up) reaches the VLDO1_POKTH threshold, the PORN_2_OTP flag is set and OTP register setting for the LDO1 is read. Consequently the output voltage will be regulated to the actual OTP settings.
- The initialization phase of the device is terminated after the preset output voltage level threshold is exceeded and the reset timeout is expired.
- After entering Standby mode the host controller can switch the device in any operation mode through the I²C or SPI interface.

Figure 6. Initialization Sequence



7.5 DCDC Converter

The high-efficiency, high-voltage, hysteretic step-down DCDC converter, operates in asynchronous mode and delivers 500mA of output load to drive the three internal LDOs and the CAN Transceiver. The low-power architecture extends hold-up time in battery-backed and critical applications where maximum up-time over a wide input supply voltage range is needed, while still providing for high efficiencies of up to 90% during peak current demands.

7.6 Voltage Regulator LDO1

The stability of the voltage output is below ±2.5% over the full input range and temperature for load current up to 100mA at 3.3V. Power Input to this LDO is the V5V_LDO1 pin. This LDO is activated in Normal, Receive-only or Standby mode. It is switched OFF in Sleep mode.

7.7 Voltage Regulator LDO2

The stability of the voltage output is below ±2.5% over input range and temperature for load current up to 120mA at 2.8V. Power Input to this LDO is the V5V_LDO2 pin. LDO2 is activated in Normal and Receive-only mode. The output voltage level can be changed through factory settings. For further information, please contact *ams* regional sales person.

7.8 Voltage Regulator LDO3

The stability of the voltage output is below ±2.5% over input range and temperature for load current up to 100mA at 1.8V. Power Input to this LDO is the V5V_LDO3 pin. LDO3 is activated in Normal and Receive-only mode. The output voltage level can be changed through factory settings. For further information, please contact *ams* regional sales person.

7.9 Over-Temperature Monitor

In Normal mode, if the junction temperature reaches the over-temperature threshold T_{jwarn}, a warning flag is set in the diagnostic register which can be accessed via the I²C and the SPI interface and an interrupt is signalled on INTN pin. The CAN transmitter is disabled and the device remains in Normal mode. If the junction temperature falls below T_{jrecv}, the CAN transmitter is enabled. The warning flag is cleared in the diagnostic register and an interrupt is signalled at the INTN pin. If the junction temperature exceeds the over-temperature threshold T_{jshut}, the device enters Sleep mode irrespective of the current mode and bus wake receiver (Low power receiver) is disabled. As soon as the temperature falls below T_{jrecv} (thermal recovery), the device goes through the power-up sequencing while entering Power-up mode and enters Standby mode if the boundary conditions of the statemachine are fulfilled.

7.10 Undervoltage Reset

Undervoltage on VSUP (Brown out Indication). If VSUP voltage falls below VSUP_UVTH threshold, the VSUP_UV_flag is set and an interrupt at INTN is generated. In this case the device enters into the Standby mode. The LDO1 voltage regulator remains activated. Two scenarios are possible at this stage:

- VSUP is recovering: If VSUP exceeds the VSUP_POKTH threshold, the VSUP_POK_flag is set and the device remains in Standby mode.
- VSUP is still falling: In this case the device continues to stay in Standby mode. If voltage falls below VSUP_RESET threshold, then the device enters Power-Off and the logic is reset.

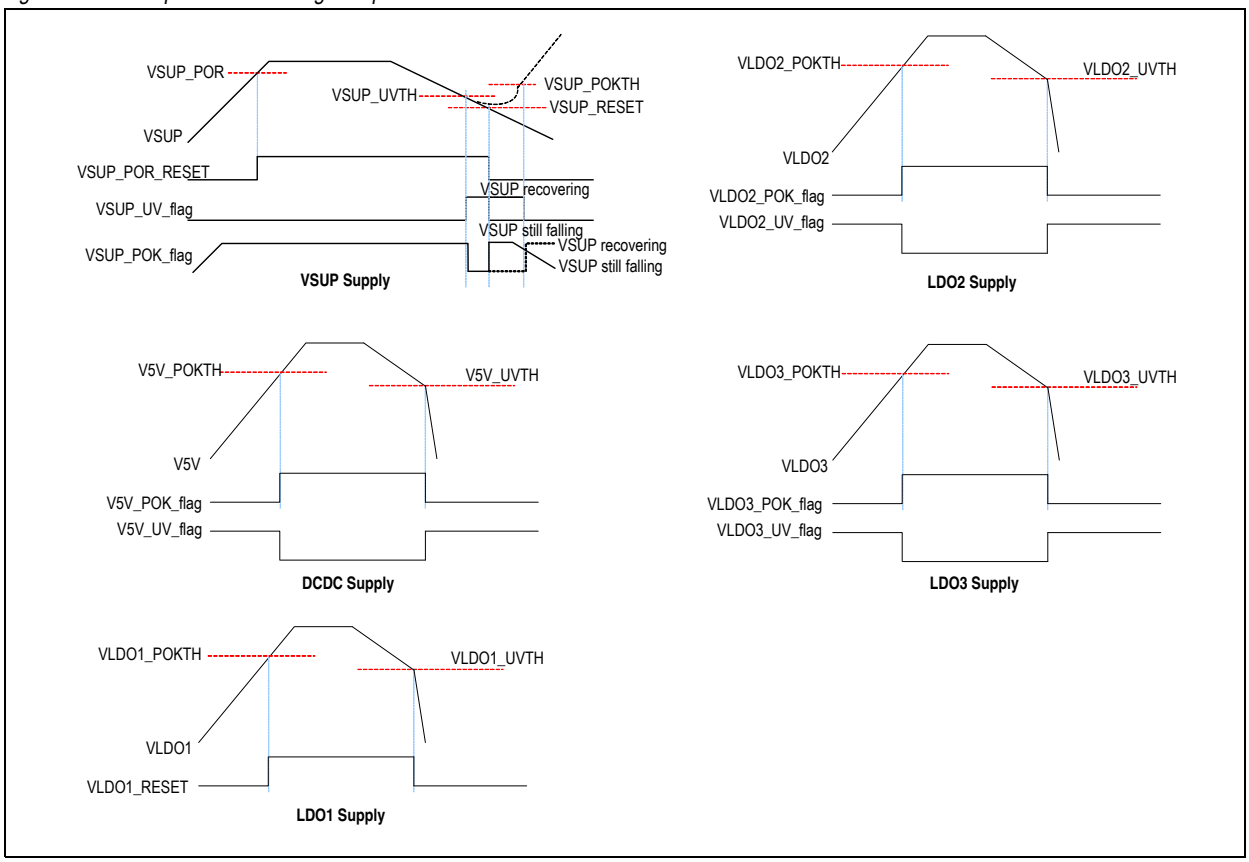
Undervoltage on V5V. If the V5V falls below V5V_UVTH threshold, the V5V_UV_flag is set. Once V5V returns to V5V_POKTH threshold value, V5V_POK_flag is set. In case a flag is set, an interrupt is generated at the INTN pin. If undervoltage on V5V occurs in Normal or Receive-only modes then CAN Transceiver is disabled and the device remains in its operation mode.

Undervoltage on LDO1. If the voltage level of LDO1 falls below the VLDO1_UVTH threshold value and device is not in Sleep mode, the device enters into power-up state while RESET signal is asserted and the voltage regulator is still active. Once the VLDO1_POKTH threshold is reached, RESET signal is de-asserted after reset timeout period and device enters into Standby mode.

Undervoltage on LDO2. If the voltage level of the LDO2 falls below the VLDO2_UVTH threshold value a VLDO2_UV_flag is set. An indication is given to microcontroller by setting a bit in interrupt register and giving interrupt on INTN pin. Once VLDO2 returns to VLDO2_POKTH threshold value, VLDO2_POK_flag is set. An indication is given to microcontroller by setting a bit in interrupt register and giving interrupt on INTN pin.

Undervoltage on LDO3. If the voltage level of the LDO3 falls below the VLDO3_UVTH threshold value a VLDO3_UV_flag is set. An indication is given to microcontroller by setting a bit in interrupt register and giving interrupt on INTN pin. Once VLDO3 returns to VLDO3_POKTH threshold value, VLDO3_POK_flag is set. An indication is given to microcontroller by setting a bit in interrupt register and giving interrupt on INTN pin.

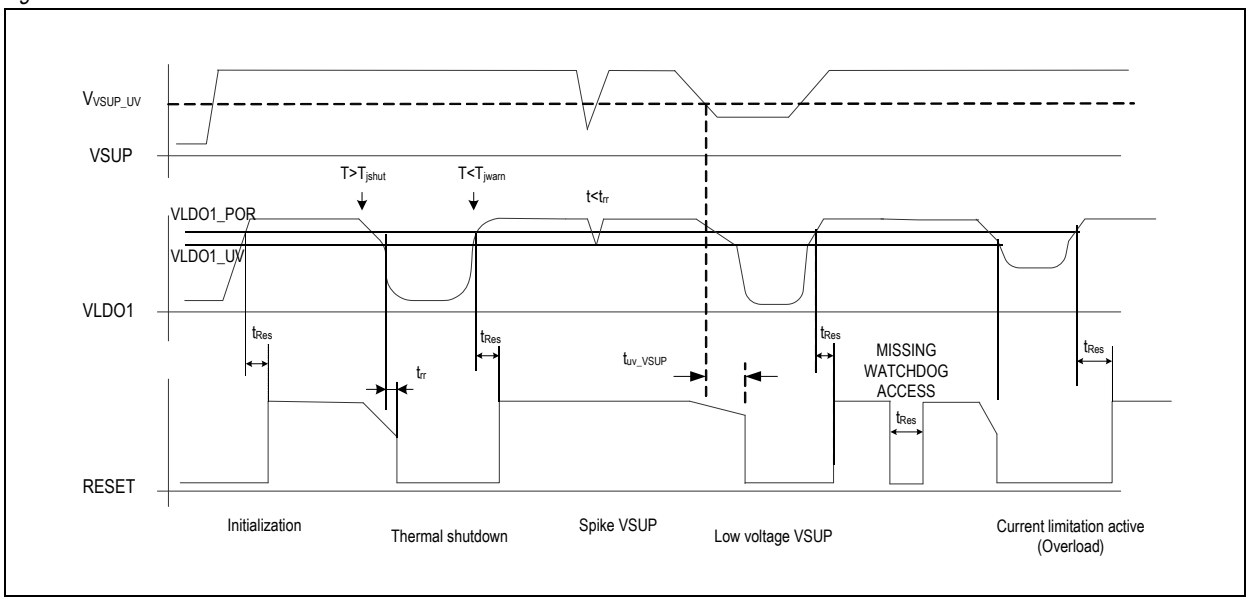
Figure 7. Power-up and Undervoltage Sequence



7.11 Reset Block

The reset block generates an external RESET signal to reset the microcontroller and all other external circuits. The reset functionality is explained in Figure 8. The reset block consists of a digital buffer at the output. The RESET signal is affected by VLDO1_RESET (during overload, reset on VLDO1) and watch dog output. All conditions which cause a drop of the VLDO1 voltage will be detected from the low voltage reset unit which in-turn generates a reset signal.

Figure 8. Reset Block Functional Waveform



7.12 CAN Transceiver

The AS8650B provides an advanced interface between the protocol controller and the physical bus in a Controller Area Network (CAN) node. This is intended for automotive high-speed CAN application (up to 1 Mbit/s), providing differential transmit capability to the bus and differential receive capability to the CAN controller. It is fully compatible to the ISO 11898-5 standard and offers excellent Electromagnetic Compatibility (EMC) performance. The CAN is a high-speed, low complexity protocol with improved EMI and EMC performance. The CAN is a serial communication protocol efficiently supporting the control of mechatronic nodes in a distributive automotive application. The basic blocks of the CAN Transceiver are described below:

7.12.1 BUS Driver

This driver has the basic functionality of relaying the data from the microcontroller on to the CAN bus. The data on the CAN needs to have a controlled slew to reduced EMI. A low side driver is used which has an inherent reverse polarity protection. It has a Short-Circuit current limitation.

7.12.2 Normal Receiver

It relays the data from the CAN bus to the microcontroller in Normal mode.

7.12.3 Low Power Receiver

It relays the data from the CAN bus to the microcontroller in low power mode state.

7.12.4 Operating Modes

The CAN Transceiver provides the following operating modes:

- NORMAL: Non low power mode
- RECEIVE-ONLY: Non low power mode
- STANDBY: Low power mode
- SLEEP: Low power mode

Normal Mode. In this mode the Transceiver is able to send and receive data signals on the bus. RxD reflects the bus data.

Receive-Only Mode. In this mode the Transceiver has the same behavior as in Normal mode but the transmitter is disabled.

Standby Mode or Sleep Mode. In this mode the Transceiver is not able to send and receive data signals from the bus, but the wake up detector is active. The power consumption is significantly reduced respect the non low power operation modes. The WAKE_REMOTE reflects the remote wake up detector output; WAKE_LOCAL reflects the input signal on WAKE pin.

Table 18. Operating Modes

State	TxD	Transmitter	Normal Receiver	Low Power Receiver	Bust State
NORMAL	L	Enabled	Enabled	Disabled	Dominant
	H	Enabled	Enabled	Disabled	Recessive
REC ONLY	X	Disabled	Enabled	Disabled	(CANH, CANL are not driven)
STANDBY	X	Disabled	Disabled	Enabled	(CANH, CANL are not driven)
SLEEP	X	Disabled	Disabled	Enabled	(CANH, CANL are not driven)

7.12.5 Local Wake-up Event

The WAKE pin is pulled-down to ground using the internal resistor. In all low power modes, if the voltage on the WAKE pin rises above V_LWUTH for longer than T_{LW_filter}, WAKE_LOCAL rises up. For valid wake-up, the WAKE pin needs to be above V_LWUTH as shown in Figure 9. Valid WAKE is detected only at the positive edge of the WAKE pin.