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**high
performance
needs great
design.**

Coverpage: AS89010 Datasheet

Please be patient while we transfer this adapted former MAZeT document to the latest ams design.

DATASHEET

AS89010

16 bit 4-channel analog-to-digital converter (ADC) with I²C control/output

SSOP16

Order No.: 305030004

Status: preliminary

FEATURES

- Conversion of 4 sensor signals of photodiodes (e.g. RGB/XYZ color plus one blank channel for compensation of parasitic currents or temperature conversion) or other sensors with current signal output
- Configurable conversion gain and integration time supports a very high dynamic range of 1 – 2.68E+08
- Up to 16 bit (internal 20 bit) signal resolution by achievable sensitivity up to 20 fA/LSB – scaling (by a divider) the internal 20 bit on 16 bit output
- Adjustable operation modes like continuous, by command and externally synchronized (by given start and start/end signal) measurement
- Option: external control of integration time and reference current (gain)
- High linearity of amplifying, no cross talking
- High absolute accuracy without additional sources
- High reliability internal reference source generation
- Consideration of negative offset
- Measurement of current for both polarities
- Measurement of integration time
- Supply and temperature independent response
- Insensitive to 50 Hz/60 Hz external disturbances
- 16 Bit/400 kHz fast I²C interface with programmable slave addresses
- Very low current consumption in active, in *Power down* and *Standby mode*
- Supply voltage 2.7 V to 3.6 V
- Temperature range -40°C to 125°C
- Deliverable in SMD package and as bare die

APPLICATIONS

- Precise conversion of average e.g. integral photo current for optical sensors and arrays (e.g. UV, VIS, IR) and other sensors with current output
- In combination with ams Sensors Germany's color sensors: measurement of lights – chromaticity coordinates (XYZ CIE 1931, DIN 5033 and similar) or color temperatures to control and process displays and backlights (e.g. LED, CCFL)
- In combination with ams Sensors Germany's color and spectral sensors: measurement of reflective and/or transmitted light – chromaticity coordinates (XYZ CIE1931, DIN5033 and similar) measurement of objects and surfaces for analyzes, quality management, sorting, etc.

MARKET SEGMENTS

- Lighting SSL, Photometry
- Chemical and biochemical analyses
- Industrial process control
- Medical and environment instrumentation
- Industrial/commercial lighting
- Infotainment (backlights and video walls) and monitors
- High quality consumer displays and tablets

FEATURES	1
APPLICATIONS	1
MARKET SEGMENTS	1
1 GENERAL DESCRIPTION	4
2 ELECTRICAL CHARACTERISTICS.....	5
2.1 Absolute Maximum Ratings	5
2.2 Recommended Operating Conditions	5
2.3 Electrical Characteristics	7
3 BLOCK DIAGRAM	8
4 PIN ASSIGNMENT.....	8
5 DESCRIPTION OF FUNCTION.....	9
5.1 Measurement Modes.....	9
5.1.1 Continuous Measurement Mode (<i>CONT Mode</i>).....	9
5.1.2 Command Measurement Mode (<i>CMD Mode</i>).....	10
5.1.3 Synchronous Measurement Start Mode (<i>SYNS Mode</i>).....	10
5.1.4 Synchronous Measurement Start and Stop Mode (<i>SYND Mode</i>).....	11
5.2 Power Down	12
5.3 Standby.....	12
5.4 A/D Conversion.....	13
5.4.1 Offset of the A/D Converter.....	15
5.4.2 Divider	15
5.5 Conversion Time Measurement	16
5.6 I ² C Communication	16
5.6.1 Write Protocol.....	17
5.6.2 Read Protocol	17
5.6.3 I ² C Addressable Register Space	18
5.6.4 Examples of using I ² C-interface.....	18
6 DESCRIPTION OF REGISTERS.....	20
6.1 Control Register Bank.....	20
6.2 Operational State Register – OSR.....	20
6.2.1 API Generation Register – AGEN	21
6.2.2 Configuration Register – CREGL and CREGH	21
6.2.3 Options Register - OPTREG.....	24
6.2.4 Register – BREAK.....	24
6.2.5 Register – EDGES	25
6.3 Output Register Bank	25
6.4 I ² C Interface	26

7 PACKAGE 27

7.1 Shape and Dimensions 27

7.2 Pin Configuration 27

7.3 Packing Information 28

7.4 Soldering Information..... 28

8 APPLICATION NOTES 30

9 NOTES FOR PCB LAYOUT 38

ORDERING INFORMATION 39

LEGAL NOTES AND WARNINGS 40

PRELIMINARY

1 GENERAL DESCRIPTION

The ASIC AS89010 is a low noise sensor interface application specific standard product (ASSP) and suitable for coupling of multi-channel optical sensors or sensors using current output. It converts input currents of for example photodiodes (both polarities) to a digital output and realizes a continuous or triggered measurement via current integration. Optional the integration time and sensitivity can be controlled by external programming to extend the internal functions and parameters. The four signal channels convert directly and simultaneously the input currents to a digital representation of the measured average. The channels may be divided into three signal channels and one dummy channel for compensation of parasitic currents. This ASIC is especially suitable for signal conditioning of photodiodes of array sensors like color or other optical sensors with maximum of 4 channels per chip¹. A configurable conversion gain factor and integration time support a dynamic range² of 1 - 2.68E+08 and achieves an accuracy of up to 16 bit signal resolution with sensitivity up to 20 fA/LSB.

The internal reference generations offers a high reliability. The converter is insensitive to a 50 Hz/60 Hz external disturbances and was especially designed to accommodate high accuracy at high sensitivity offering high robustness. Automatic *Power down* (sleep function) between subsequent measurements offers operation with very low current consumption. Further, it offers a wide range of reference currents (1.25 nA to 5 µA), integration times (1 ms to 1 s), synchronized mode and other control modes adjustable by user programming. The conversion data can be accessed via 16 bit/400 kHz fast I²C Interface with programmable slave addresses. Measurement of actual integration time for a full triggered measurement can be performed.

AS89010's supported operating modes depending on required performance:

- *CMD Mode* – single measurement and conversion (controlled via I²C bus),
- *CONT Mode* - continuous measurement and conversion (periodically recurring measuring cycles) until "Stop" controlled via I²C bus,
- SYN[x] modes - synchronized measurement and conversion:
 - [*SYNS Mode*] synchronization of start,
 - [*SYND Mode*] synchronization of start and stop of measuring cycle on the falling edge of the SYN pin.

The settings for the input current range and integration time are not affected by alternative modes. Further the converter supports functions like *Power down* and *Standby*. It represents a low power solution and is also suitable for mobile applications.

Based on the high flexibility the AS89010 is suitable as converter for a wide range of multi-channel sensors with current output. The device achieves a high dynamic range especially in (back) light applications and in measurements of integral intensity of pulsed light. The combination of ams Sensors Germany's color sensors with AS89010 is excellently suited for photometry applications (brightness, color coordinate and/or color temperature), for determining current values for control of spectrally mixed LED light sources or as sensors for display and (back)light calibration and mobile devices for light measurement. The sensor signal IC is available in SMD housing or can be supplied as a bare die.

¹ Upon consideration of that I²C address more ASICs may be used in parallel to a sensor to convert more than 4 sensor channels. In that case special operating notes must be considered.

²

$$\text{Dynamic Range} = \frac{\text{MAX measureable value} = \text{Max. Full Scale Range}}{\text{MIN measureable value} = \text{Min. Least Significant Bit}}$$

2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Violations of absolute maximum conditions are not allowed under any circumstances; otherwise the IC can be destroyed.

All voltages are referenced to VSSA = VSS = 0 V.

Table 1: Maximum conditions

PARAMETER	NAME	MIN	MAX	UNIT
Power Supply (analog)	VDDA	-0.5	5.0	V
Input and Output Voltages (analog)	VIOA	-0.5	VDDA+0.5	V
Power Supply (digital)	VDD	-0.5	5.0	V
Input and Output Voltages (digital)	VIOD	-0.5	VDD+0.5	V
Supply Voltage Difference ³ VDDD-VDDA	DIFF_VDD		0.3	V
Ambient Temperature	TOP	-40	125	°C
Storage Temperature	TSTG	-55	150	°C
Weight	m		0.076	g

2.2 Recommended Operating Conditions

Table 2: Operational conditions; VSSA=VSS=0 V

PARAMETER	NAME	MIN	TYP	MAX	UNIT	CONDITION
Supply Voltage	VDDA VDD	2.7	3.3	3.6	V	VDDA-VDD < 0.3 V
External Resistor ⁴	REXT		3.3		MΩ	±1%
Temperature Coefficient of REXT	TC _{REXT}			50 ⁵	ppm/K	
Operating Temperature	T _{AMB}	-40		125	°C	
Pull Up Resistance at SCL, SDA	R _{I2C}	1.8 ⁶	4.7		kΩ	
Load Capacity at SDA	C _L			200	pF	
Input High Level	VIH	0.7			VDD	

³ For the Digital Supply Voltage VDD it is not allowed to use a voltage above VDDA+0.3 V. This condition must be also complied during the ramp-up phase of the supply voltages.

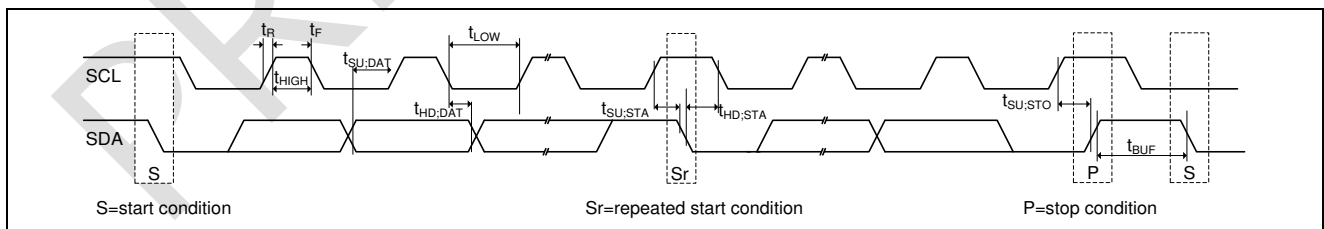
⁴ The resistor directly influences the generating of the reference current for the signal conversion. Therefore, the temperature coefficient of resistance has an important role. The smaller the temperature coefficient and the resistor value tolerance (1% better than 5%, etc.) result the more accurate the result of the converting.

⁵ The smaller the better - the result depend on the sum of all TKs of the full sensor system (photo diode, REXT, converter, ...)

⁶ Lower resistance on request

PARAMETER	NAME	MIN	TYP	MAX	UNIT	CONDITION
Input Low Level	VIL			0.3	VDD	
Output High Level	VOH	0.8			VDD	$I_{Load} = 2.5 \text{ mA}$
Output Low Level	VOL			0.4	V	$I_{Load} = 1.8 \text{ mA}$
Input Capacity at IN0 to IN3	CPD			80	pF	
SCL frequency	f_{SCL}	0		400	kHz	
SCL high pulse width	t _{HIGH}	0.6			μs	
SCL high pulse width	t _{LOW}	1.3			μs	
SCL, SDA rise time	t _R			0.3	μs	
SCL, SDA fall time	t _F			0.3	μs	
Hold time start condition	t _{HD;STA}	0.6			μs	
Setup time start condition	t _{SU;STA}	0.6			μs	
Data hold time write ⁷	t _{HD;DATM}	0.02		0.9	μs	
Data setup time	t _{SU;DAT}	0.1			μs	
Setup time stop condition	t _{SU;STO}	0.6			μs	
Bus free time between a stops and start condition	t _{BUF}	1.3			μs	
SYN negative pulse width	t _{SYN}	1.5			μs	SYN recognized as start/end of integration

Figure 1: I²C interface timing diagram



⁷ Data transfer direction from Master to slave (AS89010) - Write

2.3 Electrical Characteristics

Table 3: Specifications; VSSA=VSS=0 V; VDDA=VDD=2.7 V to 3.6 V REXT=3.3 M Ω ; TAMB = -25°C to 85°C, unless otherwise noted

PARAMETER	NAME	MIN	TYP	MAX	UNIT	CONDITION
Analog Supply Current	IVDDA		0.72	1	mA	measurement active
Digital Supply Current	IVDD		0.23	0.29	mA	measurement active or Standby mode
Power down Supply Current IPD = IVDDA_PD + IVDD_PD	IPD		0.01	1	μ A	Power down mode
Analog Standby Supply Current	IVDDA_SBY	200		400	μ A	Standby mode, no measurement
Clock Frequency	f _{CLK}	0.75	1.024	1.25	MHz	
ADC Resolution	NR	10		20	bit	internal resolution
Conversion Time Tolerance	Δ TINT	-30		30	%	-40°C to 125°C
Integral Nonlinearity	INL	-0.2 -0.05		0.2 0.05	%	R=000b to 001b R=010b to 100b
Differential Nonlinearity	DNL			0.9	LSB	no missing codes
Start Up Time from Power down	T _{START}		500		μ s	pp to measurement start
SYN Trigger Delay	T _{SYNDEL}			5	μ s	from falling SYN edge to measurement start
Full-Scale-Range Error	EIFSR	-5		6	%	referred to nominal value
Gain Error (CONT, CMD, SYNS, SYND with processing of OUTINT time)	E _{GAIN}	-5		6	%	referred to nominal value
Gain Error (SYND without processing of OUTINT time)	E _{GAIN}	-20		20	%	referred to nominal value
Gain Matching Error ⁸	E _{MATCH}	-2 -1.5		2 1.5	%	R=000b R=001b to 100b
Gain Temperature Drift	T _{CGAIN}		50	200	ppm/K	CONT, CMD, SYNS Mode
Gain Temperature Drift @ SYND	T _{CGSYND}		200	700	ppm/K	SYND Mode
Effective Resolution (TINT=64 ms, DIR=1)	ER	13.5 14.5 15.5	14 15 16		bit	R=000b R=001b to 011b R=100b
Data hold time read ⁹	t _{HD;DATS}	0.3 ¹		0.9 ¹	μ s	

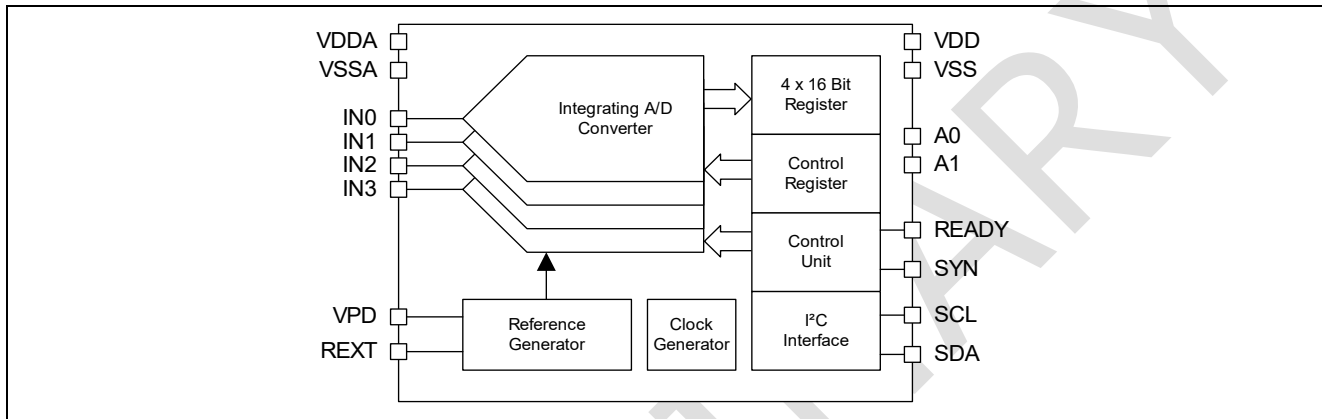
⁸ Up to -1.5%...+1.5% for all gains available on request

⁹ Data transfer direction from slave (AS89010) to Master (Read). The AS89010 provides a hold time of at least 300 ns and maximum of 900 ns for the SDA signal.

3 BLOCK DIAGRAM

The main components of the AS89010 are shown in Figure 2. The input currents are directly converted by Delta-Sigma to digital converter. The reference current for the A/D converters and optionally the bias voltage for the photodiodes VPD (see Figure 19) are provided by the internal reference generator¹⁰. The results of the A/D conversion are stored in four 16 bit registers and can be accessed via I²C interface. The input SYN can be used for an externally triggered start or start and stop of the measurement, the output READY gives the information of the status of the conversion. The I²C slave address is set by pins A0 and A1. Separated analog and digital power supply pins are used for noise decoupling.

Figure 2: Block diagram



4 PIN ASSIGNMENT

The Pin assignment is shown in the following table.

Table 4: Pin assignment (Analog/Digital)

PIN	TYPE	A/D	DESCRIPTION
VDDA	power	A	analog power supply voltage
VSSA	power	A	analog power supply voltage
VDD	power	D	digital power supply voltage (VDDA = VDD)
VSS	power	D	digital power supply voltage (VSSA = VSS)
IN0, IN1, IN2, IN3	input	A	input current
REXT	input	A	external resistor of 3.3 MΩ
VPD	output	A	photodiodes bias voltage (cathode or anode)
SCL	input	D	I ² C clock input
SDA	input / output	D	I ² C data input / output, open drain output stage
SYN	input	D	externally controlled conversion
READY	output	D	conversion status, push pull output stage
A0, A1	input	D	variable I ² C slave address

¹⁰ The external resistor REXT directly influences the generating of the reference current for the signal conversion. Therefore, the temperature coefficient of resistance has an important role. The smaller the temperature coefficient and the resistor value tolerance (1% better than 5%, etc.) result the more accurate the result of the converting.

5 DESCRIPTION OF FUNCTION

The AS89010 performs current to digital conversion by four parallel A/D converters. The sensitivity, start and stop of conversion are user defined and should be adapted to the application of interest. Upon the end of each conversion, the digital equivalents of the input currents are stored in the output register (OUT0 to OUT3). Pin READY stays at low logic level all the time during the conversion. Rising edge and following high logic level of READY signalizes the end of conversion.

5.1 Measurement Modes

There are four available modes how the measurement can be performed. According to the assignment of register CREGL:MODE (Table 11) one of four possible measurements can be performed by the device. However, it is always recommended regardless of the mode, to transfer no data via I²C during the measurement process. It is suggested to use the measurement-free time cycles for data transfer via I²C.

5.1.1 Continuous Measurement Mode (CONT Mode)

The A/D conversion will be performed sequentially. The first conversion starts with setting the SS bit in OSR register. If the Standby was active, the device deactivates it and initializes the continuous measurement. Measurement can only be stopped by resetting the SS bit. The conversion time (integration time TINT) is determined by the full-scale of the register CREGL:T (T). The rising edge of READY signalizes the end of each conversion. It is recommended to read output data during the break time between two consequent conversions in order to not disturb the integration operation. This break time can be configured in 4 μs steps up to 1,021 μs (see Table 13). The break time should be configured long enough to prevent overlapping of data fetch activity with the measurement. For further details see also Figure 21.

Figure 3: CONT Mode timing with short break time

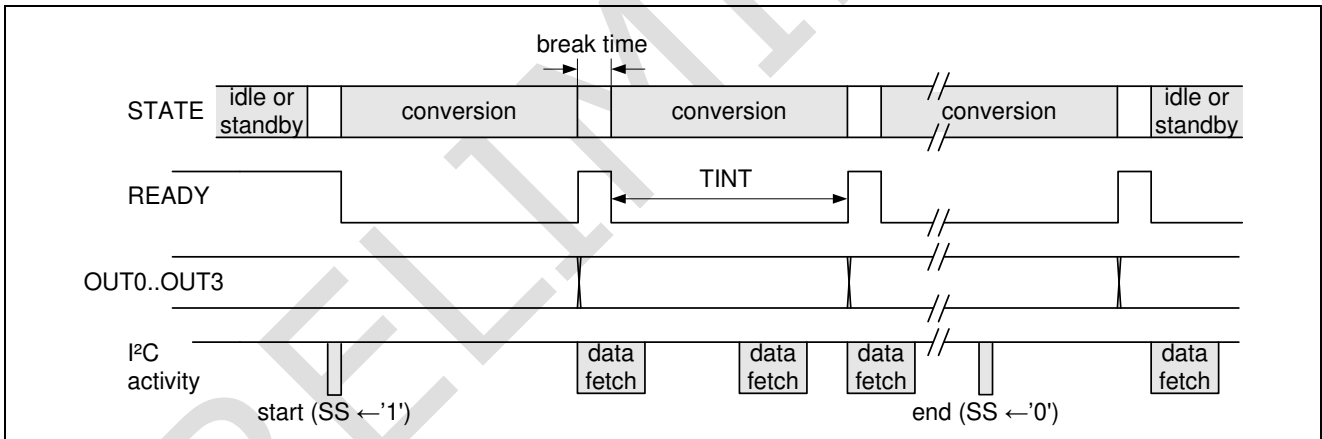
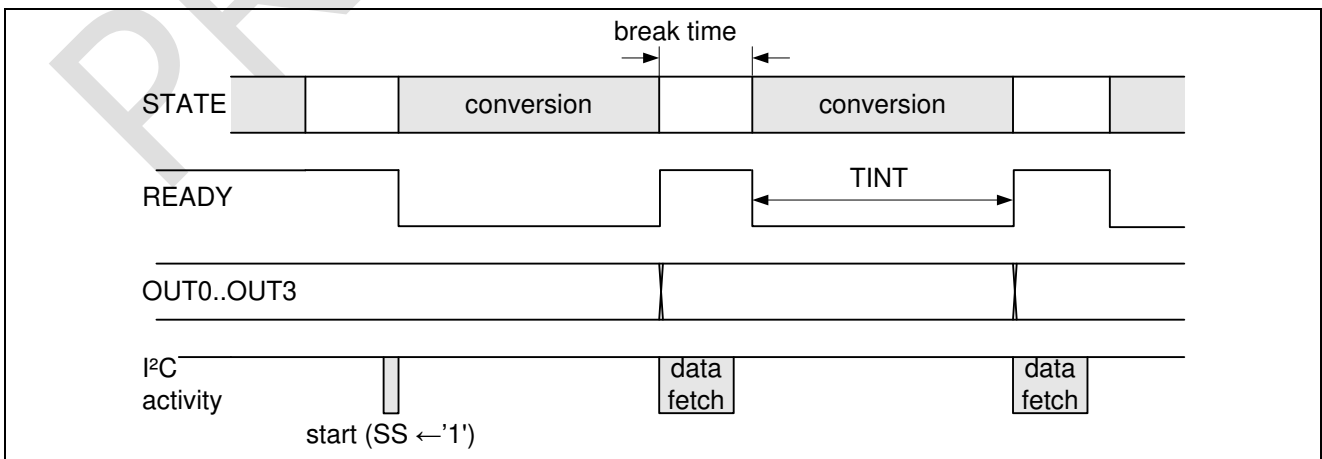


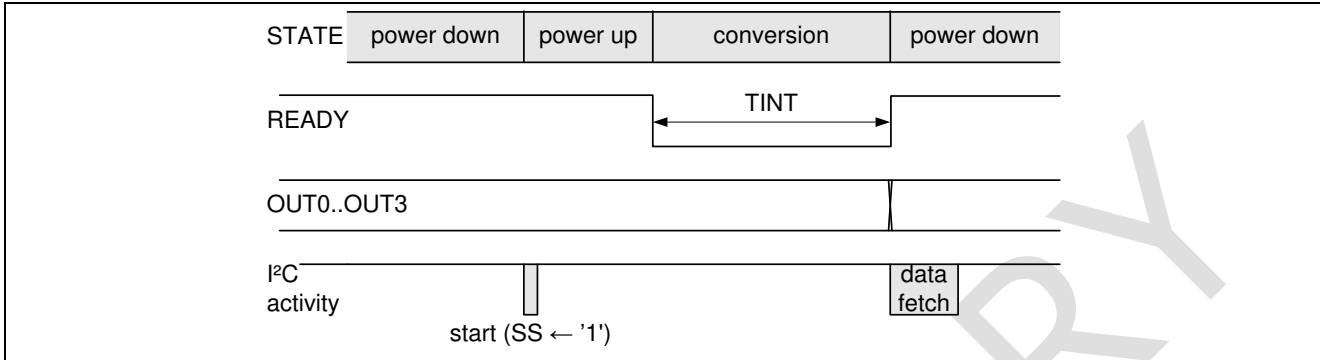
Figure 4: CONT Mode timing with long enough break time between subsequent conversions



5.1.2 Command Measurement Mode (CMD Mode)

This measurement enables a 'software start' of single conversion. Each conversion starts by setting the SS bit to '1' of OSR register. However, actually start of conversion depends on the chosen *Power down* activity. For further details see also Figure 21.

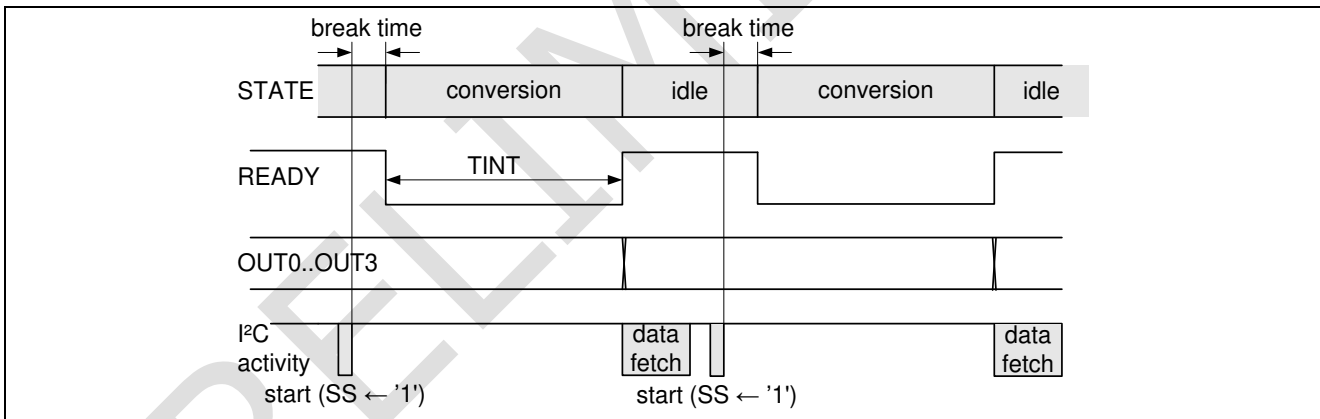
Figure 5: *CMD Mode* timing with activated *Power down*



If *Power down* has been activated (PD bit in OSR) the conversion starts after the Power-up, approximately 500 μ s after the SS bit has been set (Figure 5). Otherwise it starts immediately after delay time defined by the content of BREAK register which can be configured in 1 μ s steps up to 255 μ s (Figure 6).

The rising edge of READY signalizes the end of conversion and the output data can be read via the I²C-Interface (data fetch). After the conversion, the device returns to the *Power down* mode or stays active waiting (idle) for a new action according to the programmed configuration. The conversion time (integration time TINT) is determined by contents of the register CREGL:T (T).

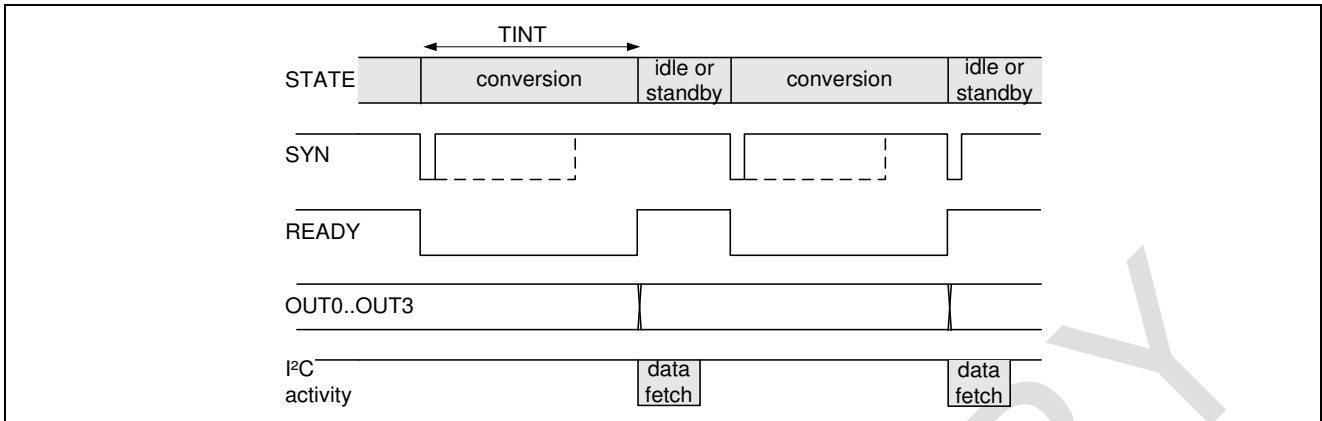
Figure 6: *CMD Mode* timing without *Power down*



5.1.3 Synchronous Measurement Start Mode (SYNS Mode)

The input pin SYN acts as a trigger event for the conversion start. The falling edge starts the measurement. The READY pin signalizes the progress of conversion, at rising edge the measurement is stopped and the current conversion results are stored into output registers. Data fetch should be performed between the rising edge of READY signal and the next falling edge of SYN in order to allow distortion free measurement. After the conversion the device changes its state to *Standby* or stays active waiting (idle), according to assignment of SB bit (CREGH register). The conversion time (integration time TINT) is determined by the contents of register CREGL:T (T). For further details see also Figure 22.

Figure 7: *SYNS Mode* timing¹¹



5.1.4 Synchronous Measurement Start and Stop Mode (*SYND Mode*)

The start and the stop of the measurement are completely controlled by the SYN signal. When the device is in the idle or *Standby* state the first coming falling edge starts the measurement. Each following falling edge of SYN, which occurs within the conversion, can stop or continue the measurement. The content of EDGES register determines which edge is the stopping one. This means that the measurement will not stop until a certain number of falling edges passed within the conversion time. This certain number of edges is represented by a value of register EDGES (see Figure 8 and Figure 9). For further details see also Figure 22.

Figure 8: *SYND Mode* timing, register EDGES = 1

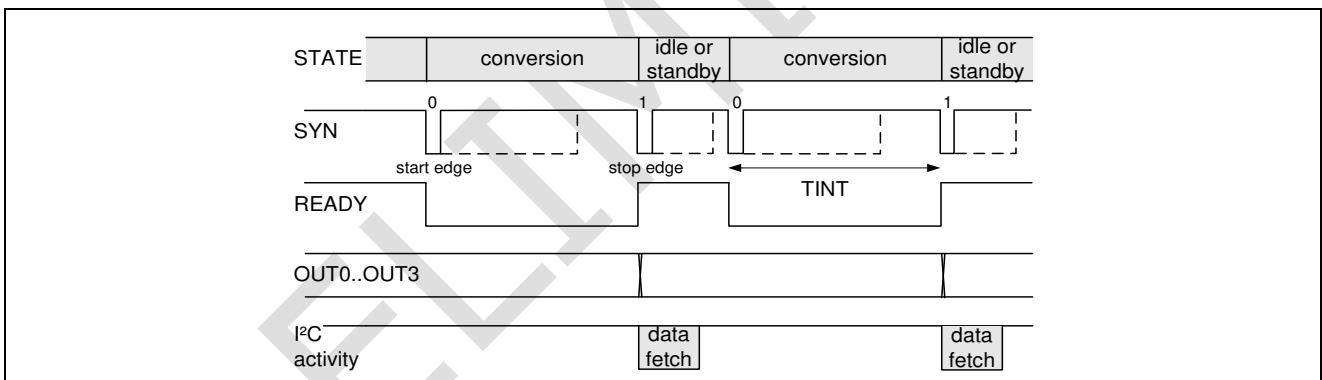
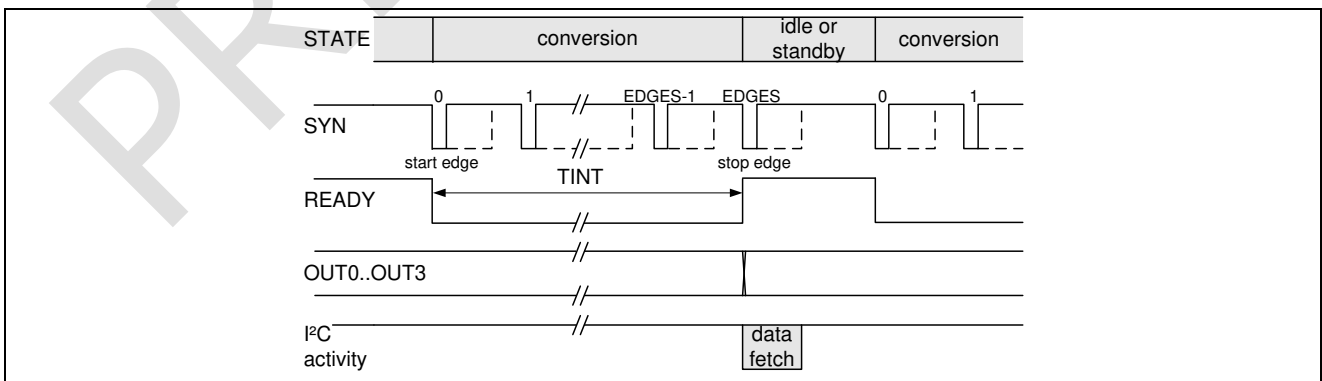
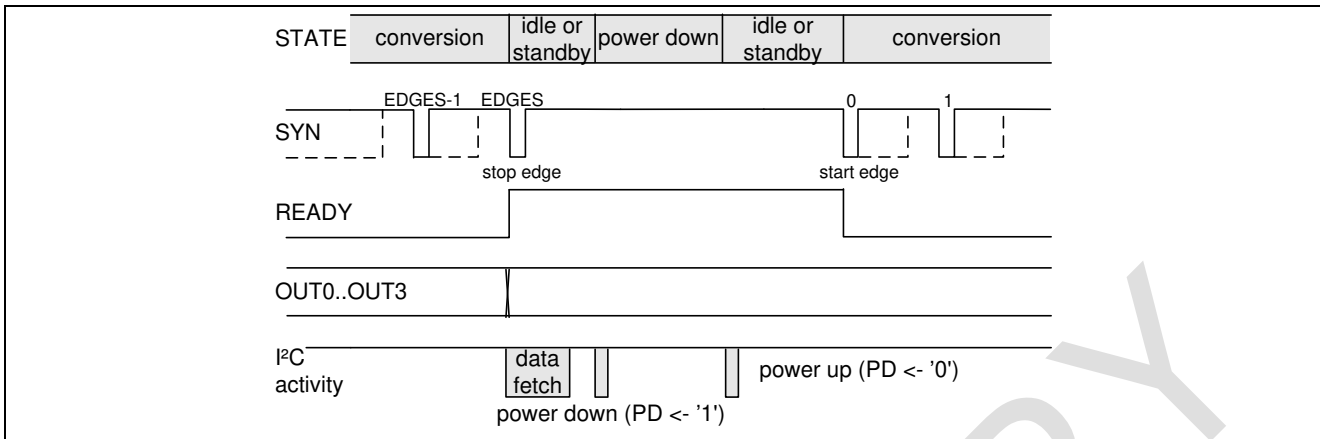


Figure 9: *SYND Mode* timing, register EDGES > 1



Data fetch should be performed between the rising edge of READY signal and the next falling edge of SYN in order to allow distortion free measurement.

¹¹ Dash lines indicate variable conditions

Figure 10: SYND Mode timing with Power down, EDGES > 1¹²

Between the subsequent conversions the device alters its state to *Standby* or *idle* according to assignment of SB bit (CREGH register). In this measurement mode it is also possible to switch the device into *Power down*. If the *Power down* is activated, the SYN signal would be ignored and no measurement will be performed.

The conversion time (integration time TINT) is determined by the duration between start and stop edge of the SYN signal. The distance between the falling edges determines the duration of the integration time TINT. It is possible to set the number of edges after which the integration time is terminated. In this way, the synchronization can be performed on different pulsed light sources. The minimum integration time TINT is 90µs, which corresponds to a resolution of at least 6Bit. The maximum integration time is 800ms.

In order to prevent measurement failures as a result of 'gain changing' (register CREGL:R), it is highly recommended to set the CMD mode or the Power down mode, before activating SYNS or SYND mode. In the case of using the Power down modus, a startup time of 500µs has to be respected to ensure that all parts of the AS89010 are fully functional again and the measurement does not start before awaking the AS89010 (CMD and CONT mode).

This waiting time can be prevented by inserting a "dummy" CMD mode before SYNS or SYND. Setting of Power down mode is not needed in this case.

5.2 Power Down

In *Power down* the clock generator and analog part of the device are turned off. The digital part stays idle, the full communication via the I²C interface is granted. Reading of measurement data and start of a measurement by setting the SS-Bit in *CMD Mode* is possible.

Power down is configured by the PD bit in OSR register (Table 8). By setting the OSR:PD bit to "1" the AS89010 immediately changes to *Power down*. By resetting the OSR:PD bit to "0" the AS89010 changes back to the measurement/idle or *Standby* depending on the settings of the CREGH register. This change to the operational state is delayed by the *Start up time* of about 500µs to ensure that all parts of the AS89010 are fully functional again. Only in the CMD measurement mode a single conversion can be started during *Power down* state by setting the OSR:SS bit to 1. In this case the *Start up time* of 500 µs between the I2C command and the start of the conversion becomes active too. After the conversion the AS89010 changes back into the *Power down* state.

5.3 Standby

In *Standby* only the A/D converters are powered down, thus the power consumption will be reduced. The *Standby* operation can be configured by the SB bit of CREGH register (Table 11).

¹² Dash lines indicate variable conditions

In the *CONT Mode* the *Standby* is automatically deactivated by starting the measurement with setting the OSR:SS bit to 1. If the OSR:SS bit is set to 0 the *Standby* becomes active again.

In the *SYNS* and *SYND* operation mode together with an activated *Standby* the start of the measurement automatically deactivates the *Standby* bit in the CREGH register. In the *CMD* operation mode the *Standby* cannot be activated.

5.4 A/D Conversion

In general the implemented A/D converter represents a delta-sigma converter, which performs and uses a charge balancing between the input I_{IN} and a reference current I_{REF} as result *OUT* of ADC. The input current integration takes place onto the integrator whose result is a pulse density modulated digital signal f_{CLK} , further filtered by up to 20 bit counter. At the end of integration the output *OUT* of this counter represents a digital equivalent of the average input current I_{IN} within the integration time interval *TINT*.

The transfer function of the A/D converter can be expressed as:

$$OUT = \frac{I_{IN}}{I_{REF}} N_{CLK}, \quad (1)$$

or:

$$OUT = \frac{I_{IN}}{I_{REF}} TINT \cdot f_{CLK}. \quad (2)$$

OUT : Digital output of conversion (corresponds to the content of output register)

I_{IN} : Average input current within a conversion time interval

I_{REF} : Reference current

TINT : Integration e.g. conversion time interval

N_{CLK} : Number of clock cycles within the conversion time interval

f_{CLK} : Clock frequency

In the *CONT*, *CMD* and *SYNS Mode* the integration time is internally generated¹³. Number of clock counts within this interval is a constant number, so that output remains independent of clock frequency. In this case an output can be represented by the equation (1).

In the *SYND Mode* integration time is externally generated, conversion result is represented by equation (2). If the conversion time measurement is activated (CREGH:ENTM = "1b", see chapter 5.5), the number of clock counts within the integration time can be also internally measured, so that conversion results may be calculated as:

$$OUT = \frac{I_{IN}}{I_{REF}} OUTINT. \quad (3)$$

OUTINT: Integration time duration expressed as the number of clock counts within this time. In this way the input current can be measured independently of internal frequency and furthermore external integration time variations in *SYND Mode*. The reference current and internal integration time are determined by the

¹³ The system clock is internally generated using an RC oscillator. It may have a little technological-inflicted tolerance, e.g. the exemplary period of time may vary slightly. This must be considered when calculating the time to be programmed (e.g. BREAK or integration time).

content of register CREGL: R and T bits (T). Their values determine directly the sensitivity e.g. LSB and full-scale range (FSR) current of A/D conversion. One overview of the possible configurations is shown in Table 5.

Table 5: Programmable FSR and LSB current (CONT, CMD, SYNS Mode)

T [b]	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
N _{CLK}	1024	2048	4096	8129	16384	32768	65536	131072	262144	524288	1048576
Resolution [bit]	10	11	12	13	14	15	16	17	18	19	20
R [b]	IFSR [nA]										
000	20							10	5	2.5	1.25
001	80							40	20	10	5
010	320							160	80	40	20
011	1280							640	320	160	80
1XX	5120							2560	1280	640	320
R [b]	LSB [pA]										
000	19.53	9.77	4.88	2.44	1.22	0.61	0.31	0.15	0.08	0.04	0.02
001	78.13	39.06	19.53	9.77	4.88	2.44	1.22	0.61	0.31	0.15	0.08
010	312.5	156.25	78.12	39.06	19.53	9.77	4.88	2.44	1.22	0.61	0.31
011	1250	625	312.5	156.25	78.13	39.06	19.53	9.77	4.88	2.44	1.22
1XX	5000	2500	1250	625	312.5	156.25	78.13	39.06	19.53	9.77	4.88

T: bit 3 to 0 of CREGL

R: bit 6 to 4 of CREGL

IFSR: full-scale range current

LSB: last significant bit

Resolution: internal A/D resolution

$$N_{CLK} = T_{INT} \cdot f_{CLK}$$

The maximum value of conversion result in the *SYND Mode* depends on the external integration time duration. This maximum achievable count is equal to *OUTINT* and differs from the full-scale count achievable in *CMD*, *CONT* and *SYNS Mode*. The value of T defines the number of clock counts during the integration time. It defines the integration e.g. conversion time duration and maximum of resolution of the A/D conversion. This is valid for the *CONT*, *CMD* and *SYNS Mode*.

In the *SYND Mode* the value of T has no meaning, integration time duration is externally defined. The values of T higher than 0110b internally lead to A/D conversion with a higher resolution up to 20 bit. But only the 16 most significant bits will be further processed and stored. As only the lower part of results is evaluated, the FSR is lower for internal resolution higher than 16 bit. The value of R defines the A/D converter reference current (see T). In combination with the values of T or the integration time duration it also defines the full-scale range current and thus the sensitivity of the A/D conversion.

During a conversion an overflow of input integrator of the A/D converter must be avoided. The maximum input current must not exceed the double value of reference current for the maximum of one clock duration, otherwise integrator overflow can occur and conversion result would be incorrect:

$$I_{IN}^{MAX} < 2 \cdot I_{REF} \quad (4)$$

I_{IN}^{MAX} : Peak Input Current

For more details and necessary steps to find the optimal parameters for amplifying please see our notices in the application note "AppNote specifying the optimal gain parameters for AS89010.pdf"¹⁴.

¹⁴ Please contact our sales team - see page 40

5.4.1 Offset of the A/D Converter

Ideally no or a very small amount of offset would be presented in the conversion output. However, an offset presented in input signal cannot be overcome. If an input leakage current occurs (at printed circuit board for example), it is possible that input current takes negative sign and makes conversion unable to operate for very low level currents. In such a case a well-known amount of an internal offset can be introduced in order to add the positive offset to the A/D transfer characteristic. Therefore, even low level negative currents can be measured precisely. This option should be set by configuring the ZERO values in OPT register (Table 12).

For this case the output of the A/D conversion can be expressed as:

$$OUT = \frac{I_{IN}}{I_{IREF}} N_{CLK} + OUT_{ZERO} \quad (5)$$

or for *SYND Mode*:

$$OUT = \frac{I_{IN}}{I_{IREF}} TINT \cdot f_{CLK} + \frac{TINT \cdot f_{CLK}}{2^{ZEROSYND}} = \frac{I_{IN}}{I_{IREF}} OUT_{TINT} + \frac{OUT_{TINT}}{2^{ZEROSYND}} \quad (6)$$

OUT_{ZERO} : Offset in *CONT*, *CMD* and *SYNS Mode*: 0, 15, 31 or 63 depends on the ZERO values of OPTREG

$ZEROSYND$: Offset factor in *SYND Mode*: $TINT \cdot f_{CLK} / 2^7$, $TINT \cdot f_{CLK} / 2^{11}$ or $TINT \cdot f_{CLK} / 2^{15}$ depending on the ZERO values of OPTREG

The offset generation is activated only for $ZERO \neq 00b$. Please note, the internally generated offset has to be subtracted from the result value by the user specific control program. It will not be performed internally or automatically.

5.4.2 Divider

For the purpose to further expand the measurement ranges an internal implemented digital divider can be used to scale the result. This may be necessary if the resolution of the conversion is set to a value of >16 bit. If the digital divider is used the conversion result is downscaled according to:

$$OUT_{DIV} = \frac{OUT}{DIV} \quad (7)$$

OUT_{DIV} : Digital output

DIV : Divider factor (2, 4, 8, 16), see Table 11

Therefore the divider acts as digital downscaling feature of the converter gain. It increases the effective dynamic range of device without changing its sensitivity or integration time.

5.5 Conversion Time Measurement

In case of SYND measurement mode the conversion time is fully controlled by the external signal at pin SYN. The relative deviation of this time to the internal clock frequency¹⁵ can produce some deviations in the conversion output. However, this time can be internally measured in time units of system clock (typically 1024 MHz) up to 20 bit word. It gives the opportunity to calculate more precisely measured input currents. That could increase the accuracy for the converter.

Even further, the measured result can be compensated for any deviation which can occur in the clock frequency due to temperature or supply voltage variations.

The time measurement can be enabled by setting the ENTM bit of register CREGH (Table 11). The result is stored into the output register OUTINT (Table 15) after a conversion has been made, synchronous with the storing of the A/D conversion data. The stored value follows the relation:

$$OUTINT = TINT \cdot f_{CLK} \quad (8)$$

The register OUTINT is only valid if this mode has been activated.

5.6 I²C Communication

The two wire serial interface is compatible to the fast mode I²C protocol and timing¹⁶. The SDA wire carries the data while the SCL wire synchronizes the transmitter and receiver. The device that initiates a data transfer is called a master and the responding device is called a slave. A device that sends data to the bus is called transmitter and a device receiving the data is called receiver.

The AS89010 can operate only as slave with unique slave address 11101'A1 A0' (7 address bit's plus read/write bit, see Figure 11), with the two lower bits defined by the input pins A1, A0. Each data transfer begins with a start (S) condition, defined by a high to low transition of SDA while SCL is high. The transfer terminates by a stop (P) condition, defined by a low to high transition of SDA while SCL is high. A repeated start condition (Sr) can be generated instead of a stop condition, if the transfer should be continued with the new data packet.

The start and repeated start condition are functionally equivalent. The data transfer consists of 8 bit long data. Each byte has to be followed by an acknowledge bit (A) (see Figure 11). The bits arrive with the MSB first. The acknowledge signal shall be pulled low by the receiver during the high period of the 9th clock pulse, while transmitter releases the SDA line. When SDA stays high during this clock pulse then this is defined as the not acknowledge signal (NA). After the not acknowledge signal, the master can either generate a stop or repeated start condition, depends on whether the master wants to abort or start a new transfer. The AS89010 generates a not acknowledge only in case when received data are not understood. The data transfer is implemented as shown in Figure 11.

A master generates the start condition and sends a 7 bit long slave address followed by the 8th bit which is a data direction bit (h). With the data direction bit set to '1' a master indicates a request for data read with a '0' a transmission is indicated. A data transfer terminates by a stop condition, but the master can also generate a repeated start condition instead of stop condition if the communication should be continued.

The sequences for a read and write data transfer are shown in Figure 12.

¹⁵ It depends on technology parameters in manufacturing. So variations and tolerances from one IC to another can occur.

¹⁶ The requirements for bus termination using standard Pull-Up's according I²C should be considered. It concerns especially noise environments and EMC in PCB design.

Figure 11: I²C bus data transfer

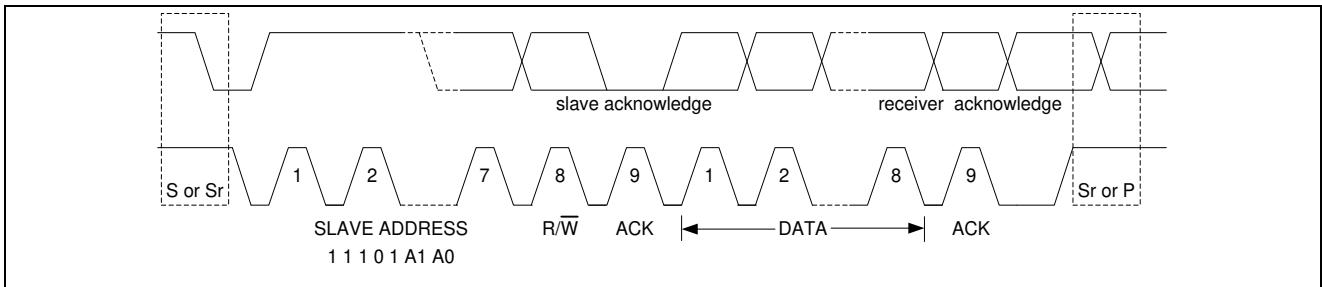
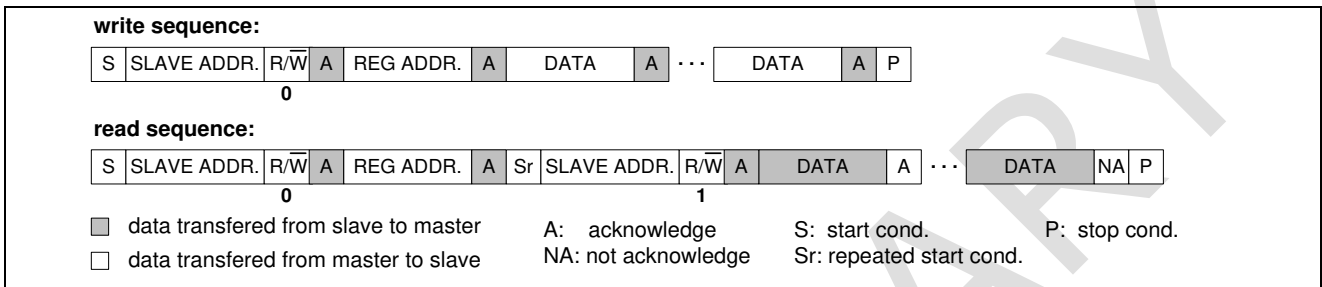


Figure 12: Write and read data sequences



5.6.1 Write Protocol

The start byte consists of the slave address, followed by R/\bar{W} set to set to '0' for the write direction. The first byte after the start byte is always the address pointer to the internal register which the master wants to write. The device acknowledges this byte (REG ADDR. in Figure 12). If the master generates a stop condition the transfer is aborted and a new write sequence must be started from the beginning. If master sends the next byte, this one will be stored in the internal register, addressed by the address pointer (REG ADDR.). The device sends acknowledge and internally increments the address pointer by 1. Then each next data byte transferred from the master will be stored sequentially in the internal register.

5.6.2 Read Protocol

The slave address is followed by R/\bar{W} set to '0' for the write direction. The first transferred byte after the start byte is always the address pointer to the internal register the master wants to read. The device acknowledges this byte (REG ADDR. see Figure 12). The master sends a repeated start condition and repeats the slave address but with the R/\bar{W} bit reversed. The slave acknowledges this byte and starts the data transfer to the master. The first transferred byte is the content of the internal register which is pointed by address pointer. Each transferred byte is acknowledged by the master. If not acknowledge occurs the master sends as next the stop condition and the transfer is finished. Internal address pointer increments carries out that the subsequent transferred data are sequentially read out from internal register.

5.6.3 I²C Addressable Register Space

Table 6 shows the overview of the internal register which can be accessed via I²C interface. The control register bank can be accessed in the configuration state and these registers are all 8 bit long.

The output registers can only be accessed for read in the measurement state. They are 16 bit long, except OUTINT which is 24 bit long. The device transfers the output data registers with the lowest byte first. The output registers data transfer can start at any address. If the transfer starts not at address (hex) 00h and during the sequential data read the highest possible address is arrived (ENTM=1: Address 04 with 3 byte; ENTM=0: Address 03 with 2 byte), the internal pointer resets back to the address 00h so that next data byte transferred corresponds to the low byte of OUT0. In this manner transfer continues with the first register (OUT0). However, the maximum of number of output data transferred must not exceed a total number of bytes accessible at all (8 bytes if integration time measurement is not activated otherwise 11 bytes). The OUTINT is only valid if CREGH:ENTM bit has been set.

Table 6: Register access overview

ADDRESS [hex]	ACCESS IN CONFIGURATION STATE		ACCESS IN MEASUREMENT STATE	
	Write	Read	Write	Read
00	OSR	-	OSR	OUT0
01	-	-	-	OUT1
02	-	AGEN	-	OUT2
03	-	-	-	OUT3
04	-	-	-	OUTINT
05	-	-	-	-
06	CREGL	-	-	-
07	CREGH	-	-	-
08	OPTREG	-	-	-
09	BREAK	-	-	-
0A	EDGES	-	-	-

5.6.4 Examples of using I²C-interface

An example of usual I²C communication set of sequences is shown in Figure 13. After a Power-up, the device is in a default configuration state. User can now set up the device for the application by writing control register. Success of the configuration can be proven by reading the control register.

Before a measurement can be started, the device must change its state into the measurement mode. In the last three bits of OSR '011b' should be loaded. Now a conversion can be started, it will start accordingly to the measurement mode selected by CREGH:MODE. When a conversion ends, rising edge of READY signalizes this (not in *SYND Mode*), the conversion data can be read.

If a new configuration should be implemented, the device has to change its state back to configuration mode, by loading '010b' into the last three bits of OSR. At this action all control registers will reset to their default values. New configuration can be made now.

6 DESCRIPTION OF REGISTERS

6.1 Control Register Bank

AS89010 configuration and operational state are controlled by the registers content defined in Table 7. The value size of all registers is 8 bit. Writing and reading of all registers is implemented in byte.

Table 7: Register addressing space

ADDRESS [hex]	ACCESS ¹⁷	NAME	DEFAULT [hex]	DESCRIPTION
00	wo	OSR	42 ¹⁸	operational state register
01	-	-	-	reserved
02	ro	AGEN	20	API generation
03	-	-	-	reserved
04	-	-	-	reserved
05	-	-	-	reserved
06	rw	CREGL	B6	configuration register
07	rw	CREGH	08	configuration register
08	rw	OPTREG	00	options register
09	rw	BREAK	20	break register
0A	rw	EDGES	01	edges register

6.2 Operational State Register – OSR

This write only register OSR¹⁹ controls the device operational state (DOS) of the AS89010 according to Table 8. This register can be written at any time, independently of the actual operational state. Please note, reading this register only results in 00 [hex] because the access is write only.

Table 8: OSR register - Address 00h

OPERATIONAL STATE REGISTER OSR	NAME	VALUE [b]	AFFECTED OPERATIONAL STATE
		0 ²⁰	stop measurement
		1	start measurement
		0	no <i>Power down</i> mode
		1 ²¹	activate <i>Power down</i> mode
bit 5 to 3	-	-	reserved
		000	reserved
		001	reserved

¹⁷ ro – Read-only, wo – Write-only, rw – Read-write

¹⁸ Reading register with access Write-only results in 00 [hex]

¹⁹ The OSR register of the AS89010 is Write-only. It's not possible to readout the content of this register, sadly. Any readout this register will always result the value 0.

²⁰ Default after power-on-reset and state change from measurement to configuration.

²¹ Default after power-on-reset.

OPERATIONAL STATE REGISTER OSR	NAME	VALUE [b]	AFFECTED OPERATIONAL STATE
	Operational State	010 ²⁰	operational state: configuration
		011	operational state: measurement
		1XX	reserved

DOS switches the operational state of the device between configuration and measurement. The configuration state enables the access to the register bank (Table 7). No measurement takes place.

The measurements can only be performed in the measurement state and any access to the control register bank (except OSR) is not permitted. The control register would be reset to their default values each time the operational state is switched back to the configuration state.

The start of the measurement is controlled by the value of the **SS** bit. These signals are evaluated only in the measurement state and only in the *CONT* and *CMD Mode* (refer to chapter 5.1).

The *Power down* mode is controlled by the **PD** value. The *Power down* takes effect in both operational states. If the PD is active in the measurement state, the *Power down* would be performed only during the breaks between two consequent conversions.

6.2.1 API Generation Register – AGEN

The value of this read only register indicates the generation of the Control Register Bank. The value of the register changes whenever any formal modification is introduced to the Control Register Bank. This case indicates that the Application Programming Interface (API) has been changed.

Table 9: AGEN register - Address 02h

AGEN	NAME	VALUE [b]	DESCRIPTION
bit 7 to 4	DEVID	0010	Device ID number; the value 0010b is reserved for MDCD devices
bit 3 to 0	MUT	0000	Mutation number of Control Register Bank

6.2.2 Configuration Register – CREGL and CREGH

The configuration register CREGL mainly serves to define full-scale-range, sensitivity and conversion time of the device.

Table 10: CREGL register - Address 06h

CREGL	NAME	VALUE [b]	AFFECTED CONFIGURATION	
		0	input current direction out of the IN0-IN4 pins (the cathodes of the photodiode connected to the input pins)	
		1 ²²	input current direction into the IN0-IN4 pin (the anodes of the photodiodes connected to the input pins)	
			ADC Reference Current IREF	ADC LSB Current (TINT=1024 ms)
		000	20 nA	20 fA
		001	80 nA	80 fA
		010	320 nA	320 fA

²² Default after power-on-reset and state change from measurement to configuration.

CREGL	NAME	VALUE [b]	AFFECTED CONFIGURATION	
		011 ²²	1.28 μ A	1.28 pA
		1XX	5.12 μ A	5.12 pA
			Integration Time (internal $f_{CLK}=1.024$ MHz)	
			TINT (ms)	number of clock counts
		0000	1	1024
		0001	2	2048
		0010	4	4096
		0011	8	8192
		0100	16	16384
		0101	32	32768
		0110 ²²	64	65536
		0111	128	131072
		1000	256	262144
		1001	512	524288
		1010	1024	1048576
		1011 to 1111	1	1024

TINT = integration time = measurement time = conversion time

It has to be set by the proper assignment of the DIR bit in which direction the input current flows. The bit R define device sensitivity, it internally sets the reference current of the A/D converters (see chapter 5.4 and Table 5 for more information).

The content of **T** controls the integration time duration and is a multiple of the internal clock periods. If start and stop of measurement are externally controlled by *SYND* signal (*SYND* Mode), T is ignored.

The register CREGH generally defines the measurement modes of the device.

Table 11: CREGH register - Address 07h

CREGH	NAME	VALUE [b]	AFFECTED CONFIGURATION
		0 ²³	access to time counts for internal integration times (register OUTINT) is disabled
		1	access to time counts for internal integration times (register OUTINT) is enabled
		0 ²³	<i>Standby</i> disable
		1	<i>Standby</i> enable
bit 5	VR	0 ²³	reserved (must be set to '0')
		00	continuous measurement mode (CONT)
		01 ²³	command measurement mode (CMD)
		10	synchronous measurement start (SYNS)

²³ Default after power-on-reset and state change from measurement to configuration.

CREGH	NAME	VALUE [b]	AFFECTED CONFIGURATION
		11	synchronous measurement start and stop (SYND)
		00 ²³	divide by 2
		01	divide by 4
		10	divide by 8
		11	divide by 16
		0 ²³	disable digital divider
		1	enable digital divider

The measurement mode is controlled by the value of **MODE**. This assignment gives the opportunity to accommodate the current measurement to the given application (see chapter 5.1 for more details). The internally implemented divider which acts as digital downscaling of the converter gain can be set by the bits **ENDIV** and **DIV**. The bit **SB** controls the *Standby* operation of the device. In *SYND Mode* the bit **ENTM** enables the access to **OUTINT** to get time counts for internal measurement of the integration time, which can be of special interest if this time has been externally controlled. The time is measured as the number of internal clock counts with a width of up to 20 bit. The result is stored in register **OUTINT** that can be accessed via I²C interface (refer to chapter 5.5 for more details).

6.2.3 Options Register - OPTREG

This register sets additional options of the device which can enhance performance according to the given application.

Table 12: OPTREG register - Address 08h

OPTREG	NAME	VALUE [b]	AFFECTED CONFIGURATION
bit 7 to 2	--	000000 ²⁴	must be used
			Offset Value (conversion output for zero input current)
		00 ²⁴	0dec (disable offset generation)
		01	15dec (in <i>SYND Mode</i> : $TINT \cdot f_{CLK} / 2^7$)
		10	31dec (in <i>SYND Mode</i> : $TINT \cdot f_{CLK} / 2^{11}$)
		11	63dec (in <i>SYND Mode</i> : $TINT \cdot f_{CLK} / 2^{15}$)

The **ZERO** enables an internal offset generation to the input current and conversion result, too. It makes the device able to measure very low e.g. zero input current even in presence of the negative leakage current, which would normally lead to an underflow.

6.2.4 Register - BREAK

Table 13: BREAK register - Address 09h

BREAK	NAME	VALUE [dec]	AFFECTED CONFIGURATION
bit 7 to 0	BREAK	1 - 255	break between measurements (only in <i>CONT</i> measurement mode) CONT: $BREAK / f_{CLK}$ typically; 5 μ s to 1021 μ s in steps (1 μ s + 4 μ s * break time) CMD: $BREAK / f_{CLK}$ typically; 1 μ s to 255 μ s in 1 μ s steps

This register takes effect only in *CONT* and *CMD* measurement mode. In the *CONT Mode* it defines the break between two consequent measurements²⁵. In the *CMD Mode* it defines the delay between a command for measurement start and the actually start of the measurement. This register gives a chance to the device to perform the measurement in the time when no disturbances occur during the I²C communication. Value of '0' cannot be written and will be ignored. The default value is 20h.

²⁴ Default after power-on-reset and state change from measurement to configuration.

²⁵ In case of an active I²C communication the AS89010 should not be active in converting. Therefore the break time between two measurements should be a minimum of >300 μ s. (25 μ s / Byte * (2 x 4 signal bytes+ 2 x control byte) * 1.25 clock tolerance).