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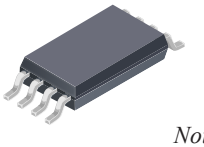
High-Precision, Highly Programmable Linear Hall-Effect Sensor IC with EEPROM, Output Protocols SENT and PWM, and Advanced Output Linearization

FEATURES AND BENEFITS

- Advanced 32-segment output linearization functionality enables high output accuracy and linearity in the presence of nonlinear input magnetic fields
- Selectable digital SENT (Single Edge Nibble Transmission) and PWM (Pulse-Width Modulation) output
- SENT output supports two modes: SAEJ2716 JAN2010 and Allegro Proprietary with Enhanced Programmable Features
- Customer-programmable magnetic range selection and offset, sensitivity, bandwidth, output clamps, 1st- and 2nd-order temperature compensation
- Simultaneous programming of all parameters for accurate and efficient system optimization
- Initial sensitivity temperature coefficient and magnetic offset drift preset at Allegro, for maximum device accuracy without requiring customer temperature testing
- Temperature-stable, mechanical stress immune, and extremely low noise device output via proprietary four-phase chopper stabilization and differential circuit design techniques
- Wide ambient temperature range: –40°C to 150°C
- Operates with 4.5 to 5.5 V supply voltage

PACKAGE: 8-PIN TSSOP (SUFFIX LE)



Not to scale

DESCRIPTION

The A1343 device is a high-precision, programmable Hall-effect linear sensor integrated circuit (IC) with an open-drain output, configurable as pulse-width modulated (PWM) or single edge nibble transmission (SENT), for both automotive and nonautomotive applications. The signal path of the A1343 provides flexibility through external programming that allows the generation of an accurate and customized output voltage from an input magnetic signal. The A1343 provides 12 bits of output resolution, and supports a maximum bandwidth of 3 kHz.

The BiCMOS, monolithic integrated circuit incorporates a Hall sensor element, precision temperature-compensating circuitry to reduce the intrinsic sensitivity and offset drift of the Hall element, a small-signal high-gain amplifier, proprietary dynamic offset cancellation circuits, and advanced output linearization circuitry.

With on-board EEPROM and advanced signal processing functions, the A1343 provides an unmatched level of customer reprogrammable options for characteristics such as gain and offset, bandwidth, output clamps, and magnetic range selection. In addition, the device supports separate hot and cold, 1st- and 2nd-order temperature compensation.

A key feature of the A1343 is its ability to produce a highly linear device output for nonlinear input magnetic fields. To achieve this, the device divides the output into 32 equal segments and applies a unique linearization coefficient factor to each segment. Linearization coefficients are stored in a lookup table in EEPROM.

The A1343 is available in a lead (Pb) free 8-pin TSSOP package (LE suffix), with 100% matte-tin leadframe plating.

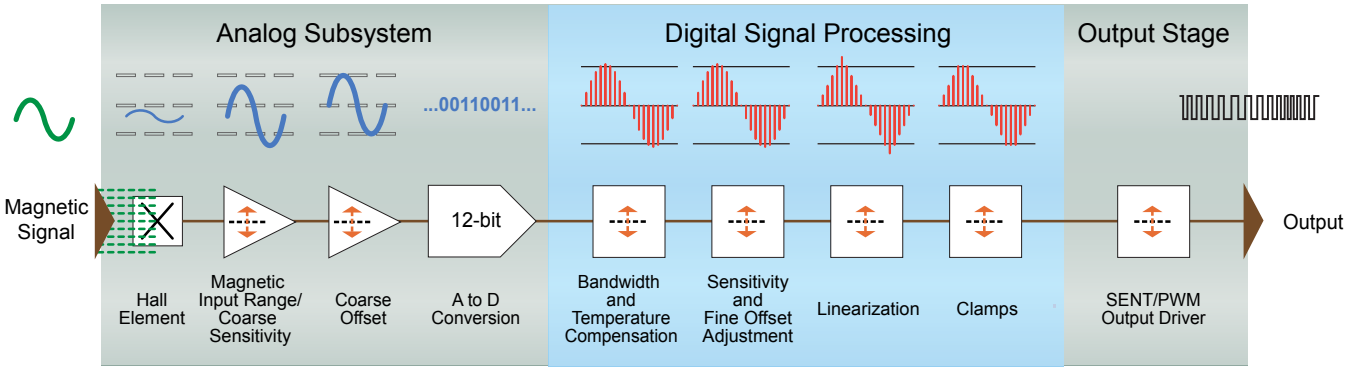


Figure 1: A1343 Signal Processing Path.
Functions with programmable parameters indicated by double-headed arrows.

Selection Guide

Part Number	Packing*
A1343LLETR-T	4000 pieces per 13-in. reel

*Contact Allegro™ for additional packing options.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		30	V
Reverse Supply Voltage	V_{RCC}		–20	V
Forward Supply Current	I_{CC}		30	mA
Reverse Supply Current	I_{RCC}		–30	mA
Forward Output Voltage (OUT Pin)	V_{OUT}		30	V
Reverse Output Voltage (OUT Pin)	V_{ROUT}		–0.5	V
Forward Output Sink Current (OUT Pin)	I_{SINK}	Current limited	60	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 165	ºC

Table of Contents

Allegro MicroSystems, LLC
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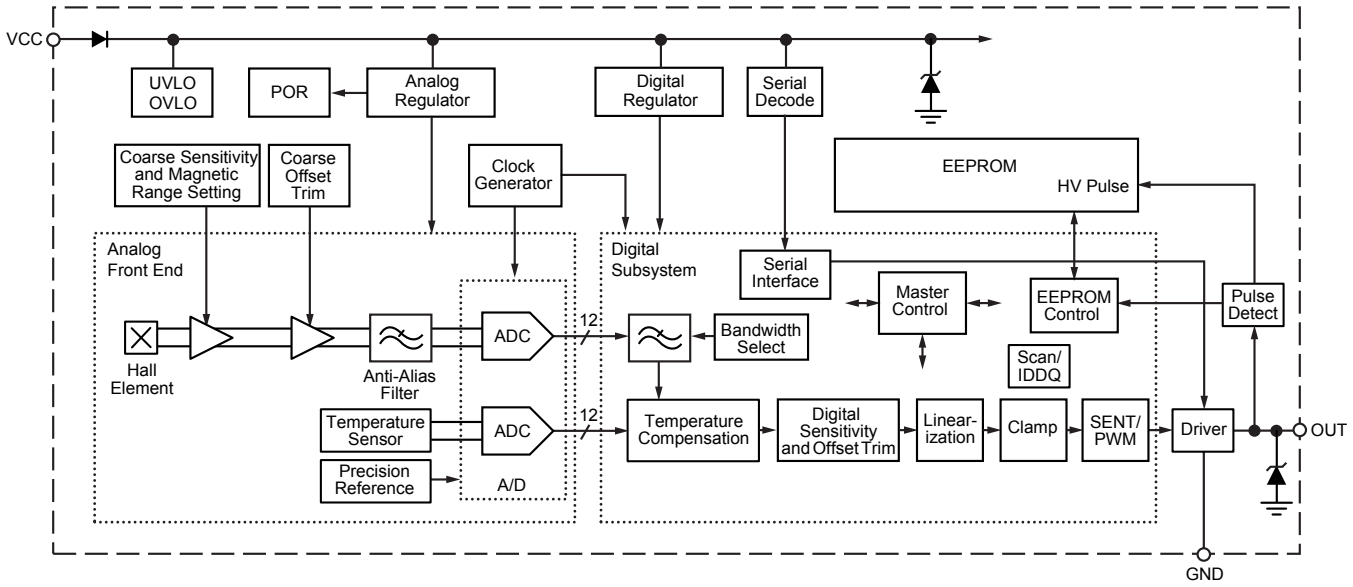
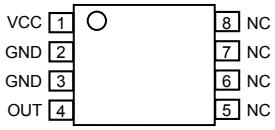
Functional Block Diagram



Pinout Diagram



Terminal List Table

Number	Name	Function
1	VCC	Input power supply
2	GND	Device ground
3	GND	Device ground
4	OUT	Output pin
5, 6, 7, 8	NC	Not connected; Recommend connecting pin to ground for application use.

ELECTRICAL CHARACTERISTICS: Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
GENERAL ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	LVD_DIS = 1	4.5	–	5.5	V
Supply Current	I_{CC}		5	–	10	mA
Reverse Supply Current	I_{RCC}	V_{RCC} = 20 V	–	–	–3	mA
Supply Zener Clamp Voltage	$V_{ZSUPPLY}$	I_{CC} = I_{CC}(max) + 3 mA, T_A = 25°C	30	–	–	V
Hall Chopping Frequency	f_C	T_A = 25°C	–	128	–	kHz
Low Voltage Detection Threshold	$V_{CC(LVD)LOW}$	LVD_DIS = 0	4.25	4.4	4.55	V
	$V_{CC(LVD)HIGH}$	LVD_DIS = 0	4.35	4.5	4.65	V
Power-On Reset	POR_{LOW}		3.5	3.7	4.1	V
	POR_{HIGH}		3.6	3.8	4.15	V
Overvoltage Lockout Threshold	$V_{CC(OV)LOW}$	OVLO_LO = 1, T_A = 25°C	5.6	–	7.6	V
		OVLO_LO = 0, T_A = 25°C	18	–	20	V
	$V_{CC(OV)HIGH}$	OVLO_LO = 1, T_A = 25°C	5.8	–	7.9	V
		OVLO_LO = 0, T_A = 25°C	18.3	–	20.3	V
SENT Message Duration	t_{SENT}	Tick time = 3 µs	–	1	–	ms
Output PWM Period[2]	V_{PERIOD}	PWM_MODE = 1	–15	–	15	%
Minimum Programmable SENT Message Duration	$t_{SENTMIN}$	Tick time = 0.25 µs, 3 data nibbles of information, nibble length = 27 ticks	–	41	–	µs
OUTPUT ELECTRICAL CHARACTERISTICS						
Output Leakage Current	$I_{OUT(LOW)}$	Output FET off	–	–	100	µA
Output Saturation Voltage[3]	V_{SAT}	I_{SINK} = 4.7 mA	–	0.3	0.45	V
Output Current Limit	I_{LIMIT}	Output FET on, T_A = 25°C	20	35	60	mA
Output Zener Clamp Voltage	V_{ZOUT}	T_A = 25°C	30	–	–	V
Output Load Capacitance[4,5]	C_{LOAD}	OUT to GND	–	–	10	nF
Power-On Time[4,6]	t_{PO}	BW parameter = 1	–	0.5	–	ms
		BW parameter = 0,2	–	0.8	–	ms
		BW parameter = 3	–	2	–	ms
		BW parameter = 4	–	3	–	ms
		BW parameter = 5	–	6	–	ms
Signal Path Propagation Delay[4,6]	t_{SDLY}	BW parameter = 1	–	0.35	–	ms
		BW parameter = 0,2	–	0.7	–	ms
		BW parameter = 3	–	1.4	–	ms
		BW parameter = 4	–	2.8	–	ms
		BW parameter = 5	–	5.6	–	ms

Continued on the next page…

ELECTRICAL CHARACTERISTICS (continued): Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
OUTPUT ELECTRICAL CHARACTERISTICS (continued)						
Full Scale Output Range[7]	FSO	PWM_MODE = 1 (PWM mode), CLAMP_HIGH = CLAMP_LOW = 0 (PWM duty cycle)	–	–	96	%D
		PWM_MODE = 0 (SENT mode)	–	–	4096	LSB

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] The PWM period is ±15% of the setting determined by the register FPWM address. See EEPROM Customer-Programmable Parameter Reference for more information.
[3] Output pin can be loaded with a 1.2 kΩ pull-up resistor without V_{SAT} rising above 0.5 V.
[4] Determined from design and lab characterization on a limited number of samples; not tested in production.
[5] Clarity of a Read Acknowledge message from the device to the controller will be affected by the amount of capacitance and wire inductance on the device output. In cases of complex loads with higher capacitance, it is recommended to slow down the communication speed, and to lower the receiver threshold for reading the digital Manchester signal.
[6] See Definitions of Terms section.
[7] SENT mode Full Scale Output Range is 12 bit, 0 to 4095.

MAGNETIC CHARACTERISTICS: Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1,2]
INITIAL DEVICE VALUES (Before Customer Programming), V_{CC} = 5 V, T_A = 25°C						
Initial Magnetic Input Signal Range	B_{INinit}	SENS_COARSE = 3	–	±250	–	G
Initial Magnetic Signal Offset	$B_{INOFFSET}$	SIG_COARSE = 3	–	0	–	%FSI
Initial Sensitivity	$Sens_{init}$	SENS_COARSE = 3, SENS_MULT = 0	–	8.19	–	LSB/G
Initial Quiescent Output	$QOUT_{init}$	B_{IN} = 0 G	–	50	–	%FSO
Initial Output Clamp	$OUT_{CLP(H)init}$	PWM_MODE = 0 (SENT mode), CLAMP_HIGH = 0	–	4095	–	LSB
	$OUT_{CLP(L)init}$	PWM_MODE = 0 (SENT mode), CLAMP_LOW = 0	–	0	–	LSB
Initial SENT Output Configuration	$SENT_{CFG(tick)init}$	PWM_MODE = 0, SENT_TICK = 2	0.4	0.5	0.6	µs
	$SENT_{CFG(fixed)init}$	PWM_MODE = 0, SENT_FIXED = 1	–	4	–	tick
	$SENT_{CFG(update)init}$	PWM_MODE = 0, SENT_UPDATE = 3	–	3	–	–
	$SENT_{CFG(data)init}$	PWM_MODE = 0, SENT_DATA = 3	–	3	–	nibble
Initial Sensitivity Drift Over Temperature[3,4]	$\Delta Sens_{init}$	T_A = –40°C to 25°C	–	<±0.03	–	%/°C
		T_A = 25°C to 150°C	–	<±0.02	–	%/°C
Initial Offset (QVO) Drift Over Temperature[4]	$\Delta OUT_{(Q)init}$	T_A = –40°C to 150°C	–	<±0.005	–	%/°C

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] *FSO* means Full Scale Output. See Definitions of Terms section.
[3] Does not include drift over lifetime and package hysteresis. Sensitivity can drift 3% typical worse case over the life of the product. Package hysteresis can result in Sensitivity drift of 2% typical worse case.
[4] Offset and Sensitivity drifts with temperature changes may vary with adjustment to the initial Magnetic Input Signal Range and Magnetic Offset. Contact Allegro for more information on application requirements with alternative SENS_COARSE and SIG_OFFSET settings.

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PROGRAMMABLE CHARACTERISTICS: Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
MAGNETIC INPUT SIGNAL RANGE						
Magnetic Input Signal Range Programming Bits		SENS_COARSE	–	4	–	bit
Magnetic Input Signal Range Programming Values	RANGE	T_A = 25°C, for programming values, see SENS_COARSE in EEPROM Structure section	±100	–	±2250	G
MAGNETIC OFFSET COMPENSATION						
Magnetic Offset Programming Bits		SIG_OFFSET	–	5	–	bit
Typical Magnetic Offset Programming Range[2]	SIG_OFFSET	T_A = 25°C	–100	–	+93.75	%FSI
Magnetic Offset Programming Step Size[2]	$Step_{SIG\_OFFSET}$	T_A = 25°C	5.62	6.25	6.875	%FSI
INTERNAL BANDWIDTH PROGRAMMING						
Bandwidth Programming Bits		BW	–	3	–	bit
Bandwidth Programming Range	BW	T_A = 25°C; for programming values, see BW in EEPROM Structure section	188	–	3000	Hz
Bandwidth Post-Programming Tolerance	ΔBW	T_A = 25°C, measured as a percentage of BW	–	±5	–	%
FINE QUIESCENT OUTPUT						
Fine Quiescent Output Programming Bits		QOUT_FINE	–	12	–	bit
Fine Quiescent Output Programming Range	QOUT_FINE	T_A = 25°C, B_{IN} = 0 G	–50	–	49.98	%FSO
Fine Quiescent Output Programming Step Size	$Step_{QOUT\_FINE}$	T_A = 25°C, B_{IN} = 0 G	–	0.0244	–	%FSO
OUTPUT SENSITIVITY						
Output Sensitivity	SENS_OUT	T_A = 25°C	0.025	–	0.5	%FSO/G
Sensitivity Multiplier Programming Bits		SENS_MULT	–	12	–	bit
Sensitivity Multipler Programming Range	SENS_MULT	T_A = 25°C	0	–	2	–
Sensitivity Multiplier Programming Step Size	$Step_{SENS\_MULT}$	T_A = 25°C	–	0.00049	–	–
LINEARIZATION						
Linearization Positions		T_A = 25°C	–	33	–	data sampling point
Linearization Position Coefficient Bits	LINPOS_COEFF	LIN_x, programmed with output fitting method	–	12	–	bit
Output Polarity Bit		OUTPUT_INVERT	–	1	–	bit
Input Polarity Bit		LIN_INPUT_INVERT	–	1	–	bit

Continued on the next page…

PROGRAMMABLE CHARACTERISTICS (continued): Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
TEMPERATURE COMPENSATION (TC) For back-biased devices, values cannot be tested in production						
1st-Order Sensitivity TC Programming Bits		TC1_SENS_CLD	–	8	–	bit
		TC1_SENS_HOT	–	8	–	bit
1st-Order Sensitivity TC Programming Range[3]	TC1_SENS_CLD TC1_SENS_HOT		–98	–	+291	m%/°C
1st-Order Sensitivity TC Programming Step Size[3]	$Step_{TC1SENS}$		–	1.53	–	m%/°C
2nd-Order Sensitivity TC Programming Bits		TC2_SENS_CLD, T_A = 150°C	–	9	–	bit
		TC2_SENS_HOT, T_A = 150°C	–	9	–	bit
2nd-Order Sensitivity TC Programming Range[3]	TC2_SENS_CLD TC2_SENS_HOT		–1.53	–	+1.53	m%/°C^2
2nd-Order Sensitivity TC Programming Step Size[3]	$Step_{TC2SENS}$		–	0.00596	–	m%/°C^2
1st-Order Magnetic Offset TC Programming Bits		TC1_OFFSET	–	8	–	bit
1st-Order Magnetic Offset TC Programming Range[4]	TC1_OFFSET	SENS_COARSE = 3	–0.488	–	+0.484	G/°C
1st-Order Magnetic Offset TC Step Size	$Step_{TC1\_OFFSET}$	SENS_COARSE = 3	–	0.0038	–	G/°C
OUTPUT CLAMPING RANGE						
Clamp Programming Bits		CLAMP_HIGH	–	6	–	bit
		CLAMP_LOW	–	6	–	bit
Output Clamp Programming Range	$OUT_{CLP(H)}$	T_A = 25°C, V_{CC} = 5 V	50.78	–	100	%FSO
	$OUT_{CLP(L)}$	T_A = 25°C, V_{CC} = 5 V	0	–	49.22	%FSO
Clamp Programming Step Size	$Step_{CLP(H)}$	T_A = 25°C	–	0.78	–	%FSO
	$Step_{CLP(L)}$	T_A = 25°C	–	0.78	–	%FSO

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PROGRAMMABLE CHARACTERISTICS (continued): Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Accuracy (After Customer Programming)						
Linearity Sensitivity Error	Lin_{ERR}		–	<±1	–	%
Symmetry Sensitivity Error	Sym_{ERR}		–	<±1	–	%
Sensitivity Drift Due to Package Hysteresis	$\Delta Sens_{PKG}$	Variation on final programmed Sensitivity value; measured at T_A = 25°C after temperature cycling	–	< ±2	–	%
Sensitivity Drift Over Lifetime	$\Delta Sens_{LIFE}$	T_A = 25°C, shift after AEC-Q100 grade 0 qualification in testing	–	±3	–	%
SENT Characteristics						
SENT Output Signal	$V_{SENT(L)}$	10 kΩ ≤ R_{pullup} ≤ 50 kΩ	–	–	0.05	V
	$V_{SENT(H)}$	Minimum R_{pullup} = 10 kΩ	0.9 × V_{CC}	–	–	V
		Maximum R_{pullup} = 50 kΩ	0.7 × V_{CC}	–	–	V
SENT Output Trigger Signal	$V_{SENTtrig(L)}$		–	–	1.2	V
	$V_{SENTtrig(H)}$		2.8	–	–	V

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] The unit %FSI = percentage of Full Scale Input. See Definitions of Terms section.
[3] The unit m% = 0.001%; for example, 25 m%/°C = 0.025 %/°C = 2.5 × 10^{-2} /°C.
[4] Parameter scales with SENS_COARSE. See programming information for more details.

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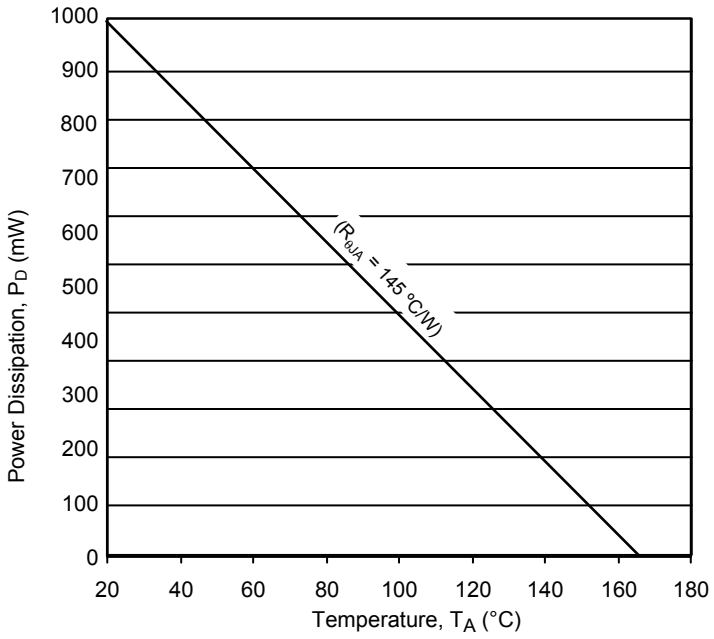
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	145	ºC/W

*Additional thermal information available on the Allegro website

Power Dissipation versus Ambient Temperature



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FUNCTIONAL DESCRIPTION

This section provides descriptions of the operating features and subsystems of the A1343. For more information on specific terms, refer to the Definitions of Terms section. Tables of EEPROM parameter values are provided in the EEPROM Structure section.

Signal Processing Parameter Setting

The A1343 has customer-programmable parameters that allow the user to optimize the signal processing performed by the A1343. Customer-programmable parameters apply to the analog front-end stages and the digital signal processing stages. Programmed settings are stored in on-board EEPROM. The programming communication protocol is described in the Programming Serial Interface section.

The initial analog processing can be customer-programmed to match the application environment in terms of magnetic field range and intensity. This allows optimization of the electrical signal presented to the digital signal processing (DSP) stage. The DSP stage provides customer-programmable sensitivity (gain) and offset adjusting, TC processing, and bandwidth, clamp, and linearization selection.

The output of the IC is a digital voltage signal, proportional to the applied magnetic signal. The format for the output signal is customer-selectable: either pulse-width modulation (PWM) or single edge nibble transmission (SENT) encoding scheme. The Full Scale Output range is proportional to the Full Scale Input range, but is optimized by customer-programmed parameters.

Analog Input Full Scale Range Determination

The Full Scale Input (FSI) range is the segment of the magnetic input signal that is used to generate the DSP input. This range is characterized by amplitude and centerpoint, which are adjustable using programming parameters for magnetic range and magnetic offset. Optimizing these two parameters allows the A1343 to best use the input range of the A-to-D converter and thereby maintain maximum input resolution (12 bits) for the DSP without clipping the magnetic input signal. The analog subsystem applies these two characteristics according to the following formula:

$$Y_{AD}\,(\%\text{FSO}) = SENS\_COARSE\,(\%\text{FSO/G}) \times B_{IN} + QOUT\_COARSE\,(\%\text{FSO}) \quad (1)$$

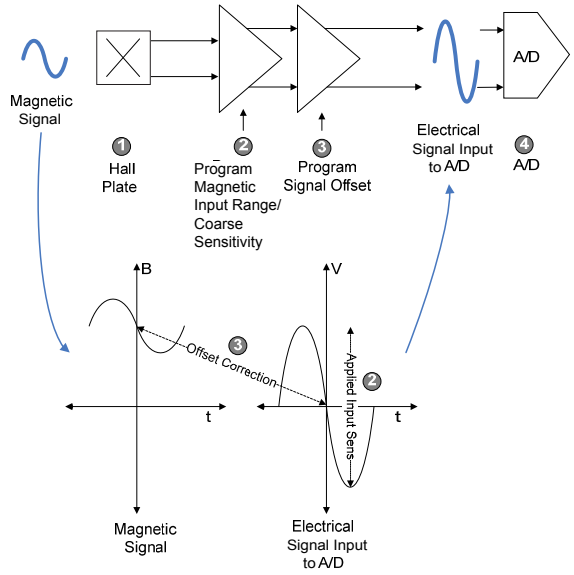

Figure 2: Signal Path for Analog Subsystem

where:

Y_{AD} is the output signal from the analog subsystem—this signal is input to the analog-to-digital converter (ADC);

SENS_COARSE is the coarse sensitivity (described below);

B_{IN} is the magnetic input signal; and

QOUT_COARSE is the coarse offset applied to the input signal—this value is determined by the initial offset, Q_{OUT}, and the parameter SIG_OFFSET.

Analog Input Range Setting

The Hall element signal voltage, V_{HALL}, is directly proportional to the applied magnetic flux density, B_{IN}. B_{IN} is essentially the impinging magnetic field that is perpendicular to the branded face of the device case. The Magnetic Input Signal, RANGE, is adjusted to best match B_{IN}, (point 2 in Figure 2). The RANGE should be sufficiently large to account for the maximum peak-to-peak value of B_{IN}. Also, it should be sufficiently small to maximize the signal input to the ADC. RANGE is customer-programmable to any of 16 values, from ±100 G (lowest) to ±2250 G (highest) by setting the SENS_COARSE parameter. The default RANGE setting is ±500 G, SENS_COARSE equal to 0. For more details on the SENS_COARSE programming codes, see the EEPROM Customer-Programmable Parameter Reference section.

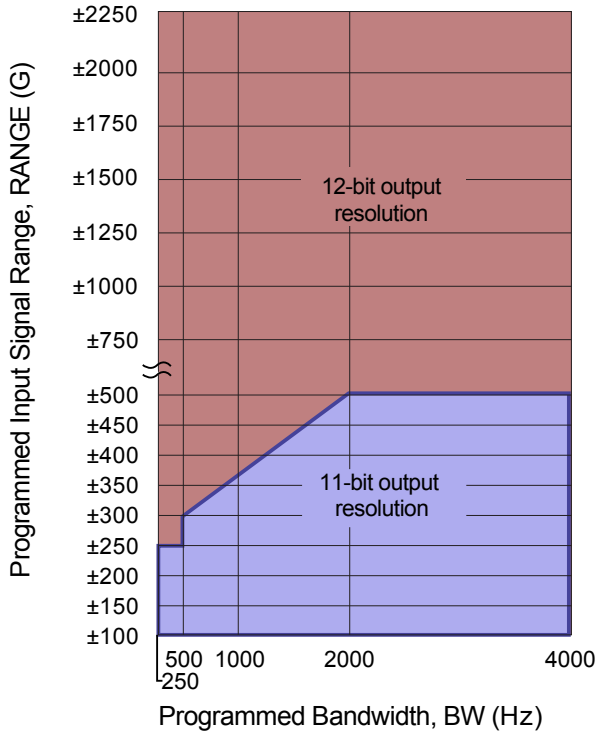

Figure 3: Output Resolution as a Function of Input Range and Bandwidth

The selected RANGE setting determines the coarse Sensitivity and impacts the output resolution. The relationship between the Magnetic Input Signal Range, Bandwidth, and maximum achievable output resolution is displayed in Figure 3.

Analog Magnetic Offset Selection

The magnetic offset parameter, SIG_OFFSET, adjusts the input signal to the center of the A-to-D range. The adjusted value is represented as QOUT_COARSE in equation 1.

The parameter SIG_OFFSET is used to adjust for typical magnetic influences in the application configuration itself (point 3 in Figure 2). It is programmed to any of 32 settings applied as percentages of FSI. These adjust the centerpoint between 100% of FSI more negative than 0 G (toward a more intense north polarity), to 93.75% of FSI more positive than 0 G (toward a more intense south polarity).

Digital Signal Processing

The adjusted input signal is converted to a digital signal for additional processing prior to the output stage. The DSP stage makes available many of the advanced programming features incorporated within the A1343. Some of the advanced programming features within the DSP include: fine Sensitivity adjustment, fine Offset adjustment, 1st- and 2nd-order Sensitivity Temperature Compensation, Offset temperature compensation, linearization, output clamps, and output configuration.

Bandwidth Selection

The 3-dB bandwidth, BW, determines the frequency at which the DSP function imports data from the analog front-end A-to-D converter. It is programmed by setting the BW parameter in EEPROM. The values chosen for BW and RANGE affect the DSP stage output resolution and the Signal Path Propagation Delay, t_{SDLY}. These tradeoffs are represented graphically in Figure 3, and in Table 1.

Table 1: Bandwidth-Related Tradeoffs

Bandwidth Selection [Internal Update Rate] (kHz)	DSP Output Resolution (bit)	Minimum RANGE for Full DSP Output Resolution (G)	Signal Path Propagation Delay, t_{SDLY} (ms)
0.500 [2.0]	11 to 12	±250	2.8
2.000 [8.0]	11 to 12	±500	0.7
4.000 [16.0]	10 to 11	±500	0.35

Temperature Compensation

The magnetic properties of materials can be affected by changes in temperature, even within the rated ambient operating temperature range, T_A. Any change in the magnetic circuit due to temperature variation causes a proportional change in the device output. The A1343 features integrated temperature compensation (TC) circuitry that can be programmed to compensate for many of these external magnetic variations. TC coefficients can be programmed for Sensitivity and magnetic offset. The effect of temperature is referred to as *drift*.

The A1343 uses the 1st-Order Magnetic Offset TC algorithm to compensate for output offset drift across the ambient temperature range (see Figure 5). The programmable parameter, TC1_OFFSET, is used to adjust the Magnetic Offset TC. It is programmable within the specified range and scales with the SENS_COARSE parameter. The step size of TC1_OFFSET decreases with decreased RANGE and increases with increased RANGE. For an example of 1st-Order Magnetic Offset compensation, refer to the EEPROM Customer-Programmable Parameter Reference section.

In addition to the offset TC compensation, the A1343 also provides a means to compensate for variation of the applied magnetic flux density with temperature. This is accomplished by utilizing 1st- and 2nd-order segmented algorithms to dynamically adjust the sensitivity of the sensor IC. There are two segments that can be programmed: temperatures above 25°C, Hot, and temperatures below 25°C, Cold. See Table 2 and Figure 6 for illustrations of the Sensitivity TC compensation.

The algorithm is flexible in a way such that 1st- and 2nd-order coefficients are applied independently from one another, from hot to cold. This method allows the end user to select either, both, or neither of the coefficients. The 1st-order coefficients are adjusted using the programmable parameters, TC1_SENS_HOT and TC1_SENS_CLD. The 2nd-order coefficients are adjusted using the programmable parameters, TC2_SENS_HOT and TC2_SENS_CLD. The coefficients are applied according to equation 2.

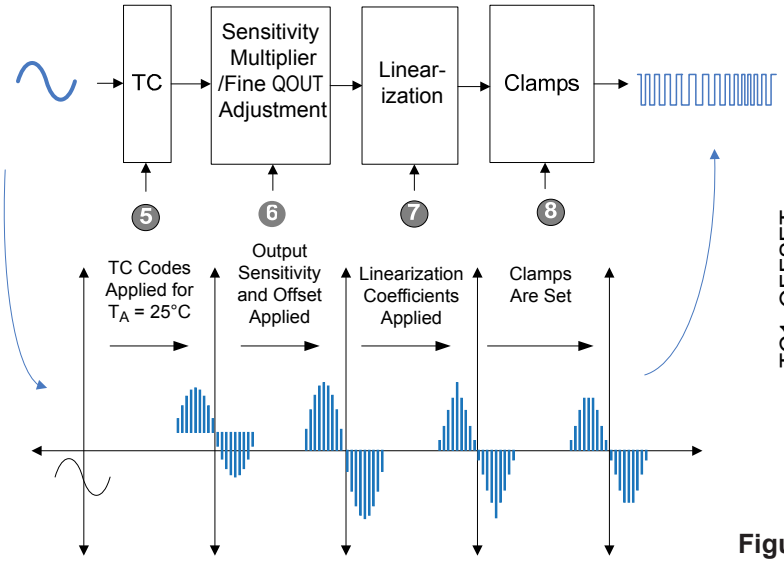

Figure 4: Signal Path for Digital Subsystem

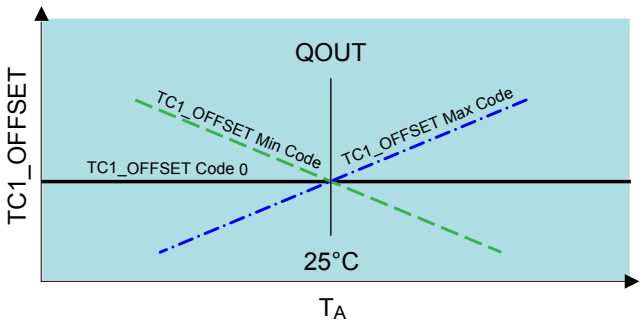

Figure 5: The 1st-Order Magnetic Offset Temperature Compensation coefficient, TC1_OFFSET, is used for linear adjustment of device output for temperature changes.

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The programmed values set the temperature compensation, Y_{TC}, according to the following formula:

$$Y_{TC}\,(\%FSO) = Y_{AD}\,(\%FSO) + [\,(TC1\_SENS\,(m\%/°C) \times \Delta T_A\,(°C)) + (TC2\_SENS\,(m\%/°C^2) \times \Delta T_A^2\,(°C))\,] \times Y_{AD}\,(\%FSO) + TC1\_OFFSET\,(G/°C) \times \Delta T_A\,(°C) \quad (2)$$

where:

Y_{AD} is the input from the analog subsystem via the A-to-D converter;

TC1_SENS is the first-order coefficient—either TC1_SENS_HOT or TC1_SENS_CLD depending on T_A;

TC2_SENS is the second-order coefficient—either TC2_SENS_HOT or TC2_SENS_CLD depending on T_A;

ΔT_A is the change in ambient temperature from 25°C (for example: at 150°C, ΔT_A = 150°C – 25°C = 125°C, or at –40°C, ΔT_A = –40°C – 25°C = –65°C);

SIG_OFFSET is the addition to the magnetic offset parameter (sets the centerpoint of Y_{AD}).

Table 2: Sensitivity Temperature Compensation Options

	T_A Range	
	< 25°C	**> 25°C**
1st Order	TC1_SENS_CLD	TC1_SENS_HOT
2nd Order	TC2_SENS_CLD	TC2_SENS_HOT

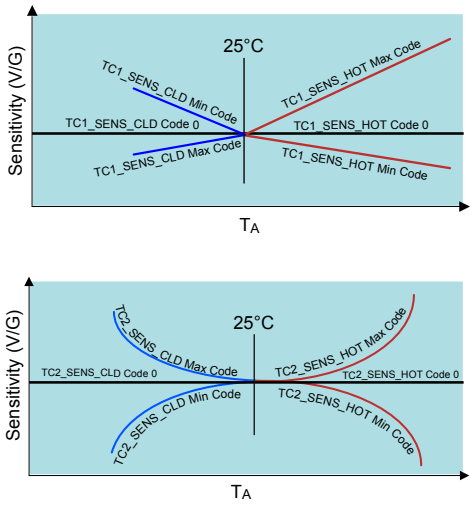

Figure 6: Sensitivity TC Functions — (upper) First Order, (lower) Second Order

Final Sensitivity (Gain) Adjustment

The A1343 has two programmable parameters to adjust Sensitivity, SENS_COARSE and SENS_MULT. The coarse Sensitivity value is determined by SENS_COARSE. For example, SENS_COARSE = 0 is approximately ±500G over 100% of the FSO range. This equates to an approximate Sensitivity of 0.1% FSO/G. Figure 7 shows approximate Sensitivity versus SENS_COARSE setting. The programmable parameter SENS_MULT, 6 in Figure 4, is used as a fine adjustment for Sensitivity. The value of this 12-bit parameter, applied in the digital subsystem, is multiplied to the coarse Sensitivity value (see equation 4). For example, SENS_MULT = 0 has a multiplier value of 1, SENS_MULT = 2047 has multiplier value of 2, and SENS_MULT = 2048 has a multiplier value of approximately 0. Please refer to the EEPROM Customer-Programmable Parameter Reference section for more information on parameter SENS_MULT.

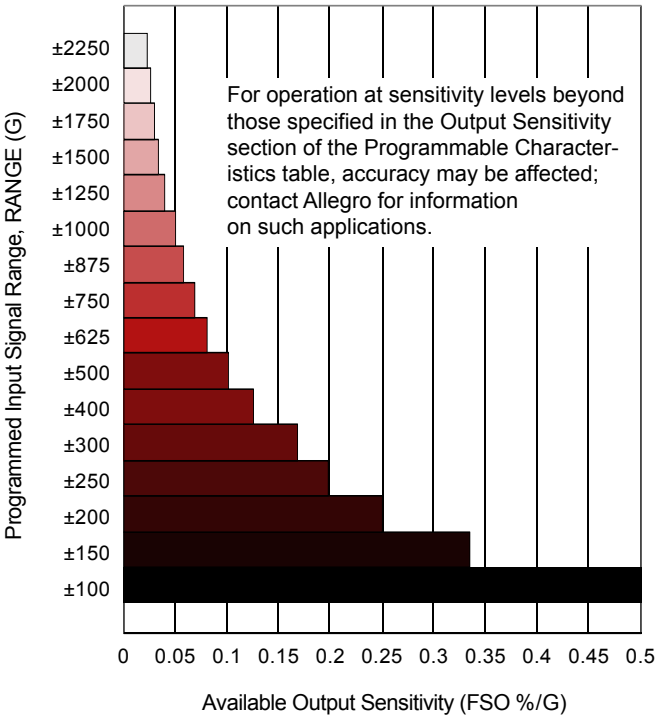

Figure 7: Correspondence of Magnetic Input Ranges and Resulting Available Output Sensitivity Levels

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Output Fine Offset Adjustment

The A1343 DSP subsystem also includes a parameter to adjust the Quiescent Output, or offset. This programmable parameter QOUT_FINE, 6 in Figure 4, is used as a fine adjustment to the Quiescent Output. The value of QOUT_FINE is a percentage of the FSO. It is programmable to add or subtract as much as 50% of FSO. Refer to the EEPROM Customer-Programmable Parameter Reference section for more information on parameter QOUT_FINE.

The output of the digital subsystem, Y_{DA}, after applying the parameters for fine adjustment of Sensitivity and offset is shown in equation 3. This value is prior to the linearization and clamps.

$$Y_{DA}\,(\%\text{FSO}) = SENS\_MULT \times Y_{TC}\,(\%\text{FSO}) + QOUT\_FINE\,(\%\text{FSO}) \quad (3)$$

$$SENS\_OUT\,(\%\text{FSO/G}) = SENS\_MULT \times SENS\_COARSE\,(\%\text{FSO/G}) \quad (4)$$

where SENS_MULT is the multiplication factor from 0 to 2.

Linearization of Output

The A1343 programmable linear Hall-effect sensor IC provides an output that is proportional to a magnetic input, within a specified range. In some applications, the magnetic input signal is often nonideal and nonlinear. However, it is optimal for the sensor to best approximate the ideal linear output. The A1343 provides a programmable linearization feature for this purpose. Applied in the digital subsystem (7 in Figure 4) the A1343 linearization algorithm uses 33 programmable coefficients, 32 segments, to manipulate the output function.

The coefficients are stored in EEPROM as 12-bit two's complement integers, where B_{IN}(min) is indicated by –2048 and B_{IN}(max) is indicated by 2047. Figure 8 shows an example input-output curve. The *y*-axis represents the 32 equal full-scale position segments, and the *x*-axis represents the the application input range.

Contact Allegro for more information on using the Linearization feature and available tools for calculating linearization coefficients.

The polarity of the output function can be inverted by reversing the mapping of either the input or the output of the algorithm.

Setting the LIN_INPUT_INVERT parameter to 1 inverts the polarity of the calculated linearization coefficients by inverting the input values.

Output Polarity Setting

The OUTPUT_INVERT parameter sets the device output signal polarity with respect to the applied magnetic field polarity. The default (0) is increasing in a south magnetic field and decreasing in a north magnetic field. Setting this parameter to 1 causes output voltage decrease in a south field and increase in a north field.

Output Clamps Setting

The A1343 digital subsystem contains programmable clamp features to adjust the normal operating output range; see 8 in Figure 4. The A1343 output clamps are initially set to 0% and 100% of FSO, for low and high output clamp respectively. The parameters, CLAMP_HIGH and CLAMP_LOW are available to adjust limits for the normal operating output. The A1343 Diagnostic outputs levels are not bound by these parameters.

Output Protocol Selection

The A1343 supports an output in either PWM or SENT format. The PWM_MODE parameter in EEPROM sets the format. (Output format programming is described in the Linear Output Protocols section.)

Protection Features

Lockout and clamping features protect the A1343 internal circuitry and prevent spurious output when supply voltage is out of specification.

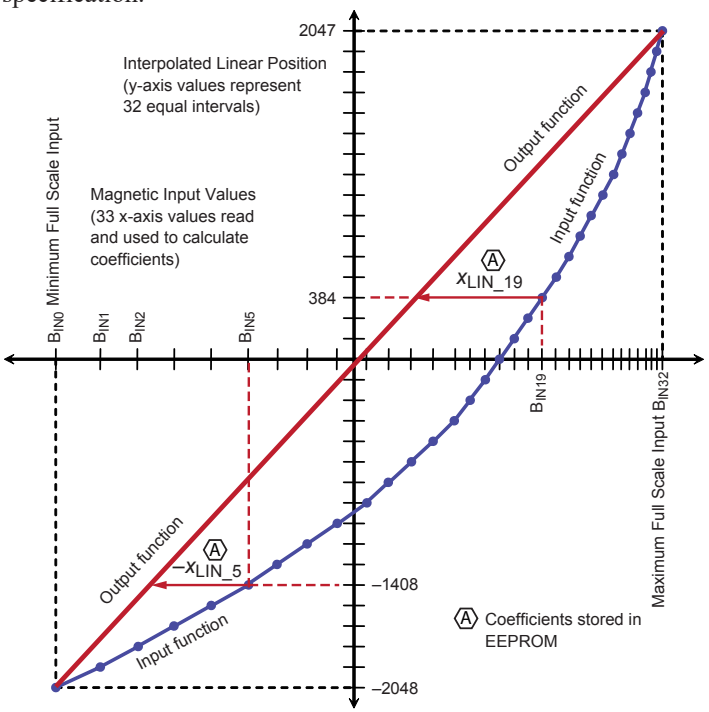

Figure 8: Sample of Linearization Function Transfer Characteristic

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Preprogrammed Default Values

Default values prevent system failures due to communication errors during real-time customer reprogramming of EEPROM. The default values also can be used as defaults for normal operation, reducing the initial customer programming requirements.

Operating Overvoltage and Undervoltage Lockout

Supply voltage detection features protect the A1343 internal circuitry and prevent spurious output when V_{CC} is out of specification. Diagnostic circuitry reuses the output pin (OUT) to provide feedback to the external controller. The A1343 provides protection for both overvoltage and undervoltage on the supply line.

The A1343 has two active circuits to identify when the supply voltage is below the minimum operating level. The internal power-on reset circuitry, POR, controls when an internal reset is triggered. If the supply voltage drops below POR_{LOW}, an internal reset occurs and the output is forced to a high-impedance state. When the supply voltage rises above POR_{HIGH}

The Low Voltage Detection feature, LVD, provides feedback to the external controller when V_{CC} is below minimum operating level but above the POR threshold. This feature is enabled by default and is disabled by setting LVD_DIS to logic 1. When configured for SENT output, if the supply voltage drops below $V_{CC(LVD)LOW}$, a status bit is set in the SENT message to indicate a low supply voltage condition. When configured for PWM output, if the supply voltage drops below $V_{CC(LVD)LOW}$, the output is forced to V_{SAT}. As the supply voltage rises above $V_{CC(LVD)HIGH}$, the output returns to normal operating state.

The Overvoltage Lockout Threshold, $V_{CC(OV)}$, is customer-programmable to one of two specified values, by setting the OVLO_LO parameter. When OVLO_LO = 1, programming pulses can cause the part to enter into and exit out of overvoltage lockout mode, resulting in an invalid output. If overvoltage conditions are reached, the PWM output will be brought to V_{SAT} or the SENT_STATUS bits will be set to indicate the condition.

Open Circuit Detection

Diagnostic circuitry reuses the output pin (OUT) to provide feedback to the external controller. A sense resistor, R_{OCD}, can be placed between OUT and a separate V_{BAT} reference, as shown in Table 3.

Memory Locking Mechanisms

The A1343 is equipped with two distinct memory locking mechanisms:

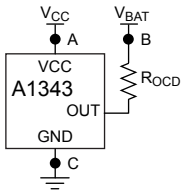
• **Default Lock.** At power-up, all registers of the A1343 are locked by default. EEPROM and volatile memory cannot be read or written. To disable Default Lock, a specific 30-bit customer access code is written to address 0x24 in less than 70 ms from power-up; see Write Access code. After this, device registers are accessible through the programming interface.

If VCC is power-cycled, the Default Lock automatically re-enables. This ensures that during normal operation, memory content will not be altered due to unwanted glitches on VCC or the output pin.

• **Lock Bit.** This is used after EEPROM parameters are programmed by the customer.

The customer programmable EELOCK feature disables the ability to read or write any register. This feature takes effect after writing the EELOCK bit and resetting power to the device. This prevents the ability to disable Default Lock using the method described above. Note that after EELOCK bit is set and VCC pin power-cycled, the customer will not have the ability to clear the EELOCK bit or to read/write any register.

Table 3: Open Circuit Diagnostic Truth Table

	Node A	Node B	Node C	OUT State
V_{BAT} Referenced				
	Open	Closed	Closed	0 V to V_{BAT}
	Closed	Open	Closed	GND
	Open	Open	Closed	GND
	Open	Closed	Open	V_{BAT}
	Closed	Open	Open	V_{CC}
	Closed	Closed	Open	V_{CC} to V_{BAT}

Typical Application

Multiple A1343 linear devices can be connected to the external controller as shown in Figure 9. However, EEPROM programming in the A1343 occurs when the external control unit excites the A1343 OUT pin by EEPROM pulses generated by the ECU. Whichever A1343s that are excited by EEPROM pulses on their OUT pin will accept commands from the controller.

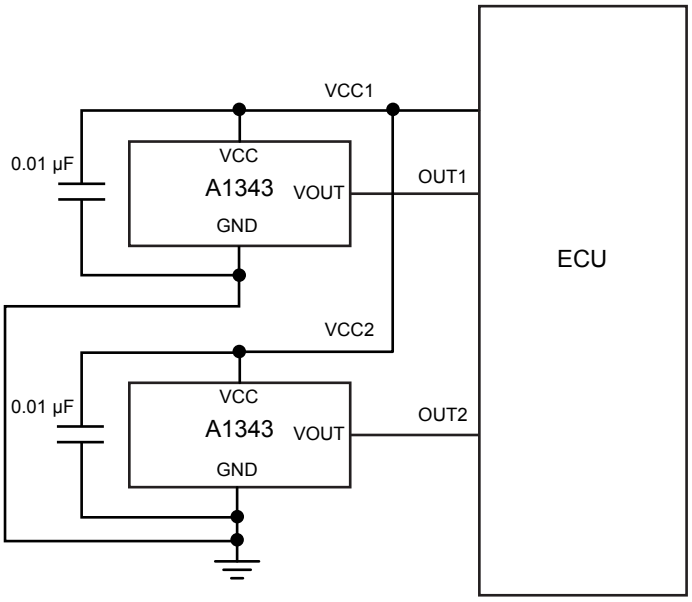


Figure 9: Typical Application

PROGRAMMING SERIAL INTERFACE

The A1343 incorporates a serial interface that allows an external controller to read and write registers in the A1343 EEPROM and volatile memory. The A1343 uses a point-to-point communication protocol, based on Manchester encoding per G. E. Thomas (a rising edge indicates 0 and a falling edge indicates 1), with address and data transmitted MSB first.

Transaction Types

Each transaction is initiated by a command from the controller. The A1343 does not initiate any transactions. Two commands are recognized by the A1343: Write and Read. There also is a special function Write command: Write Access Code. One response frame type is generated by the A1343, Read Acknowledge.

If the command is Read, the A1343 responds by transmitting the requested data in a Read Acknowledge frame. If the command is any other type, the A1343 does not acknowledge.

As shown in Figure 10, the A1343 receives all commands via the VCC pin. It responds to Read commands via the OUT pin. This implementation of Manchester encoding requires the communication pulses be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages for the VCC line and the OUT line. The Write command pulses to EEPROM are supported by two high-voltage pulses on the OUT line.

Writing the Access Code

If the external controller will write to or read from the A1343 memory during the current session, it must establish serial communication with the A1343 by sending a Write command including the Access Code within 70 ms after powering up the A1343. If this deadline is missed, all write and read access is disabled until the next power-up.

Writing to EEPROM

When a Write command requires writing to EEPROM (all standard Writes), after the Write command the controller must also send two *Programming pulses*, well-separated, long high-voltage strobes via the OUT pin. These strobes are detected internally, allowing the A1343 to boost the voltage on the EEPROM gates.

The required sequence is shown in Figure 11.

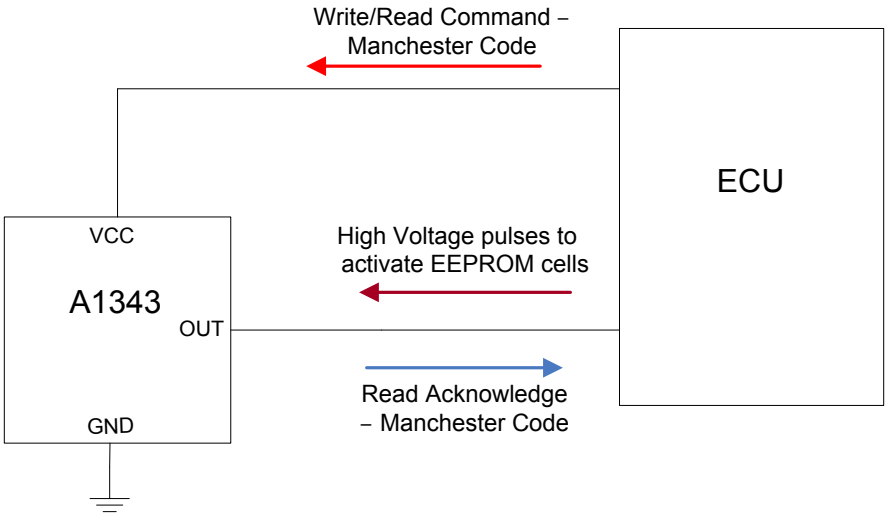


Figure 10: Top-Level Programming Interface

Reading from EEPROM

A Read command with the register number is sent from the controller to the A1343. The device responds with a Read Acknowledge frame. Output is automatically disabled after the Read command from the controller is received and output is enabled after a Read Acknowledge command is sent.

Error Checking

The serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check).

The CRC algorithm is based on the polynomial

$$g(x) = x^3 + x + 1 \ ,$$

and the calculation is represented graphically in Figure 12.

The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111.

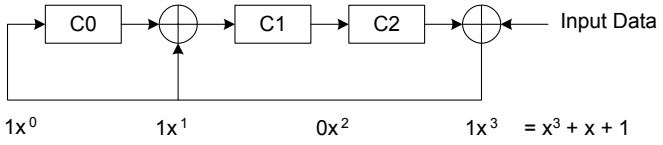


Figure 12: CRC Calculation

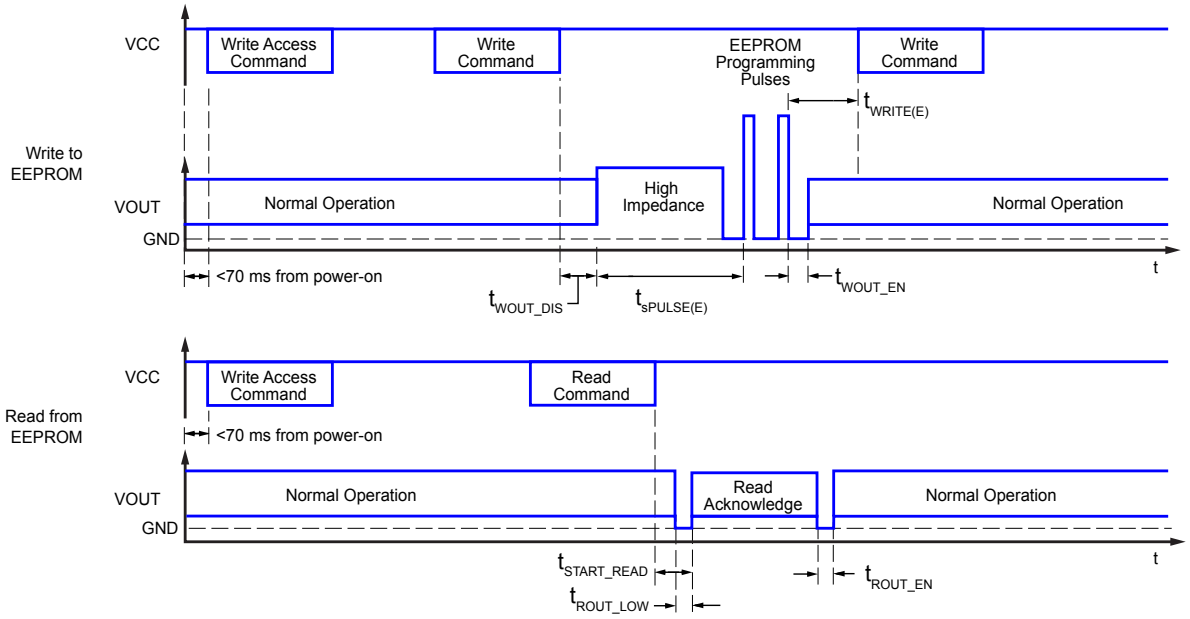


Figure 11: Programming Read and Write Timing Diagrams (see Serial Interface Reference section for definitions)

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SERIAL INTERFACE REFERENCE

Table 4: Serial Interface Protocol Characteristics [1]

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
INPUT/OUTPUT SIGNAL TIMING						
Access Code Timeout	t_{acc}	Customer Access Code should be fully entered in less than t_{ACC}, measured from when V_{CC} crosses $V_{CC(UV\_high)}$.	–	–	70	ms
Bit Rate		Defined by the input message bit rate sent from the external controller	4	–	100	kbps
Bit Time	t_{BIT}	Data bit pulse width at 4 kbps	243	250	257	µs
		Data bit pulse width at 100 kbps	9.5	10	10.5	µs
Bit Time Error	err_{TBIT}	Deviation in t_{BIT} during one command frame	–11	–	+11	%
Write Output Disable Delay	t_{WOUT_DIS}	Required delay from the trailing edge of certain Write command frames to output entering the high-impedance state	–	7 µs – 0.25 × t_{BIT}	60	µs
Write Delay	$t_{WRITE(E)}$	Required delay from the trailing edge of the second EEPROM Programming pulse to the leading edge of a following command frame	2 × t_{BIT}	–	–	µs
Write Output Enable Delay	t_{WOUT_EN}	Delay from the trailing edge of the final EEPROM programming pulse to output entering the normal operation state	–	6	60	µs
Read Acknowledge Delay	t_{READ}	Required delay from the trailing edge of a Read Acknowledge frame to the leading edge of a following command frame	2 × t_{BIT}	–	–	µs
Read Output Disable Delay	t_{ROUT_LOW}	Time the output is pulled low by device before Read Acknowledge message	–	45	60	µs
Read Delay [2]	t_{START_READ}	Delay from the trailing edge of a Read command frame to the leading edge of the Read Acknowledge frame	25 µs – 0.25 × t_{BIT}	50 µs – 0.25 × t_{BIT}	150 µs – 0.25 × t_{BIT}	µs
Read Output Enable Delay	t_{ROUT_EN}	Required delay from the trailing edge of the final Read Acknowledge pulse to output entering the normal operation state	–	45	60	µs
Disable Output Delay [2]	t_{DIS_OUT}	Delay from the trailing edge of a Disable Output command frame to the device output going from normal operation to the high-impedance state	1 µs – 0.25 × t_{BIT}	7 µs – 0.25 × t_{BIT}	15 µs – 0.25 × t_{BIT}	µs
Enable Output Delay [2]	t_{ENB_OUT}	Delay from the trailing edge of an Enable Output command frame to the device output going from the high-impedance state to normal operation	1 µs – 0.25 × t_{BIT}	7 µs – 0.25 × t_{BIT}	15 µs – 0.25 × t_{BIT}	µs
EEPROM PROGRAMMING PULSE						
EEPROM Programming Pulse Setup Time	$t_{sPULSE(E)}$	Delay from last edge of write command to start of EEPROM programming pulse	40	–	–	µs
INPUT/OUTPUT SIGNAL VOLTAGE						
Manchester Code High Voltage	$V_{MAN(H)}$	Applied to VCC line	7.3	–	–	V
		Read from OUT line	V_{CC} – 0.2	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	Applied to VCC line	–	–	5.7	V
		Read from OUT line	–	–	V_{SAT}	V

[1] Determined by design.
[2] In the case where a slower baud rate is used, the output responds before the transfer of the last bit in the command message is completed.

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Serial Interface Message Structure

The general format of a command message frame is shown in Figure 13. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary.

The bits are described in Table 5.

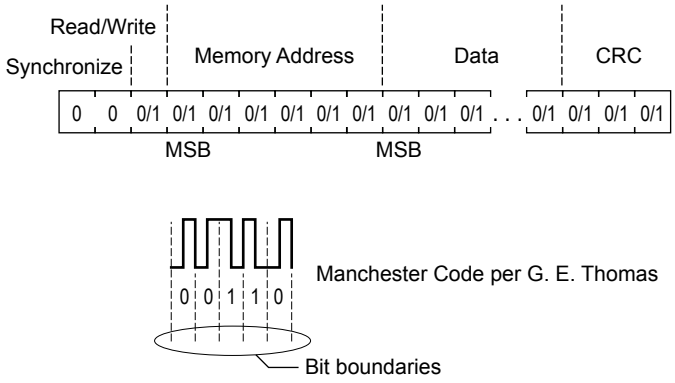


Figure 13: General Format for Serial Interface Commands

Table 5: Serial Interface Command General Format

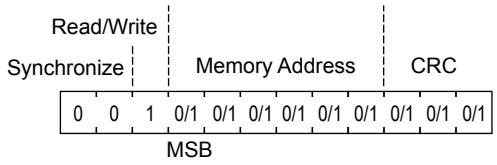
Bits	Parameter Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
30	Data	0/1	[As required]
3	CRC	0/1	Incorrect value indicates errors

The following command messages can be exchanged between the device and the external controller:

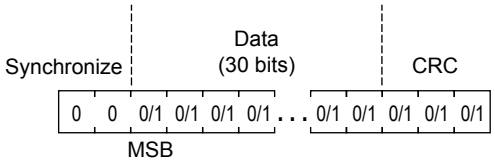
- Read
- Read Acknowledge
- Write
- Write Access Code

For EEPROM address information, refer to the EEPROM Structure section.

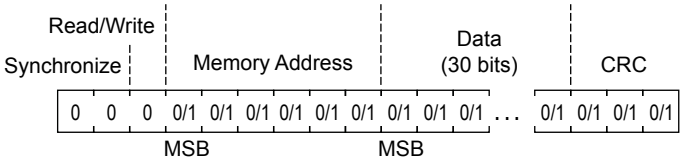
READ

Function	Provides the address in A1343 memory to be accessed to transmit the contents to the external controller in the next Read Acknowledge command.
Syntax	Sent by the external controller on the A1343 VCC pin.
Related Commands	Read Acknowledge
Pulse Sequence	
Options	Requires disabling of memory locking mechanisms.
Examples	Read address 0x08 Read/Write = 1 Memory Address = 001000 CRC bits = 110

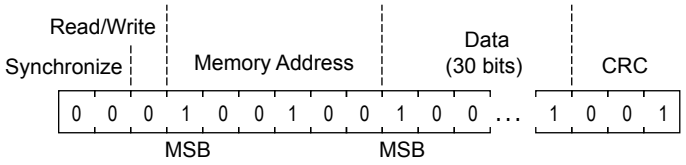
READ ACKNOWLEDGE

Function	Transmits to the external controller data retrieved from the A1343 memory in response to the most recent Read command.
Syntax	Sent by the A1343 on the A1343 OUT pin. Sent after a Read command.
Related Commands	Read
Pulse Sequence	
Options	The 6 MSBs are EEPROM data error checking bits. Refer to the EEPROM Structure section for more information.
Examples	–

WRITE

Function	Transmits to the A1343 data prepared by the external controller.
Syntax	Sent by the external controller on the A1343 VCC pin.
Related Commands	Write Access Code
Pulse Sequence	
Options	Requires disabling of memory locking mechanisms.
Examples	–

WRITE ACCESS CODE

Function	Transmits the Access Code to the A1343; data prepared by the external controller, but must match the internal 30-bit code in the A1343 memory.
Syntax	Sent by the external controller on the A1343 VCC pin. Sent within 10 ms of A1343 power-on, and before any other command.
Related Commands	
Pulse Sequence	
Options	None
Examples	Standard Customer Access Code: 0x2781_1F77 to address 0x24 Read/Write = 0 Memory Address = 100100 Data bits = 10 0111 1000 0001 0001 1111 0111 0111 CRC bits = 001

LINEAR OUTPUT PROTOCOLS

The operating output of the A1343 is digital voltage signal that transfers information proportionally to the applied magnetic input signal. Two customer-selectable options are provided for output signal formatting: pulse-wave modulated (PWM), and single edge nibble transmission encoding scheme (SENT, SAEJ2716).

Note: The device response to the applied magnetic field is on the OUT pin. However, that pin is also used to transmit data in response to a serial read command, during which the normal output operation is suppressed. Refer to the Programming Serial Interface section for more information. The EEPROM is described in the EEPROM Structure section.

The output falling edge slew rate is adjustable using the OUTDRV_CFG parameter. Adjusting this can improve EMC performance by reducing high-frequency currents. This parameter can also increase the output fall time and result in longer minimum pulse durations for serial communication or SENT transmission.

PWM Output Mode

PWM involves converting the output voltage amplitude to a series of constant-frequency binary pulses, with the percentage of the of high portion of the pulse varied in direct proportion to the applied magnetic field.

The PWM output mode is configured by setting the following parameters in EEPROM:

- PWM_MODE set to 1 to select the PWM option (for programming parameters, see EEPROM Structure section)
- FPWM sets the PWM carrier frequency
- CALIBRATE_PWM parameter can be set to enable calibration of the output 50% duty cycle level at power-on

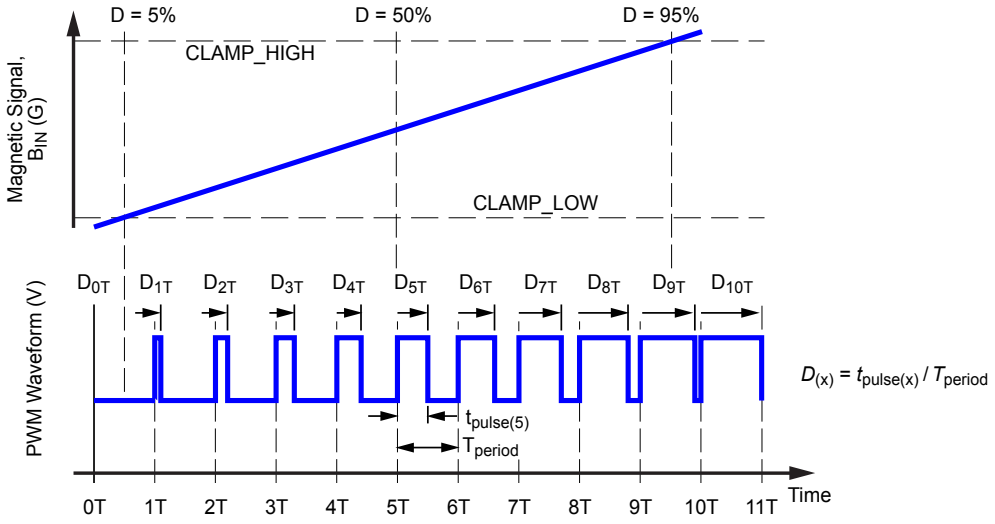


Figure 14: PWM mode outputs a duty-cycle-based waveform that can be read by the external controller as a cumulatively changing continuous voltage.

SENT Output Mode

The SENT output mode converts the input magnetic signal to a binary value mapped to the Full Scale Output, FSO, range of 0 to 4095, shown in Figure 15. This data is inserted into a binary pulse message, referred to as a *frame*, that conforms to the SENT data transmission specification (SAEJ2716 JAN2010). Certain parameters for configuration of the SENT messages can be set in EEPROM.

The SENT output mode is configured by setting the following parameters in EEPROM:

- PWM_MODE set to 0 (default) to select the SENT option
- SENT_x programming parameters (see EEPROM Structure section)

Message Structure

A SENT message is a series of *nibbles*, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval
- Either interval can be the *delimiting state*, which only sets a boundary for the nibble; to assign the delimiting state, select a fixed duration for the interval (the SENT_LOVAR parameter selects the interval, and SENT_FIXED sets the duration)
- The other interval in the pair becomes the *information state* and is variable in duration in order to contain the data payload of the nibble

The duration of a nibble is denominated in clock *ticks*. The period of a tick is set by dividing a 4-MHz clock by the value of the SENT_TICK parameter. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The nibbles of a SENT message are arranged in the following required sequence (see Figure 16):

1. Synchronization and Calibration: flags the start of the SENT message
2. Status and Communication: provides A1343 status and the format of the data
3. Data: magnetic field and optional data
4. CRC: error checking
5. Pause Pulse (optional): sets timing relative to A1343 updates

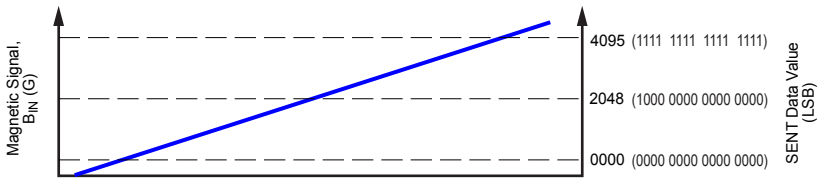


Figure 15: SENT mode outputs a digital value that can be read by the external controller and combined with accompanying range setting data to calculate the corresponding voltage level.

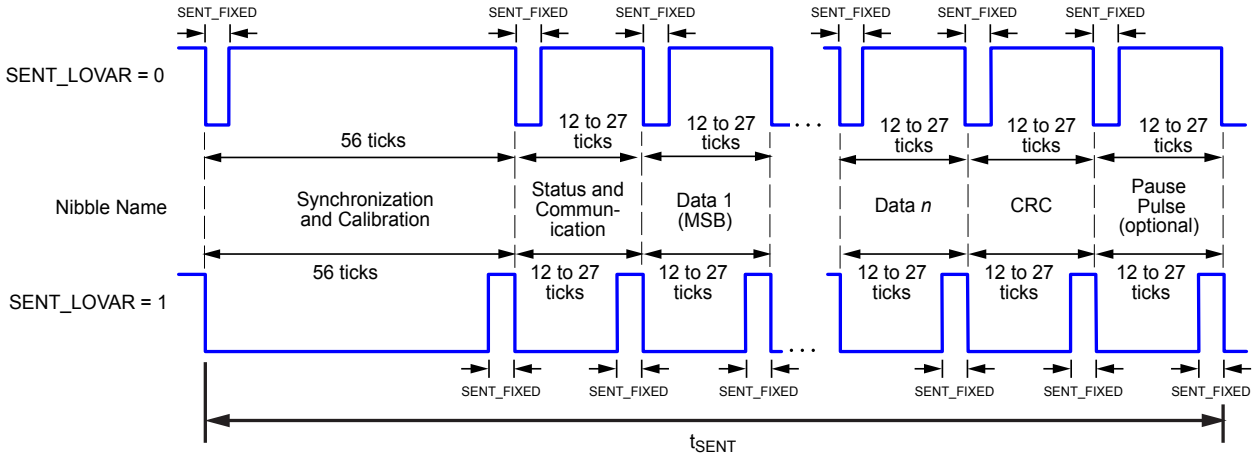


Figure 16: General Format for SENT Message Frame — (upper panel) low state fixed, (lower panel) high state fixed

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com