Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Low-Noise, High-Precision, Programmable Linear Hall-Effect Sensor IC with High-Bandwidth (120 kHz) Analog Output and Integrated Fault Comparator with Self-Test Diagnostic Mode

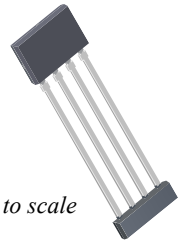
FEATURES AND BENEFITS

- Proprietary segmented linear temperature compensation (TC) technology provides a typical accuracy of 1% over the full operating temperature range
- Self-Test diagnostic mode can be used to achieve a high level of functional safety within a system
- 120 kHz nominal bandwidth achieved via proprietary packaging and chopper stabilization techniques
- Over Field Fault signal with 6-bit programmable trigger levels, 2-bit programmable hysteresis, and latching or non-latching behavior
- Over Field Fault response time < 4.5 µs (typ)
- Extremely low noise and high resolution achieved via proprietary Hall element and low-noise amplifier circuits
- Customer-programmable, high-resolution offset and sensitivity trim
- Available in a 1-mm-thick SIP through-hole package

Continued on the next page…

PACKAGE:

4-Pin SIP (suffix KT)



Not to scale

DESCRIPTION

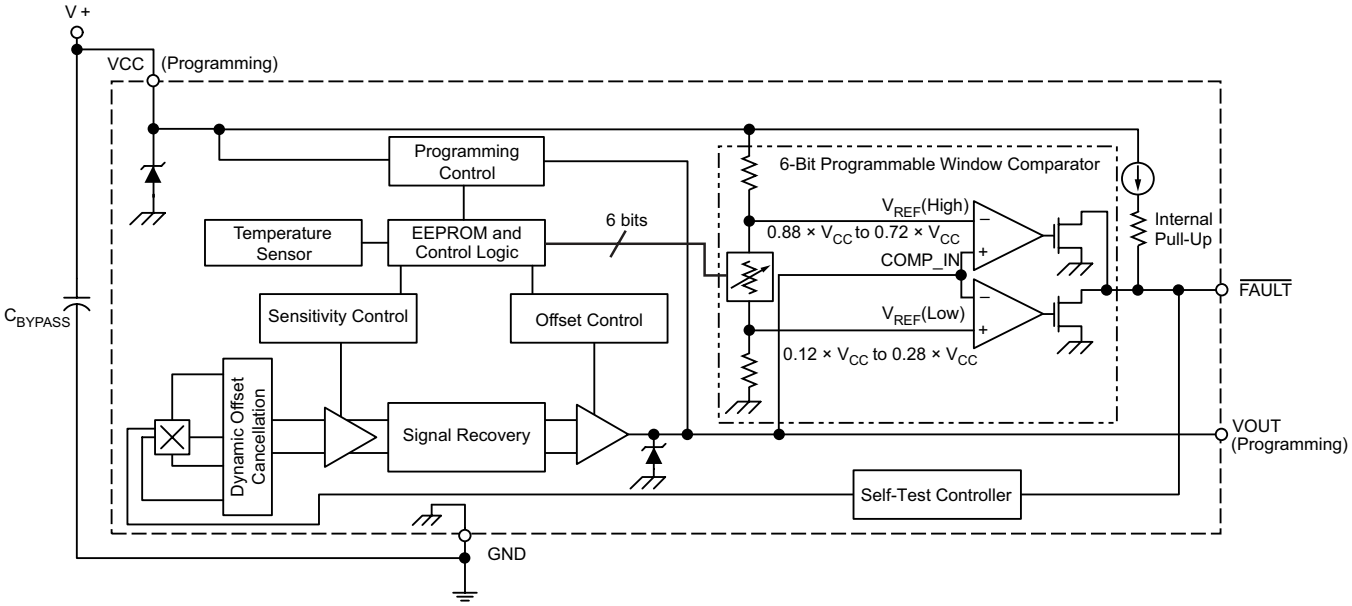
The A1365 linear output Hall-effect sensor IC is specifically designed to provide a highly accurate output with improved resolution at high bandwidth for use in current-sensing applications. This device employs a segmented, linearly interpolated temperature compensation technology, which provides greater accuracy in sensitivity and offset voltage trimming and hence virtually zero temperature drift. This improvement greatly reduces the total error of the device across the operating temperature range.

A user-activated Self-Test diagnostic mode verifies the A1365 Sensitivity and Over Field Fault functionality and can be used to achieve a high level of functional safety in application.

The highly programmable Over Field Fault signal ($\overline{\text{FAULT}}$ pin) can be used to detect a high magnetic field condition. Broken ground wire detection, undervoltage lockout for V_{CC} below specification, and user-selectable output voltage clamps are also included, which are important for high reliability in automotive applications. The sensor accuracy and diagnostic capability make it ideally suited for automotive sockets such as HEV inverter and DC-to-DC converter applications.

The A1365 Hall-effect sensor IC is extremely sensitive, fast, and temperature-stable. The accuracy and flexibility of this device is enhanced by user programmability, performed via the V_{CC} supply and the output pins, which allows the device to be optimized in the application.

Continued on the next page…



Functional Block Diagram

FEATURES AND BENEFITS (CONTINUED)

- Factory-programmed sensitivity and quiescent output voltage TC with extremely stable temperature performance
- Selectable sensitivity range between 0.6 and 14 mV/G through use of coarse sensitivity program bits
- Ratiometric sensitivity, quiescent voltage output, and clamps enable simple interface with application A-to-D converter (ADC)
- Output voltage clamps provide short-circuit diagnostic capabilities
- Open-circuit detection on ground pin (broken wire)
- Undervoltage lockout for V_{CC} below specification
- Wide ambient temperature range: –40°C to 150°C

DESCRIPTION (CONTINUED)

This ratiometric Hall-effect sensor IC provides a voltage output that is proportional to the applied magnetic field. The quiescent output voltage is user-adjustable around 50% (bidirectional) of the supply voltage, V_{CC}. The device sensitivity is adjustable within the range of 0.6 to 14 mV/G.

The A1365 incorporates a highly sensitive Hall element with a BiCMOS interface integrated circuit that employs temperature-compensation circuitry to reduce the intrinsic sensitivity and offset drift of the Hall element. The IC also includes a small-signal high-gain amplifier, a clamped low-impedance output stage, and a proprietary high-bandwidth dynamic offset cancellation technique.

Device specifications apply across an extended ambient temperature range: –40°C to 150°C. The A1365 sensor IC is provided in an extremely thin case (1 mm thick), 4-pin SIP (single inline package, suffix KT) that is lead (Pb) free, with 100% matte-tin leadframe plating. The thin package allows for better magnetic coupling because the smaller the air gap in the core is, the higher the coupling from current to magnetic field will be.

Table of Contents

SELECTION GUIDE

Part Number	Package	Packing [1]	Sensitivity Range [2] (mV/G)
A1365LKTTN-1-T	4-pin SIP	4000 pieces per 13-inch reel	0.6 to 1.3
A1365LKTTN-2-T	4-pin SIP	4000 pieces per 13-inch reel	1.3 to 2.9
A1365LKTTN-5-T	4-pin SIP	4000 pieces per 13-inch reel	2.9 to 6.4
A1365LKTTN-10-T	4-pin SIP	4000 pieces per 13-inch reel	6.4 to 14

[1] Contact Allegro for additional packing options.
[2] Allegro recommends against changing Coarse Sensitivity settings when programming devices that will be used in production. Each A1365 has been factory temperature compensated at a specific sensitivity range, and changing the coarse bits setting could cause sensitivity drift through temperature range ($\Delta Sens_{TC}$) to exceed specified limits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

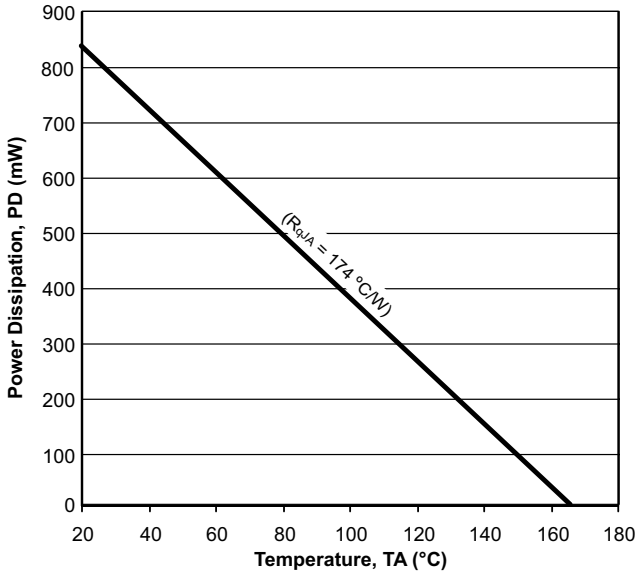
Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		6	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward Output Voltage	V_{OUT}		25	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Forward Fault Voltage	$V_{\overline{FAULT}}$		6	V
Reverse Fault Voltage	$V_{R\overline{FAULT}}$		–0.1	V
Output Source Current	$I_{OUT(source)}$	VOUT to GND	2.8	mA
Output Sink Current	$I_{OUT(sink)}$	VCC to VOUT	10	mA
Maximum Number of EEPROM Write Cycles	$EEPROM_{w(max)}$		100	cycles
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	$T_J(max)$		165	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

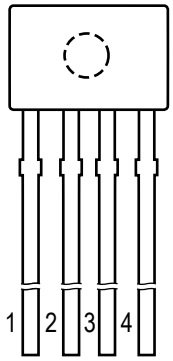
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 1-layer PCB with exposed copper limited to solder pads	174	°C/W

*Additional thermal information available on the Allegro website

Power Dissipation versus Ambient Temperature



PINOUT DIAGRAM AND TERMINAL LIST TABLE



KT Package Pinout Diagram

(Ejector pin mark on opposite side)

Terminal List Table

Number	Name	Function
1	VCC	Input Power Supply, use bypass capacitor to connect to ground; also used for programming
2	VOUT	Output Signal, also used for programming
3	$\overline{\text{FAULT}}$	Over Field Fault Detection Flag
4	GND	Ground

OPERATING CHARACTERISTICS: Valid through the full operating temperature range T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}	No load on VOUT, $\overline{FAULT}$ pin in high-impedance state, connected through a 10 kΩ resistor to VCC	–	10	15	mA
Power-On Time [2]	t_{PO}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF	–	100	–	µs
Temperature Compensation Power-On Time [2]	t_{TC}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF	–	90	–	µs
Undervoltage Lockout (UVLO) Threshold [2]	V_{UVLOH}	V_{CC} rising and device function enabled	–	4	4.3	V
	V_{UVLOL}	V_{CC} falling and device function disabled	3.05	3.2	–	V
UVLO Enable/Disable Delay Time [2]	t_{UVLOE}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF, V_{CC} fall time (5 V to 3 V) = 1.5 µs	–	67	–	µs
	t_{UVLOD}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF, V_{CC} recover time (3 V to 5 V) = 1.5 µs	–	6	–	µs
Power-On Reset Voltage [2]	V_{PORH}	T_A = 25°C, V_{CC} rising	–	2.9	–	V
	V_{PORL}	T_A = 25°C, V_{CC} falling	–	2.5	–	V
Power-On Reset Release Time [2]	t_{PORR}	T_A = 25°C, V_{CC} rising	–	85	–	µs
Supply Zener Clamp Voltage	V_z	T_A = 25°C, I_{CC} = 30 mA	6.5	7.5	–	V
Internal Bandwidth	BW_i	Small signal –3 dB, C_L = 1 nF, T_A = 25°C	–	120	–	kHz
Chopping Frequency [3]	f_C	T_A = 25°C	–	500	–	kHz
V_{OUT} CHARACTERISTICS						
Propagation Delay Time [2]	t_{pd}	T_A = 25°C, step magnetic field of 400 G, C_L = 1 nF, Sens = 2 mV/G	–	2.2	–	µs
Rise Time [2]	t_r	T_A = 25°C, step magnetic field of 400 G, C_L = 1 nF, Sens = 2 mV/G	–	3.6	–	µs
Response Time [2]	$t_{RESPONSE}$	T_A = 25°C, step magnetic field of 400 G, C_L = 1 nF, Sens = 2 mV/G	–	3.7	–	µs
Delay to Clamp [2][4]	t_{CLP}	T_A = 25°C, step magnetic field from 160 to 240 G, C_L = 1 nF, Sens = 10 mV/G	–	10	–	µs
Output Voltage Clamp [5]	$V_{CLP(HIGH)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	4.55	–	4.85	V
	$V_{CLP(LOW)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	0.15	–	0.45	V
Output Saturation Voltage [2]	$V_{SAT(HIGH)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	4.8	–	–	V
	$V_{SAT(LOW)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to VCC	–	–	300	mV
Broken Wire Voltage [2]	$V_{BRK(HIGH)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	–	V_{CC}	–	V
	$V_{BRK(LOW)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	–	200	–	mV
Noise [6]	V_N	T_A = 25°C, CL = 1 nF	–	1.1	_	mG/√(Hz)
		T_A = 25°C, CL = 1 nF, Sens = 2 mV/G, bandwidth = BW_i	–	6.3	_	mV_{p-p}
		T_A = 25°C, CL = 1 nF, Sens = 2 mV/G, bandwidth = BW_i	–	1	_	mV_{RMS}

Continued on the next page…

OPERATING CHARACTERISTICS (continued): Valid through the full operating temperature range T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
V_{OUT} CHARACTERISTICS (continued)						
DC Output Resistance	R_{OUT}	T_A = 25°C	–	< 10	–	Ω
Output Load Resistance	$R_{L(PULLUP)}$	VOUT to VCC	4.7	–	–	kΩ
	$R_{L(PULLDWN)}$	VOUT to GND	4.7	–	–	kΩ
Output Load Capacitance [7]	C_L	VOUT to GND	–	1	10	nF
Output Slew Rate [8]	SR	Sens = 2 mV/G, C_L = 1 nF, T_A = 25°C; step magnetic field of 400 G	–	230	–	V/ms
OVER FIELD FAULT CHARACTERISTICS						
Fault Switchpoint Programming Bits	FAULT_ THRESH		–	6	–	bit
Positive Field Fault Switchpoint Range [9]	V_{FPSP}	T_A = 25°C, programmable using FAULT_THRESH bits	0.72 × V_{CC}	–	0.88 × V_{CC}	V
Negative Field Fault Switchpoint Range [9]	V_{FNSP}	T_A = 25°C, programmable using FAULT_THRESH bits	0.12 × V_{CC}	–	0.28 × V_{CC}	V
Fault Switchpoint Step Size	$Step_{FAULT}$	T_A = 25°C, Average Fault Switchpoint step size, V_{CC} = 5 V	–	16	–	mV
Fault Hysteresis Programming Bits	FAULT_HYST		–	2	–	bit
Fault Hysteresis Level Range [9]	V_{FHYST}	T_A = 25°C, FAULT_HYST = 0 (decimal), FAULT_THRESH = 0, no hysteresis	–	0	–	mV
		T_A = 25°C, FAULT_HYST = 1 (decimal), FAULT_THRESH = 0, V_{CC} = 5 V	–	30	–	mV
		T_A = 25°C, FAULT_HYST = 2 (decimal), FAULT_THRESH = 0, V_{CC} = 5 V	–	60	–	mV
		T_A = 25°C, FAULT_HYST = 3 (decimal), FAULT_THRESH = 0, maximum hysteresis value, V_{CC} = 5 V	–	120	–	mV
Enable Latched Fault Bit	FAULT_ LATCH		–	1	–	bit
DC Fault Switchpoint Error	Err_{DFS}	FAULT_THRESH = 0 (decimal), $R_{F(PULLUP)}$ = 10 kΩ from $\overline{FAULT}$ to VCC; measured under DC conditions, V_{FHYST} = 60 mV	–	±40	–	mV
DC Fault Switchpoint Symmetry Error	Err_{DFSS}	FAULT_THRESH = 0 (decimal), $R_{F(PULLUP)}$ = 10 kΩ from $\overline{FAULT}$ to VCC; measured under DC conditions, V_{FHYST} = 60 mV	–	±60	–	mV
$\overline{FAULT}$ Pin Low Output Voltage	$V_{\overline{FAULT}L}$	$R_{F(PULLUP)}$ = 10 kΩ from $\overline{FAULT}$ to VCC	–	–	0.3	V
Transient Fault Response Time [10]	t_{TFR}	$R_{F(PULLUP)}$ = 10 kΩ from $\overline{FAULT}$ to VCC, C_F = Open, FAULT_THRESH = 0, VOUT step from $V_{OUT(Q)}$ to V_{OUT} = 1.3 × (V_{FPSP} – $V_{OUT(Q)}$) + $V_{OUT(Q)}$	–	4.5	–	µs
Transient Fault Release Time	t_{TFRL}	$R_{F(PULLUP)}$ = 10 kΩ from $\overline{FAULT}$ to VCC, C_F = Open, FAULT_THRESH = 0, V_{FHYST} = 0 mV, VOUT step from VOUT = 1.1 × (V_{FPSP} – $V_{OUT(Q)}$) + $V_{OUT(Q)}$	–	2.5	–	µs

Continued on the next page…

OPERATING CHARACTERISTICS (continued): valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
FAULT CHARACTERISTICS (continued)						
Fault Delay Due to Load Capacitance	t_{FDC}	$R_{F(PULLUP)}$ = 10 kΩ from $\overline{FAULT}$ to VCC	–	0.5	–	µs/nF
External Pull-Up Supply Voltage	$V_{F(PULLUP)}$		1.65	V_{CC}	V_{CC}	V
External $\overline{FAULT}$ Pull-Up Resistor	$R_{F(PULLUP)}$		4.7	–	–	kΩ
External $\overline{FAULT}$ Capacitance	C_F		–	–	10	nF
Internal $\overline{FAULT}$ Pull-Up Resistor	$R_{IF(PULLUP)}$		–	10	–	kΩ
Internal $\overline{FAULT}$ Pull-Up Current	$I_{IF(PULLUP)}$		–	40	–	µA
QUIESCENT VOLTAGE OUTPUT ($V_{OUT(Q)}$) [2]						
Initial Unprogrammed Quiescent Voltage Output [2][11]	$V_{OUT(Q)init}$	T_A = 25°C	2.4	2.5	2.6	V
Quiescent Voltage Output Programming Range [2][5][12]	$V_{OUT(Q)PR}$	T_A = 25°C	2.3	–	2.7	V
Quiescent Voltage Output Programming Bits [13]	QVO		–	9	–	bit
Average Quiescent Voltage Output Programming Step Size [2][14][15]	$Step_{VOUT(Q)}$	T_A = 25°C	1.9	2.3	2.8	mV
Quiescent Voltage Output Programming Resolution [2][16]	$Err_{PGVOUT(Q)}$	T_A = 25°C	–	±0.5 × $Step_{VOUT(Q)}$	–	mV
SENSITIVITY (Sens) [2]						
Initial Unprogrammed Sensitivity [11]	$Sens_{init}$	SENS_COARSE = 00, T_A = 25°C	–	1	–	mV/G
		SENS_COARSE = 01, T_A = 25°C	–	2.2	–	mV/G
		SENS_COARSE = 10, T_A = 25°C	–	4.7	–	mV/G
		SENS_COARSE = 11, T_A = 25°C	–	9.6	–	mV/G
Sensitivity Programming Range [5][12]	$Sens_{PR}$	SENS_COARSE = 00, T_A = 25°C	0.6	–	1.3	mV/G
		SENS_COARSE = 01, T_A = 25°C	1.3	–	2.9	mV/G
		SENS_COARSE = 10, T_A = 25°C	2.9	–	6.4	mV/G
		SENS_COARSE = 11, T_A = 25°C	6.4	–	14	mV/G
Coarse Sensitivity Programming Bits [17]	SENS_COARSE		–	2	–	bit
Fine Sensitivity Programming Bits [13]	SENS_FINE		–	9	–	bit
Average Fine Sensitivity and Temperature Compensation Programming Step Size [2][14][15]	$Step_{SENS}$	SENS_COARSE = 00, T_A = 25°C	2.4	3.2	4.1	µV/G
		SENS_COARSE = 01, T_A = 25°C	5	6.6	8.5	µV/G
		SENS_COARSE = 10, T_A = 25°C	11	14.2	18	µV/G
		SENS_COARSE = 11, T_A = 25°C	22	29	38	µV/G
Sensitivity Programming Resolution [2][16]	Err_{PGSENS}	T_A = 25°C	–	±0.5 × $Step_{SENS}$	–	µV/G
FACTORY-PROGRAMMED SENSITIVITY TEMPERATURE COEFFICIENT						
Sensitivity Temperature Coefficient [2]	TC_{SENS}	T_A=150°C, T_A= –40°C, calculated relative to 25°C	–	0	–	%/°C
Sensitivity Drift Through Temperature Range [2][12][18][23]	$\Delta Sens_{TC}$	T_A = 25°C to 150°C	–2.5	–	2.5	%
		T_A = –40°C to 25°C	–3	–	3	%

Continued on the next page…

OPERATING CHARACTERISTICS (continued): valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
FACTORY-PROGRAMMED QUIESCENT VOLTAGE OUTPUT TEMPERATURE COEFFICIENT						
Quiescent Voltage Output Temperature Coefficient [2]	TC_{QVO}	T_A = 150°C, T_A = –40°C, calculated relative to 25°C	–	0	–	mV/°C
Quiescent Voltage Output Drift Through Temperature Range [2][12][18]	$\Delta V_{OUT(Q)TC}$	SENS_COARSE = 00, SENS_COARSE = 01, or SENS_COARSE = 10, T_A = 25°C to 150°C	–10	–	10	mV
		SENS_COARSE = 11, T_A = 25°C to 150°C	–15	–	15	mV
		T_A = –40°C to 25°C	–30	–	30	mV
Average Quiescent Voltage Output Temperature Compensation Step Size	$Step_{QVOTC}$		–	2.3	–	mV
LOCK BIT PROGRAMMING						
EEPROM Lock Bit	EELOCK		–	1	–	bit
ERROR COMPONENTS						
Linearity Sensitivity Error [2][19]	Lin_{ERR}		–1	< ±0.25	1	%
Symmetry Sensitivity Error [2]	Sym_{ERR}		–0.5	< ±0.25	0.5	%
Ratiometry Quiescent Voltage Output Error [2][20]	$Rat_{ERRVOUT(Q)}$	Relative to V_{CC} = 5 V ±5%	–0.3	0	0.3	%
Ratiometry Sensitivity Error [2][20]	$Rat_{ERRSens}$	Relative to V_{CC} = 5 V ±5%	–1	< ±0.5	1	%
Ratiometry Clamp Error [2][21]	Rat_{ERRCLP}	T_A = 25°C, Relative to V_{CC} = 5 V ±5%	–	< ±1	–	%
Sensitivity Drift Due to Package Hysteresis [2]	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling, 25°C to 150°C and back to 25°C	–	-1.25 ±1.25	–	%
Sensitivity Drift Over Lifetime [22]	$\Delta Sens_{LIFE}$	T_A = 25°C, shift after AEC Q100 grade 0 qualification testing	–	±1%	–	%

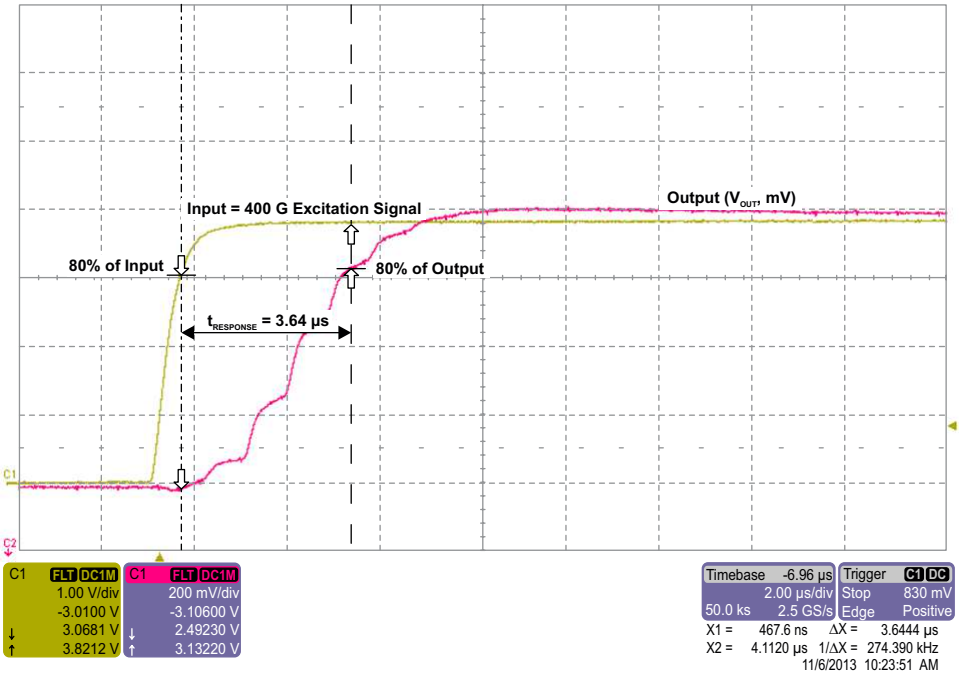
[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] See Characteristic Definitions section.
[3] f_C varies up to approximately ±5% over the full operating ambient temperature range, T_A.
[4] If the programmed Fault Switchpoint exceeds the clamp voltage, Fault operation will have priority over clamp operation.
[5] Sens, $V_{OUT(Q)}$, $V_{CLP(LOW)}$, and $V_{CLP(HIGH)}$ scale with V_{CC} due to ratiometry.
[6] Noise, measured in mV_{PP} and in mV_{RMS}, is dependent on the sensitivity of the device.
[7] Output stability is maintained for capacitive loads as large as 10 nF.
[8] High-to-low transition of output voltage is a function of external load components and device sensitivity.
[9] Fault Switchpoint and Fault Hysteresis are ratiometric.
[10] Refer to Fault Characteristics section for the impact of load circuit and different Fault switchpoint settings on Transient Fault Response Time.
[11] Raw device characteristic values before any programming.
[12] Exceeding the specified ranges will cause sensitivity and Quiescent Voltage Output drift through the temperature range to deteriorate beyond the specified values.
[13] Refer to Functional Description section.
[14] Step size is larger than required, in order to provide for manufacturing spread. See Characteristic Definitions section.
[15] Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be greater than twice the maximum specified value of $Step_{VOUT(Q)}$ or $Step_{SENS}$.
[16] Overall programming value accuracy. See Characteristic Definitions section.
[17] Each A1365 part number is factory-programmed and temperature compensated at a different coarse sensitivity setting. Changing coarse bits setting could cause sensitivity drift through temperature range ,$\Delta Sens_{TC}$, to exceed specified limits.
[18] Allegro will be testing and temperature compensating each device at 150°C. Allegro will not be testing devices at –40°C. Temperature compensation codes will be applied based on characterization data.
[19] Linearity applies to output voltage ranges of ±2 V from the quiescent output for bidirectional devices.
[20] Percent change from actual value at V_{CC} = 5 V, for a given temperature, through the supply voltage operating range.
[21] Percent change from actual value at V_{CC} = 5 V, T_A = 25°C, through the supply voltage operating range.
[22] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[23] Includes sensitivity drift due to package hysteresis after exposing the sensor to a temperature of 150°C for 60 seconds during test.

CHARACTERISTIC PERFORMANCE DATA

Response Time ($t_{RESPONSE}$)

400 G Excitation Signal with 10% to 90% rise time = 1 µs

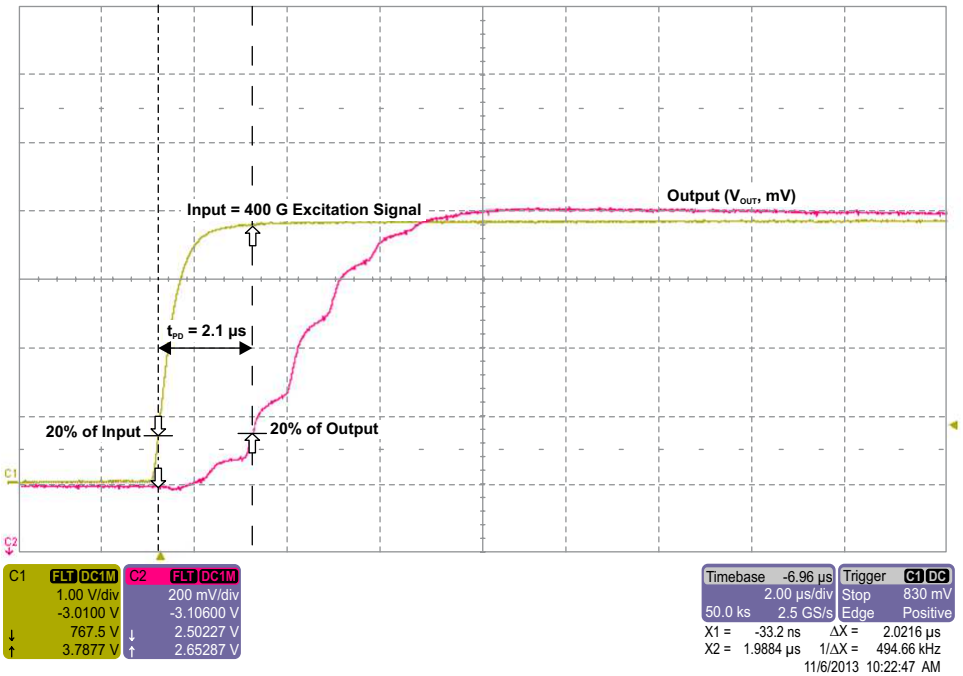
Sensitivity = 2 mV/G, C_{BYPASS} = 0.1 µF, C_L = 1 nF



Propagation Delay (t_{PD})

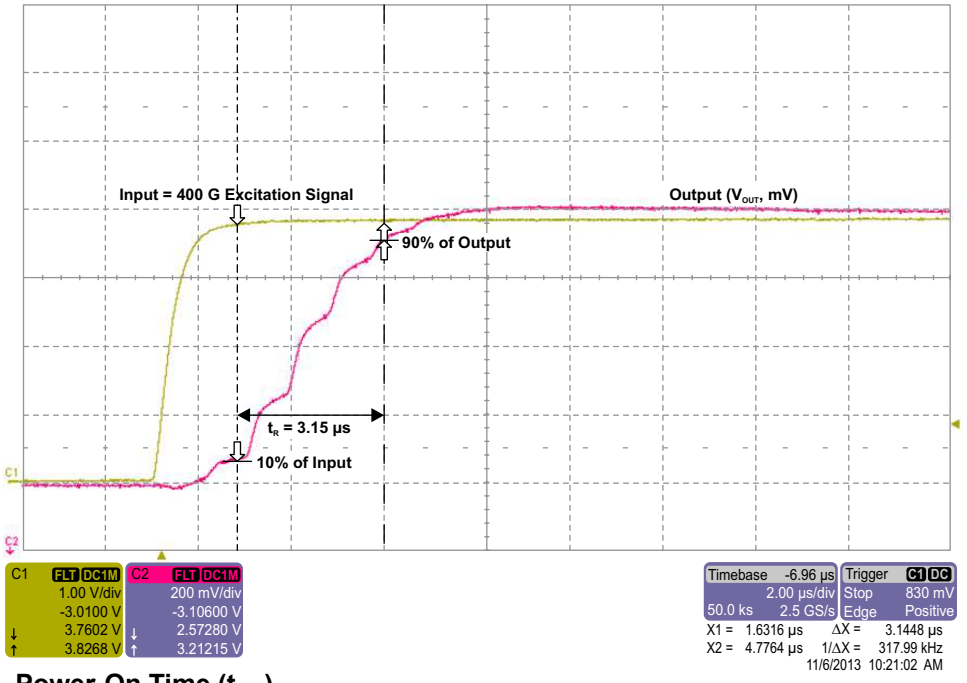
400 G Excitation Signal with 10% to 90% rise time = 1 µs

Sensitivity = 2 mV/G, C_{BYPASS} = 0.1 µF, C_L = 1 nF



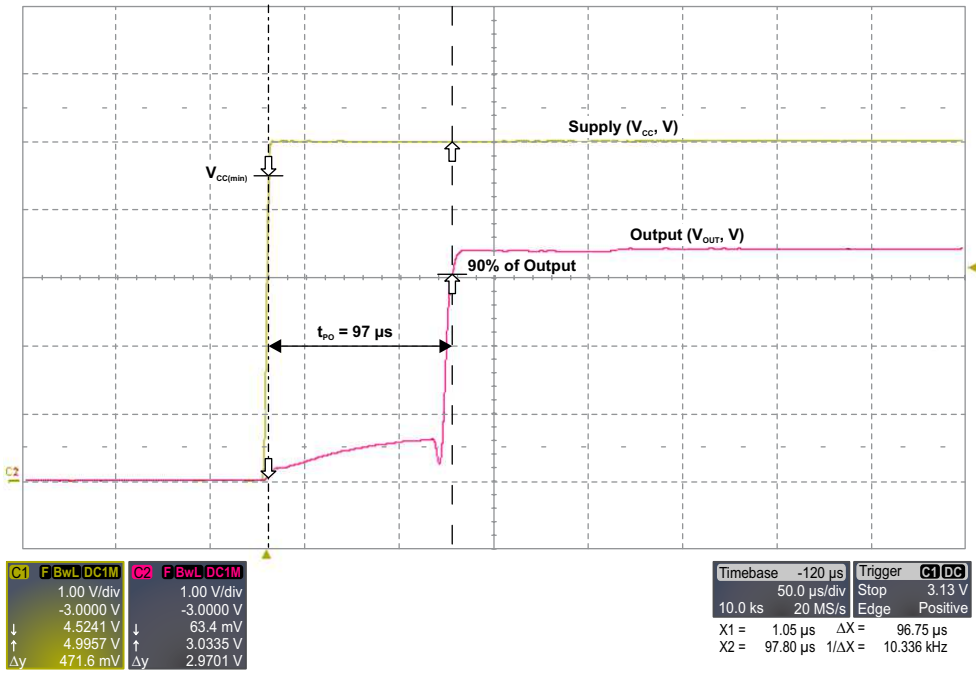
Rise Time (t_r)

400 G Excitation Signal with 10% to 90% rise time = 1 µs
Sensitivity = 2 mV/G, C_{BYPASS} = 0.1 µF, C_L = 1 nF



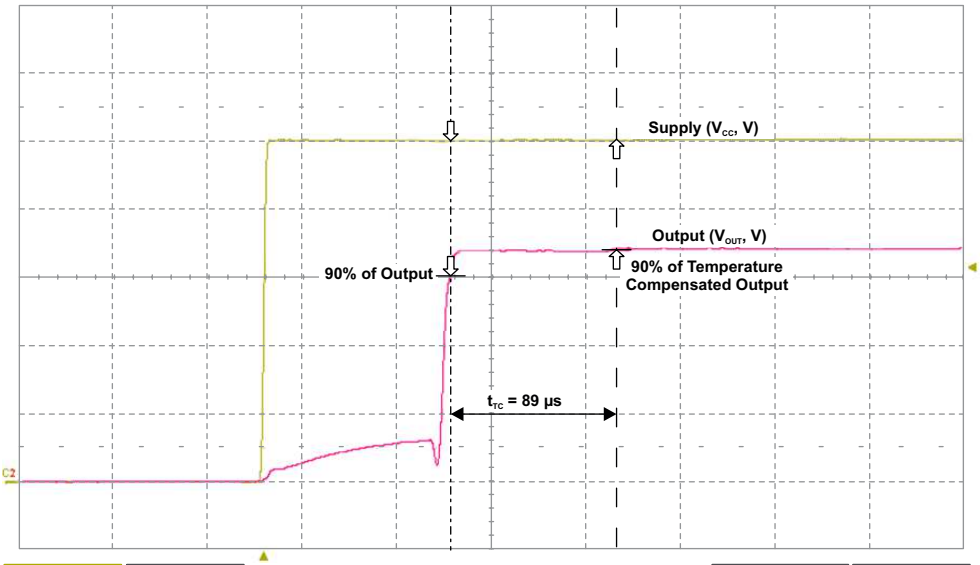
Power-On Time (t_{PO})

400 G Constant Excitation Signal with V_{CC} 10% to 90% rise time = 1 µs
Sensitivity = 2 mV/G, C_{BYPASS} = Open, C_L = 1 nF



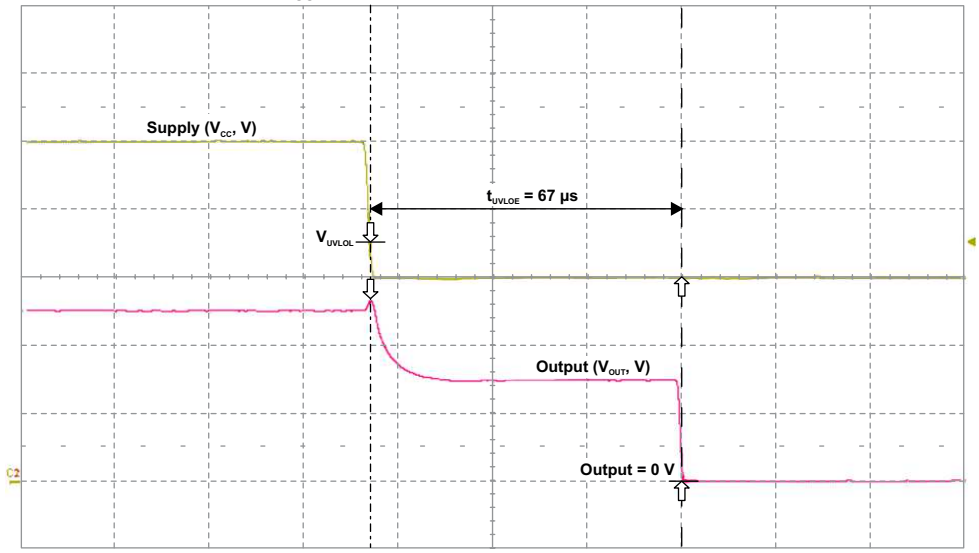
Temperature Compensation Power-On Time (t_{TC})

400G Constant Excitation Signal, with V_{CC} 10% to 90% rise time = 1.5 µs
Sensitivity = 2mV/G, C_{BYPASS} = Open, C_L = 1 nF



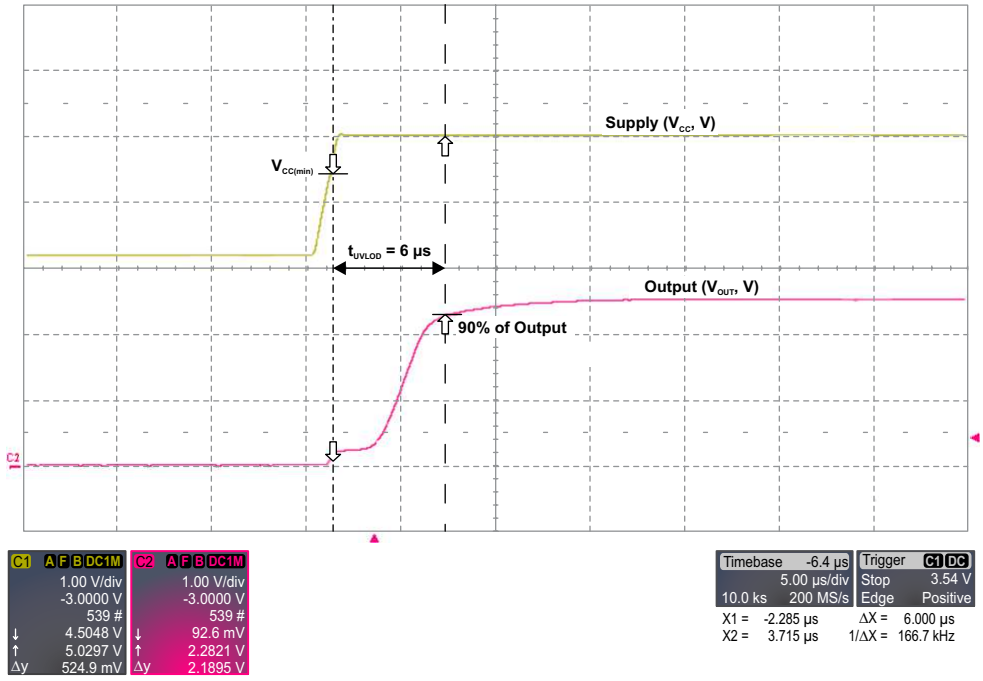
UVLO Enable Time (t_{UVLOE})

V_{CC} 5 V to 3 V fall time = 1.5 µs
Sensitivity = 2 mV/G, C_{BYPASS} = Open, C_L = 1 nF



UVLO Disable Time (t_{UVLOD})

V_{CC} 3.2 V to 5 V Recovery Time = 1.5 µs
Sensitivity = 2 mV/G, C_{BYPASS} = Open, C_L = 1 nF



CHARACTERISTIC DEFINITIONS

Power-On Time (t_{PO})

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-On Time (t_{PO}) is defined as: the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage ($V_{CC(min)}$) as shown in Figure 1.

Temperature Compensation Power-On Time (t_{TC})

After Power-On Time (t_{PO}) elapses, t_{TC} is also required before a valid temperature compensated output.

Propagation Delay (t_{pd})

The time interval between a) when the applied magnetic field reaches 20% of its final value, and b) when the output reaches 20% of its final value (see Figure 2).

Rise Time (t_r)

The time interval between a) when the sensor IC reaches 10% of its final value, and b) when it reaches 90% of its final value (see Figure 2). Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

Response Time ($t_{RESPONSE}$)

The time interval between a) when the applied magnetic field reaches 80% of its final value, and b) when the sensor reaches 80% of its output corresponding to the applied magnetic field (see Figure 3).

Delay to Clamp (t_{CLP})

A large magnetic input step may cause the clamp to overshoot its steady-state value. The Delay to Clamp (t_{CLP}) is defined as: the time it takes for the output voltage to settle within steady-state clamp voltage ±1% of Clamp Voltage Dynamic Range, after initially passing through its steady-state voltage, as shown in Figure 4. Clamp Voltage Dynamic Range is defined as $V_{CLP(HIGH)(min)} - V_{CLP(LOW)(max)}$.

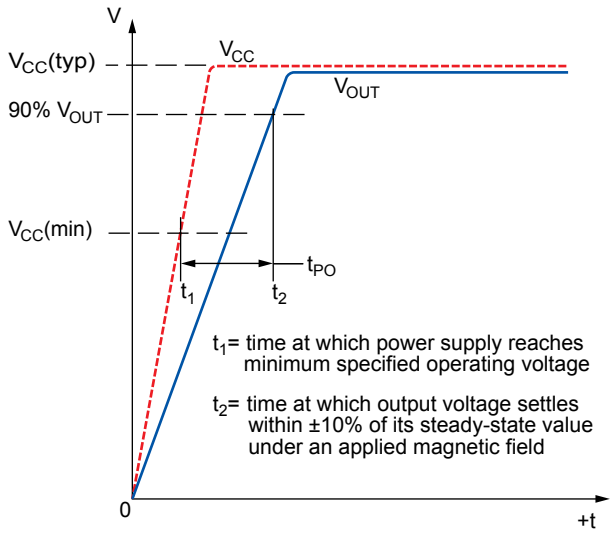


Figure 1: Power-On Time Definition

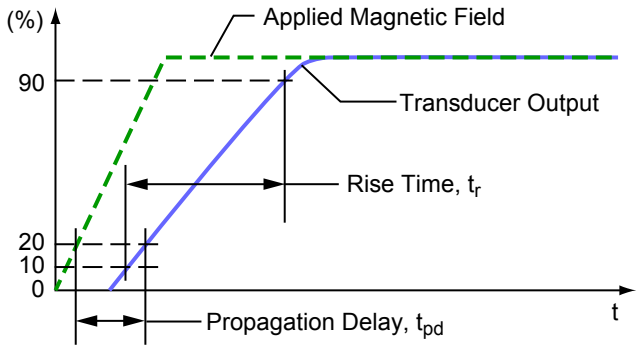


Figure 2: Propagation Delay and Rise Time Definitions

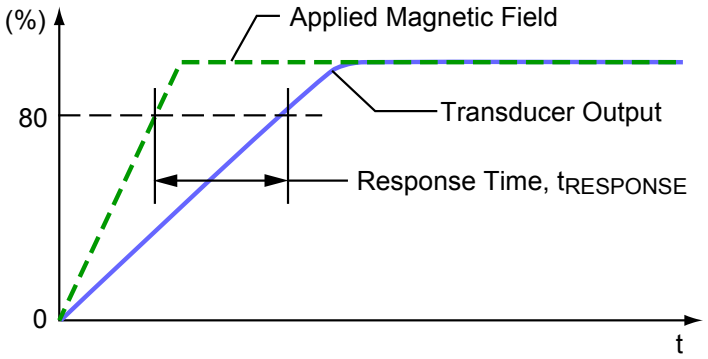


Figure 3: Response Time Definition

Quiescent Voltage Output ($V_{OUT(Q)}$)

In the quiescent state (no significant magnetic field: B = 0 G), the output ($V_{OUT(Q)}$) has a constant ratio to the supply voltage (V_{CC}) throughout the entire operating ranges of V_{CC} and ambient temperature (T_A).

Initial Unprogrammed Quiescent Voltage Output ($V_{OUT(Q)init}$)

Before any programming, the Quiescent Voltage Output ($V_{OUT(Q)}$) has a nominal value of V_{CC} /2, as shown in Figure 5.

Quiescent Voltage Output Programming Range ($V_{OUT(Q)PR}$)

The Quiescent Voltage Output ($V_{OUT(Q)}$) can be programmed within the Quiescent Voltage Output Range limits: $V_{OUT(Q)PR(min)}$ and $V_{OUT(Q)PR(max)}$. Exceeding the specified Quiescent Voltage Output Range will cause Quiescent Voltage Output Drift Through Temperature Range $\Delta V_{OUT(Q)TC}$ to deteriorate beyond the specified values, as shown in Figure 5.

Average Quiescent Voltage Output Programming Step Size ($Step_{VOUT(Q)}$)

The Average Quiescent Voltage Output Progamming Step Size ($Step_{VOUT(Q)}$) is determined using the following calculation:

$$Step_{VOUT(Q)} = \frac{V_{OUT(Q)maxcode} - V_{OUT(Q)mincode}}{2^n - 1}, \quad (1)$$

where n is the number of available programming bits in the trim range, 9 bits, $V_{OUT(Q)maxcode}$ is at decimal code 255, and $V_{OUT(Q)mincode}$ is at decimal code 256.

Quiescent Voltage Output Programming Resolution ($Err_{PGVOUT(Q)}$)

The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution will be:

$$Err_{PGVOUT(Q)}(typ) = 0.5 \times Step_{VOUT(Q)}(typ) \quad (2)$$

Quiescent Voltage Output Temperature Coefficient (TC_{QVO})

Device $V_{OUT(Q)}$ changes as temperature changes, with respect to its programmed Quiescent Voltage Output Temperature Coefficient, TC_{QVO}. TC_{QVO} is programmed at 150°C and is calculated relative to the nominal $V_{OUT(Q)}$ programming temperature of 25°C. TC_{QVO} (mV/°C) is defined as:

$$TC_{QVO} = [V_{OUT(Q)T2} - V_{OUT(Q)T1}][1/(T2 - T1)] \quad (3)$$

where T1 is the nominal $V_{OUT(Q)}$ programming temperature of 25°C, and T2 is the TC_{QVO} programming temperature of 150°C. The expected $V_{OUT(Q)}$ through the full ambient temperature range ($V_{OUT(Q)EXPECTED(TA)}$) is defined as:

$$V_{OUT(Q)EXPECTED}(T_A) = V_{OUT(Q)T1} + TC_{QVO}(T_A - T1) \quad (4)$$

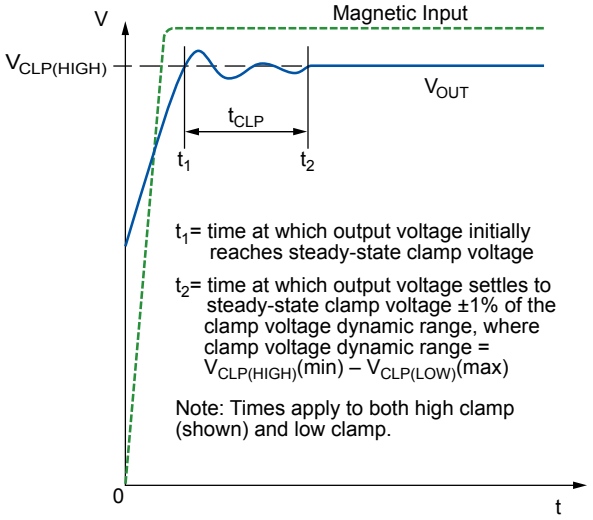


Figure 4: Delay to Clamp Definition

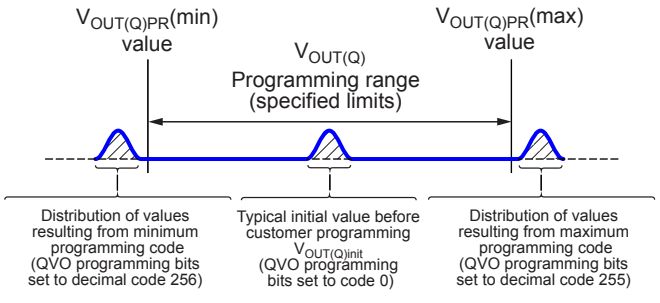


Figure 5: Quiescent Voltage Output Range Definition

$V_{OUT(Q)EXPECTED(TA)}$ should be calculated using the actual measured values of $V_{OUT(Q)T1}$ and TC_{QVO} rather than programming target values.

Quiescent Voltage Output Drift Through Temperature Range ($\Delta V_{OUT(Q)TC}$)

Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output ($V_{OUT(Q)}$) may drift from its nominal value through the operating ambient temperature (T_A). The Quiescent Voltage Output Drift Through Temperature Range ($\Delta_{VOUT(Q)TC}$) is defined as:

$$D_{VOUT(Q)TC} = V_{OUT(Q)(TA)} - V_{OUT(Q)EXPECTED(TA)} \qquad (5)$$

$\Delta V_{OUT(Q)TC}$ should be calculated using the actual measured values of $\Delta V_{OUT(Q)(TA)}$ and $\Delta V_{OUT(Q)EXPECTED(TA)}$ rather than programming target values.

Sensitivity (Sens)

The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.

Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mv/G), of the device, and it is defined as:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG}, \qquad (6)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

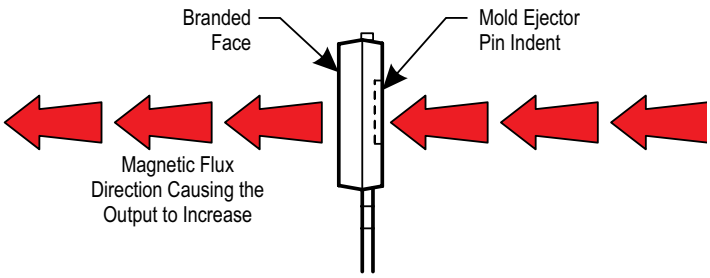


Figure 6: Magnetic Flux Polarity

Initial Unprogrammed Sensitivity ($Sens_{init}$)

Before any programming, Sensitivity has a nominal value that depends on the SENS_COARSE bits setting. Each A1365 variant has a different SENS_COARSE setting.

Sensitivity Programming Range ($Sens_{PR}$)

The magnetic sensitivity (Sens) can be programmed around its initial value within the sensitivity range limits: $Sens_{PR}$(min) and $Sens_{PR}$(max). Exceeding the specified Sensitivity Range will cause Sensitivity Drift Through Temperature Range $\Delta Sens_{TC}$ to deteriorate beyond the specified values. Refer to the Quiescent Voltage Output Range section for a conceptual explanation of how value distributions and ranges are related.

Average Fine Sensitivity Programming Step Size ($Step_{SENS}$)

Refer to the Average Quiescent Voltage Output Programming Step Size section for a conceptual explanation.

Sensitivity Programming Resolution (Err_{PGSENS})

Refer to the Quiescent Voltage Output Programming Resolution section for a conceptual explanation.

Sensitivity Temperature Coefficient (TC_{SENS})

Device sensitivity changes as temperature changes, with respect to its programmed sensitivity temperature coefficient, TC_{SENS}. TC_{SENS} is programmed at 150°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{SENS} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\% \right) \left(\frac{1}{T2 - T1} \right), \qquad (7)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 150°C. The expected value of Sens over the full ambient temperature range, $Sens_{EXPECTED(TA)}$, is defined as:

$$Sens_{EXPECTED(TA)} = Sens_{T1} \times \left[100\% + \frac{TC_{SENS}\,(T_A - T1)}{100} \right] \qquad (8)$$

$Sens_{EXPECTED(TA)}$ should be calculated using the actual measured values of $Sens_{T1}$ rather than programming target values.

Sensitivity Drift Through Temperature Range ($\Delta Sens_{TC}$)

Second-order-sensitivity temperature-coefficient effects cause the magnetic sensitivity, Sens, to drift from its expected value over the operating ambient temperature range (T_A). The Sensitivity Drift Through Temperature Range ($\Delta Sens_{TC}$) is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{TA} - Sens_{EXPECTED(TA)}}{Sens_{EXPECTED(TA)}} \times 100\% \quad . \qquad (9)$$

Sensitivity Drift Due to Package Hysteresis ($\Delta Sens_{PKG}$)

Package stress and relaxation can cause the device sensitivity at $T_A = 25°C$ to change during and after temperature cycling. The sensitivity drift due to package hysteresis ($\Delta Sens_{PKG}$) is defined as:

$$\Delta Sens_{PKG} = \frac{Sens_{(25°C)2} - Sens_{(25°C)1}}{Sens_{(25°C)1}} \times 100\% \quad , \qquad (10)$$

where $Sens_{(25°C)1}$ is the programmed value of sensitivity at $T_A = 25°C$, and $Sens_{(25°C)2}$ is the value of sensitivity at $T_A = 25°C$, after temperature cycling T_A up to 150°C and back to 25°C.

Linearity Sensitivity Error (Lin_{ERR})

The A1365 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error

Linearity error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity Error (%) is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{Sens_{BPOS2}}{Sens_{BPOS1}}\right) \times 100\% \quad ,$$

$$Lin_{ERRNEG} = \left(1 - \frac{Sens_{BNEG2}}{Sens_{BNEG1}}\right) \times 100\% \quad , \qquad (11)$$

where:

$$Sens_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \quad , \qquad (12)$$

and BPOSx and BNEGx are positive and negative magnetic fields, with respect to the quiescent voltage output such that |BPOS2| = 2 × |BPOS1| and |BNEG2| = 2 × |BNEG1|.

Then:

$$Lin_{ERR} = \max(Lin_{ERRPOS}, Lin_{ERRNEG}) \quad . \qquad (13)$$

Symmetry Sensitivity Error (Sym_{ERR})

The magnetic sensitivity of an A1365 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry Error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{BPOS}}{Sens_{BNEG}}\right) \times 100\% \quad , \qquad (14)$$

where $Sens_{Bx}$ is as defined in equation 12, and BPOSx and BNEGx are positive and negative magnetic fields such that |BPOSx| = |BNEGx|.

Ratiometry Error (Rat_{ERR})

The A1365 device features ratiometric output. This means that the Quiescent Voltage Output ($V_{OUT(Q)}$) magnetic sensitivity, Sens, and Output Voltage Clamp ($V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$) are proportional to the Supply Voltage (V_{CC}). In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in Quiescent Voltage Output, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage (V_{CC}) is defined as:

$$Rat_{ERRVOUT(Q)} = \left(1 - \frac{V_{OUT(Q)(VCC)} / V_{OUT(Q)(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \qquad (15)$$

The ratiometric error in magnetic sensitivity, $Rat_{ERRSens}$ (%), for a given Supply Voltage (V_{CC}) is defined as:

$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (16)$$

The ratiometric error in the clamp voltages, Rat_{ERRCLP} (%), for a given supply voltage (V_{CC}) is defined as:

$$Rat_{ERRCLP} = \left(1 - \frac{V_{CLP(VCC)} / V_{CLP(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \ , \qquad (17)$$

where V_{CLP} is either $V_{CLP(HIGH)}$ or $V_{CLP(LOW)}$.

Power-On Reset Voltage (V_{POR})

On power-up, to initialize to a known state and avoid current spikes, the A1365 is held in Reset state. The Reset signal is disabled when V_{CC} reaches V_{UVLOH} and time t_{PORR} has elapsed, allowing the output voltage to go from a high-impedance state into normal operation. During power-down, the Reset signal is enabled when V_{CC} reaches V_{PORL}, causing the output voltage to go into a high-impedance state. (Note that a detailed description of POR and UVLO operation can be found in the Functional Description section).

Power-On Reset Release Time (t_{PORR})

When V_{CC} rises to V_{PORH}, the Power-On Reset Counter starts. The A1365 output voltage will transition from a high-impedance state to normal operation only when the Power-On Reset Counter has reached t_{PORR} and V_{CC} has exceeded V_{UVLOH}.

Undervoltage Lockout Threshold (V_{UVLO})

If V_{CC} drops below V_{UVLOL}, the output voltage will be pulled to GND. If V_{CC} starts rising, the A1365 will come out of this lock state when V_{CC} reaches V_{UVLOH}.

UVLO Enable/Disable Delay Time (t_{UVLO})

When a falling V_{CC} reaches V_{UVLOL}, time t_{UVLOE} is required to engage the Undervoltage Lockout state. When V_{CC} rises above V_{UVLOH}, time t_{UVLOD} is required to disable UVLO and to have a valid output voltage.

Output Saturation Voltage (V_{SAT})

When output voltage clamps are disabled, the output voltage can swing to a maximum of $V_{SAT(HIGH)}$ and to a minimum of $V_{SAT(LOW)}$.

Broken Wire Voltage (V_{BRK})

If the GND pin is disconnected (broken wire event), output voltage will go to $V_{BRK(HIGH)}$ if a load resistor is connected to VCC, or to $V_{BRK(LOW)}$ if a load resistor is connected to GND.

DC Fault Switchpoint Error (Err_{DFS})

The Over Field Fault Switchpoint is user-programmable with a step size of $Step_{FAULT}$. DC Fault Switchpoint Error is a deviation from the user-programmed value that occurs over the operating temperature range.

DC Fault Switchpoint Symmetry Error (Err_{DFSS})

Writing FLT_THRESH bits sets the DC Fault Switchpoint for positive and negative magnetic fields as follows:

Positive Field Fault Switchpoint (V_{FPSP}) = Xpos × V_{CC} and Negative Field Fault Switchpoint (V_{FNSP}) = Xneg × V_{CC} where Xpos + Xneg = 1. For example, programming V_{FPSP} = 0.8 × V_{CC} should automatically set V_{FNSP} = 0.2 × V_{CC}. For a measured V_{FPSP}, the DC Fault Switchpoint Symmetry error is the delta between the expected V_{FNSP} and the measured one.

Transient Fault Response Time (t_{TFR})

The time interval between a) when the input crosses the DC Fault Switchpoint and b) when the $\overline{FAULT}$ pin reaches 20% of its final value.

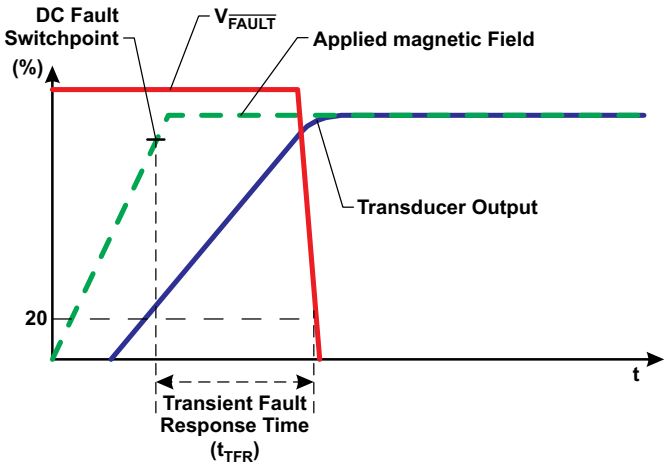


Figure 7: Transient Fault Response Time (t_{TFR})

Transient Fault Release Time (t_{TFRL})

As the Over Field Fault condition goes away, t_{TFRL} is the time interval between a) when the recovering input crosses the DC Fault Switchpoint and when the $\overline{FAULT}$ pin reaches 80% of its final value. Note that the DC Fault Switchpoint will be impacted by the programmed Fault Hysteresis Level (V_{FHSYT}).

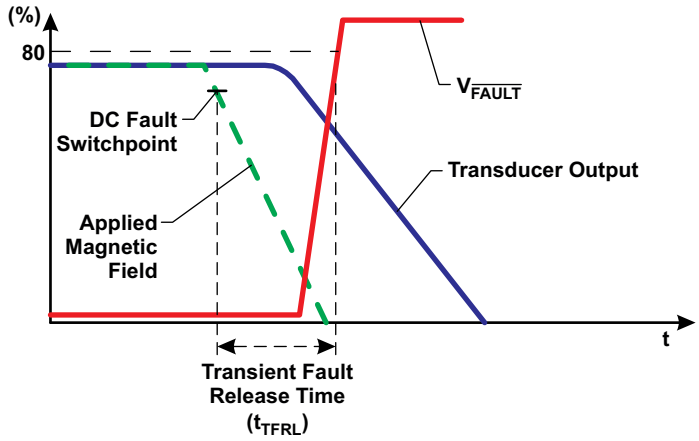


Figure 8: Transient Fault Release Time (t_{TFRL})

FUNCTIONAL DESCRIPTION

Programming Sensitivity and Quiescent Voltage Output

Sensitivity and $V_{OUT(Q)}$ can be adjusted by programming SENS_FINE and QVO bits, as illustrated in Figure 9 and Figure 10.

Users should not program sensitivity or $V_{OUT(Q)}$ beyond the maximum or minimum programming ranges specified in the Operating Characteristics table. Exceeding the specified limits will cause the sensitivity and $V_{OUT(Q)}$ drift over the temperature range ($\Delta Sens_{TC}$ and $\Delta V_{OUT(Q)TC}$) to deteriorate beyond the specified values.

Programming sensitivity might cause a small drift in $V_{OUT(Q)}$. As a result, Allegro recommends programming sensitivity first, then $V_{OUT(Q)}$.

Coarse Sensitivity

Each A1365 variant is programmed to a different coarse sensitivity setting. Devices are tested, and temperature compensation is factory-programmed under that specific coarse sensitivity setting. If the coarse sensitivity setting is changed, by programming SENS_COARSE bits, Allegro cannot guarantee the specified sensitivity drift through temperature range limits ($\Delta Sens_{TC}$).

Memory-Locking Mechanisms

The A1365 is equipped with two distinct memory-locking mechanisms:

- ***Default Lock*** At power-up, all registers of the A1365 are locked by default. EEPROM and volatile memory cannot be read or written. To disable Default Lock, a specific 30-bit customer access code has to be written to address 0x24 within Access Code Timeout (t_{ACC} = 8 ms) from power-up. After doing so, registers can be accessed. If VCC is power-cycled, the Default Lock will automatically be re-enabled. This ensures that during normal operation, memory content will not be altered due to unwanted glitches on VCC or the output pin.
- ***Lock Bit*** After EEPROM has been programmed by the user, the EELOCK bit can be set high and VCC power-cycled to permanently disable the ability to read or write any register. This will prevent the ability to disable Default Lock using the method described above. Note that after the EELOCK bit is set high and the VCC pin is power-cycled, you will not have the ability to clear the EELOCK bit or read/write any register.

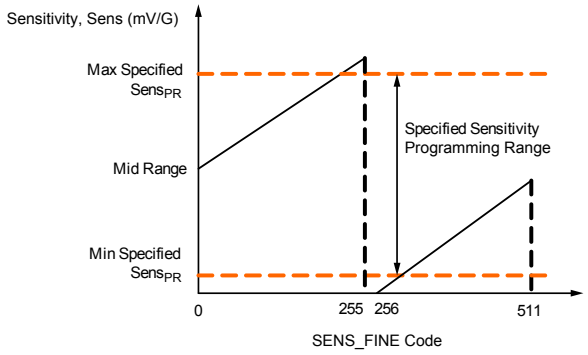


Figure 9: Device Sensitivity versus SENS_FINE Programmed Value

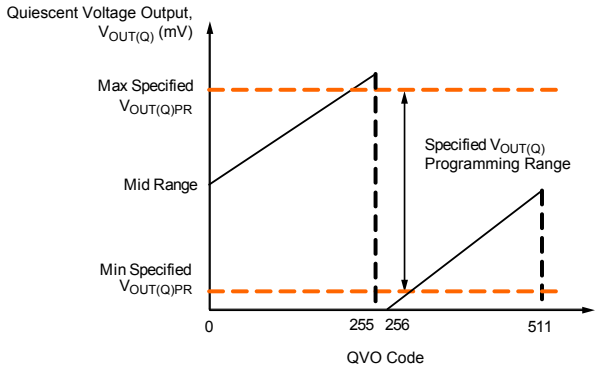


Figure 10: Device $V_{OUT(Q)}$ versus QVO Programmed Value

Power-On Reset (POR) and Undervoltage Lockout (UVLO) Operation

The descriptions in this section assume: $T_A = 25°C$, no output load (R_L, C_L), and no significant magnetic field is present.

- ***Power-Up*** At power-up, as V_{CC} ramps up, the output is in a high-impedance state. When V_{CC} crosses V_{PORH} (location [1] in Figure 11 and [1'] in Figure 12), the POR Release counter starts counting for t_{PORR}. At this point, if V_{CC} exceeds V_{UVLOH} [2'], the output will go to V_{CC} / 2 after t_{UVLOD} [3']. If V_{CC} does not exceed V_{UVLOH} [2], the output will stay in the high-impedance state until V_{CC} reaches V_{UVLOH} [3] and then go to V_{CC} / 2 after t_{UVLOD} [4].
- ***V_{CC} drops below V_{CC}(min)= 4.5 V*** If V_{CC} drops below V_{UVLOL} [4', 5], the UVLO Enable Counter starts counting. If V_{CC} is still below V_{UVLOL} when the counter reaches t_{UVLOE}, the UVLO function will be enabled and the ouput will be pulled near GND [6]. If V_{CC} exceeds V_{UVLOL} before the UVLO Enable Counter reaches 64 µs [5'], the output will continue to be V_{CC}/2.
- ***Coming out of UVLO*** While UVLO is enabled [6], if V_{CC} exceeds V_{UVLOH} [7], UVLO will be disabled after t_{UVLOD}, and the output will be V_{CC} / 2 [8].
- ***Power-Down*** As V_{CC} ramps down below V_{UVLOL} [6', 9], the UVLO Enable Counter will start counting. If V_{CC} is higher than V_{PORL} when the counter reaches t_{UVLOE}, the UVLO function will be enabled and the ouput will be pulled near GND [10]. The output will enter a high-impedance state as V_{CC} goes below V_{PORL} [11]. If V_{CC} falls below V_{PORL} before the UVLO Enable Couner reaches t_{UVLOE}, the output will transition directly into a high-impedance state [7'].

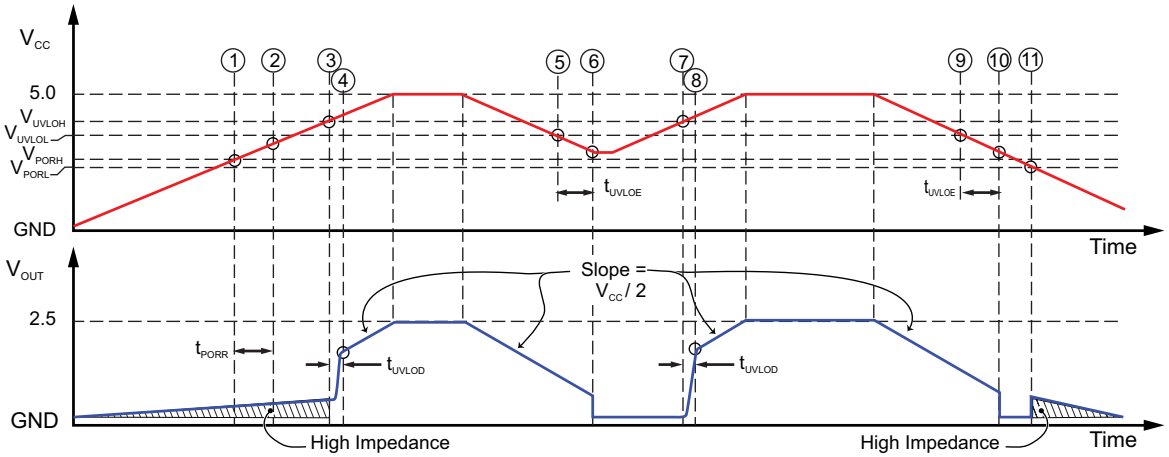


Figure 11: POR and UVLO Operation – Slow Rise Time Case

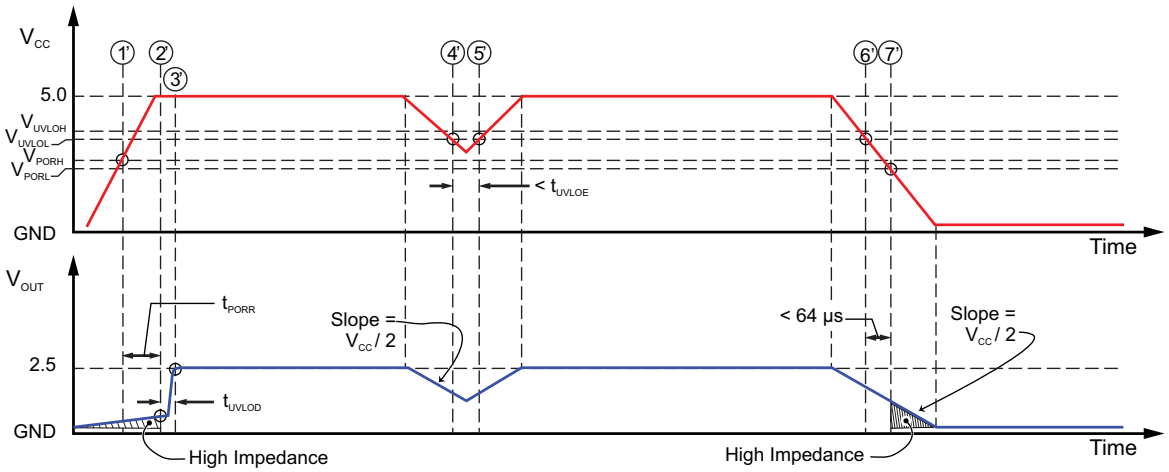


Figure 12: POR and UVLO Operation – Fast Rise Time Case

Detecting Broken Ground Wire

If the GND pin is disconnected, node A becoming open (see Figure 14), the VOUT pin will go to a high-impedance state. The output voltage will go to $V_{BRK(HIGH)}$ if a load resistor $R_{L(PULLUP)}$ is connected to V_{CC} or to $V_{BRK(LOW)}$ if a load resistor $R_{L(PULLDWN)}$ is connected to GND. The device will not respond to any applied magnetic field.

If the ground wire is reconnected, the A1365 will resume normal operation.

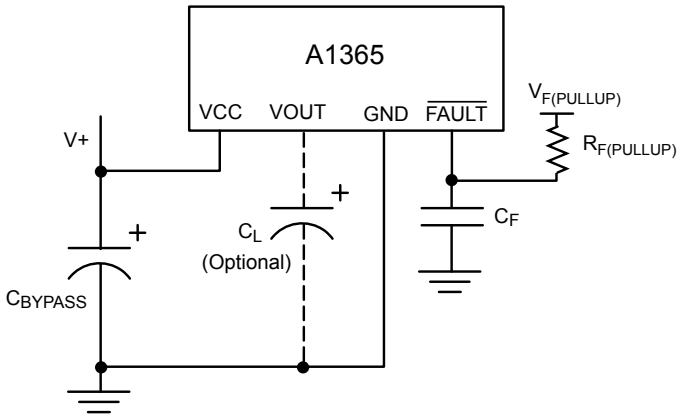


Figure 13: Typical Application Drawing

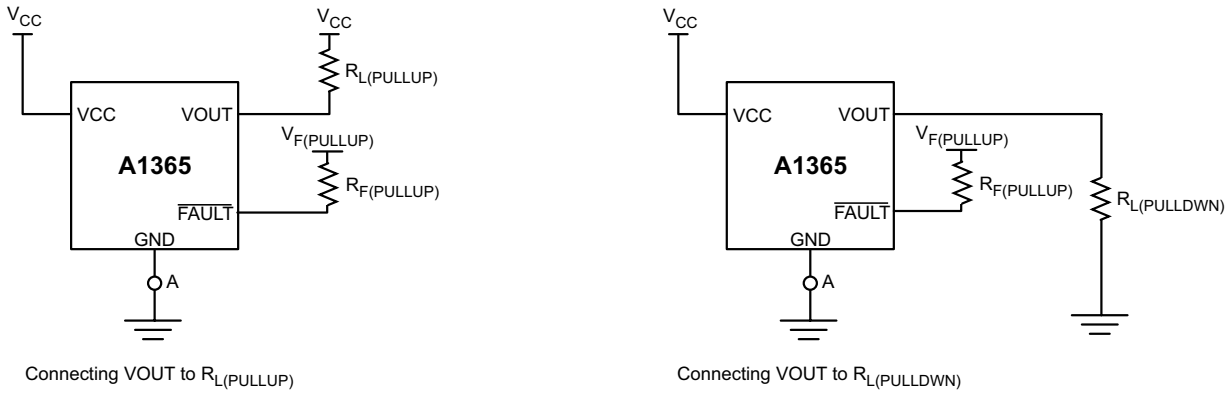


Figure 14: Connections for Detecting Broken Ground Wire

Self-Test Diagnostic Operation after Power-Up

The A1365 has a Self-Test Diagnostics operating mode, allowing the user to verify at any point: connectivity of the Analog Signal path, drifts in sensitivity and quiescent output voltage, and connectivity and functionality of the Over Field Fault Signal path. Timing of various parts of the self-test sequence are user programmable.

Self-Test Start Mode

After power-up is complete, the VOUT pin responds to the applied magnetic field, and the Over Field $\overline{\text{FAULT}}$ pin responds to a magnetic field exceeding the programmed fault threshold. Self-Test Diagnostic mode can be started at any point after power-up by pulling $V_{\overline{\text{FAULT}}}$ below V_{STTH} level (location [1] in Figure 15), causing the sensor IC to enter the Self-Test Start mode and the self-test counter to start. The VOUT pin will continue responding to the magnetic field during this mode, but if the sensor IC is exposed to a magnetic field exceeding the fault threshold, the self-test counter will be reset. After the counter reaches the programmed Self-Test Start Time (t_{STS} [2]), the VOUT pin will go to V_{STL}, indicating that the sensor IC has entered Self-Test Sens mode.

Self-Test Sens Mode

Self-Test Sens mode allows the user to verify the sensitivity of the sensor IC. Setting $V_{\overline{\text{FAULT}}} > V_{STTH}$ [4] causes VOUT to respond by going to V_{STH}, [6]. Setting $V_{\overline{\text{FAULT}}} < V_{STTH}$ [7] causes VOUT to become equal to V_{STL} [9]. By measuring VOUT and comparing it to the specified values, the user can detect failures in the Analog Signal path as well as drifts in sensitivity. Quiescent voltage can be measured during the Self-Test Start waiting period as long as no external magnetic fields are present. When the $V_{\overline{\text{FAULT}}}$ value is changed in either direction [4, 7], Self-Test Sens Output Propagation Delay Time (t_{STSOPD}) is required before a change is observed on VOUT [5, 8]. VOUT will settle to a stable value after Self-Test Sens Output Rise Time (t_{STSORT} [6]) or Self-Test Sens Output Fall Time (t_{STSOFT} [9]). The sensor IC can stay in Self-Test Sens mode as long as required by the user. To exit, the $\overline{\text{FAULT}}$ pin should be released, causing $V_{\overline{\text{FAULT}}}$ to exceed V_{STTH} [10] and to be pulled near V_{CC} by the pull-up resistor. When the programmed Self-Test Fault Request Time (t_{STFR}) expires [11], the device will enter Self-Test Fault mode.

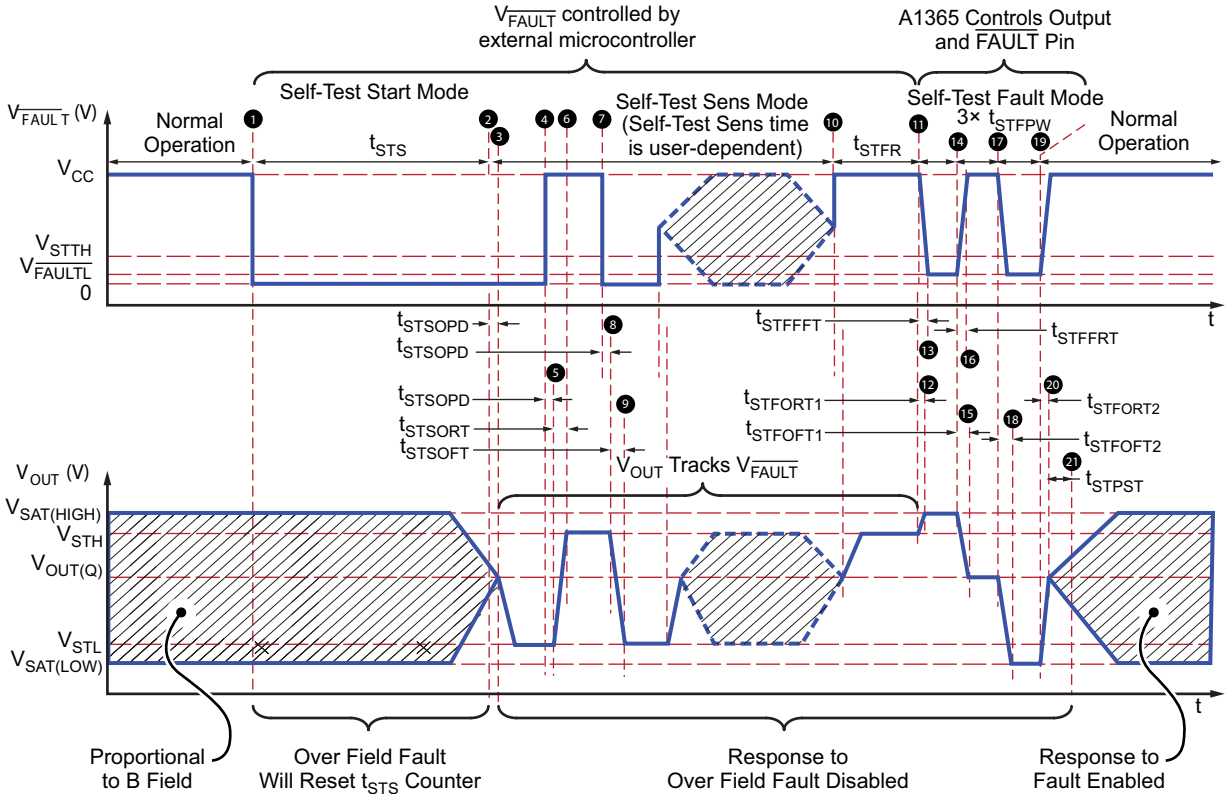


Figure 15: Self-Test Diagnostic Mode Fault Behavior

Self-Test Fault Mode

During Self-Test Fault mode, the $\overline{\text{FAULT}}$ pin should be released by the user. The A1365 will automatically apply an internal positive stimulus to the internal signal path, causing the output to reach $V_{SAT(HIGH)}$ [12]. After V_{OUT} crosses the programmed fault threshold, the $\overline{\text{FAULT}}$ pin will be pulled to $V_{\overline{\text{FAULT}}L}$ [13]. After the programmed Self-Test Fault Pulse Width time (t_{STFPW}) has expired [14], the positive internal stimulus will be removed, causing the output to settle at $V_{OUT(Q)}$ [15], which in turn will cause the $\overline{\text{FAULT}}$ pin to be released and pulled to V_{CC} [16].

After the Self-Test Fault Pulse Width time (t_{STFPW}) has expired [17], a negative internal stimulus will be applied to the signal path, causing the output to reach $V_{SAT(LOW)}$ [18]. After V_{OUT} crosses the programmed fault threshold, the $\overline{\text{FAULT}}$ pin will be pulled to GND. After the Self-Test Fault Pulse Width time (t_{STFPW}) has expired [19], the output will be released and should reach $V_{OUT(Q)}$ in the absence of an external magnetic field [20]. The A1365 will then automatically exit Self-Test mode, release the $\overline{\text{FAULT}}$ pin, and resume normal operation after the Post Self-Test Settling Time (t_{STPST} [21]). The user can determine if the Over Fault Signal path is functional by ensuring the VOUT pin and the $\overline{\text{FAULT}}$ pin toggle as described in Figure 13 and reach the appropriate voltage levels.

Self-Test Operating Conditions

For proper functionality, no magnetic field should be present during any Self-Test mode. If a read/write transaction is received during any Self-Test mode, the sensor IC will exit Self-Test and service the transaction. A Self-Test Start request is ignored during a read/write transaction. If V_{CC} drops below V_{UVLOL}, the sensor IC will exit Self-Test mode.

Table 1: Self-Test Operating Characteristics: Valid through the full operating temperature range T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, and no magnetic field is present, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SELF-TEST START MODE						
Self-Test Start Time [1]	t_{STS}	Programmable	0.05	–	200	ms
Self-Test Threshold Voltage [2]	V_{STTH}		0.85	1	1.15	V
Self-Test Comparator Hysteresis	V_{STHYST}		–	75	–	mV
Self-Test Sens Mode						
Self-Test Sens Output Propagation Delay	t_{STSOPD}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	4	–	µs
Self-Test Sens Output Rise Time	t_{STSORT}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	8	–	µs
Self-Test Sens Output Fall Time	t_{STSOFT}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	8	–	µs
Self-Test Fault Request Time [1]	t_{STFR}	Programmable	0.05	–	10	ms
Self-Test High Output Voltage [2]	V_{STH}		$V_{OUT(Q)}$ + 1.275	$V_{OUT(Q)}$ + 1.5	$V_{OUT(Q)}$ + 1.725	V
Self-Test Low Output Voltage [2]	V_{STL}		$V_{OUT(Q)}$ – 1.725	$V_{OUT(Q)}$ – 1.5	$V_{OUT(Q)}$ – 1.275	V
Ratiometry Self-Test Sensitivity Error	$Rat_{ERRSTSens}$	T_A = 25°C to 150°C relative to V_{CC} = 5 V ±5%	–4	–	4	%
		T_A = –40°C to 25°C relative to V_{CC} = 5 V ±5%	–5	–	5	%
SELF-TEST FAULT MODE						
Self-Test Fault Pulse Width Time [1]	t_{STFPW}	Programmable	0.05	–	10	ms
Self-Test Fault Fall Time	t_{STFFFT}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	0.7	–	µs
Self-Test Fault Rise Time	t_{STFFRT}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	17	–	µs
Self-Test Fault Output Rise Time	$t_{STFORT1}$	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	0.1	–	µs
	$t_{STFORT2}$	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	1	–	µs
Self-Test Fault Output Fall Time	$t_{STFOFT1}$	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	1	–	µs
	$t_{STFOFT2}$	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	1	–	µs
Post Self-Test Settling Time	t_{STPST}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	5	–	µs

[1] Programmed timer could have a typical error of ±5%.
[2] Ratiometric with V_{CC}.

Table 2: Self-Test Timers DAC Profiles

Self-Test Start Time		Self-Test Fault Request Time		Self-Test Fault Pulse Width Time	
4-Bit Code (Decimal Equivalent)	t_{STS} (ms)	3-Bit Code (Decimal Equivalent)	t_{STFR} (ms)	3-Bit Code (Decimal Equivalent)	t_{STFPW} (ms)
0	0.05	0	0.05	0	0.05
1	0.1	1	0.1	1	0.1
2	0.2	2	0.2	2	0.2
3	0.5	3	0.5	3	0.5
4	1	4	1	4	1
5	2	5	2	5	2
6	5	6	5	6	5
7	10	7	10	7	10
8	20				
9	50				
10	100				
11	200				
12	200				
13	200				
14	200				
15	200				