



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

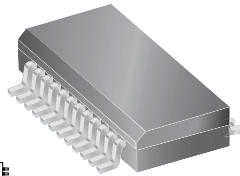


## 12 V High-Side Hot-Swap Hall Effect Based Current Monitor IC

### Features and Benefits

- Hall-effect current monitor—no external sense resistor required
- Analog output voltage (factory trimmed for gain and offset) proportional to applied current
- External high-side FET gate drive
- 240V\*A Power Fault Protection with user-programmable delay
- User programmable Overcurrent Fault Protection with programmable delay
- 1.5 mΩ internal conductor resistance
- Short Circuit Protection isolates failed supply from output in < 2 μs
- Active low Fault indicator output signal
- External FET failure detection with active low S1 Short failure indicator output signal
- User controlled soft start / hot-swap function
- Logic enable input pin
- 10.8 to 13.2 V, single-supply operation
- 2 kV ESD protection for all pins

### Package: 24 pin QSOP (suffix LF)



Approximate Scale 

### Description

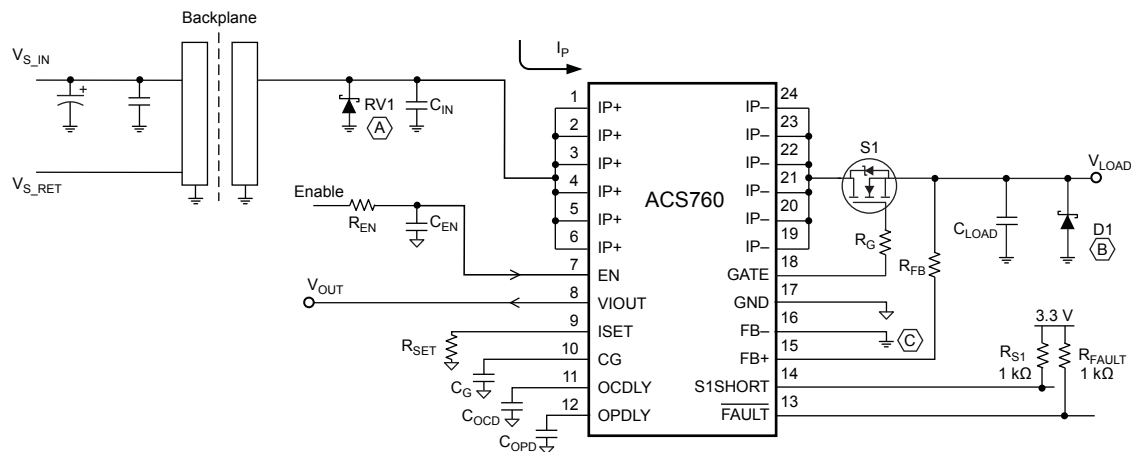
The ACS760 combines Allegro™ Hall-effect current sense technology with a hot-swap controller resulting in a more efficient integrated controller for 12 V applications. By eliminating the need for a shunt resistor, the I<sup>2</sup>R losses in the power path are reduced.

When the ACS760 is externally enabled, and the voltage rail is above the internal UVLO threshold, the internal charge pump drives the gate of the external FET. When a fault is detected, the gate is disabled while simultaneously alerting the application that a fault has occurred.

The integrated protection in the ACS760 incorporates three levels of fault protection, which includes a Power Fault with user-programmable delay, a user-programmable Overcurrent Fault threshold with programmable delay, and Short Circuit protection, which disables the gate in less than 2 μs.

Additionally, in the event the external high-side FET fails short, the ACS760 detects the S1 Short failure and immediately disables the gate and alerts the host system. Unlike the three protection faults, cycling the EN pin does not reset the S1 Short failure. Power to the device must be cycled.

### Typical Application



- (A) RV1 is required only for inductive loads.
- (B) D1 should be a Schottky for inductive loads, to eliminate over-stress of the ACS760.
- (C) FB- is tied to GND at the point of load.

## Selection Guide

Part Number	Package	Packing*
ACS760ELFTR-20B-T	QSOP24 surface mount	2500 pieces/reel

\*Contact Allegro for additional packing options

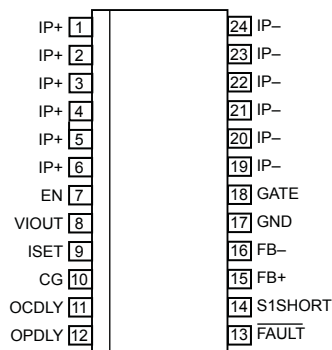
## Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Forward Voltage, IPx pins*	$V_{CC}$		24	V
GATE Drive Output Voltage*	$V_{GATE}$		32	V
FB+ Forward Voltage*	$V_{FB+}$		24	V
EN Forward Voltage*	$V_{EN}$		32	V
All Other Pins Forward Voltage	$V_{IN}$		8	V
Reverse DC Voltage, All Pins*	$V_R$		-0.5	V
Reverse Transient DC Voltage, All Pins*	$V_r$	10 $\mu$ s pulse	-5	V
Current Level Output Current Source	$I_{VIOUT(SOURCE)}$		1	mA
Current Level Output Current Sink	$I_{VIOUT(SINK)}$		1	mA
Operating Ambient Temperature	$T_A$	Range E	-40 to 85	$^{\circ}$ C
Maximum Junction Temperature	$T_J(max)$		165	$^{\circ}$ C
Storage Temperature	$T_{stg}$		-65 to 170	$^{\circ}$ C

\* With respect to GND.



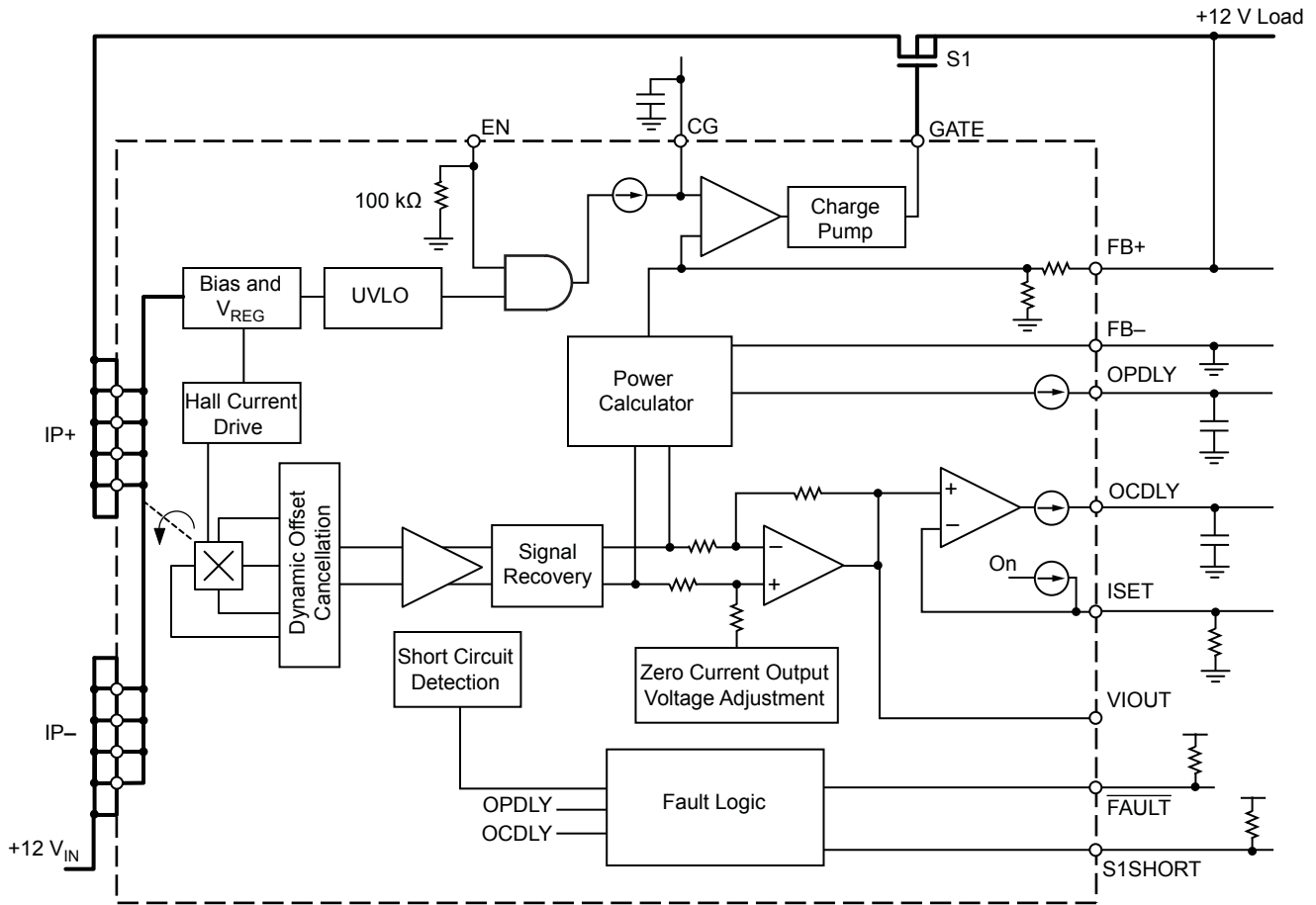
## Pin-out Diagram



## Terminal List Table

Number	Name	Function
1-6	IP+	Primary sampled current conduction path input; power input pins: connected to $V_{CC}$
7	EN	Enable pin. Toggling this pin to the low state after a FAULT condition resets the ACS760.
8	VIOUT	Analog current level output. Output voltage on this pin is proportional to the current flowing from the IP+ pins to the IP- pins.
9	ISET	Terminal for $R_{SET}$ resistor. Sets Fault Current Threshold, $I_{PF}$ , via external resistor, $R_{SET}$ , connected between this terminal and GND. Factory trimmed 100 $\mu A$ current source flows out of this pin.
10	CG	Terminal for $C_G$ capacitor. May be used to adjust the turn-on time and soft start control of an external MOSFET, S1. Voltage on this pin limits inrush current through MOSFET S1. Set via external capacitance, $C_G$ , connected between this pin and GND. This capacitor is charged by an internal 20 $\mu A$ current source.
11	OCDLY	Terminal for external capacitor, $C_{OCD}$ . Used to adjust delay for overcurrent shutdown, set via the external capacitor, $C_{OCD}$ , connected between this pin and GND.
12	OPDLY	Terminal for external capacitor, $C_{OPD}$ . Used to adjust delay for overpower shutdown, set via the external capacitor, $C_{OPD}$ , connected between this pin and GND.
13	FAULT	Active low; output signal for short circuit and 240 V*A overload faults; does not trip for S1 short circuit fault. Connect a 1 k $\Omega$ pull-up resistor between this pin and the 3.3 V rail.
14	S1SHORT	Active low; output signal for MOSFET S1 failure. Connect a 1 k $\Omega$ pull-up resistor between this pin and the 3.3 V rail.
15	FB+	Input of positive feedback on output voltage. Used to determine 240 V*A threshold by difference between FB+ and FB- pins.
16	FB-	Input of negative feedback on output voltage. Used to determine 240 V*A threshold by difference between FB+ and FB- pins. Pulling the FB- pin to 3.3 V, and the OPDLY pin to GND, disables the 240 V*A power fault, which allows the ACS760 to operate purely in Current Mode.
17	GND	Terminal for ground connection.
18	GATE	Terminal for external MOSFET, S1. Provides output voltage to drive S1. Current through S1 is controlled at start-up by external capacitance connected between the CG pin and GND.
19-24	IP-	Primary sampled current conduction path output; power output pins.

Functional Block Diagram



**OPERATING CHARACTERISTICS** valid at  $V_{CC} = 12\text{ V}$ ,  $T_A = 0^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
<b>GENERAL ELECTRICAL CHARACTERISTICS</b>						
Linear Sensing Range	$I_P$	Current flows from IP+ to IP- pins	0	–	55	A
Primary Conductor Resistance	$R_{PRIMARY}$	$T_A = 25^\circ\text{C}$	–	1.5	–	m $\Omega$
Supply Voltage	$V_{CC}$	Voltage applied to IP+ pins	–	12	–	V
Supply Current	$I_{CC}$		–	10	12	mA
Undervoltage Lockout (UVLO)	$V_{UVLOH}$	$V_{CC}$ rising and CG pin current source turns on, EN pin = high	–	–	10.5	V
	$V_{UVLOL}$	$V_{CC}$ falling and CG pin current source turns off, EN pin = high	7.1	–	–	V
UVLO Delay to Chip Enable/ Disable	$t_{UVLOE}$	Enabling, measured from rising $V_{CC} > V_{UVLOH}$ to $V_{GATE} > 1\text{ V}$	–	500	900	$\mu\text{s}$
	$t_{UVLOD}$	Disabling, from falling $V_{CC} < V_{UVLOL}$ to $V_{GATE} < 1\text{ V}$	–	–	2	$\mu\text{s}$
FB+ to FB– Input Resistance	$R_{FB}$	$T_A = 25^\circ\text{C}$	–	240	–	k $\Omega$
<b>CURRENT SENSE PERFORMANCE CHARACTERISTICS</b>						
VIOUT Analog Output Propagation Time	$t_{PROP}$	$T_A = 25^\circ\text{C}$ , $I_P = 0 \rightarrow 20\text{ A}$ , capacitance from VIOUT to GND = 100 pF	–	2	–	$\mu\text{s}$
VIOUT Analog Output 10-90% Rise Time	$t_r$	$T_A = 25^\circ\text{C}$ , $I_P = 0 \rightarrow 20\text{ A}$ , capacitance from VIOUT to GND = 100 pF	–	5	–	$\mu\text{s}$
VIOUT Analog Signal Bandwidth <sup>1</sup>	$f_{3dB}$	–3 dB, $I_P = 10\text{ A}$ peak-to-peak, $T_A = 25^\circ\text{C}$ , no external device filter, capacitance from VIOUT to GND = 100 pF	–	50	–	kHz
VIOUT Analog Signal Sensitivity	Sens	$T_A = 25^\circ\text{C}$	–	65	–	mV/A
		Over full ambient operating temperature range	61.5	–	67.5	mV/A
		$T_A = 25^\circ\text{C}$	–	5.416	–	mV/G
		Over full ambient operating temperature range	5.275	–	5.558	mV/G
Sensitivity Slope Over Temperature	$\Delta\text{Sens}_{TA}$	$T_A = 0^\circ\text{C}$ to $25^\circ\text{C}$	–	0.042	–	mV/A/ $^\circ\text{C}$
		$T_A = 25^\circ\text{C}$ to $85^\circ\text{C}$	–	0.027	–	mV/A/ $^\circ\text{C}$
VIOUT Analog Noise Level	$V_{NOISE(PP)}$	Mean peak-to-peak, $T_A = 25^\circ\text{C}$ , 50 kHz external device filter	–	20	–	mV
VIOUT Analog Nonlinearity	$E_{LIN}$	Over full ambient operating temperature range and linear sensing range	–	$\pm 0.5$	$\pm 2.0$	%
Zero Current Output Voltage	$V_{IOUT(Q)}$	$T_A = 0^\circ\text{C}$ to $55^\circ\text{C}$	0.38	–	0.42	V
		$T_A = 0^\circ\text{C}$ to $85^\circ\text{C}$	0.37	0.4	0.43	V
Zero Current Output Slope Over Temperature	$\Delta I_{OUT(Q)TA}$	$T_A = 0^\circ\text{C}$ to $25^\circ\text{C}$	–	–0.148	–	mV/ $^\circ\text{C}$
		$T_A = 25^\circ\text{C}$ to $85^\circ\text{C}$	–	–0.057	–	mV/ $^\circ\text{C}$
Output Voltage Saturation Limits <sup>2</sup>	$V_{OL}$	$T_A = 25^\circ\text{C}$	–	0.25	–	V
	$V_{OH}$	$T_A = 25^\circ\text{C}$	–	3.6	–	V
VIOUT Total Error % of $I_P$	$E_{TOT}$	$T_A = 25^\circ\text{C}$ , $I_P = 20\text{ A}$	–	$\pm 1.0$	–	%
		$T_A = 0^\circ\text{C}$ to $85^\circ\text{C}$ , $I_P = 20\text{ A}$	–	–	$\pm 3.5$	%
VIOUT DC Output Resistance	$R_{VIOUT}$	$I_{VIOUT} = 1\text{ mA}$	–	1	–	$\Omega$
<b>CURRENT FAULT PERFORMANCE CHARACTERISTICS</b>						
Load Power Fault Threshold	$P_{F(th)}$		222	230	238	W
240 V*A Fault Signal Delay	$t_{PFH}$	$T_A = 25^\circ\text{C}$ , measured from FAULT signal to $V_{GATE} < 1\text{ V}$ , 2.2 $\mu\text{F}$ capacitance from OPDLY pin to GND, load step from 17 A to 23 A in 100 ns	–	425	–	ms
	$t_{PFL}$	$T_A = 25^\circ\text{C}$ , measured from FAULT signal to $V_{GATE} < 1\text{ V}$ , OPDLY pin open, load step from 17 A to 23 A in 100 ns	–	10	12	$\mu\text{s}$
240 V*A Fault Signal Delay Drift	$\Delta t_{PF}$	Over full operating ambient temperature range, external capacitor with $\pm 5\%$ tolerance	–15	–	15	%
Internal –3 dB Filter Frequency for FB+ and FB– Pins	$f_{FBFILT}$	$T_A = 25^\circ\text{C}$	–	50	–	kHz

Continued on the next page...

**OPERATING CHARACTERISTICS, (continued)** Valid at  $V_{CC} = 12\text{ V}$ ,  $T_A = 0^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
$I_P$ Fault Switchpoint Tolerance <sup>3</sup>	$E_{PF}$	Percentage error of $I_{PF}$	-15	-	15	%
$I_{PF}$ Fault Signal Delay <sup>4</sup>	$t_{IPFLmax}$	Measured from FAULT signal to $V_{GATE} < 1\text{ V}$ , OCDLY pin open, load step from 17 A to 45 A in 100 ns	-	8	12	$\mu\text{s}$
	$t_{IPFH}$	Measured from FAULT signal to $V_{GATE} < 1\text{ V}$ , 2.2 nF capacitance from OCDLY pin to GND, load step from 17 A to 45 A in 100 ns	-	425	-	$\mu\text{s}$
Maximum Short Circuit/Overcurrent Fault Threshold <sup>5</sup>	$I_{SC}$		60	110	160	A
Short Circuit/Overcurrent Fault Gate Delay	$t_{SC}$	Measured from FAULT signal to $V_{GATE} < 1\text{ V}$ , Includes $t_{GF}$	-	2	3	$\mu\text{s}$
<b>VOLTAGE FAULT PERFORMANCE CHARACTERISTICS</b>						
Internal Pull Down Resistance Between EN and GND	$R_{EN}$	$T_A = 25^\circ\text{C}$	-	100	-	k $\Omega$
EN Voltage Threshold <sup>6</sup>	$V_{ENH}$	IC enabled when $V_{EN} > V_{ENH}$	1.93	-	-	V
	$V_{ENL}$	IC disabled when $V_{EN} < V_{ENL}$	-	-	1	V
S1 Short Circuit Detection Current <sup>7</sup>	$I_{S1S}$	IC enabled or disabled	0.9	1.5	2.1	A
S1 Short Circuit Detection Delay	$t_{S1S}$	Measured from disablement of the device to detection of an S1 fault	-	-	45	$\mu\text{s}$
S1SHORT Output Voltage	$V_{S1SOL}$	$I_{S1SHORT} = 3\text{ mA}$ sink current	-	-	0.4	V
S1SHORT Output Leakage Current	$I_{S1SIH}$	$V_{S1SHORT} = 3.3\text{ V}$	-	-	5	$\mu\text{A}$
FAULT Output Voltage	$V_{FAULTOL}$	$I_{FAULT} = 3\text{ mA}$ sink current	-	-	0.4	V
FAULT Output Leakage Current	$I_{FAULTIH}$	$V_{FAULT} = 3.3\text{ V}$	-	-	5	$\mu\text{A}$
<b>GATE DRIVE PERFORMANCE CHARACTERISTICS</b>						
Internal Charge Pump Voltage	$V_{CP}$	$T_A = 25^\circ\text{C}$	-	$V_{CC} + 10$	-	V
Average GATE Drive Current	$I_{GD}$	$V_{CC} = 12\text{ V}$ , $T_A = 25^\circ\text{C}$	25	50	-	$\mu\text{A}$
Charge Pump Switching Frequency	$f_{CP}$	$T_A = 25^\circ\text{C}$	-	1	-	MHz
GATE Rise Time	$t_{GR}$	$T_A = 25^\circ\text{C}$ , external MOSFET S1 gate capacitance = 5.8 nF, measured from $V_{GATE} = 0\text{ V}$ to 15 V, CG pin open, no output load capacitance	-	1	-	ms
		$T_A = 25^\circ\text{C}$ , external MOSFET S1 gate capacitance = 5.8 nF, measured from $V_{GATE} = 0\text{ V}$ to 15 V, 3.75 $\mu\text{F}$ capacitor connected between CG and GND pins	-	500	-	ms
GATE Sink Resistance	$R_{GSink}$		-	20	30	$\Omega$
GATE Discharge Current	$I_{GD}$	$V_{GATE} = V_{CC} + 10\text{ V}$	-	1000	-	mA
GATE Shutdown Delay	$t_{GSD}$	Measured from fault event to start of GATE pull down	-	200	-	ns
GATE Maximum Fall Time	$t_{GF}$	Measured from $V_{GATE} = 90\%$ of maximum to $V_{GATE} < 1\text{ V}$ , external MOSFET S1 gate capacitance = 5.8 nF. EN pin switched from high to low, FAULT or S1SHORT signal	-	800	-	ns
CG Output Current	$I_{SLEW}$	$T_A = 25^\circ\text{C}$	18	20	22	$\mu\text{A}$

<sup>1</sup>The small signal, AC bandwidth of this device is approximately 90 kHz.

<sup>2</sup>This test requires currents sufficient to swing the output driver between the fully off state and the saturated state. Assumes that the VIOUT pin is connected to an analog-to-digital converter that saturates at 2.5 V. The VIOUT signal is linear above 2.5 V, however, this test is NOT intended to indicate a range of linear operation.

<sup>3</sup>Assumes that a 1% resistor with a flat temperature coefficient is connected between the ISET and GND pins.

<sup>4</sup>Can exceed  $t_{IPFH(max)}$  delay period via the use of a larger external capacitor. Voltage trip point on the high side of the capacitor is 3.85 V.

<sup>5</sup>This parameter is internally programmed and cannot be controlled by the end user.

<sup>6</sup>The FAULT output signal is latched. After a latched fault event, the device will be reset only when either: (a)  $V_{EN}$  drops below  $V_{ENL}$ , or (b) the power to the device (applied to the IP+ pins) is toggled off and then back on.

<sup>7</sup>The voltage on the gate of the external MOSFET S1 does not need to be  $< 1\text{ V}$  in order for the device to detect an S1 short circuit condition. The device does detect a faulty S1 when the gate of S1 is shorted to the S1 source or drain terminal.

### Soft Start and Fault Characteristics

**Gate turn on rise time,  $t_{GR}$ .** Set by external capacitance,  $C_G$ , on the CG pin, such that  $C_G = 7.5 \times t_{GR}$ , where  $C_G$  is in  $\mu\text{F}$  and  $t_{GR}$  is rise time in seconds. For example, a 3.9  $\mu\text{F}$  capacitor connected from the CG pin to GND (without an output load) will yield a rise time of approximately 500 ms:  $C_G \cong 7.5 \times 0.5 \text{ s} = 3.75 \mu\text{F}$ ,  $\cong 3.9 \mu\text{F}$  (a common capacitor value).

When the CG pin is kept open, the ACS760 has a minimum  $t_{GR}$  of 1 ms typical.

**$I_{PF}$  fault signal delay,  $t_{IPF}$ .** This is the delay from high current level fault sense to the start of turn-off of the external MOSFET S1 turn-off. Set by external capacitance,  $C_{OCD}$ , on the OCDLY pin, such that  $C_{OCD} = 5.17 \times t_{OCD}$ ; where  $C_{OCD}$  is in  $\mu\text{F}$  and  $t_{OCD}$  is rise time in seconds.

When the OCDLY pin is kept open, the IC has a minimum fault delay,  $t_{IPFL_{max}}$ , of 8  $\mu\text{s}$  maximum.

**Load power fault signal delay,  $t_{PFL}$ .** This is the delay from maximum power level fault,  $P_{F(th)}$ , sense to the start of external MOSFET S1 turn-off. Set by external capacitance,  $C_{OPD}$ , on the OPDLY pin, such that  $C_{OPD} = 5.17 \times t_{OPD}$ ; where  $C_{OPD}$  is in  $\mu\text{F}$  and  $t_{OPD}$  is rise time in seconds.

The IC has a minimum fault delay when the OPDLY pin kept open of 10  $\mu\text{s}$  typical.

**$I_{PF}$  fault current setting,  $I_{PF}$ .** The  $I_{PF}$  upper trip level may be set by using a resistor between the ISET pin and GND, such that  $R_{SET} = 10^4 (0.4 + 0.065 \times I_{PF})$ , where  $I_{PF}$  is in A and  $R_{SET}$  in  $\Omega$ .

### Accuracy Characteristics

**Sensitivity, Sens.** The change in device output in response to a 1 A change through the primary conductor. Sens is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is trimmed at Allegro final test to optimize the sensitivity (mV/A) for the full-scale current range of the device.

**Noise,  $V_{NOISE(PP)}$ .** The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall effect linear IC. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

**Nonlinearity,  $E_{LIN}$ .** The linearity of the  $V_{IOUT}$  signal is the degree to which the voltage output from the device varies in direct proportion to the primary sensed current, up to 20 A. Nonlinearity reveals the maximum deviation in the slope of the device transfer function compared to the slope of the ideal transfer curve for this transducer. The following equation is used to derive the linearity:

$$100 \left\{ 1 - \left[ \frac{(V_{IOUT\_full\text{-}scale\text{ amperes}} - V_{IOUT(Q)})}{2(V_{IOUT\_half\text{-}scale\text{ amperes}} - V_{IOUT(Q)})} \right] \right\},$$

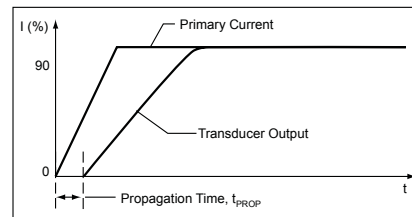
where full-scale current is 20 A, and half-scale current is 10 A.

**Zero Current Output Voltage,  $V_{IOUT(Q)}$ .** The output of the device when the primary current,  $I_p$ , is 0 A. Variation in  $V_{IOUT(Q)}$  can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

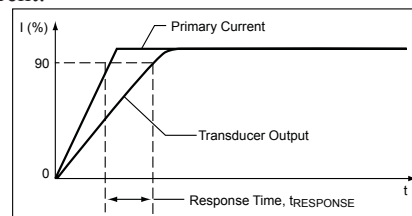
**$V_{IOUT}$  Total Error,  $E_{TOT}$ .** The maximum percentage deviation of the actual output from its ideal value, based on an ideal sensitivity of 65.7 mV/A at 25°C and 64.3 mV/A at 85°C.

### Dynamic Response Characteristics

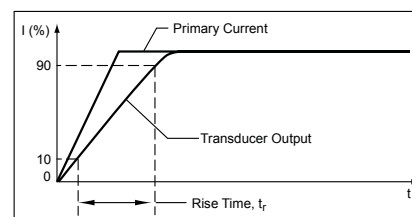
**Propagation delay,  $t_{PROP}$ .** The time required for the device output to reflect a change in the primary current signal. Propagation delay is attributed to inductive loading within the linear IC package, as well as in the inductive loop formed by the primary conductor geometry. Propagation delay can be considered as a fixed time offset and may be compensated.



**Response time,  $t_{RESPONSE}$ .** The time interval between a) when the primary current signal reaches 90% of its final value, and b) when the device reaches 90% of its output corresponding to the applied current.



**Rise time ( $t_r$ ).** The time interval between a) when the device reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the device, in which  $f(-3 \text{ dB}) = 0.35/t_r$ . Both  $t_r$  and  $t_{RESPONSE}$  are detrimentally affected by eddy current losses observed in the conductive IC ground plane.





**240 V\*A Fault Operation**

The timing diagram in figure 1 shows characteristic operation of the ACS760 when the power consumed from the 12 V system bus exceeds a 240 V\*A or 240 W level. The system power supply bus reaches the nominal steady state level of 12 V before the EN pin (Enable pin, active high) of the ACS760 transitions to the high state at time  $t_{EN1}$ . Note that, when the EN pin is in the low state, the GATE pin is actively pulled low. However, as shown in the timing diagram, the voltage on the GATE pin increases with a positive slope after the EN pin transitions to the high state. The ramp rate of the GATE pin is controlled by the value of the capacitor connected to the CG pin.

At a certain GATE voltage, current begins to flow through the external protection MOSFET, S1, and this current increases as the GATE voltage increases. The voltage at the VIOUT pin, which is the current device output voltage of the ACS760, proportionally tracks the current that flows through the MOSFET.

In the timing diagram, the system is in normal, steady state operation up until the time  $t_{INIT\_F}$ . At  $t_{INIT\_F}$ , the current load on the 12 V power supply increases from 19.2 to 22 A and the ACS760 internally registers a 240 V\*A fault condition. At this time, the

voltage on the OPDLY pin increases with a constant slope. (This slope is controlled by the value of the capacitor connected to the OPDLY pin). This voltage continues to increase with a constant slope until either:

- The OPDLY pin voltage reaches a threshold of 3.85 V (if this occurs, the FAULT signal is latched in the low state), or
- The power consumption of the system falls below 240 V\*A (at which time the OPDLY pin voltage is pulled to ground)

A 240 V\*A fault event is detected at  $t_{240VA\_F}$ . At this time, the FAULT signal transitions to the low state and the GATE pin is pulled to ground. The FAULT signal is latched and the chip will pull down the GATE voltage until the EN pin of the ACS760 transitions to the low state and then back to the high state. As shown in the timing diagram, certain ACS760 signals (the FAULT signal and the OPDLY pin voltage) are reset when the EN pin transitions to the low state. These signals are reset in order to guarantee normal device operation (soft start and fault monitoring) when the EN signal transitions back to the high state.

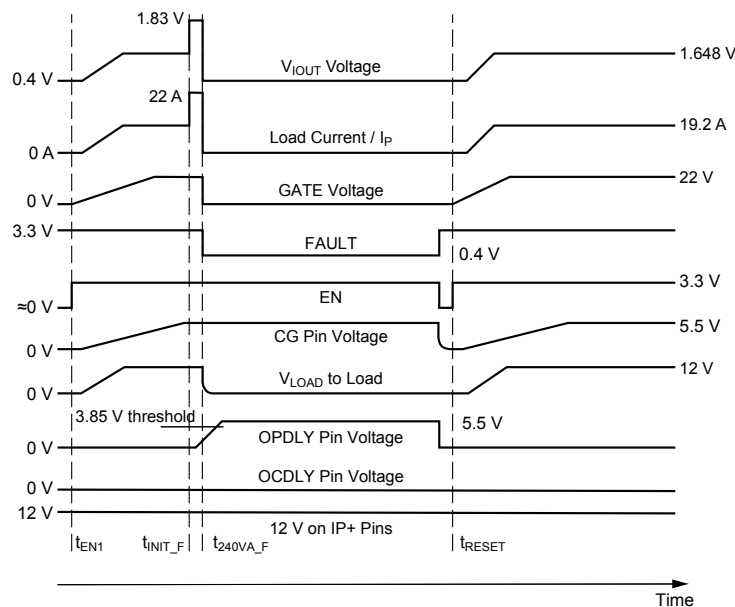


Figure 1. Timing Diagram for 240 V\*A Fault

**Soft Short Circuit Fault Operation**

The timing diagram in figure 2 shows the characteristic operation of the ACS760 when the current load on the 12 V system bus jumps from the 19 to 20 A level to the 40 A level. The 40 A load is typically indicative of a soft short circuit on the I<sub>LOAD</sub> side of the external MOSFET.

In figure 2, the system power supply bus reaches the nominal steady state level of 12 V before the EN pin (Enable pin, active high) of the ACS760 transitions to the high state at time t<sub>EN1</sub>. Note that when the EN pin is in the low state, the GATE pin is actively pulled low. However, as shown in the timing diagram, the voltage on the GATE pin increases with a positive slope after the EN pin transitions to the high state. The ramp rate of the GATE pin is controlled by the value of the capacitor connected to the CG pin.

At a certain GATE voltage, current begins to flow through the external protection MOSFET, S1, and this current increases as the GATE voltage increases. The voltage at the V<sub>IOUT</sub> pin, which is the current device output voltage of the ACS760, proportionally tracks the current that flows through the MOSFET.

In the timing diagram the system is in normal, steady state operation up until the time t<sub>INIT\_F</sub>. At t<sub>INIT\_F</sub> the current load on the 12 V power supply increases from 19.2 A to 40 A and the ACS760 internally registers both a 240 V\*A fault condition and an I<sub>PF</sub> fault condition. In this example, the I<sub>SET</sub> voltage was set at 3.0 V, which corresponds to a 40 A fault threshold. At t<sub>INIT\_F</sub>,

the voltage on the OPDLY and OCDLY pins increases with a constant slope. The slope of the voltage on the two delay pins is controlled by the value of the capacitor connected to each pin. In this case the capacitor on the OCDLY pin is smaller than the capacitor on the OPDLY pin and the voltage on the OCDLY pin ramps much faster than the voltage on the OPDLY pin (both pins are connected to separate 20 μA current sources). The voltages on each delay pin continues to increase with a constant slope until either:

- Either the OPDLY or the OCDLY pin voltages reach a threshold of 3.85 V (if this occurs, the FAULT signal is latched in the low state), or
- The current load of the system falls below 20 A for the OPDLY pin and 40 A for the OCDLY pin

In figure 2 a short circuit fault event is detected at t<sub>40A\_F</sub>. At this time, the FAULT signal transitions to the low state and the GATE pin is pulled to ground. The FAULT state is latched and the chip will pull down the GATE voltage until the EN pin of the ACS760 transitions to the low state and then back to the high state. As shown in the timing diagram, certain ACS760 signals (the FAULT signal and the OCDLY pin voltage) are reset when the EN pin transitions to the low state. These signals are reset in order to guarantee normal device operation (soft start and fault monitoring) when the EN signal transitions back to the high state.

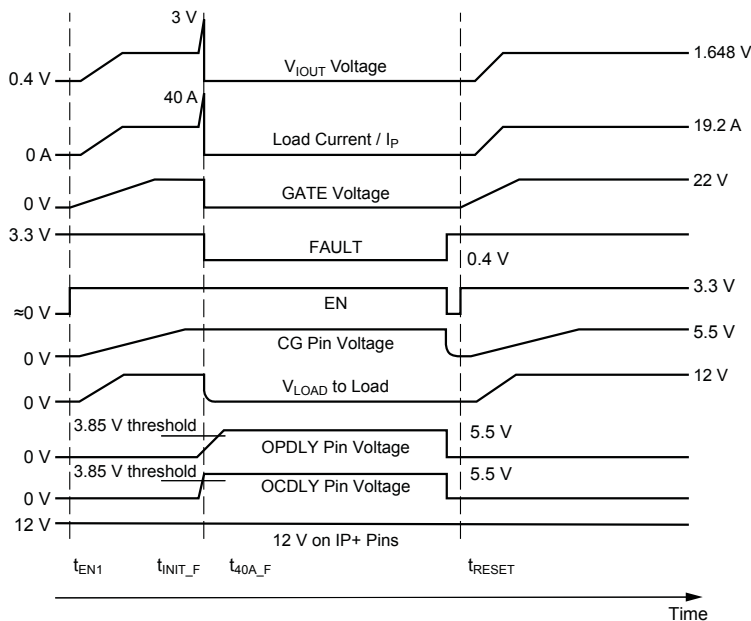


Figure 2. Timing Diagram for 30 to 40 A Load Fault

**Hard Short Circuit (50 mΩ from V<sub>LOAD</sub> to GND)  
Fault Operation**

The timing diagram below specifically shows characteristic operation of the ACS760 when the device is powered on (via the EN pin) and a 50 mΩ short circuit is present from load side of the external MOSFET, S1, to ground.

In figure 3 the system power supply bus reaches the nominal steady state level of 12 V before the EN pin of the ACS760 transitions to the high state at time t<sub>EN1</sub>. The voltage on the GATE pin increases with a positive slope after the EN pin transitions to the high state. The ramp rate of the GATE pin is controlled by the value of the capacitor connected to the CG pin. In the example shown below a small capacitor is connected to the CG pin and the pin ramps to 5.5 V in < 10 μs.

In panel A of figure 3, the device is enabled into a 50 mΩ short circuit. Therefore, as the GATE voltage increases the current through the external MOSFET increases at a rapid rate. In this example case it is assumed that there is no capacitor on the OCDLY pin. When the current through the MOSFET exceeds the threshold set by the R<sub>SET</sub> resistor, the voltage on the OCDLY pin rises quickly beginning at t<sub>40A\_F</sub>. As the voltage on the OCDLY pin rises, so does the voltage on the CG pin and the current through the external MOSFET. If there is no capacitor on the OCDLY pin, and if the ACS760 Short Circuit Fault Threshold,

I<sub>SC</sub>, is greater than 100 A, then the OCDLY pin will reach the 3.85 V threshold before the current through the external MOSFET exceeds I<sub>SC</sub>. This is the case depicted in the panel A. The fault event is detected at t<sub>GATE\_LOW</sub>. At this time, the FAULT signal transitions to the low state and the GATE pin is pulled to ground.

In the event that a large capacitor is connected to the OCDLY pin, the ACS760 will not pull down the gate of the external MOSFET until the current flowing through the MOSFET exceeds I<sub>SC</sub> (shown in panel B, under the assumption that I<sub>SC</sub> equals 130 A). The device pulls down the MOSFET GATE approximately 2 μs after the load current exceeds this threshold. If a large capacitor is connected to the OCDLY pin a significant current (> 40 A but < 160 A) may flow through the MOSFET for tens of microseconds before the Short Circuit Fault Threshold trips. These tens of microseconds elapse as the GATE charges and the load current increases, finally exceeding the short circuit threshold.

The FAULT signal is latched and the chip will pull down the GATE voltage until the EN pin of the ACS760 transitions to the low state and then back to the high state. Certain ACS760 signals (soft start and fault monitoring) are reset when the EN pin transitions to the low state. These signals are reset in order to guarantee normal device operation when the EN signal transitions to the high state.

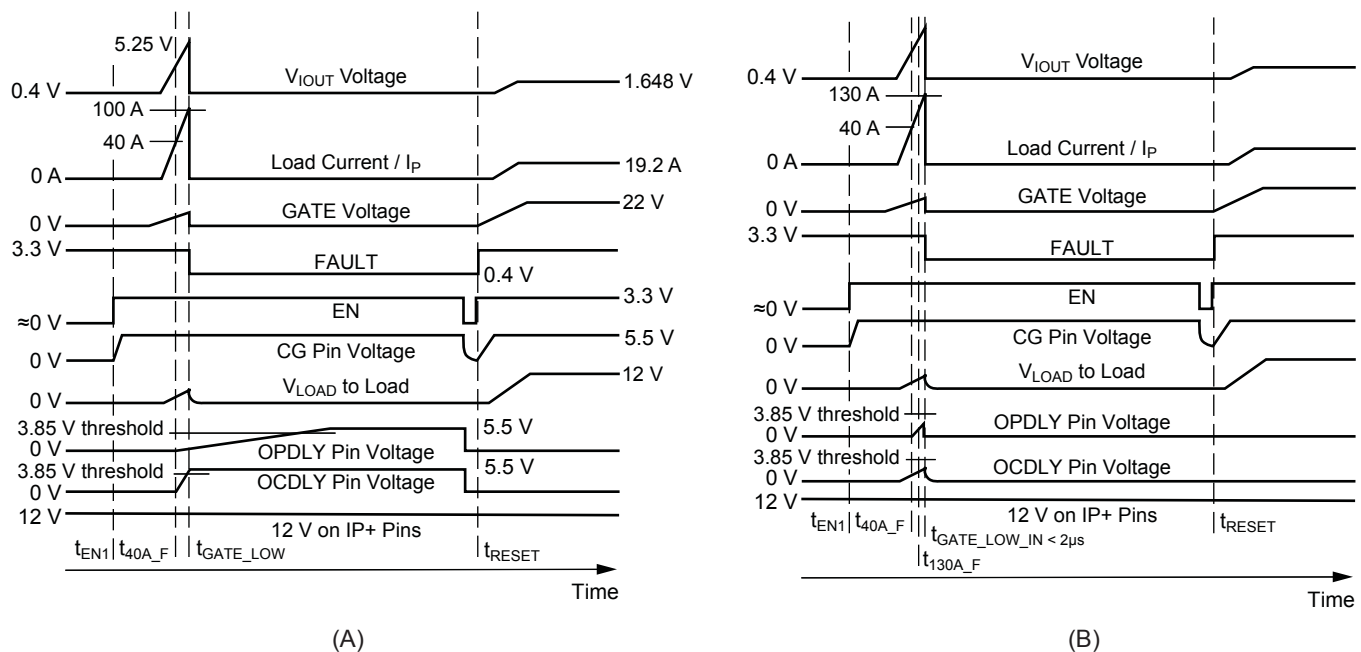


Figure 3. (A) Timing Diagram for a 50 mΩ Short Circuit from V<sub>LOAD</sub> to GND; (B) Timing Diagram for a 50 mΩ Short Circuit from V<sub>LOAD</sub> to GND, capacitor C<sub>OCD</sub> with high rating connected.

**S1 Short Fault Operation**

The timing diagram in figure 4 shows the characteristic operation of the ACS760 when the power consumed from the 12 V system bus exceeds a 240 V\*A or 240 W level. For the operation during a 240 V\*A fault condition, refer to figure 1. That section describes the operation of the ACS760 until the time  $t_{240VA\_F}$ . Figure 4 depicts a 240 V\*A fault, but continues on to demonstrate the ability of the ACS760 to detect damage and improper operation of the external MOSFET in an S1 short circuit event.

At  $t_{240VA\_F}$  the FAULT signal transitions to the low state and the ACS760 pulls down the voltage on the GATE pin. During normal

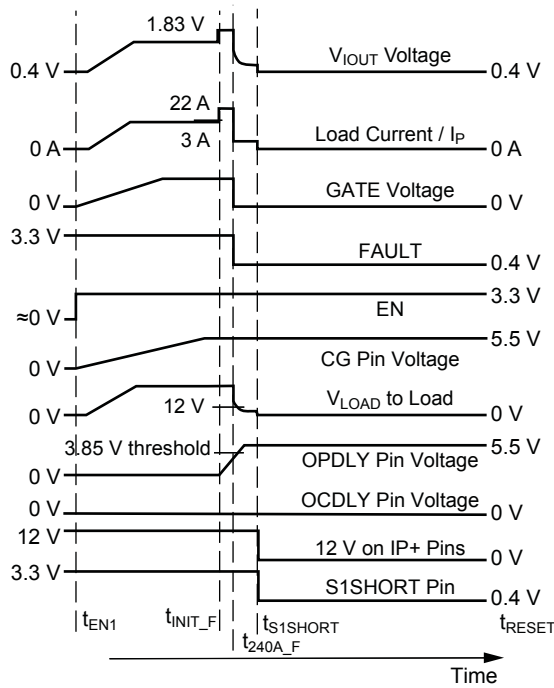


Figure 4. Timing Diagram for S1 Short

operation, when the GATE pin is at 0 V, the current through the S1 MOSFET (and therefore through the ACS760) equals approximately 0 A. However, in the case depicted in figure 4, current through the S1 MOSFET flows even though the GATE pin is pulled low. If a FAULT has occurred and more than 2.1 A flow through the ACS760, then the S1SHORT signal transitions to the low state. When the S1SHORT signal is low, that indicates to the system that the ACS760 cannot turn off the external MOSFET (for example, when a short circuit exists between the source and the drain of the MOSFET). In the case depicted, the system shuts down the 12 V power supply after the S1SHORT signal transitions to the low state.

Note that, in some cases, the GATE of the S1 MOSFET may be shorted to the source or drain of the MOSFET. In this case the ACS760 may not be able to pull down the gate of the S1 MOSFET. However, in this case the ACS760 will still register an S1 Short even if the gate potential is equal to or greater than 12 V.

If the ACS760 is disabled (EN pin in the low state) and greater than 2.1 A flows through the ACS760, then the device will register an S1 Short condition and the S1SHORT pin will transition to the low state. The voltage on the GATE pin is not used as a determining factor when sensing an S1 Short condition.

The S1SHORT signal will not reset to a high state until power to the device is cycled. Toggling the EN pin does not reset the latched S1 Short state.

**Determining the Root Cause of an ACS760 Fault Event**

The following truth table provides system debugging information in the event of a fault event during use of the ACS760. Note that for all of the fault conditions listed, it is possible to monitor the voltages of various ACS760 output pins and determine the cause of the ACS760 FAULT event.

**Fault Condition Truth Table**

Pin Logic State			Probable Root Cause
FAULT Pin	OPDLY Pin	OCDLY Pin	
Low	High	Low	240 V*A system power level, $P_{F(th)}$ , exceeded
Low	Don't Care	High	$I_P$ Fault Current Threshold, $I_{PF}$ , exceeded
Low	Low	Low	Short Circuit Fault Threshold, $I_{SC}$ , exceeded



Fault Condition Characteristics

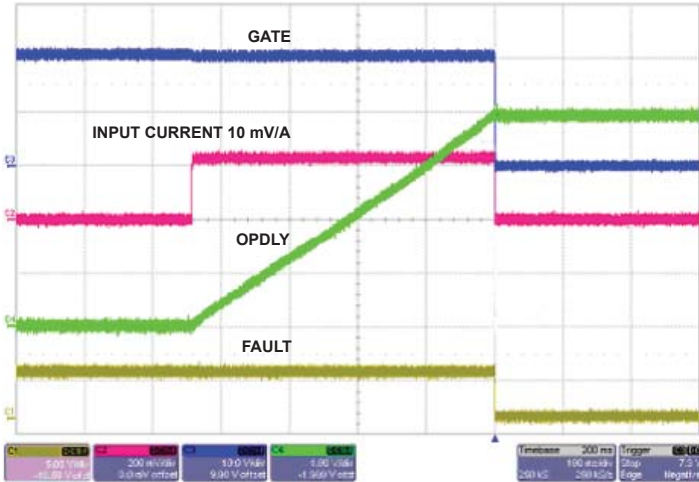


Figure 5. 240 V\*A fault: with  $V_{CC} = 12\text{ V}$  and ACS760 enabled, apply load

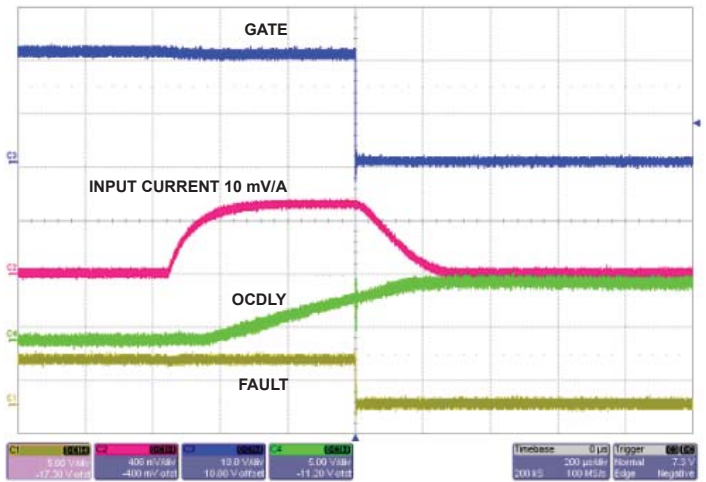


Figure 6.  $I_{PF}$  event: with  $V_{CC} = 12\text{ V}$  and ACS760 enabled, apply load

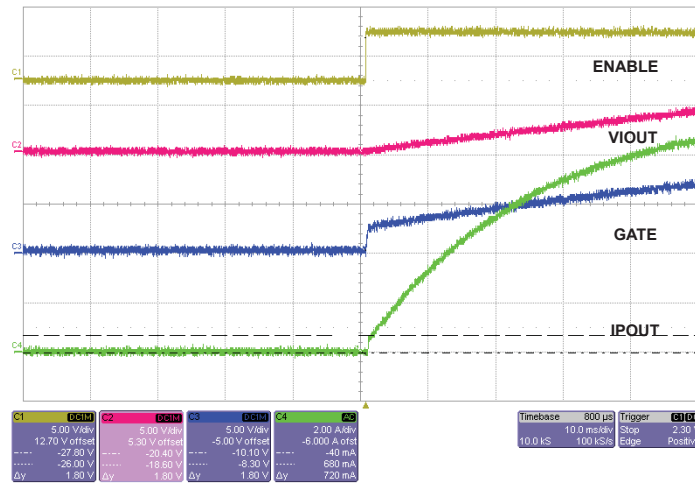


Figure 7. Hot-swap with  $1\ \mu\text{F}$  capacitor from CG pin to GND, resistive load approximately  $0.17\ \Omega$ , capacitive load approximately  $3300\ \mu\text{F}$ ;  $C_G$  capacitor limits inrush current to 720 mA during hot swap event (15 A current probe used)

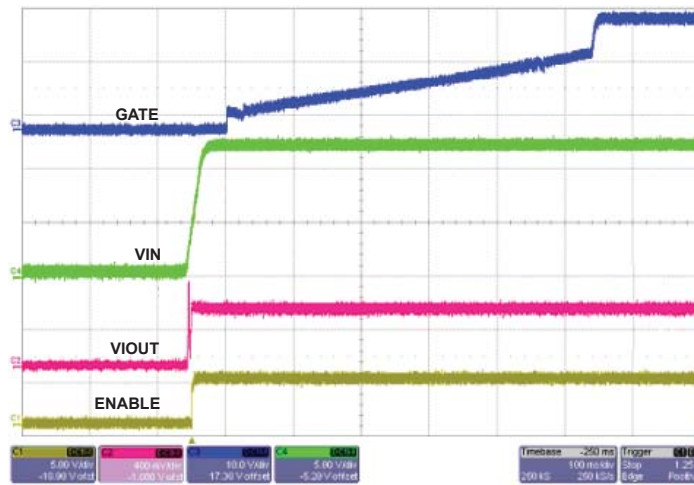


Figure 8. Power-up: with the enable jumper on, apply  $V_{CC}$

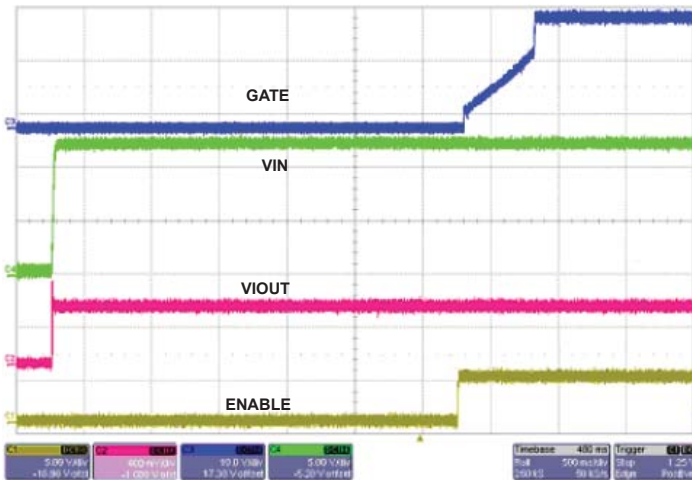


Figure 9. Power-up: with  $V_{CC}$  on, apply the enable jumper (enables ACS760)

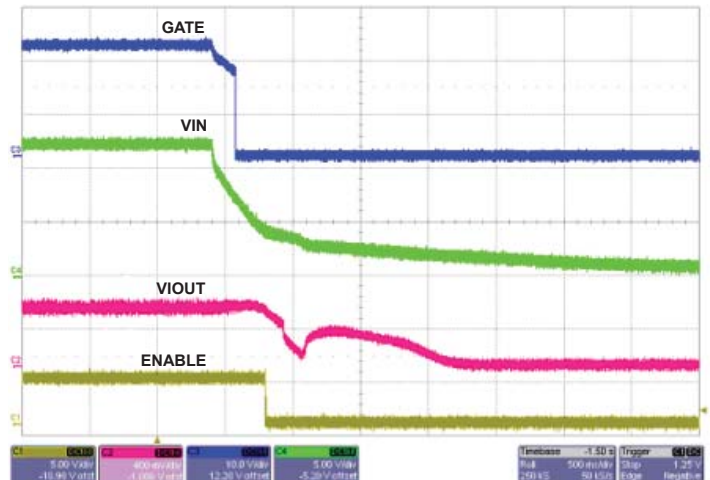


Figure 10. Power-down: with enable jumper on, remove supply (disables ACS760)

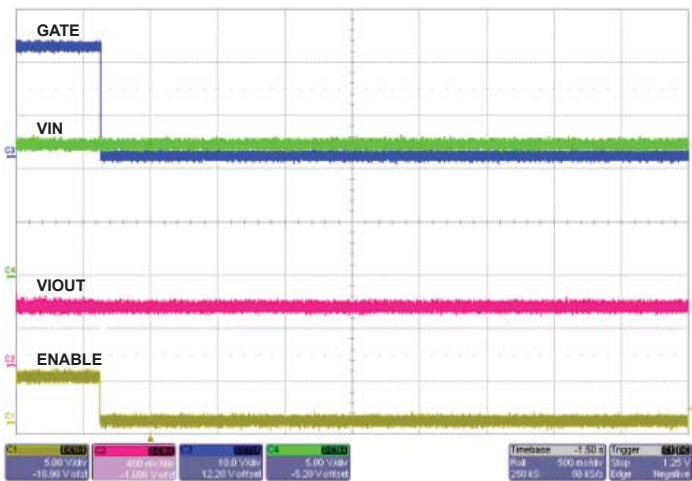


Figure 11. Power-up to power-down (a): remove enable jumper (disables ACS760, but  $V_{CC}$  and  $V_{IOUT}$  stay high (see figure 12)

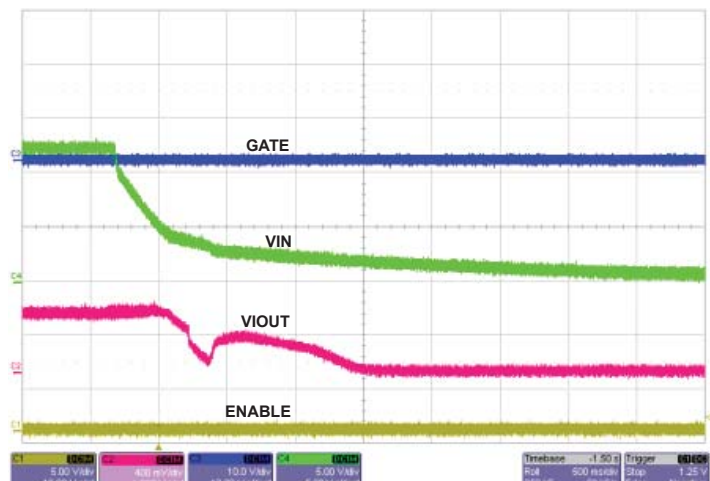


Figure 12. Power-up to power-down (b): with ACS760 disabled (see figure 11), remove supply ( $V_{CC}$  and  $V_{IOUT}$  brought low)

Application Information

Current Mode Operation

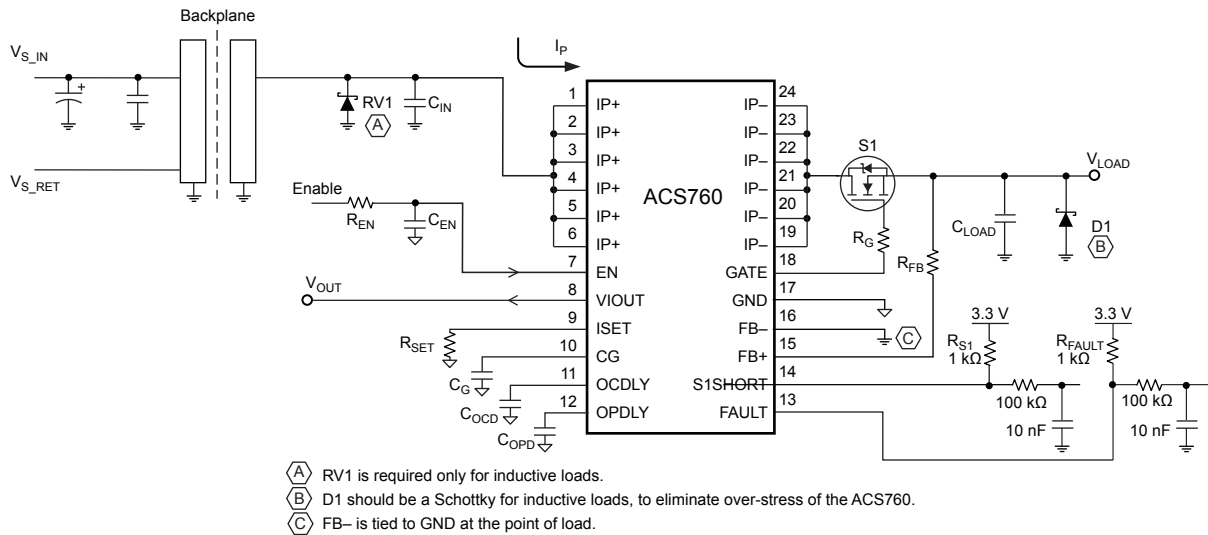
The ACS760 has the ability to operate in pure Current Mode. If the Allegro ACS760 detects power in excess of 240 V\*A, the FAULT output of the device transitions from a logic high to a logic low level and the integrated gate driver circuitry pulls the gate of an external MOSFET to GND. The delay between the detection of an excess power condition and gate shutdown is set by an external capacitor on the OPDLY pin to GND. The ACS760, however, has the ability to override the Power Mode fault condition to operate in pure Current Mode.

Pulling the OPDLY pin to GND, disables the 240 V\*A power fault to allow the ACS760 to operate in pure Current Mode. The user may then set the current fault threshold by adjusting the resistor value from the ISET pin to GND. If the current exceeds

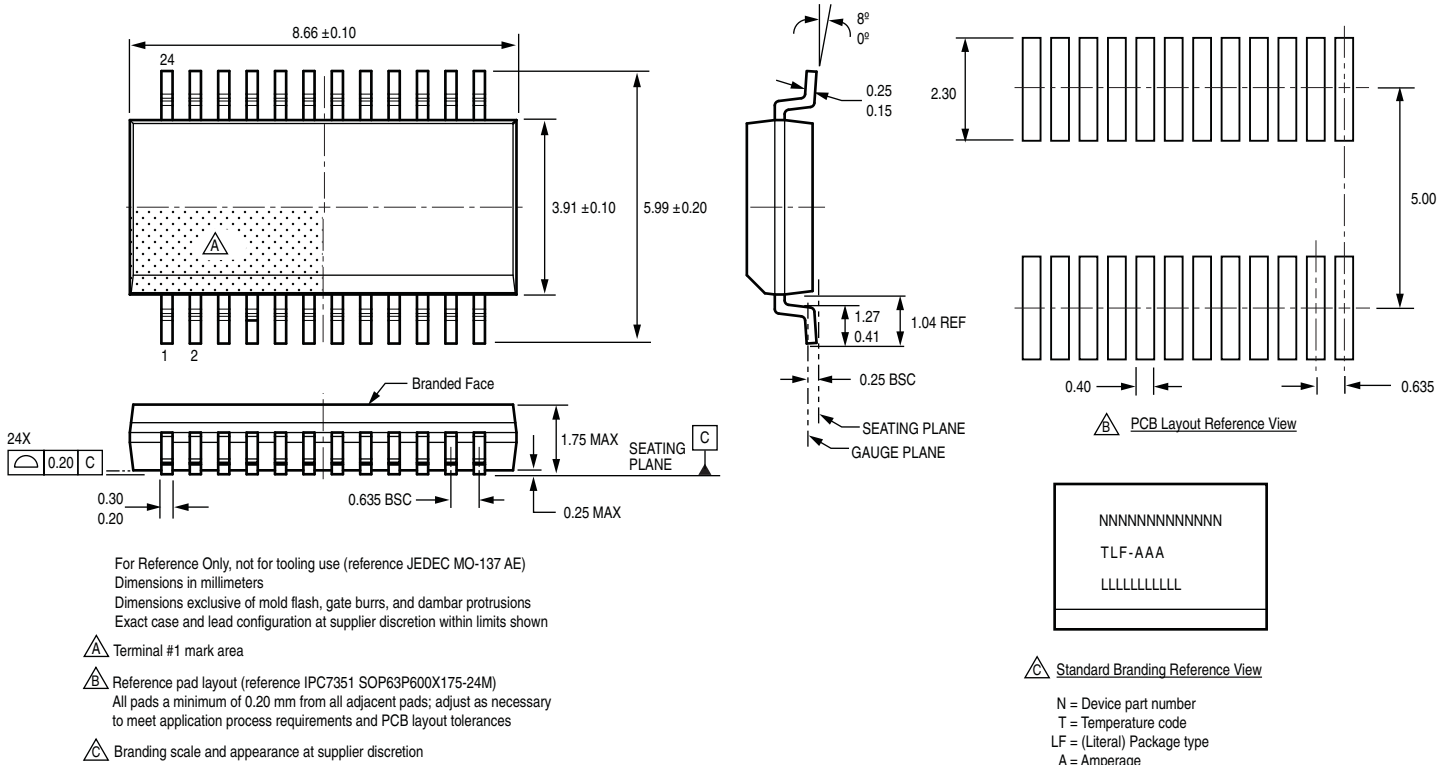
the set threshold, the FAULT output of the device trips and the gate of the external MOSFET is pulled to GND. The delay between the detection of a soft short circuit condition and gate shutdown is set by the capacitor on the OCDLY pin. In Current Mode Operation, the ACS760 has the ability to detect a S1 Short and Hard Short.

Filtering

In applications where the FAULT and S1SHORT pins are pulled-up prior to providing power to the device, be sure to add an RC filter with the pull-up resistor closest to the FAULT and S1SHORT pins. This will ensure that the ACS760 S1 Short and Fault logic levels remain proper under this application condition. See diagram below.



Package LF, 24-pin QSOP



Copyright ©2006-2013, Allegro MicroSystems, LLC

The products described herein are manufactured under one or more of the following U.S. patents: 5,619,137; 5,621,319; 6,781,359; 7,075,287; 7,166,807; 7,265,531; 7,425,821; or other patents pending.

Allegro MicroSystems, LLC reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in life support devices or systems, if a failure of an Allegro product can reasonably be expected to cause the failure of that life support device or system, or to affect the safety or effectiveness of that device or system.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, LLC assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

For the latest version of this document, visit our website:

[www.allegromicro.com](http://www.allegromicro.com)

