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AS-Interface Spec. V3.0 Compliant Universal AS-i IC

**ASI4U /
ASI4U-E /
ASI4U-F**
Datasheet

Brief Description

The ASI4U is a next-generation CMOS integrated circuit for AS-i networks. This low-level field bus AS-i (Actuator Sensor Interface) was designed for easy, safe, and cost-effective interconnection of sensors, actuators, and switches. It transports both power and data over the same two-wire unshielded cable.

The ASI4U is used as part of a master or slave node and functions as an interface to the physical bus. It provides the power supply, physical data transfer, and communication protocol handling. The ASI4U is fully compliant with the *AS-Interface Complete Specification V3.0*. It is function and pin compatible with the A²SI IC.

All configuration data are stored in an internal EEPROM that can be easily programmed by a stationary or handheld programming device. The special AS-i safety option assures short response times for security-related events.

Features

- Compliant with *AS-Interface Complete Specification V3.0*
- Universal application: slaves, masters, repeaters, and bus-monitors
- Floating AS-i transmitter and receiver for highly symmetrical high-power applications
- On-chip electronic inductor with current drive capability of 55 mA
- Two configurable LED outputs to support all *AS-Interface Complete Specification V3.0* status indication modes
- Several data pre-processing functions, including configurable data input filters and bit-selective data inverting
- Additional addressing channel for easy wireless module setup
- Support of 8 and 16 MHz crystals by automatic frequency detection
- Special AS-i safety option
- Clock watchdog for high system security

Related Products

- SAP5 Universal AS-Interface IC

Benefits

- Flexible, separated I/O pins
- Flexible AS-i Bus adoption (isolated transceiver)
- Very small package SSOP28 (ASI4U and ASI4U-F)
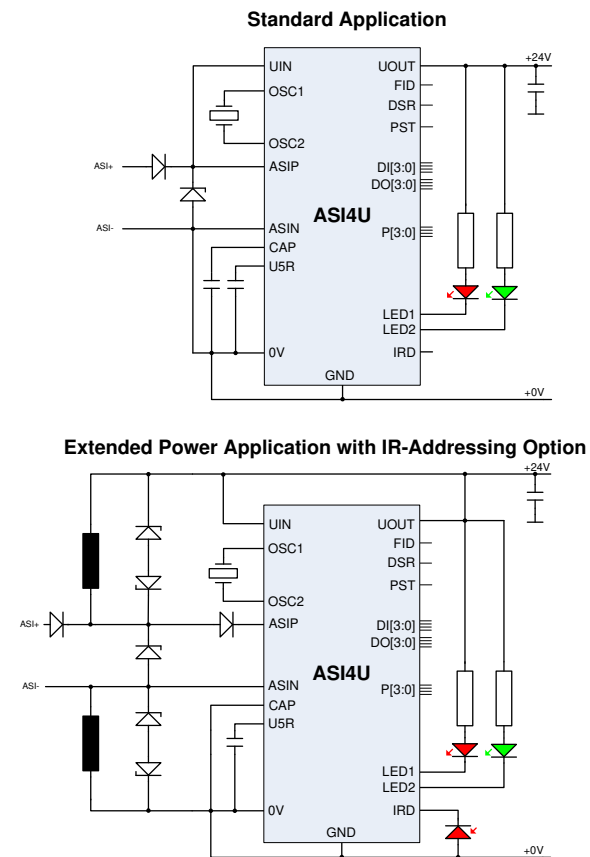- High ambient temperature applications (ASI4U-E)

Physical Characteristics

- ASI4U operational temperature: -25 to +85 °C
- ASI4U-F operational temperature: -40 to +85 °C
- ASI4U-E operational temperature: -25 to +105 °C
- RoHS-conformant package: SSOP28 (ASI4U and ASI4U-F) / SOP28 (ASI4U-E)

Available Support

- IDT AS-Interface Programmer Kit V2.0
- IDT ASI4U Evaluation Board V2.0

ASI4U Basic Application Circuits

Standard Application

Extended Power Application with IR-Addressing Option

**ASI4U /
ASI4U-E /
ASI4U-F
Datasheet**

AS-Interface Spec. V3.0
Compliant Universal AS-i IC

ASI4U Block Diagram

Typical Applications

- AS-i Master Modules
- AS-i Slave Modules
- AS-i Safety Modules
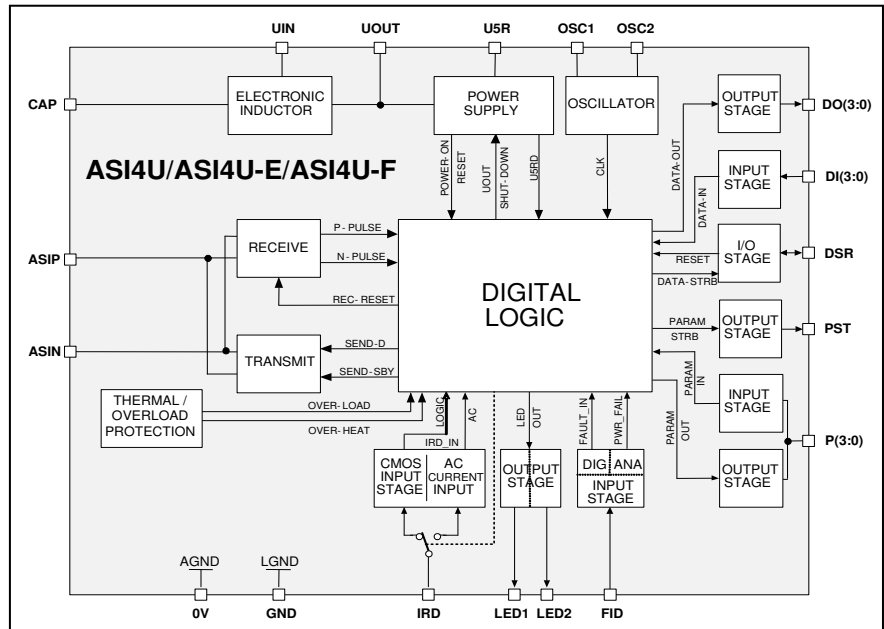
Ordering Information

Ordering Code	Type	Package	T_a [°C]	RoHS Conform	Packaging	Minimum Order
ASI4UE-G1-ST	Standard	SSOP28	-25 to 85	Y	Tube (47 parts/tube)	470
ASI4UE-G1-SR	Standard	SSOP28	-25 to 85	Y	Tape & Reel (1500 parts/reel)	1500
ASI4UE-G1-SR-7	Standard	SSOP28	-25 to 85	Y	Tape & Reel 7" (500 parts/reel)	500
ASI4UE-G1-MT	Master	SSOP28	-25 to 85	Y	Tube (47 parts/tube)	470
ASI4UE-G1-MR	Master	SSOP28	-25 to 85	Y	Tape & Reel (1500 parts/reel)	1500
ASI4UE-E-G1-ST	Standard	SOP28	-25 to 105	Y	Tube (27 parts/tube)	270
ASI4UE-E-G1-SR	Standard	SOP28	-25 to 105	Y	Tape & Reel (1000 parts/reel)	1000
ASI4UE-F-G1-ST	Standard	SSOP28	-40 to 85	Y	Tube (47 parts/tube)	470
ASI4UE-F-G1-SR	Standard	SSOP28	-40 to 85	Y	Tape & Reel (1500 parts/reel)	1500

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1   Important Safety Advice

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Important Safety Notice: This IDT product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high-reliability applications, such as military, medical life-support, or life-sustaining equipment, are specifically not recommended without additional mutually agreed upon processing by IDT for such applications.

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1.1.   AS-i-Safety Applications

The ASI4U/ASI4U-E/ASI4U-F is designed to allow replacement of IDT's A²SI ICs in existing board layouts and applications (also see section 1.2 for important restrictions). However, since the ASI4U/ASI4U-E/ASI4U-F provides additional data preprocessing functions at the data input channel, the fault reaction time of an AS-i Safety module could increase by 40ms if some of the new features become activated by intention, by accident, or hardware fault.

IDT strongly recommends the use of the Safety Mode feature of the ASI4U/ASI4U-E/ASI4U-F if it is replacing the A²SI in existing ASI-Safety designs. The same fault reaction times as with the A²SI are guaranteed only in this Safety Mode. For compatibility with the modified data input routing in Safety Mode, the user must adapt the safety code table stored in the external microcontroller. Only safety code sequences that contain the value **1110** are permitted.

If the IC is operated in Safety Mode, the user must ensure that the Synchronous Data I/O Mode as well as the data input filters remain disabled by appropriate EEPROM configuration.

Application of the ASI4U/ASI4U-E/ASI4U-F in Standard Mode (no Safety Mode enabled) for AS-i Safety products is possible if an additional fault reaction time of 40ms is taken into account.

The user must also adhere to the additional security advice provided in *Production and Repair of AS-i Safety Slaves*, which is available on the IDT web page www.IDT.com (see section 8).

1.2.   Repair of ASI-Safety Modules

Important: If an A²SI-based ASI-Safety module must be repaired, replacing the A²SI IC with the newer ASI4U/ASI4U-E/ASI4U-F is **<u>explicitly prohibited</u>**. This is to prevent safety-relevant deviations of module properties that can result from the different data input paths and the possible increase in fault reaction time discussed in section 1.1.

The user must also adhere to the additional security advice provided in *Production and Repair of AS-i Safety Slaves*, which is available on the IDT web page www.IDT.com.

2 General Device Specifications

Important: Stresses beyond those listed under "Absolute Maximum Ratings" (section 2.1) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" are not implied. Exposure to conditions rated as the absolute maximum for extended periods might affect device reliability.

2.1. Absolute Maximum Ratings (Non-Operating)

Table 2.1   Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Max	Unit
Voltage reference	V_{0V}, V_{GND}		0	0	V
Voltage difference between ASIP and ASIN (V_{ASIP} - V_{ASIN}) [1]	$V_{ASIP-ASIN}$		-0.3	40	V
Pulse voltage between ASIP and ASIN (V_{ASIP} - V_{ASIN})	$V_{ASIP-ASIN\_P}$	Pulse width ≤ 50µs Repetition rate ≤ 0.5Hz	-0.3	50	V
Pulse voltage between ASIP and 0V (V_{ASIP} – V_{0V}) [2]	V_{ASIP}	Pulse width ≤ 50µs Repetition rate ≤ 0.5Hz	-0.3	50	V
Voltage between ASIN and 0V (V_{ASIN} – V_{0V}) [2]	V_{ASIN}		-6.0	6.0	V
Power supply input voltage	V_{UIN}		-0.3	40	V
Pulse voltage at power supply input	V_{UIN_P}	Pulse width ≤ 50µs Repetition rate ≤ 0.5Hz	-0.3	50	V
Voltage at DI3, DI2, DI1, DI0, DO3, DO2, DO1, DO0, P3, P2, P1, P0, DSR, PST, LED1, LED2, FID, IRD, and UOUT pins	$V_{inputs1}$		-0.3	V_{UOUT} + 0.3	V
Voltage at OSC1, OSC2, CAP, and U5R pins	$V_{inputs2}$		-0.3	7	V
Input current into any pin except supply pins	I_{in}	Latch-up resistance, reference to pin 0V	-50	50	mA
Humidity – non-condensing	H	Level 4 according to JEDEC-020D standard			
Electrostatic discharge – Human Body Model (HBM1)	V_{HBM1}	C = 100pF charged to V_{HBM1} with resistor R = 1.5kΩ in series	3500		V
Electrostatic discharge – Human Body Model (HBM2)	V_{HBM2}	C = 100pF charged to V_{HBM2} with resistor R = 1.5kΩ in series	2000		V

Parameter	Symbol	Conditions	Min	Max	Unit
Electrostatic discharge – Equipment Discharge Model (EDM)	V_{EDM}	C = 200pF charged to V_{EDM} with no resistor in series	400		V
Storage temperature	T_{STG}		-55	125	°C
Soldering temperature Sn/Pb	T_{Lead}	JEDEC-J-STD-020D		240	°C
Soldering temperature 100%Sn	T_{Lead}	JEDEC-J-STD-020D		260	°C
Total power dissipation [6]	P_{tot}			0.85	W
Thermal resistance of SSOP 28 package (ASI4U and ASI4U-F)	R_{thj}	Single layer board P_{tot} = 0.5W Air velocity = 0m/s at maximum value Air velocity = 2.5m/s at minimum value	40	80	K/W
Thermal resistance of SOP 28 package (ASI4U-E)			60	80	K/W

1) Reverse polarity protection must be performed externally.

2) VASIP-ASIN and VASIP-ASIN_P must not be exceeded.

3) Valid for ASIP-ASIN only.

4) Valid for all pins except ASIP-ASIN.

5) Valid for ASIP-ASIN only.

6) At the maximum operating temperature, the maximum total power dissipation allowed depends on additional the thermal resistance from the package to the ambient air and on the operational ambient temperature as shown in Figure 2.1

Figure 2.1 $P_{tot} = f(T_a)$
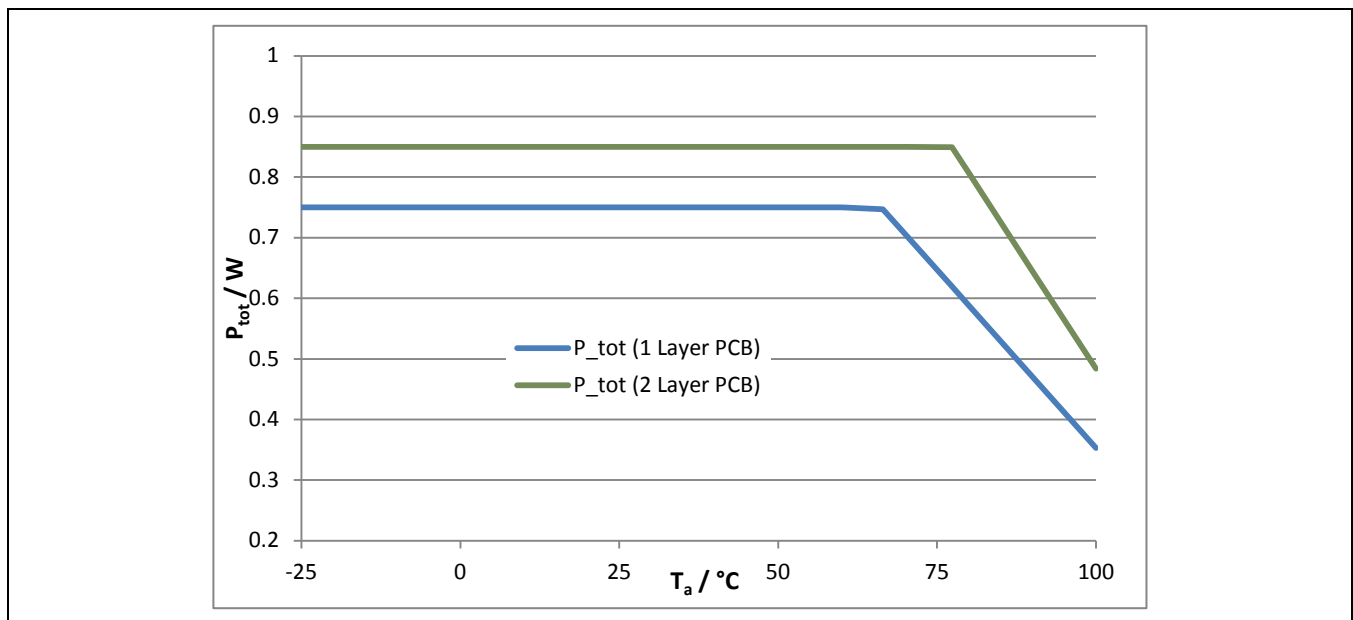
2.2. Operating Conditions

Table 2.2   Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX.	UNIT
Positive supply voltage for IC operation [1]	V_{UIN}	DC parameter: $V_{UINmin} = V_{UOUTmin} + V_{DROPmax}$ $V_{UINmax} = V_{UOUTmax} + V_{DROPmin}$	16	33.1	V
Negative supply voltage	V_{0V}, V_{GND}		0	0	V
DC voltage at ASIP [2]	V_{ASIP}	Relative to V_{0V}	16	33.1	V
DC voltage at ASIN [2]	V_{ASIN}	Relative to V_{0V}	-4	4	V
Operating current	I_{UIN}	$V_{UIN} = 30V$ $f_c = 8.000$ MHz; no load at any pin; transmitter turned off; digital State Machine is in idle state		6	mA
Maximum output sink current at DO0, DO1, DO2, DO3, and DSR pins	I_{CL1}			10	mA
Maximum output sink current at P0, P1, P2, P3, and PST pins	I_{CL2}			10	mA
Ambient temperature range, operating range	T_a	ASI4U	-25	85	°C
		ASI4U-E	-25	105	°C
		ASI4U-F	-40	85	°C

1) Below V_{UINmin}, the power supply block might not be able to provide the specified output currents at UOUT and U5R.
2) Outside the maximum and minimum limits, the send current shape and send current amplitude cannot be guaranteed.

Table 2.3   Crystal Frequency

PARAMETER	SYMBOL	CONDITIONS	NOMINAL	UNIT
Crystal frequency [1]	f_c		8.000/16.000	MHz

1) The IC automatically detects whether the crystal frequency is 8.000MHz or 16.000MHz and controls the internal clock circuit accordingly. The frequency detection is locked as soon as one AS-i telegram has been correctly received **at any input channel**. It can be reset by a power-on reset only.
Note: In Slave Mode, the locking occurs if a Master Call has been received. In the Master, Repeater, or Monitor Modes, a Master Call or a Slave Response that has been received on any input channel triggers the frequency locking.

The ASI4U/ASI4U-E/ASI4U-F supports an integrated clock watchdog. If no crystal or clock oscillation is recognized for 150µs, the IC generates a RESET event until clock oscillation is available. More detailed oscillator pin definitions can be found in section 4.10.

2.3. Quality Standards

The quality of the ASI4U/ASI4U-E/ASI4U-F is ensured according to the IDT quality standards. Functional device parameters are valid for device operating conditions specified in section 2.2. Unless otherwise stated, production device tests are performed at $T_a = +25°C$ within the recommended ranges of (V_{ASIP} - V_{ASIN}) and (V_{IN} - V_{0V}). Additional sample base testing is done at +85°C and -25°C (-40°C for the ASI4U-F).

3 Basic Functional Description

3.1. Functional Block Diagram

Figure 3.1   ASI4U Functional Block Diagram
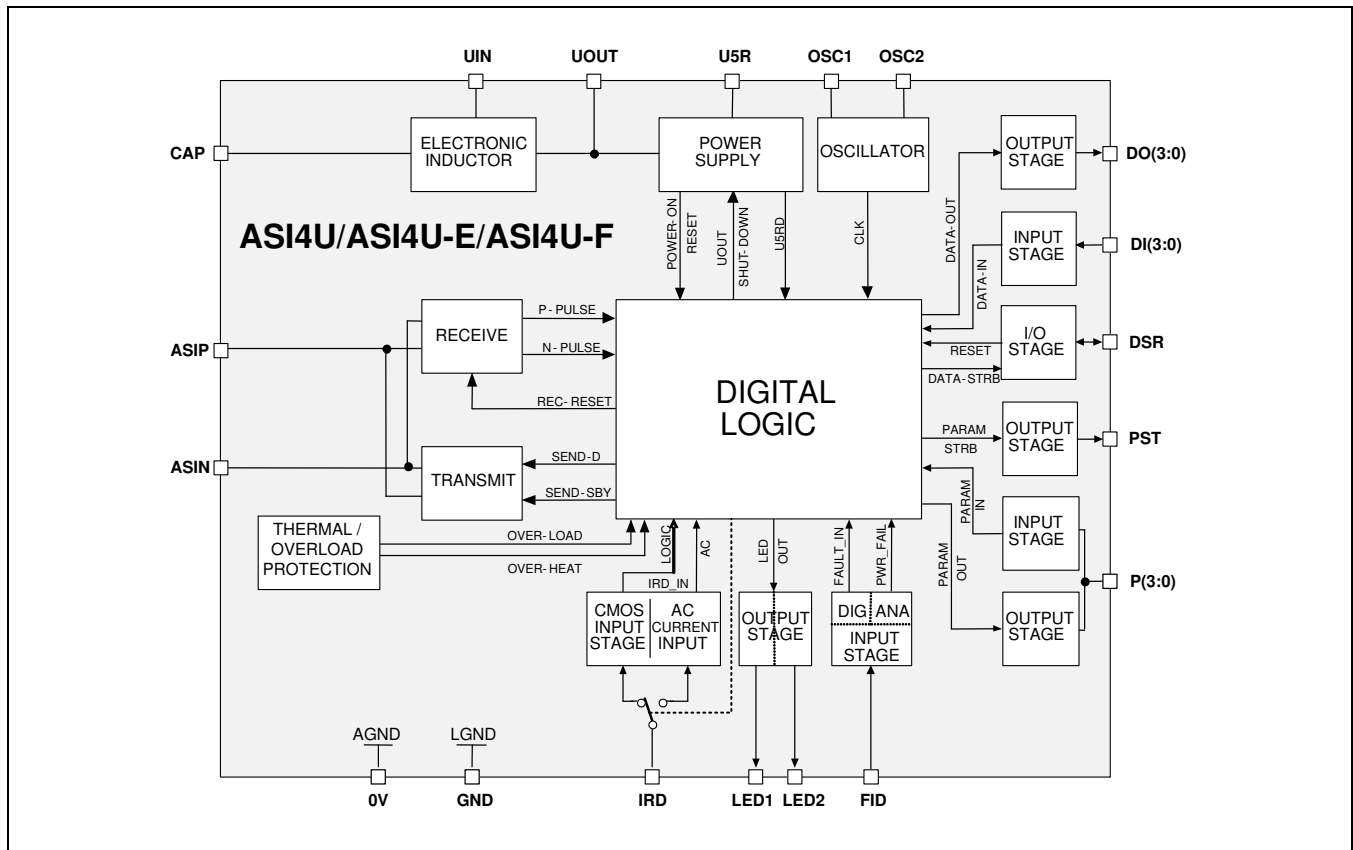
Following device functions are associated with the different blocks of the IC:

RECEIVE   The RECEIVE block converts the analog telegram waveform from the AS-i bus to a digital pulse-coded signal that can be processed further by a digital UART circuit.

The RECEIVE block is directly connected to the ASIP and ASIN pins, which connect to the AS-i line. It converts the differential AS-i telegram to a single-ended signal and removes the DC offset by high-pass filtering. To adapt quickly to changing signal amplitudes in telegrams from different network users, the amplitude of the first telegram pulse is measured by a 3-bit flash ADC and the threshold of a positive and a negative comparator is set accordingly to about 50% of the measured level. The comparators generate the P-pulse and N-pulse signals.

TRANSMIT The TRANSMIT block transforms a digital response signal to a correctly shaped send current signal that is applied to the AS-i bus. Due to the inductive network behavior of the network, the changing send current induces voltage pulses on the network line that overlay the DC operating voltage. The voltage pulses must have $\sin^2$-wave shapes; therefore the send current shape must follow the integral of the $\sin^2$-wave function.

DIGITAL LOGIC The DIGITAL LOGIC block contains the UART, Main State Machine, EEPROM memory and other control logic. EEPROM write access and other I/O operations of the Main State Machine are supported in Slave Mode only (see description of general IC operational modes below). In Master Mode, the IC is basically equivalent to a physical layer transceiver.

If Slave Mode is activated, the UART demodulates the received telegrams, verifies telegram syntax and timing, and controls a register interface to the Main State Machine. After reception of a correct telegram, the UART generates appropriate Receive Strobe signals that tell the Main State Machine to start further processing. The Main State Machine decodes the telegram information and starts respective I/O processes or EEPROM access. A second register interface is used to send data back to the UART for construction of a telegram response. The UART modulates the response data into a Manchester-II-coded bit stream that is used to control the TRANSMIT unit.

ELECTRONIC INDUCTOR The ELECTRONIC INDUCTOR block is basically a gyrator circuit. It provides an inductive behavior between the IC's UIN and UOUT pins while the inductance is controlled by the capacitor on the CAP pin. The inductor decouples the power regulator of the IC as well as the external load circuit from the AS-i bus, and this prevents cross talk or switching noise from disturbing the telegram communication on the bus.

The *AS-Interface Complete Specification V3.0* describes the input impedance behavior of a slave module by an equivalent circuit that consists of a resistance (R), an inductance (L), and a capacitance (C) in parallel. For example, a slave module in Extended Address Mode must have R > 13.5kΩ, L > 13.5mH and C < 50pF. The electronic inductor of the ASI4U/ASI4U-E/ASI4U-F delivers values that are well within the required ranges for output currents up to 55mA. More detailed parameters can be found in section 4.18.2.

The electronic inductor requires an external capacitor of at least 10µF at the UOUT pin for stability.

POWER SUPPLY The POWER SUPPLY block consists of a bandgap-referenced 5V regulator and other reverence voltage and bias current generators for internal use. The 5V regulator requires an external capacitor at pin U5R of at least 1µF for stability. It can source up to 4mA for external use; however, the power dissipation and the resulting device heating become a major concern if too much current is drawn from the regulator.

OSCILLATOR The OSCILLATOR block supports direct connection to 8.000 MHz or 16.000 MHz crystals with a dedicated load capacity of 12pF and parasitic pin capacities of up to 8pF. The IC automatically detects the oscillation frequency of the connected crystal and controls the internal clock generator circuit accordingly.

After power-on reset, the IC is set to 16.000 MHz operation by default. After approximately 200µs, it will either switch to 8.000 MHz operation or remain in the 16.000 MHz mode. The frequency detection is active until the first AS-i telegram has been successfully received in order to ensure that the IC has found the correct clock frequency setting. The detection result is locked thereafter to increase resistance against burst or other interferences.

The oscillator unit also contains a clock watchdog circuit that can generate an unconditional IC reset if there has been no clock oscillation for more than approximately 20µs. This is to prevent the IC from unpredictable behavior if a clock signal is no longer available.

THERMAL/OVERLOAD PROTECTION The IC is self-protected against overheating and short-circuiting of the UOUT pin toward IC ground.

If the silicon die temperature rises above approximately 140°C for more than 2 seconds, the IC detects overheating, switches off the electronic inductor, performs an IC reset, and sets all analog blocks to power down mode. Although the 5V regulator is turned off in this state, there will still remain a voltage of approximately 3V to 3.5V available at U5R that is derived from the internal start circuitry. The overheating protection state can only be de-activated by power-cycling the AS-i voltage.

Short-circuiting the UOUT pin toward IC ground causes the same IC behavior as overheating.

IRD CMOS / AC CURRENT INPUT The IRD pin is the input for the additional addressing channel in Slave Mode (see section 3.2 for a description of general IC operational modes) or the direct AS-i transmitter input in Master Mode. In Slave Mode, the IRD pin can be operated either in CMOS Mode or AC Current Input Mode. The latter is provided for direct connection of a photodiode. More detailed information can be found in section 4.3.

FID DIGITAL / ANALOG STAGE The FID pin can be set to the Digital CMOS Mode or Analog Voltage Input Mode. In Slave Mode, it is set to CMOS operation; in Master Mode, it works in Analog Mode and functions as the input for the power fail comparator.

INPUT STAGE All digital inputs, except the oscillator pins, have high voltage capabilities and partial Schmitt trigger and pull-up features. For more details, see section 4.4.

OUTPUT STAGE All digital output stages, except for the oscillator pins, have high voltage capabilities and are implemented as NMOS open-drain buffers. Each pin can sink up to 10mA of current.

3.2. General Operational Modes

The ASI4U/ ASI4U-E/ASI4U-F provides two main operational modes and two additional sub-operational modes. The two main operation modes are Slave Mode and Master Mode. Sub-operation modes are Repeater Mode and Monitor Mode. The latter were derived from Master Mode for providing different output signals at the Parameter Port.

The active operational mode is selected by programming the *Master_Mode* and *Repeater_Mode* flags in the "Firmware Area" block of the EEPROM (also see Table 3.4). The EEPROM is read at every initialization of the IC. Online mode switching is not provided. Table 3.1 gives the bit configurations for the operational modes.

Table 3.1   Assignment of Operational Modes

SELECTED OPERATIONAL MODE	MASTER MODE FLAG	REPEATER MODE FLAG
Slave Mode	0	0
Master Mode	1	0
Repeater Mode	1	1
Monitor Mode	0	1

In Slave Mode, the IC operates as a full-feature AS-i slave IC according to the *AS-Interface Complete Specification V3.0*.

In Master Mode, the IC translates a digital output signal from the master control logic (e.g., a programmable logic controller or microcontroller) to a correctly shaped, analog AS-i pulse sequence and vice versa. Every AS-i telegram received is checked for consistency with the AS-Interface communication protocol specifications, and if no errors were found, an appropriate Receive Strobe signal is generated.

Master Mode and Monitor Mode differ in the kind of telegrams signaled. In Master Mode, a single Receive Strobe signal is provided validating every correctly received Slave Response; in Monitor Mode, two different Receive Strobe signals are available indicating every correctly received Master and Slave telegram separately. The Monitor Mode is intended for use in intelligent slaves and bus monitors that provide their own telegram decoding mechanisms but do not check for correct telegram timing or syntax.

The Repeater Mode is specifically provided for AS-i bus repeater applications.

3.3.   Slave Mode

The Slave Mode is the most complex operational mode of the IC. The IC supports all mandatory AS-i Slave functions and also a variety of additional features that make AS-i slave module design very easy and flexible.

3.3.1.   AS-Interface Communication Channel

In Slave Mode, the ASI4U can work on two different communication channels: the AS-i channel and the IRD channel. The AS-i channel is directly connected to the AS-i bus via the ASIP and ASIN pins. A receiver and a transmitter unit are connected in parallel to the pins. This allows fully bi-directional communication through ASIP and ASIN.

The ASI4U/ASI4U-E/ASI4U-F is the first IC that supports floating operation of the AS-i receiver and transmitter (within specified limits) relative to IC ground. Previously, the ASIN pin always had to be on the same potential as the IC ground (see Figure 3.2 for an example), preventing full symmetrical input circuits with external coils. Figure 3.3 illustrates the new enhanced functionality. The relation Z1/Z2 is a measure of the symmetry of the AS-i module input relative to machine ground. The application in Figure 3.3 is more symmetrical since Z1 and Z2 are more equal than in the conventional solution. Note: This is not a complete application circuit.

Figure 3.2   Conventional Application for AS-i IC with One External Coil
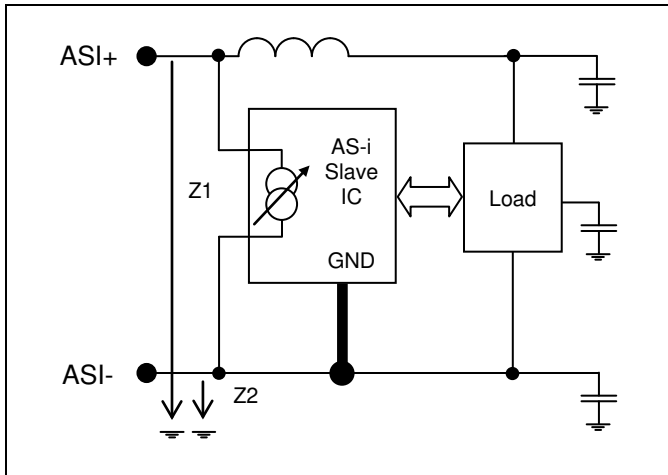
Figure 3.3   Application for AS-i IC with Two External Coils
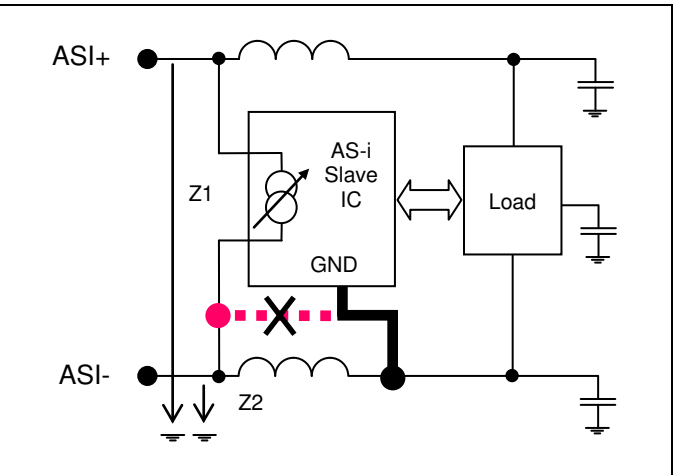
3.3.2. IRD Communication Channel

In addition to the AS-Interface communication channel, the ASI4U can also operate on a second input channel: the IRD Input Channel or Addressing Channel. In this mode, the IRD pin is the input for an AS-i signal in Manchester-II-coded format. The signal can be either an AC-current signal generated by a photodiode or a 5V-CMOS signal. The IC automatically detects the type of the signal and switches the input path accordingly.

The output pin in IRD Communication Mode is LED1. It transmits the slave response as an inverted Manchester-II-coded AS-i signal. A red LED connected to LED1 can form the response transmitter in an optical communication system, or LED1 can be directly connected to external circuitry.

Activation of the IRD communication channel is achieved by a transmission referred to as a "Magic Sequence" that is sent in advance of the desired communication. The construction of a Magic Sequence is described in detail in section 4.3. The IRD communication mode is deactivated by an IC reset, except in a special case described in section 4.3.

3.3.3. Parameter Port Pins

The ASI4U features a 4-bit-wide parameter port and a related parameter strobe signal on the PST pin. There is a defined phase relation between a parameter output event, the parameter input sampling, and the activation of the PST signal, so it can be used to trigger external logic or a microcontroller to process the received parameter data or to provide new input data for the AS-i slave response.

Version 3.0 of the *AS-Interface Complete Specification* defines a bidirectional mode for parameter data. The ASI4U/ASI4U-E/ASI4U-F supports this feature, which can be activated by special EEPROM setting.

See section 4.6 for further details.

3.3.4. Data Port Pins

An important feature of the ASI4U/ASI4U-E/ASI4U-F is the 8-bit wide data port that consists of a 4-bit-wide input section and a 4-bit-wide output section. The input and output sections work independently from each other allowing a maximum of 8 devices (4 input and 4 output devices) to be connected to the ASI4U/ASI4U-E/ASI4U-F. For special applications (compatibility), the Multiplex Mode can be activated, which limits the output activation to a specific time frame. With this feature, a 4-bit wide bi-directional data I/O port can be achieved by external connection of the corresponding data input and output pins.

The data port is accompanied by the data strobe signal on the DSR pin. There is a defined phase relation between a data output event, the input data sampling, and the activation of the DSR signal, so it can be used to trigger external logic or a microcontroller to process the received data or to provide new input data for the AS-i slave response. See section 4.7 for further details.

3.3.5. Data Input Inversion

By default, the logic signal (HIGH/LOW) that is present at the data input pins during the input sampling phase is transferred without modification to the send register, which is interfaced by the UART so that the signal directly becomes part of the slave response.

Some applications function with inverted logic levels. To avoid additional external inverters, the input signal can be inverted by the ASI4U/ASI4U-E/ASI4U-F before the signal is transferred to the send register. The inversion of the input signals can either be done bit-selectively or jointly for all data input pins. See section 4.7.2.

3.3.6. Data Input Filtering

To prevent input signal bouncing being transferred to the AS-Interface Master, the data input signals can be digitally filtered. Filter times can be configured in seven steps from 128µs up to 8.192ms. When the AS-i Cycle Mode is activated, the filter time is determined by the actual AS-i cycle time. For more detailed information, refer to section 4.7.2.

The filter function can be enabled bit-selectively. Activation of the filters can be done jointly either by EEPROM configuration or by the logic state of the parameter port pin P2. See section 4.7.2.

3.3.7. Fixed-Data Output Driving

The fixed-data output-driving feature is intended to facilitate board-level design for similar products that do not require the full data output port width. The user can select one or more bits from the data output port to be driven by a distinct logic level instead of by the data that was sent by the master. The distinct output data is stored in the EEPROM and can be set during final module configuration. With this feature, it is possible to signal the actual IC profile to external circuitry and to allow reuse of some types of board designs for different product applications.

See section 4.7.3.

3.3.8. Synchronous Data I/O Mode

Version 3.0 of the *AS-Interface Complete Specification* defines a synchronous data I/O feature that allows a number of slaves in the network to switch their outputs at the same time and to have their inputs sampled jointly. This feature is especially useful if more than 4-bit wide data are to be provided synchronously to an application.

The synchronization point is defined as the data exchange event of the slave with the lowest address in the network. This definition relies on the cyclical slave polling with incrementing slave addresses each cycle, which is one of the basic communication principles of AS-i. The IC always monitors the data communication and detects the change from a higher to a lower slave address. If such a change has been recognized, the IC assumes that the slave with the lower address has the lowest address in the network.

There are some special procedures that become active during the start of synchronous I/O mode operation and if more than three consecutive telegrams have been sent to the same slave address. This is described in more detail in section 4.7.4.

3.3.9. 4 Input / 4 Output Processing in Extended Address Mode

Version 3.0 of the *AS-Interface Complete Specification* also supports 4-bit wide output data in Extended Address Mode. Up to *AS-Interface Complete Specification V2.11*, it was only possible to send three data output bits from the master to the slave in Extended Address Mode because telegram bit I3 was used to select between the A and B slave types for extended slave addressing (up to 62 slaves per network). In Normal Address Mode, bit I3 carries output data for pin D3.

The version 3.0 definition introduces a multiplexed data transfer so that all 4-bits of the data output port can be used again. A first AS-i cycle transfers the data for a 2-bit output nibble only, while the second AS-i cycle transfers the data for the contrary 2-bit nibble. Nibble selection is done by the remaining third bit. To ensure continuous alternation of bit information I2 and thus continued data transfer to both nibbles, a special watchdog was implemented that observes the state of the I2 bit. The watchdog can be activated or deactivated by EERPOM setting. It provides a watchdog filter time of about 327ms.

The multiplexed transfer increases the refresh time per output by a factor of two; however, some applications can tolerate this increase for the benefit of less external circuitry and better slave address efficiency. The sampling cycle of the data inputs remains unchanged since the meaning of the I3 bit was not changed in the slave response with the definition of the Extended Address Mode.

For more detailed information, see section 4.7.5.

3.3.10. AS-i Safety Mode

The enhanced data input features described in previous sections require additional registers in the data input path that store the input values for a specific time before they transfer them to the AS-i transmitter. This causes a time delay in the input path that could lead to a delayed "turn off" event if the registers are activated by intention or unintentionally in AS-i Safety applications.

To safely exclude an activation of the enhanced data I/O features in AS-i Safety applications, the IC provides a special Safety Mode that is strongly recommended for AS-i Safety communication purposes. See section 4.7.6 for further details.

3.3.11. Enhanced LED Status Indication

ASI4U now supports enhanced status indication by two LED outputs. A special mode for direct application of dual LEDs and the respective different signaling modes are also implemented. Compared to the A^{2}SI, the former U5RD pin was reassigned as LED2 pin. Thus, compatibility to existing A^{2}SI board layouts is still guaranteed. However, it will require keeping the LED2 pin disabled (default state at delivery) in order to avoid short-circuiting U5R to ground. More detailed information on the different signaling schemes and their activation can be found in section 4.9.

3.3.12. Communication Monitor/Watchdog

Data and parameter communication are continuously observed by a communication monitor. If neither *Data_Exchange* nor *Write_Parameter* calls were addressed to and received by the IC within a time frame of approximately 41ms, a *No Data/Parameter Exchange* status is detected and signaled at LED1.

If the respective flags are set in the EEPROM, the communication monitor can also act as communication watchdog that initiates a complete IC reset after expiration of the watchdog timer. The watchdog mode can also be activated and deactivated by a signal at parameter port pin P0. See section 4.15 for more detailed information.

3.3.13. Write Protection of *ID_Code_Extension_1*

As defined in the *AS-Interface Complete Specification V3.0,* the ASI4U/ASI4U-E/ASI4U-F also supports write protection for *ID_Code_Extension_1*. This feature allows the activation of new manufacturer-protected slave profiles and is enabled by an EEPROM setting. For more details, see section 4.17.

3.3.14. Summary of Master Calls

Table 3.2 and the diagram on the following page show the complete set of Master calls that are decoded by the ASI4U/ASI4U-E/ASI4U-F in Slave Mode. The "Enter Program Mode" call is intended for programming of the IC by the slave manufacturer only. It becomes deactivated as soon as the *Program_Mode_Disable* flag is set in the "Firmware Area" block of the EEPROM.

> Important note regarding full compliance with the *AS-Interface Complete Specification*: In order to achieve full compliance to the *AS-Interface Complete Specification*, the *Program_Mode_Disable* flag must be set by the manufacturer of AS-i slave modules during the final manufacturing and configuration process and before an AS-i slave device is delivered to field application users.

Table 3.2   ASI4U Master Calls and Related Slave Responses

Instruction	MNE	Master Request														Slave Response						
		ST	CB	A4	A3	A2	A1	A0	I4	I3	I2	I1	I0	PB	EB	SB	I3	I2	I1	I0	PB	EB
Data Exchange	DEXG	0	0	A4	A3	A2	A1	A0	0	D3 ~Sel	D2	D1	D0	PB	1	0	D3 E3	D2 E2	D1 E1	D0 E0	PB	1
Write Parameter	WPAR	0	0	A4	A3	A2	A1	A0	1	P3 ~Sel	P2	P1	P0	PB	1	0	P3 I3	P2 I2	P1 I1	P0 I0	PB	1
Address Assignment	ADRA	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	PB	1	0	0	1	1	0	0	1
Write Extended ID Code_1	WID1	0	1	0	0	0	0	0	0	ID3	ID2	ID1	ID0	PB	1	0	0	0	0	0	0	1
Delete Address	DELA	0	1	A4	A3	A2	A1	A0	0	0 Sel	0	0	0	PB	1	0	0	0	0	0	0	1
Reset Slave	RES	0	1	A4	A3	A2	A1	A0	1	1 ~Sel	1	0	0	PB	1	0	0	1	1	0	0	1
Read IO Configuration	RDIO	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	0	PB	1	0	IO3	IO2	IO1	IO0	PB	1
Read ID Code	RDID	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	1	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read ID Code_1	RID1	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	0	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read ID Code_2	RID2	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	1	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read Status	RDST	0	1	A4	A3	A2	A1	A0	1	1 ~Sel	1	1	0	PB	1	0	S3	S2	S1	S0	PB	1
Broadcast (Reset)	BR01	0	1	1	1	1	1	1	1	0	1	0	1	1	1	--- no slave response ---						
Enter Program Mode	PRGM	0	1	0	0	0	0	0	1	1	1	0	1	1	1	--- no slave response ---						

Note: In Extended Address Mode, the "Select Bit" defines whether the A-Slave or B-Slave is being addressed. Depending on the type of master call, bit I3 carries the select bit information (Sel = A-Slave) or the inverted select bit information (~Sel = B-Slave).

| | | B-Slave with Profile 0.A (green shaded) | | ASI Master Request (black/green) | ASI Slave Response (blue) | | | | No Slave Response (blue shaded) |

Legend: B-Slave with Profile 0.A (green shaded) — ASI Master Request (black/green) — ASI Slave Response (blue) — No Slave Response (blue shaded)

ADR != 0	I2 I1 I0	000	001	010	011	100	101	110	111
CB I4 I3	I3=Sel	(Slave Address != 0) AND (Progam Mode not activated)							
000	Sel=0	Data_Exchange /Sel D2 D1 D0							
001	Sel=1	Data_Exchange D3 D2 D1 D0			D3 D2 D1 D0				
010	Sel=0	Write_Parameter /Sel P2 P1 P0							
011	Sel=1	Write_Parameter P3 P2 P1 P0			P3 P2 P1 P0				
100	Sel=0	Delete_Addr x0							
101	Sel=1	Delete_Addr x0							
110	Sel=0	Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6	Broadcast	Rd_Status <S3:S0>	
111	Sel=1	Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6		Rd_Status <S3:S0>	

ADR == 0	I2 I1 I0	000	001	010	011	100	101	110	111
CB I4 I3		(Slave Address == 0) AND (Progam Mode not activated)							
000									
001				Address_Assignment A4 A3 A2 A1 A0					
010					0x6				
011									
100				Write_Var_Ext_Code1 ID3 ID2 ID1 ID0					
101					0x0				
110		Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>		Broadcast		
111						Reset_Slave 0x6	EnterPmode	Rd_Status <S3:S0>	

|	I2 I1 I0	000	001	010	011	100	101	110	111
CB I4 I3		Progam Mode activated							
000									
001			Data_Exchange - - - -		I3 I2 I1 I0	(EEPROM READ ACCESS)			
010									
011			Write_Parameter I3 I2 I1 I0		I3 I2 I1 I0	(EEPROM WRITE ACCESS)			
100				Write_Var_ID_Code ID3 ID2 ID1 ID0					
101					0x0				
110		Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6	Broadcast	Rd_Status <S3:S0>	reserved
111		Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6	EnterPmode	Rd_Status <S3:S0>	reserved

3.4. Master Mode

Master Mode and the related Repeater and Monitor Modes differ completely in their functional properties from the Slave Mode. While the IC can autonomously perform different tasks in Slave Mode, it will only act as a physical layer transceiver in the Master, Repeater, and Monitor Modes.

The basic property of these modes is a modulation/demodulation of AS-i signals to Manchester-II code and vice versa. The following figure shows the different data path configurations.

Figure 3.4   Data Path in the Master, Repeater, and Monitor Modes
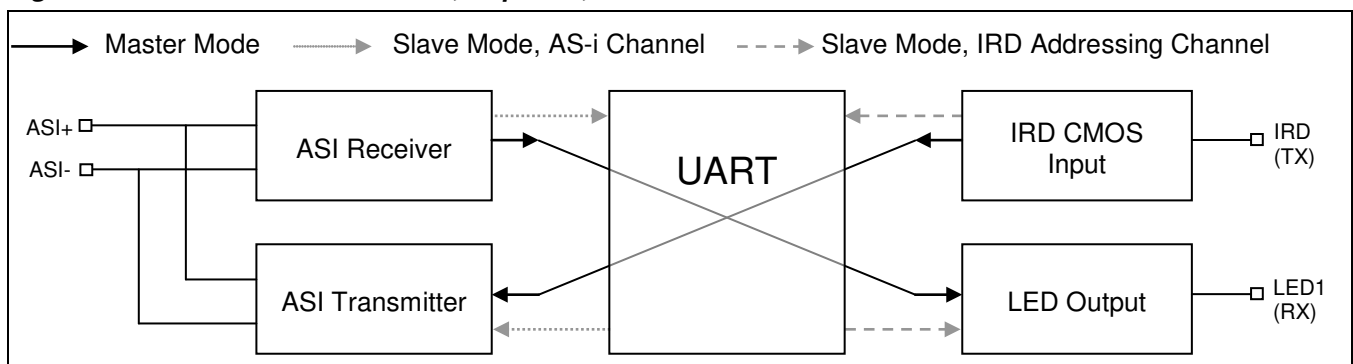
Master Mode, Repeater Mode, and Monitor Mode differ from each other in the kind of signals that are available at the data I/O and parameter port pins of the IC. The signal assignments in Table 3.3 are provided:

Table 3.3   Signal Assignments for Data I/O and Parameter Port Pins

PIN	MASTER MODE	REPEATER MODE	MONITOR MODE
P0	Receive Clock	Hi-Z	Receive Clock
P1	Power Fail	Hi-Z	Power Fail
P2	Receive Strobe – Slave Telegram	Hi-Z	Receive Strobe – Slave Telegram
P3	Hi-Z	Hi-Z	Receive Strobe – Master Telegram
DI0	Inverting of IRD input signal. If these two are on different levels, the IRD input signal is inverted before further processing; otherwise it is directly forwarded to the UART.		
DI1			
DI2	Inverting of LED output signal. If these two inputs are on different levels, the LED output signal is inverted after processing; otherwise it is directly forwarded to the LED1 output.		
DI3			
DO0	Hi-Z	Hi-Z	Pulse Code Error
DO1	Hi-Z	Hi-Z	No Information Error
DO2	Hi-Z	Hi-Z	Parity Bit Error
DO3	Hi-Z	Hi-Z	Manchester-II-Code Error at IRD Input

More detailed signal descriptions can be found in sections 4.6, 4.7, and 4.12.

3.5. EEPROM

The ASI4U provides an on-chip EEPROM with typical write times of 12.5ms and read times of 110ns. For security reasons, the memory area is structured in two independent data blocks and a single bit *Security* flag.

The data blocks are named the "User Area" and "Firmware Area." The Firmware Area block contains all manufacturing-related configuration data (e.g., selection of operational modes, ID codes). It can be protected against undesired data modification by setting the *Program_Mode_Disable* flag to 1.

The User Area contains only data that is relevant for changes in the final application (i.e., field installation of the slave module). The environment, where modifications of the user data might become necessary, can sometimes be rough and unpredictable. In order to ensure a write access cannot result in an undetected corruption of EEPROM data, additional security is provided when programming the User Area.

Any write access to the User Area (by the calls *Address_Assignment* or *Write_ID_Code1*) is accompanied by two write steps to the *Security* flag, one before and one after the actual modification of user data.

The following procedure is executed when writing to the *User Area* of the EEPROM:

1. The *Security* flag is programmed to 1.
2. The content of the *Security* flag is read back, verifying it was programmed to 1.
3. The user data is modified.
4. A read back of the written data is performed.
5. If the read back has proven successful programming of the user data, the *Security* flag is programmed back to 0.
6. The content of the *Security* flag is read back, verifying it was programmed to 0.

In addition to a read out of the data areas, the *Security* flag of the EEPROM is also read and evaluated during IC initialization. If the value of the *Security* flag equals 1 (e.g., due to an undesired interruption of a User Area write access), the entire User Area data is treated as corrupted and the Slave Address is set to 0_{HEX} in the corresponding volatile shadow registers during initialization. Then the programming of the User Area data can be repeated.

Table 3.4   EEPROM Contents

☐ User Area   ▨ Firmware Area

ASI4U Internal EEPROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
0	0 to 3	*A0 to A3*	Slave address low nibble
1	0	*A4*	Slave address high nibble
2	0 to 2	*ID1_Bit0 to ID1_Bit2*	*ID_Code_Extension_1*
2	3	*ID1_Bit3*	*ID_Code_Extension_1*, A/B slave selection in extended address mode
3 to 7			Not implemented
8	0 to 3	*ID_Bit0 to ID_Bit3*	*ID_Code*
9	0 to 3	*ID2_Bit0 to ID2_Bit3*	*ID_Code_Extension_2*
A	0 to 3	*IO_Bit0 to IO_Bit3*	*IO_Code*

ASI4U Internal EEPROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
B	0	Multiplex_Data	Multiplexed bi-directional Data Port mode
	1	Multiplex_Parameter	Multiplexed bi-directional Parameter Port mode
	2	P0_Watchdog_Activation	Watchdog can be activated/deactivated by the logic value at parameter pin P0. Watchdog_Active must **not** be set.
	3	Watchdog_Active	Communication watchdog is continuously activated.
C	0	Master_Mode	If set, Firmware Area cannot be accessed.
	1	Program_Mode_Disable	If set, Firmware Area is protected against overriding.
	2	Repeater_Mode	If set, Firmware Area cannot be accessed.
	3	Invert_Data_In	All Data Port inputs are inverted.
D	0 to 3	DI_Invert_Configuration	Enables separate input data inverting for selected DI pins. Invert_Data_In must **not** be set.
E	0 to 3	DI_Filter_Configuration	Enables anti-bouncing filters for selected DI pins
F	0 to 2	DI_Filter_Time_Constant	Defines a time constant for the input filter. For coding rules, see section 4.7.2.
	3	P1_Filter_Activation	If flag is set, the logic value at the parameter pin P1 determines whether the filter function is active or inactive (see section 4.6.2.) If flag is not set, DI_Filter_Configuration activates the filter function.
10	0 to 3	Data_Out_Configuration	Defines whether the corresponding Data Port output pin is driven by the Data Output Register (sensitive to the Data_Exchange command) or the Data_Out_Value register (EEPROM configured).
11	0 to 3	Data_Out_Value	Stores static Data Port output value if selected by Data_Out_Configuration

ASI4U Internal EEPROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
12	0	Enhanced_Status_Indication	If set, Enhanced Status Indication Mode according to the AS-Interface Complete Specification is activated. **Activates LED2 output! For compatibility to A²SI board layouts, this flag must not be set (= 0).**
	1	Dual_LED_Mode	If set, LED1 and LED2 output signals are controlled to comply with the dual LED indication configurations of AS-i. Generated signals also depend on the value of the Enhanced_Status_Indication flag. Direct connection of a dual LED is supported. **Activates LED2 output! For compatibility to A²SI board layouts, this flag must not be set (= 0).**
	2	FID_Invert	The FID input value is inverted before further processing.
	3	Safety_Mode	If set, the ASI4U/ASI4U-E/ASI4U-F Safety Mode is enabled and a special data input routing is activated.
13	0	Synchronous_Data_IO	Enables Synchronized Data I/O Mode
	1	P2_Sync_Data_IO_Activation	If flag is set, the logic value at the parameter pin P2 determines whether the Synchronous Data IO Mode is active or inactive. If flag is not set, the Synchronous Data IO Mode is always active if it was enabled by the Synchronous_Data_IO flag.
	2	Ext_Addr_4I/4O_Mode	Enables 4 Input / 4 Output support in Extended Address Mode.
	3	ID_Code1_Protect	If flag is set, ID_Code_Extension_1 is write-protected for user access. In Extended Address Mode, only bits 2 to 0 are blocked. Bit 3 is used for A/B slave selection and must remain user accessible.
14	0 to 3	ID1_Bit0 to ID1_Bit3	Protected_ID_Code_Extension_1 If the ID_Code1_Protect flag is set, a Read_ID_Code_1 request will be answered with the data stored in this register.
15	0 to 3		
16	0 to 3	Trim Area; accessible by IDT only	
17	0 to 3		

4 Detailed Functional Description

4.1. AS-i Receiver

The receiver detects (telegram) signals on the AS-i line, converts them to digital pulses, and forwards them to the UART for further processing. The receiver is internally connected between the ASIP and ASIN pins. It supports floating (ground free) input signals within the voltage limits of ASIP and ASIN given in Table 2.2.

Functionally, the receiver removes the DC value of the input signal, band-pass filters the AC signal, and extracts the digital output signals from the $\sin^2$-shaped input pulses via a set of comparators. The amplitude of the first pulse determines the threshold level for all subsequent pulses. This amplitude is digitally filtered to guarantee stable conditions and to suppress burst spikes. This approach combines a fast adaptation to changing signal amplitudes with a high detection safety. The comparators are reset after every detection of a telegram pause at the AS-i line. When the receiver is turned on, the transmitter is turned off to reduce the power consumption.

Table 4.1   Receiver Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
AC signal peak-peak amplitude (between ASIP and ASIN)	V_{SIG}		3	8	V_{PP}
Receiver comparator threshold level (refer to Figure 4.1)	V_{LSIGon}	Related to 1st pulse amplitude	45	55	%

Figure 4.1   Simplified Receiver Comparator Threshold Setup

DC Level

The IC determines the amplitude of the first negative pulse of the AS-i telegram. This amplitude is asserted to be V_{SIG} / 2.

First negative pulse of the AS-i telegram

V_{LSIGon}

$V_{LSIGon} = (0.45 \text{ to } 0.55) * V_{SIG} / 2$

$V_{SIG} / 2$