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ASM2I9940L

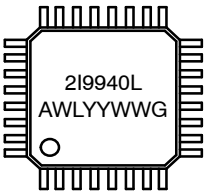
Low Voltage 1:18 Clock Distribution Chip

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

LQFP−32
CASE 873A



2I9940L = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

Functional Description

The ASM2I9940L is a 1:18 low Voltage Clock distribution chip with 2.5 V or 3.3 V LVCMOS output capabilities. The device features the capability to select either a differential LVPECL or LVCMOS compatible input. The 18 outputs are 2.5 V or 3.3 V LVCMOS compatible and feature the drive strength to drive 50 Ω series or parallel terminated transmission lines. With output−to−output skews of 150 pS, the ASM2I9940L is ideal as a clock distribution chip for the most demanding of Synchronous systems. The 2.5 V outputs also make the device ideal for supplying clocks for a high performance microprocessor based design.

With low output impedance (≈20 Ω), in both the HIGH and LOW logic states, the output buffers of the ASM2I9940L are ideal for driving series terminated transmission lines. With a 20 Ω output impedance the ASM2I9940L has the capability of driving two series terminated lines from each output. This gives the device an effective fanout of 1:36.

The differential LVPECL inputs of the ASM2I9940L allow the device to interface directly with a LVPECL fanout buffer to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the LVCMOS level clock input. All inputs of the ASM2I9940L have internal pullup/pulldown resistor, so they can be left open if unused.

The ASM2I9940L is a single or dual supply device. The device power supply offers a high degree of flexibility. The device can operate with a 3.3 V core and 3.3 V output, a 3.3 V core and 2.5 V outputs as well as a 2.5 V core and 2.5 V outputs. The 32−lead LQFP Package was chosen to optimize performance, board space and cost of the device. The 32−lead LQFP Package has a 7 x 7 mm^2 body size with conservative 0.8 mm pin spacing.

Features

- LVPECL or LVCMOS Clock Input
- 2.5 V LVCMOS Outputs for Intel® Pentium® II Microprocessor Support
- 150 pS Maximum Output−to−Output Skew
- Maximum Output Frequency of 250 MHz
- 32 Lead LQFP Package
- Dual or Single Supply Device:
  - Dual V_{CC} Supply Voltage, 3.3 V Core and 2.5 V Output
  - Single 3.3 V V_{CC} Supply Voltage for 3.3 V Outputs
  - Single 2.5 V V_{CC} Supply Voltage for 2.5 V I/O
- Pin and Function compatible to MPC940L, MPC9109, CY29940 and CY29940−1
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

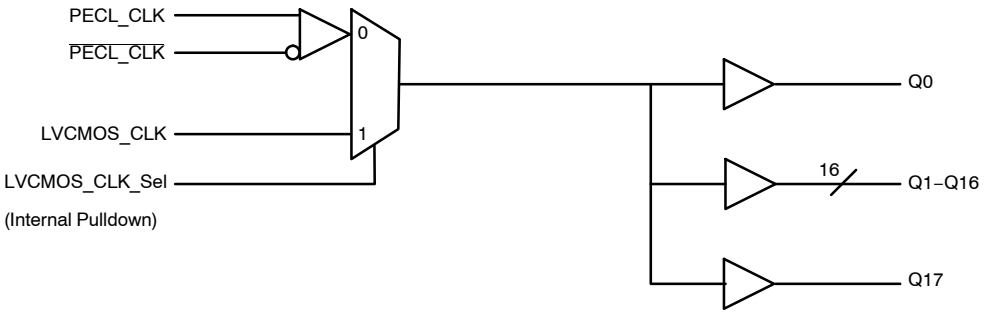


Figure 1. Block Diagram

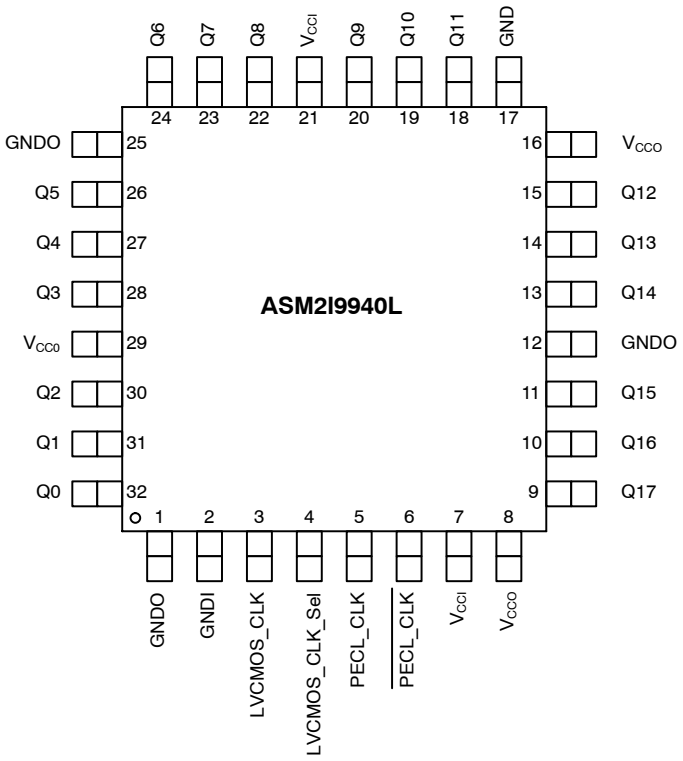


Figure 2. Pin Diagram

Table 1. FUNCTION TABLE

LVCMOS_CLK_Sel	Input
0	PECL_CLK
1	LVCMOS_CLK

Table 2. POWER SUPPLY VOLTAGES

Supply Pin	Voltage Level
V_{CCI}	2.5 V or 3.3 V ± 5%
V_{CCO}	2.5 V or 3.3 V ± 5%

Table 3. PIN CONFIGURATIONS

Pin #	Pin Name	I/O	Type	Function
5 6	PECL_CLK $\overline{\text{PECL\_CLK}}$	Input	LVPECL	LVPECL Clock Inputs
3	LVCMOS_CLK	Input	LVCMOS	LVCMOS Clock Input
4	LVCMOS_CLK_Sel	Input	LVCMOS	Selects either LVPECL or LVCMOS input as Clock Source
32, 31, 30, 28, 27, 26, 24, 23, 22, 20, 19, 18, 15, 14, 13, 11, 10, 9	Q0 – Q17	Output	LVCMOS	Clock Outputs
2	GNDI		Supply	Core Negative Power Supply
1, 12, 17, 25	GNDO		Supply	Output Negative Power Supply
7, 21	V_{CCI}		Supply	Core Positive Power Supply
8, 16, 29	V_{CCO}		Supply	Output Positive Power Supply

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C
T_s	Max. Soldering Temperature (10 sec)		260	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22–A114–B)		2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CCI} = 3.3 V ± 5%, V_{CCO} = 3.3 V ± 5%)

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage	CMOS_CLK		2.4		V_{CCI}	V
V_{IL}	Input LOW Voltage	CMOS_CLK				0.8	V
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK		500		1000	mV
V_{CMR}	Common Mode Range	PECL_CLK		V_{CCI} – 1.4		V_{CCI} – 0.6	V
V_{OH}	Output HIGH Voltage		I_{OH} = –20 mA	2.4			V
V_{OL}	Output LOW Voltage		I_{OL} = 20 mA			0.5	V
I_{IN}	Input Current					±200	μA
C_{IN}	Input Capacitance				4.0		pF
C_{pd}	Power Dissipation Capacitance		per output		10		pF
Z_{OUT}	Output Impedance			18	23	28	Ω
I_{CC}	Maximum Quiescent Supply Current				0.5	1.0	mA

Table 6. AC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CCI} = 3.3 V ± 5%, V_{CCO} = 3.3 V ± 5%)

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
F_{max}	Maximum Input Frequency					250	MHz
t_{PLH}	Propagation Delay	PECL_CLK ≤ 150 MHz CMOS_CLK ≤ 150 MHz	(Note 1)	2.0 1.7	2.7 2.5	3.4 3.0	nS
t_{PLH}	Propagation Delay	PECL_CLK > 150 MHz CMOS_CLK > 150 MHz		2.0 1.8	2.9 2.5	3.7 3.2	nS
$t_{sk(o)}$	Output−to−output Skew	PECL_CLK CMOS_CLK	(Note 1)			150 150	pS
$t_{sk(pp)}$	Part−to−Part Skew	PECL_CLK ≤ 150 MHz CMOS_CLK ≤ 150 MHz	(Notes 1 and 2)			1.5 1.3	nS
$t_{sk(pp)}$	Part−to−Part Skew	PECL_CLK > 150 MHz CMOS_CLK > 150 MHz	(Notes 1 and 2)			1.8 1.5	nS
$t_{sk(pp)}$	Part−to−Part Skew	PECL_CLK CMOS_CLK	(Notes 1 and 3)			850 750	pS
DC	Output Duty Cycle	f_{CLK} < 134 MHz f_{CLK} ≤ 250 MHz	Input DC = 50% Input DC = 50%	45 40	50 50	55 60	%
t_r, t_f	Output Rise/Fall Time		0.5 − 2.4 V	0.3		1.1	nS

1. Tested using standard input levels, Production tested @ 150 MHz.
2. Across temperature and voltage ranges, includes output skew.
3. For a specific temperature and voltage, includes output skew.

Table 7. DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CCI} = 3.3 V ± 5%, V_{CCO} = 2.5 V ± 5%)

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage	CMOS_CLK		2.4		V_{CCI}	V
V_{IL}	Input LOW Voltage	CMOS_CLK				0.8	V
V_{PP}	Peak−to−Peak Input Voltage	PECL_CLK		500		1000	mV
V_{CMR}	Common Mode Range	PECL_CLK		V_{CCI} − 1.4		V_{CCI} − 0.6	V
V_{OH}	Output HIGH Voltage		I_{OH} = −12 mA	1.8			V
V_{OL}	Output LOW Voltage		I_{OL} = 12 mA			0.5	V
I_{IN}	Input Current					±200	μA
C_{IN}	Input Capacitance				4.0		pF
C_{pd}	Power Dissipation Capacitance		per output		10		pF
Z_{OUT}	Output Impedance				23		Ω
I_{CC}	Maximum Quiescent Supply Current				0.5	1.0	mA

Table 8. AC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CCI} = 3.3 V ± 5%, V_{CCO} = 2.5 V ± 5%)

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
F_{max}	Maximum Input Frequency					250	MHz
t_{PLH}	Propagation Delay	PECL_CLK ≤ 150 MHz CMOS_CLK ≤ 150 MHz	(Note 4)	2.0 1.7	2.8 2.5	3.5 3.0	nS
t_{PLH}	Propagation Delay	PECL_CLK > 150 MHz CMOS_CLK > 150 MHz		2.0 1.8	2.9 2.5	3.8 3.3	nS
$t_{sk(o)}$	Output−to−output Skew	PECL_CLK CMOS_CLK	(Note 4)			150 150	pS
$t_{sk(pp)}$	Part−to−Part Skew	PECL_CLK ≤ 150 MHz CMOS_CLK ≤ 150 MHz	(Notes 4 and 5)			1.5 1.3	nS
$t_{sk(pp)}$	Part−to−Part Skew	PECL_CLK > 150 MHz CMOS_CLK > 150 MHz	(Notes 4 and 5)			1.8 1.5	nS
$t_{sk(pp)}$	Part−to−Part Skew	PECL_CLK CMOS_CLK	(Notes 4 and 6)			850 750	pS
DC	Output Duty Cycle	f_{CLK} < 134 MHz f_{CLK} ≤ 250 MHz	Input DC = 50% Input DC = 50%	45 40	50 50	55 60	%
t_r, t_f	Output Rise/Fall Time		0.5 − 1.8 V	0.3		1.2	nS

4. Tested using standard input levels, Production tested @ 150 MHz.
5. Across temperature and voltage ranges, includes output skew.
6. For a specific temperature and voltage, includes output skew.

Table 9. DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CCI} = 2.5 V ± 5%, V_{CCO} = 2.5 V ± 5%)

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage	CMOS_CLK		2.0		V_{CCI}	V
V_{IL}	Input LOW Voltage	CMOS_CLK				0.8	V
V_{PP}	Peak−to−Peak Input Voltage	PECL_CLK		500		1000	mV
V_{CMR}	Common Mode Range	PECL_CLK		V_{CCI} − 1.0		V_{CCI} − 0.6	V
V_{OH}	Output HIGH Voltage		I_{OH} = −12 mA	1.8			V
V_{OL}	Output LOW Voltage		I_{OL} = 12 mA			0.5	V
I_{IN}	Input Current					±200	μA
C_{IN}	Input Capacitance				4.0		pF
C_{pd}	Power Dissipation Capacitance		per output		10		pF
Z_{OUT}	Output Impedance			18	23	28	Ω
I_{CC}	Maximum Quiescent Supply Current				0.5	1.0	mA

Table 10. AC Characteristics (T_A = 0°C to 70°C, V_{CCI} = 2.5 V ± 5%, V_{CCO} = 2.5 V ± 5%)

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
F_{max}	Maximum Input Frequency					200	MHz
t_{PLH}	Propagation Delay	PECL_CLK ≤ 150 MHz CMOS_CLK ≤ 150 MHz	(Note 7)	2.6 2.3	4.0 3.1	5.2 4.0	nS
t_{PLH}	Propagation Delay	PECL_CLK > 150 MHz CMOS_CLK > 150 MHz		2.8 2.3	3.8 3.1	5.0 4.0	nS
$t_{sk(o)}$	Output−to−output Skew Within one bank	PECL_CLK CMOS_CLK	(Note 7)			200 200	pS
$t_{sk(pp)}$	Part−to−Part Skew	PECL_CLK ≤ 150 MHz CMOS_CLK ≤ 150 MHz	(Notes 7 and 8)			2.6 1.7	nS
$t_{sk(pp)}$	Part−to−Part Skew	PECL_CLK > 150 MHz CMOS_CLK > 150 MHz	(Notes 7 and 8)			2.2 1.7	nS
$t_{sk(pp)}$	Part−to−Part Skew	PECL_CLK CMOS_CLK	(Notes 7 and 9)			1.2 1.0	nS
DC	Output Duty Cycle	f_{CLK} < 134 MHz f_{CLK} ≤ 200 MHz	Input DC = 50% Input DC = 50%	45 40	50 50	55 60	%
t_r, t_f	Output Rise/Fall Time		0.5 − 1.8 V	0.3		1.2	nS

7. Tested using standard input levels, Production tested @ 150 MHz.
8. Across temperature and voltage ranges, includes output skew.
9. For a specific temperature and voltage, includes output skew.

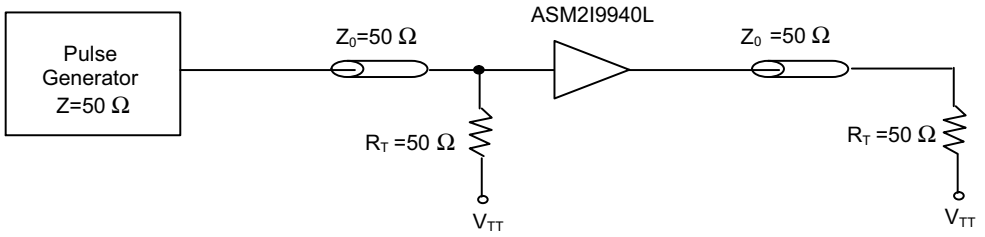


Figure 3. LVCMOS_CLK ASM2I9940L AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

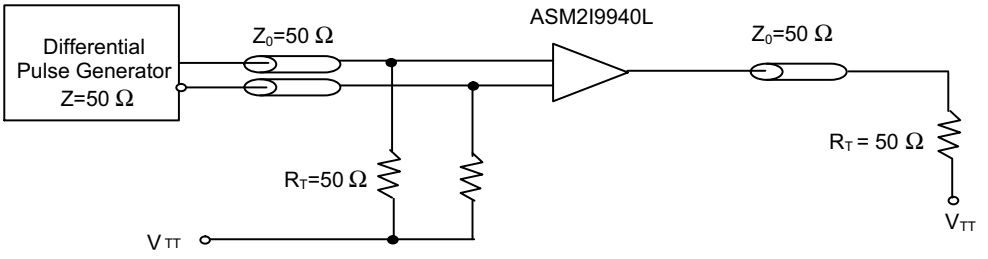


Figure 4. PECL_CLK ASM2I9940L AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

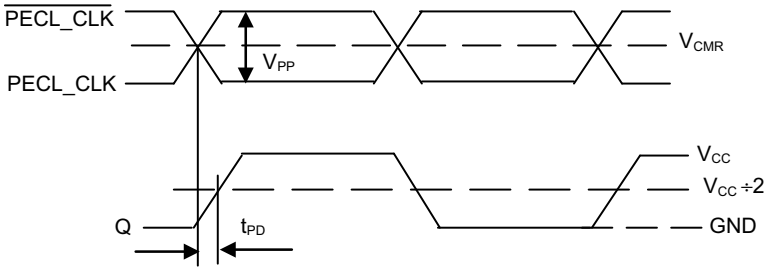


Figure 5. Propagation Delay (t_{PD}) Test Reference

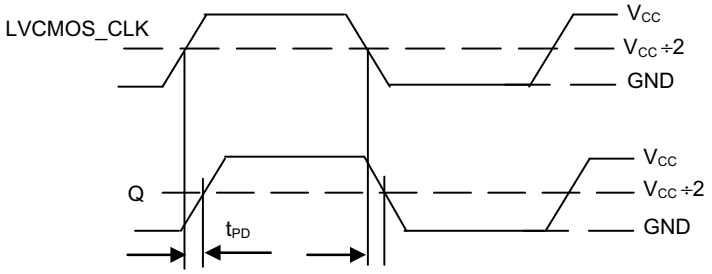
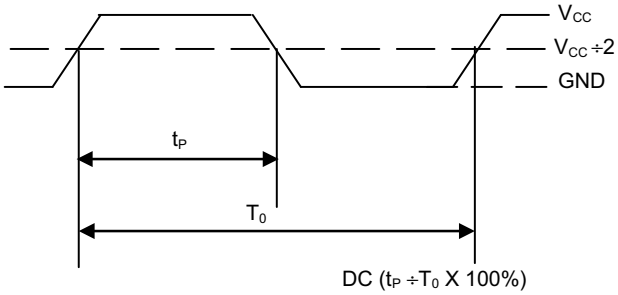
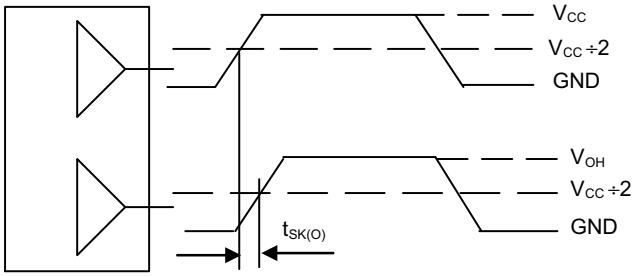


Figure 6. LVCMOS Propagation Delay (t_{PD}) Test Reference



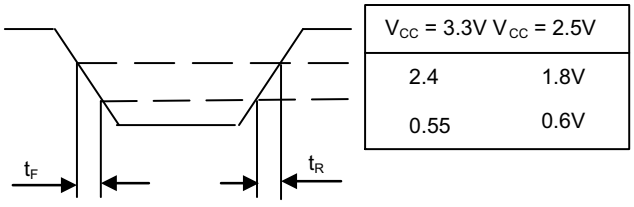
The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 7. Output Duty Cycle (DC)



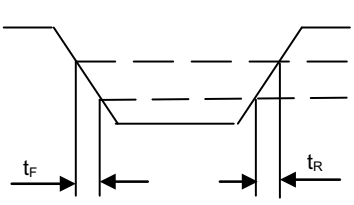
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output–to–Output Skew $t_{SK(O)}$



V_{CC} = 3.3V	V_{CC} = 2.5V
2.4	1.8V
0.55	0.6V

Figure 9. Output Transition Time Test Reference



V_{CC} = 3.3V	V_{CC} = 2.5V
2.0	1.7V
0.8	0.7V

Figure 10. Input Transition Time Test Reference

Power Consumption of the ASM2I9940L and Thermal Management

The ASM2I9940L AC specification is guaranteed for the entire operating frequency range up to 250 MHz. The ASM2I9940L power consumption and the associated long−term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the ASM2I9940L die junction temperature and the associated device reliability.

Table 11. DIE JUNCTION TEMPERATURE AND MTBF

Junction Temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system−defined tolerable MTBF, the die junction temperature of the ASM2I9940L needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the ASM2I9940L is represented in Equation 1.

Where I_{CCQ} is the static current consumption of the ASM2I9940L, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 12 in case of the ASM2I9940L). The ASM2I9940L supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from Equation 1. Using parallel termination output termination results in Equation 2 for power dissipation.

In Equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL}, I_{OL}, V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in Equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

Where $R_{\theta ja}$ is the thermal impedance of the package (junction−to−ambient) and T_A is the ambient temperature. According to Table 11, the junction temperature can be used to estimate the long−term device reliability. Further, combining Equation 1 and Equation 2 results in a maximum operating frequency for the ASM2I9940L in a series terminated transmission line system, Equation 4.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \quad \text{(eq. 1)}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[DC_Q \cdot I_{OH}\left(V_{CC} - V_{OH}\right) + \left(1 - DC_Q\right) \cdot I_{OL} \cdot V_{OL} \right] \quad \text{(eq. 2)}$$

$$T_J = T_A + P_{TOT} \cdot R_{\theta JA} \quad \text{(eq. 3)}$$

$$f_{CLOCKMAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}{}^2} \cdot \left[\frac{T_{JMAX} - T_A}{R_{\theta JA}} - \left(I_{CCQ} \cdot V_{CC} \right) \right] \quad \text{(eq. 4)}$$

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 11. $R_{\theta ja}$ can be derived from Table 12. The $R_{\theta ja}$ represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

Table 12. THERMAL PACKAGE IMPEDANCE OF THE 32LQFP

Convection, LFPM	R_{thja} (1P2S board), °C/W	R_{thja} (2P2S board), °C/W
Still air	86	61
100 lfpm	76	56
200 lfpm	71	54
300 lfpm	68	53
400 lfpm	66	52
500 lfpm	60	49

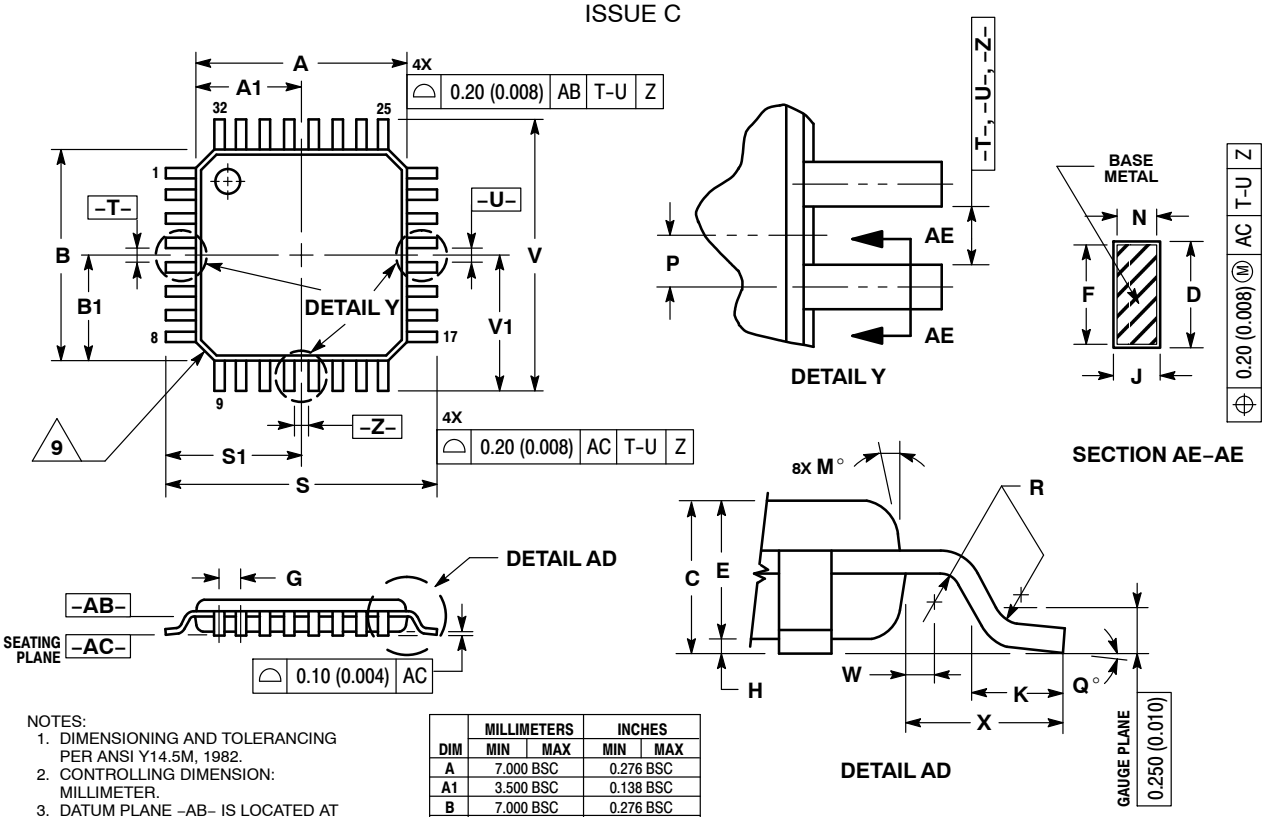
If the calculated maximum frequency is below 250 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the ASM2I9940L. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to an estimated MTBF of 9.1 years (4 years), a supply voltage of 3.3 V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.

ORDERING INFORMATION

Part Number	Marking	Package	Temperature	Shipping†
ASM2I9940LG−32LT	2I9940L	32−pin LQFP Pb−Free	−40°C to +85°C	250 Units / Tray

PACKAGE DIMENSIONS

32 LEAD LQFP
CASE 873A–02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.750	0.018	0.030
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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