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Rev. Date: Aug, 06, 2015

ATPAT16L64A6SQC4M

128MB DDR-400 UNBUFFERED NON-ECC SODIMM

DESCRIPTION

The ATP AT16L64A6SQC4M is a high performance 128MB DDR-400 Unbuffered NON-ECC SDRAM memory module. It is organized as 16M x 64 in a 200-pin Small Outline Dual-In-Line Memory Module (SODIMM) package. The module utilizes four 16Mx16 DDR SDRAMs in TSOP-II package. The module consists of a 256-byte serial EEPROM, which contains the module configuration information.

KEY FEATURES

- High Density: 128MB (16M x 64)
- DIMM Rank: 1 Rank
- Cycle Time: 5ns (200MHz)
- CAS Latency: 3
- Double-data rate architecture; two data transfers per clock cycle
- Power supply: 2.5V ± 0.2V
- RoHS compliant
- Burst lengths: 2, 4, 8
- Auto & Self refresh
- 7.8 μs refresh interval (8K/64ms refresh)
- SSTL_2 Interface
- PCB Height: 1.25 inches
- Minimum Thickness of Golden Finger: 30 Micro-inch

Part No.	Max Freq	Interface
AT16L64A6SQC4M	200MHz (5ns@CL=3) x2	SSTL_2

PIN DESCRIPTION

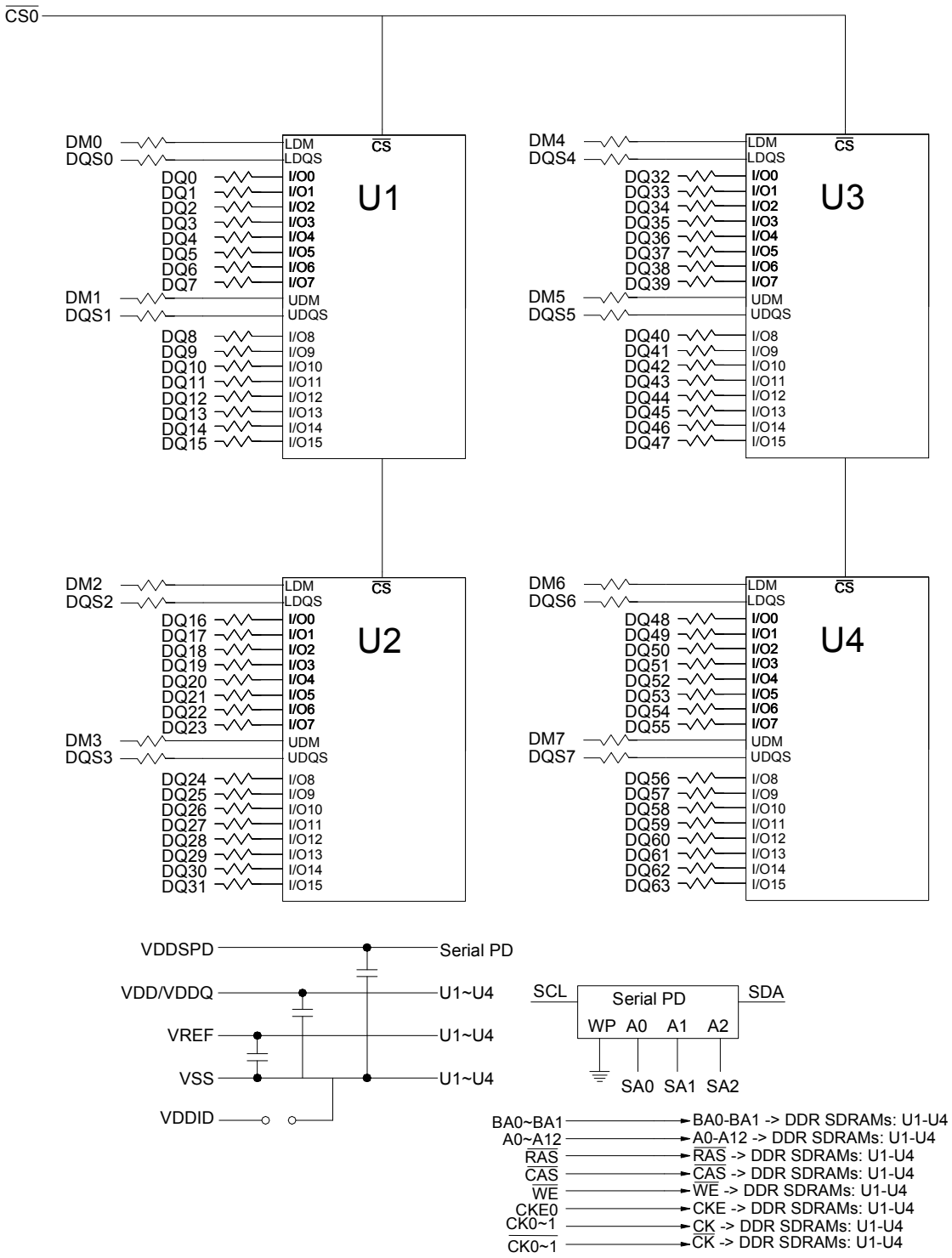
Pin Name	Description	Pin Name	Description
A0~A12	Address bus	CK0~CK1	Clock (Positive line of differential pair)
BA0~BA1	Bank select	$\overline{CK0}$ ~ $\overline{CK1}$	Clock (negative line of differential)
DQ0~DQ63	Memory data bus	SCL	IIC serial bus clock for EEPROM
$\overline{RAS}$	Row address strobe	SDA	IIC serial bus data line for EEPROM
$\overline{CAS}$	Column address strobe	SA0-SA2	IIC slave address select for EEPROM
$\overline{WE}$	Write strobe	VDD	Positive power supply
$\overline{CS0}$	Chip select lines	VDDQ	I/O Driver positive power supply
CKE0	Clock enable lines	VREF	I/O reference supply
DQS0~DQS7	Low data strobes	VSS	Power supply return (ground)
NC	No Connection	VDDSPD	EEPROM positive power supply (2.5V)
DNU	Do Not Useable	DM0~DM7	Input data mask

Your Ultimate Memory Solution!

PIN ASSIGNMENT

No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	VREF	101	A9	2	VREF	102	A8
3	VSS	103	VSS	4	VSS	104	VSS
5	DQ0	105	A7	6	DQ4	106	A6
7	DQ1	107	A5	8	DQ5	108	A4
9	VDD	109	A3	10	VDD	110	A2
11	DQS0	111	A1	12	DM0	112	A0
13	DQ2	113	VDD	14	DQ6	114	VDD
15	VSS	115	A10	16	VSS	116	BA1
17	DQ3	117	BA0	18	DQ7	118	$\overline{RAS}$
19	DQ8	119	$\overline{WE}$	20	DQ12	120	$\overline{CAS}$
21	VDD	121	$\overline{CS0}$	22	VDD	122	NC
23	DQ9	123	NC	24	DQ13	124	NC
25	DQS1	125	VSS	26	DM1	126	VSS
27	VSS	127	DQ32	28	VSS	128	DQ36
29	DQ10	129	DQ33	30	DQ14	130	DQ37
31	DQ11	131	VDD	32	DQ15	132	VDD
33	VDD	133	DQS4	34	VDD	134	DM4
35	CK0	135	DQ34	36	VDD	136	DQ38
37	$\overline{CK0}$	137	VSS	38	VSS	138	VSS
39	VSS	139	DQ35	40	VSS	140	DQ39
KEY		141	DQ40	KEY		142	DQ44
41	DQ16	143	VDD	42	DQ20	144	VDD
43	DQ17	145	DQ41	44	DQ21	146	DQ45
45	VDD	147	DQS5	46	VDD	148	DM5
47	DQS2	149	VSS	48	DM2	150	VSS
49	DQ18	151	DQ42	50	DQ22	152	DQ46
51	VSS	153	DQ43	52	VSS	154	DQ47
53	DQ19	155	VDD	54	DQ23	156	VDD
55	DQ24	157	VDD	56	DQ28	158	$\overline{CK1}$
57	VDD	159	VSS	58	VDD	160	CK1
59	DQ25	161	VSS	60	DQ29	162	VSS
61	DQS3	163	DQ48	62	DM3	164	DQ52
63	VSS	165	DQ49	64	VSS	166	DQ53
65	DQ26	167	VDD	66	DQ30	168	VDD
67	DQ27	169	DQS6	68	DQ31	170	DM6
69	VDD	171	DQ50	70	VDD	172	DQ54
71	DNU	173	VSS	72	DNU	174	VSS
73	DNU	175	DQ51	74	DNU	176	DQ55
75	VSS	177	DQ56	76	VSS	178	DQ60
77	DNU	179	VDD	78	DNU	180	VDD
79	DNU	181	DQ57	80	DNU	182	DQ61
81	VDD	183	DQS7	82	VDD	184	DM7
83	DNU	185	VSS	84	DNU	186	VSS
85	NC	187	DQ58	86	NC	188	DQ62
87	VSS	189	DQ59	88	VSS	190	DQ63
89	DNU	191	VDD	90	VSS	192	VDD
91	DNU	193	SDA	92	VDD	194	SA0
93	VDD	195	SCL	94	VDD	196	SA1
95	NC	197	VDDSPD	96	CKE0	198	SA2
97	NC	199	NC	98	NC	200	NC
99	A12			100	A11		

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM DC RATINGS

Item	Symbol	Rating	Units	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-1.0V ~ 3.6V	V	1
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5V ~ 3.6V	V	1
Storage Temperature	T_{STG}	-55 to +150	°C	1,2
Operating Temperature (Ambient)	T_A	0 to +70	°C	1

Note:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. It is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC OPERATING CONDITIONS (SSTL_2)

Recommended operating conditions

Item	Symbol	Min.	Typical	Max.	Units
Supply Voltage	V_{DD}	2.3	2.5	2.7	V
Supply Voltage for Output [4]	V_{DDQ}	2.3	2.5	2.7	V
Input Reference Voltage[1,2]	V_{REF}	0.49 * V_{DDQ}	0.50 * V_{DDQ}	0.51 * V_{DDQ}	V
Termination Voltage[3]	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
Input High Voltage (DC)	V_{IH} (DC)	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V
Input High Voltage (AC)	V_{IH} (AC)	V_{REF} + 0.31	-	-	V
Input Low Voltage (DC)	V_{IL} (DC)	-0.3	-	V_{REF} - 0.15	V
Input Low Voltage (AC)	V_{IL} (AC)	-	-	V_{REF} - 0.31	V

Note:
1. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
2. Peak to peak AC noise on V_{REF} may not exceed ±2% V_{REF} (DC).
3. V_{TT} of transmitting device must track V_{REF} of receiving device.
4. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

CAPACITANCE

(V_{DD}=2.5V, V_{DDQ}=2.5V, TA=25°C)

Parameter	Symbol	Max.	Unit
Input Capacitance (CKE, /CS)	C_{I1}	38	pF
Input Capacitance (Addr, /RAS, /CAS, /WE)	C_{I2}	45	pF
Input Capacitance (CK, /CK)	C_{CK}	30	pF
Input/Output Capacitance (DQ, DM)	C_{IO}	7	pF

IDD SPECIFICATION PARAMETER

Values are for the AT16L64A6SQC4M DDR SDRAM only and are computed from values specified in the MT46V16M16P-5B:M component data sheet

Symbol	Proposed Conditions	Value	Units
IDD0	**Operating one bank active-precharge current;** tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRAS(IDD); DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	540	mA
IDD1	**Operating current**; **(one bank active)** Burst=2 t_{RC} min, I_{OUT}=0mA, Active-Read-Precharge	740	mA
IDD2P	**Precharge power-down standby current;** CKE ≤ V_{IL}, t_{CK} min., All banks idle	16	mA
IDD2F	**Precharge Floating standby current;** CS# > =V_{IH}(min);All banks idle; CKE > = V_{IH}(min); t_{CK}= tCK(IDD); Address and other control inputs changing once per clock cycle; V_{IN} = Vref for DQ,DQS and DM	240	mA
IDD3P	**Active standby current in power-down mode;** All banks idle, CKE ≤ V_{IL} (max), t_{CK} min.	160	mA
IDD3N	**Active standby current in Non power-down mode;** One bank; Active-Precharge, t_{RC}=t_{RAS} (max.), t_{CK} min	280	mA
IDD4W	**Operating burst write current;** Burst=2, t_{CK} min.	860	mA
IDD4R	**Operating burst read current;** Burst=2, t_{CK} min., I_{OUT}=0 mA	1,040	mA
IDD5	**Burst auto refresh current;** t_{RFC} = t_{RFC} (min)	1,040	mA
IDD5A	**Burst auto refresh current;** t_{RFC} =7.8125µs	24	mA
IDD6	**Self refresh current**; CKE ≤ 0.2V	16	mA
IDD7	**Operating current - Four bank operation**; Four bank interleaving with BL=4	2,046	mA

TIMING PARAMETER

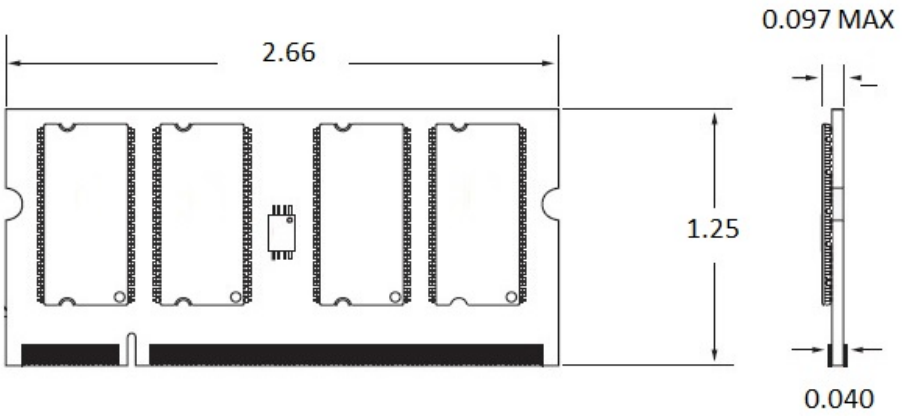
Parameter	Symbol	DDR-400		Units
		min	Max	
Clock cycle time at CL=3	tCK	5	10	ns
$\overline{RAS}$ to $\overline{CAS}$ delay	tRCD	15	-	ns
Row precharge time	tRP	15	-	ns
Row cycle time	tRC	55	-	ns
Row active time	tRAS	40	70000	ns
DQ output access time from CK, $\overline{CK}$	tAC	-650	650	ps
DQS output access time from CK, $\overline{CK}$	tDQSCK	-550	550	ps
CK high-level width	tCH	0.45	0.55	tCK
CK low-level width	tCL	0.45	0.55	tCK
CK half period	tHP	min(tCL, tCH)	-	ns
DQ and DM input hold time	tDH(base)	400	-	ps
DQ and DM input setup time	tDS(base)	400	-	ps
Control & Address input pulse width for each input	tIPW	2.2	-	ns
DQ and DM input pulse width for each input	tDIPW	1.75	-	ns
Data-out high-impedance time from CK, $\overline{CK}$	tHZ	tAC(min)	tAC (max)	ps
DQ low-impedance time from CK, $\overline{CK}$	tLZ	tAC(min)	tAC (max)	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	400	ps
DQ hold skew factor	tQHS	-	500	ps
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	ps
First DQS latching transition to associated clock edge	tDQSS	0.72	1.28	tCK
DQS input high pulse width	tDQSH	0.35	-	tCK
DQS input low pulse width	tDQSL	0.35	-	tCK
DQS falling edge to CK setup time	tDSS	0.2	-	tCK
DQS falling edge hold time from CK	tDSH	0.2	-	tCK
Mode register set command cycle time	tMRD	10	-	ns
Write postamble	tWPST	0.4	0.6	tCK
Write preamble	tWPRE	0.25	-	tCK
Address and control input hold time	tIH(base)	600	-	ps
Address and control input setup time	tIS(base)	600	-	ps
Read preamble	tRPRE	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	tCK
Active to active command period	tRRD	10	-	ns
Write recovery time	tWR	15	-	ns
Auto precharge write recovery + precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		tCK
Internal write to read command delay	tWTR	2	-	tCK
Exit self refresh to a non-read command	tXSNR	75	-	ns
Exit self refresh to a read command	tXSRD	200	-	tCK

PHYSICAL DIMENSIONS (UNITS IN INCHES)

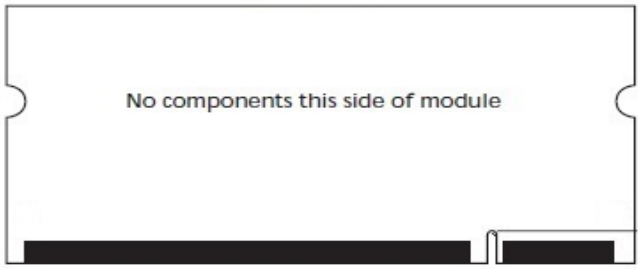
(Drawing not to scale)

200-pin SODIMM

Front



Back



Note: Tolerance on all dimensions ±0.006 inch (0.15mm) unless otherwise noted