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PRELIMINARY PRODUCT SPECIFICATION

SHARP

Integrated Circuits Group

# LHF00L15
## Flash Memory
## 32M (2Mb x 16)

(Model Number: LHF00L15)

Spec. Issue Date: June 16, 2004
Spec No: EL163056A

SHARP

| SPEC No. | EL163056A |
|---|---|

ISSUE: Jun. 16, 2004

To;

# SPECIFICATIONS

Product Type 32Mbit Flash Memory

**LHF00L15**

Model No. (LHF00L15)

If you have any objections, please contact us before issuing purchasing order.

* This specifications contains 34 pages including the cover and appendix.
* Refer to LHF00LXX series Appendix (FUM03802).

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY: Y. Hotta

Y. HOTTA
Dept. General Manager

REVIEWED BY:

PREPARED BY: Sotani

Product Development Dept. I
System-Flash Division
Integrated Circuits Group
SHARP CORPORATION

• When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliance
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

• Please direct all queries regarding the products covered herein to a sales representative of the company.

# CONTENTS

# LHF00L15
# 32Mbit (2Mbit×16)
# Flash MEMORY

■ 32-M density with 16-bit I/O Interface

■ Read Operation
- 90ns

■ Low Power Operation
- 2.7V Read and Write Operations
- Automatic Power Savings Mode reduces $I_{CCR}$ in Static Mode

■ Enhanced Code + Data Storage
- 5µs Typical Erase/Program Suspends

■ OTP (One Time Program) Block
- 4-Word Factory-Programmed Area
- 4-Word User-Programmable Area

■ Operating Temperature -40°C to +85°C

■ CMOS Process (P-type silicon substrate)

■ Flexible Blocking Architecture
- Eight 4-Kword Parameter Blocks
- One 32-Kword Block
- Thirty-one 64-Kword Blocks
- Bottom Parameter Location

■ Enhanced Data Protection Features
- Individual Block Lock and Block Lock-Down with Zero-Latency
- All blocks are locked at power-up or device reset.
- Block Erase, Full Chip Erase, Word Program Lockout during Power Transitions

■ Automated Erase/Program Algorithms
- 3.0V Low-Power 10µs/Word (Typ.) Programming
- 12.0V No Glue Logic 9µs/Word (Typ.) Production Programming and 0.8s Erase (Typ.)

■ Cross-Compatible Command Support
- Basic Command Set
- Common Flash Interface (CFI)

■ Extended Cycling Capability
- Minimum 100,000 Block Erase Cycles

■ 48-Lead TSOP (Normal Bend)

■ ETOX™* Flash Technology

■ Not designed or rated as radiation hardened

The product is a low power, high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at $V_{CC}$=2.7V-3.6V. Its low voltage operation capability greatly extends battery life for portable applications.

The memory array block architecture utilizes Enhanced Data Protection features, which provides maximum flexibility for safe nonvolatile code and data storage.

Special OTP (One Time Program) block provides an area to store permanent code such as an unique number.

* ETOX is a trademark of Intel Corporation.

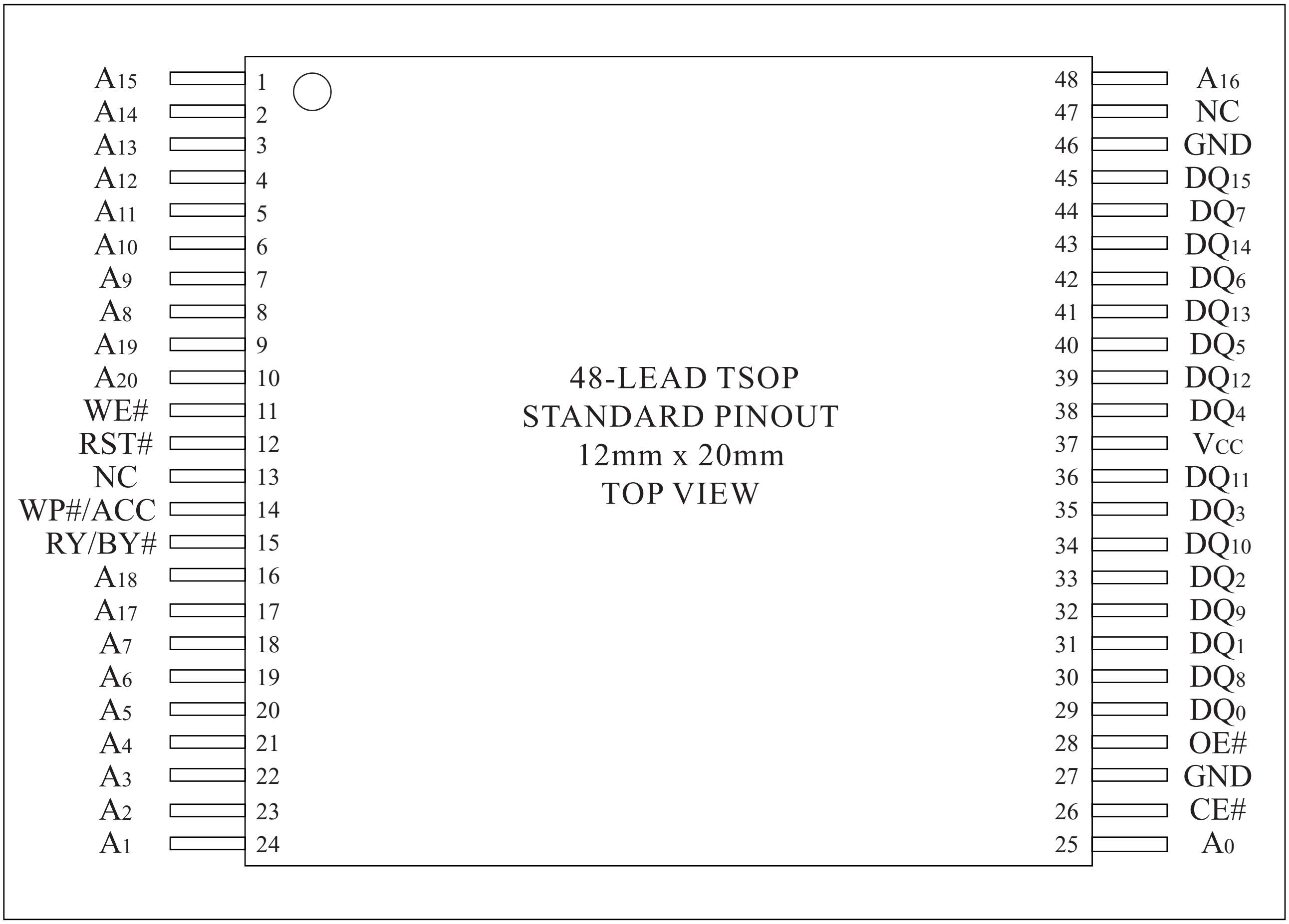



Figure 1. 48-Lead TSOP (Normal Bend) Pinout

Table 1. Pin Descriptions

| Symbol | Type | Name and Function |
|---|---|---|
| $A_{20}$-$A_0$ | INPUT | ADDRESS INPUTS: Inputs for addresses. |
| $DQ_{15}$-$DQ_0$ | INPUT/ OUTPUT | DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code, identifier code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle. |
| CE# | INPUT | CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high ($V_{IH}$) deselects the device and reduces power consumption to standby levels. |
| RST# | INPUT | RESET: When low ($V_{IL}$), RST# resets internal automation and inhibits write operations which provides data protection. RST#-high ($V_{IH}$) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RST# must be low during power-up/down. |
| OE# | INPUT | OUTPUT ENABLE: Gates the device's outputs during a read cycle. |
| WE# | INPUT | WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of CE# or WE# (whichever goes high first). |
| WP#/ACC | INPUT/ SUPPLY | WRITE PROTECT: When WP#/ACC is $V_{IL}$, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and not locked-down. When WP#/ACC is $V_{IH}$, lock-down is disabled.<br>Applying 12.0V±0.3V to WP#/ACC provides fast erasing or fast programming mode. In this mode, WP#/ACC is power supply pin. Applying 12.0V±0.3V to WP#/ACC during erase/program can only be done for a maximum of 1,000 cycles on each block. WP#/ ACC may be connected to 12.0V±0.3V for a total of 80 hours maximum. Use of this pin at 12.0V+0.3V beyond these limits may reduce block cycling capability or cause permanent damage. |
| RY/BY# | OPEN DRAIN OUTPUT | READY/BUSY#: Indicates the status of the internal WSM (Write State Machine). When low, WSM is performing an internal operation (block erase, full chip erase, program or OTP program). RY/BY#-High Z indicates that the WSM is ready for new commands, block erase is suspended and program is inactive, program is suspended, or the device is in reset mode. |
| $V_{CC}$ | SUPPLY | DEVICE POWER SUPPLY (2.7V-3.6V): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid $V_{CC}$ voltage (see DC Characteristics) produce spurious results and should not be attempted. |
| GND | SUPPLY | GROUND: Do not float any ground pins. |
| NC | | NO CONNECT: Lead is not internally connected; it may be driven or floated. |

| [$A_{20}$-$A_0$] | |
|---|---|
| 1EFFFF<br>1F0000 | 64-Kword Block 39 |
| 1EFFFF<br>1E0000 | 64-Kword Block 38 |
| 1DFFFF<br>1D0000 | 64-Kword Block 37 |
| 1CFFFF<br>1C0000 | 64-Kword Block 36 |
| 1BFFFF<br>1B0000 | 64-Kword Block 35 |
| 1AFFFF<br>1A0000 | 64-Kword Block 34 |
| 19FFFF<br>190000 | 64-Kword Block 33 |
| 18FFFF<br>180000 | 64-Kword Block 32 |
| 17FFFF<br>170000 | 64-Kword Block 31 |
| 16FFFF<br>160000 | 64-Kword Block 30 |
| 15FFFF<br>150000 | 64-Kword Block 29 |
| 14FFFF<br>140000 | 64-Kword Block 28 |
| 13FFFF<br>130000 | 64-Kword Block 27 |
| 12FFFF<br>120000 | 64-Kword Block 26 |
| 11FFFF<br>110000 | 64-Kword Block 25 |
| 10FFFF<br>100000 | 64-Kword Block 24 |
| 0FFFFF<br>0F0000 | 64-Kword Block 23 |
| 0EFFFF<br>0E0000 | 64-Kword Block 22 |
| 0DFFFF<br>0D0000 | 64-Kword Block 21 |
| 0CFFFF<br>0C0000 | 64-Kword Block 20 |
| 0BFFFF<br>0B0000 | 64-Kword Block 19 |
| 0AFFFF<br>0A0000 | 64-Kword Block 18 |
| 09FFFF<br>090000 | 64-Kword Block 17 |
| 08FFFF<br>080000 | 64-Kword Block 16 |
| 07FFFF<br>070000 | 64-Kword Block 15 |
| 06FFFF<br>060000 | 64-Kword Block 14 |
| 05FFFF<br>050000 | 64-Kword Block 13 |
| 04FFFF<br>040000 | 64-Kword Block 12 |
| 03FFFF<br>030000 | 64-Kword Block 11 |
| 02FFFF<br>020000 | 64-Kword Block 10 |
| 01FFFF<br>010000 | 64-Kword Block 9 |
| 00FFFF<br>008000 | 32-Kword Block 8 |
| 007FFF<br>007000 | 4-Kword Block 7 |
| 006FFF<br>006000 | 4-Kword Block 6 |
| 005FFF<br>005000 | 4-Kword Block 5 |
| 004FFF<br>004000 | 4-Kword Block 4 |
| 003FFF<br>003000 | 4-Kword Block 3 |
| 002FFF<br>002000 | 4-Kword Block 2 |
| 001FFF<br>001000 | 4-Kword Block 1 |
| 000FFF<br>000000 | 4-Kword Block 0 |

Figure 2. Memory Map (Bottom Parameter)

Table 2. Identifier Codes and OTP Address for Read Operation

| | Code | Address $[A_{20}\text{-}A_0]$ | Data $[DQ_{15}\text{-}DQ_0]$ | Notes |
|---|---|---|---|---|
| Manufacturer Code | Manufacturer Code | 000000H | 00B0H | |
| Device Code | Device Code | 000001H | 00A1H | |
| Block Lock Configuration Code | Block is Unlocked | Block Address + 2 | $DQ_0 = 0$ | 1 |
| | Block is Locked | | $DQ_0 = 1$ | 1 |
| | Block is not Locked-Down | | $DQ_1 = 0$ | 1 |
| | Block is Locked-Down | | $DQ_1 = 1$ | 1 |
| OTP | OTP Lock | 000080H | OTP-LK | 2 |
| | OTP | 000081-000088H | OTP | 3 |

NOTES:
1. Block Address = The beginning location of a block address. $DQ_{15}$-$DQ_2$ are reserved for future implementation.
2. OTP-LK=OTP Block Lock configuration.
3. OTP=OTP Block data.

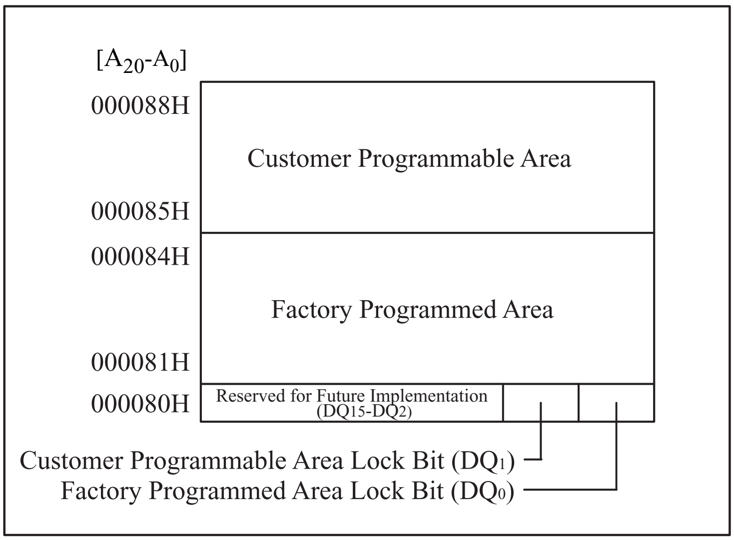



Figure 3. OTP Block Address Map for OTP Program
(The area outside 80H~88H cannot be used.)

Table 3. Bus Operation[1, 2]

| Mode | Notes | RST# | CE# | OE# | WE# | Address | $DQ_{15-0}$ | RY/BY# [8] |
|---|---|---|---|---|---|---|---|---|
| Read Array | 6 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $D_{OUT}$ | High Z |
| Output Disable | | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | High Z | X |
| Standby | | $V_{IH}$ | $V_{IH}$ | X | X | X | High Z | X |
| Reset | 3 | $V_{IL}$ | X | X | X | X | High Z | High Z |
| Read Identifier Codes/OTP | 6 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | See Table 2 | See Table 2 | High Z |
| Read Query | 6,7 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | See Appendix | See Appendix | High Z |
| Read Status Register | 6 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $D_{OUT}$ | X |
| Write | 4,5,6 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | $D_{IN}$ | X |

NOTES:
1. Refer to DC Characteristics for $V_{IL}$ or $V_{IH}$ voltages.
2. X can be $V_{IL}$ or $V_{IH}$ for control pins and addresses.
3. RST# at GND±0.2V ensures the lowest power consumption.
4. Command writes involving block erase, full chip erase, program or OTP program are reliably executed when $V_{CC}$=2.7V-3.6V.
5. Refer to Table 4 for valid $D_{IN}$ during a write operation.
6. Never hold OE# low and WE# low at the same timing.
7. Refer to Appendix of LHF00LXX series for more information about query code.
8. RY/BY# is $V_{OL}$ when the WSM (Write State Machine) is executing internal block erase, full chip erase, program or OTP program algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with program inactive), program suspend mode, or reset mode.

Table 4. Command Definitions[10]

| Command | Bus Cycles Req'd | Notes | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|---|---|
| | | | Oper[1] | Addr[2] | Data | Oper[1] | Addr[2] | Data[3] |
| Read Array | 1 | | Write | X | FFH | | | |
| Read Identifier Codes/OTP | ≥ 2 | 4 | Write | X | 90H | Read | IA or OA | ID or OD |
| Read Query | ≥ 2 | 4 | Write | X | 98H | Read | QA | QD |
| Read Status Register | 2 | | Write | X | 70H | Read | X | SRD |
| Clear Status Register | 1 | | Write | X | 50H | | | |
| Block Erase | 2 | 5 | Write | BA | 20H | Write | BA | D0H |
| Full Chip Erase | 2 | 5, 8 | Write | X | 30H | Write | X | D0H |
| Program | 2 | 5,6 | Write | WA | 40H or 10H | Write | WA | WD |
| Block Erase and Program Suspend | 1 | 7, 8 | Write | X | B0H | | | |
| Block Erase and Program Resume | 1 | 7, 8 | Write | X | D0H | | | |
| Set Block Lock Bit | 2 | | Write | BA | 60H | Write | BA | 01H |
| Clear Block Lock Bit | 2 | 9 | Write | BA | 60H | Write | BA | D0H |
| Set Block Lock-down Bit | 2 | | Write | BA | 60H | Write | BA | 2FH |
| OTP Program | 2 | 8 | Write | OA | C0H | Write | OA | OD |

NOTES:
1. Bus operations are defined in Table 3.
2. All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.
   X=Any valid address within the device.
   IA=Identifier codes address (See Table 2).
   QA=Query codes address. Refer to Appendix of LHF00LXX series for details.
   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA=Address of memory location for the Program command.
   OA=Address of OTP block to be read or programmed (See Figure 3).
3. ID=Data read from identifier codes. (See Table 2).
   QD=Data read from query database. Refer to Appendix of LHF00LXX series for details.
   SRD=Data read from status register. See Table 8 for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.
   OD=Data within OTP block. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code and the data within OTP block (See Table 2).
   The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase, full chip erase or program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is $V_{IH}$.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. If the program operation and the erase operation are both suspended, the suspended program operation will be resumed first.
8. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.

9. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when WP#/ACC is $V_{IL}$. When WP#/ACC is $V_{IH}$, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
10. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Table 5. Functions of Block Lock(5) and Block Lock-Down

| Current State | | | | | Erase/Program Allowed (2) |
|---|---|---|---|---|---|
| State | WP#/ACC | $DQ_1$(1) | $DQ_0$(1) | State Name | |
| [000] | 0 | 0 | 0 | Unlocked | Yes |
| [001](3) | 0 | 0 | 1 | Locked | No |
| [011] | 0 | 1 | 1 | Locked-down | No |
| [100] | 1 | 0 | 0 | Unlocked | Yes |
| [101](3) | 1 | 0 | 1 | Locked | No |
| [110](4) | 1 | 1 | 0 | Lock-down Disable | Yes |
| [111] | 1 | 1 | 1 | Lock-down Disable | No |

NOTES:
1. $DQ_0$=1: a block is locked; $DQ_0$=0: a block is unlocked.
   $DQ_1$=1: a block is locked-down; $DQ_1$=0: a block is not locked-down.
2. Erase and program are general terms, respectively, to express: block erase, full chip erase and program operations.
3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (WP#/ACC=0) or [101] (WP#/ACC=1), regardless of the states before power-off or reset operation.
4. When WP#/ACC is driven to $V_{IL}$ in [110] state, the state changes to [011] and the blocks are automatically locked.
5. OTP (One Time Program) block has the lock function which is different from those described above.

Table 6. Block Locking State Transitions upon Command Write(4)

| Current State | | | | Result after Lock Command Written (Next State) | | |
|---|---|---|---|---|---|---|
| State | WP#/ACC | $DQ_1$ | $DQ_0$ | Set Lock(1) | Clear Lock(1) | Set Lock-down(1) |
| [000] | 0 | 0 | 0 | [001] | No Change | [011](2) |
| [001] | 0 | 0 | 1 | No Change(3) | [000] | [011] |
| [011] | 0 | 1 | 1 | No Change | No Change | No Change |
| [100] | 1 | 0 | 0 | [101] | No Change | [111](2) |
| [101] | 1 | 0 | 1 | No Change | [100] | [111] |
| [110] | 1 | 1 | 0 | [111] | No Change | [111](2) |
| [111] | 1 | 1 | 1 | No Change | [110] | No Change |

NOTES:
1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block ($DQ_0$=0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that WP#/ACC is not changed and fixed $V_{IL}$ or $V_{IH}$.

Table 7. Block Locking State Transitions upon WP#/ACC Transition[4]

| Previous State | Current State | | | | Result after WP#/ACC Transition (Next State) | |
|---|---|---|---|---|---|---|
| | State | WP#/ACC | $DQ_1$ | $DQ_0$ | WP#/ACC=0→1[1] | WP#/ACC=1→0[1] |
| - | [000] | 0 | 0 | 0 | [100] | - |
| - | [001] | 0 | 0 | 1 | [101] | - |
| [110][2] | [011] | 0 | 1 | 1 | [110] | - |
| Other than [110][2] | | | | | [111] | - |
| - | [100] | 1 | 0 | 0 | - | [000] |
| - | [101] | 1 | 0 | 1 | - | [001] |
| - | [110] | 1 | 1 | 0 | - | [011][3] |
| - | [111] | 1 | 1 | 1 | - | [011] |

NOTES:
1. "WP#/ACC=0→1" means that WP#/ACC is driven to $V_{IH}$ and "WP#/ACC=1→0" means that WP#/ACC is driven to $V_{IL}$.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When WP#/ACC is driven to $V_{IL}$ in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

Table 8. Status Register Definition

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| WSMS | BESS | EPS | EPS | WPACCS | PSS | DPS | R |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| | NOTES: |
|---|---|
| SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R) | |
| SR.7 = WRITE STATE MACHINE STATUS (WSMS)<br>1 = Ready<br>0 = Busy | Status Register indicates the status of the WSM (Write State Machine). |
| SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)<br>1 = Block Erase Suspended<br>0 = Block Erase in Progress/Completed | Check SR.7 or RY/BY# to determine block erase, full chip erase, program or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0". |
| SR.5, SR.4 = ERASE, PROGRAM STATUS (EPS)<br>SR.5=1 and SR.4=1: Command Sequence Error<br>SR.5=1 or SR.4=1: Error in Block Erase, Full Chip Erase, Program or OTP Program<br>SR.5=0 and SR.4=0: Successful Block Erase, Full Chip Erase, Program or OTP Program | If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, program, set/clear block lock bit, set block lock-down bit attempt, an improper command sequence was entered.<br><br>For the period of time required to check the status register in erase and program operation, refer to the specifications of block erase, full chip erase, program and OTP Program time. |
| SR.3 = WP#/ACC STATUS (WPACCS)<br>1 = $V_{CC}$+0.4V < WP#/ACC < 11.7V Detect, Operation Abort<br>0 = WP#/ACC OK | SR.3 does not provide a continuous indication of WP#/ACC level. The WSM interrogates and indicates the WP#/ACC level only after Block Erase, Full Chip Erase, Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when WP#/ACC≠$V_{ACCH}$. |
| SR.2 = PROGRAM SUSPEND STATUS (PSS)<br>1 = Program Suspended<br>0 = Program in Progress/Completed | |
| SR.1 = DEVICE PROTECT STATUS (DPS)<br>1 = Erase or Program Attempted on a Locked Block, Operation Abort<br>0 = Unlocked | SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/ OTP command indicates block lock bit status. |
| SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R) | SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register. |

# 1 Electrical Specifications

## 1.1 Absolute Maximum Ratings*

Operating Temperature

During Read, Erase and Program ...-40°C to +85°C (1)

Storage Temperature

During under Bias.............................. -40°C to +85°C

During non Bias............................... -65°C to +125°C

Voltage On Any Pin (except $V_{CC}$ and WP#/ACC)

................................................ -0.5V to $V_{CC}$+0.5V (2)

$V_{CC}$ Supply Voltage .......................... -0.2V to +3.9V (2)

WP#/ACC Supply Voltage ......... -0.2V to +12.6V (2, 3, 4)

Output Short Circuit Current.......................... 100mA (5)

**WARNING:* Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:
1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on $V_{CC}$ and WP#/ACC pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is $V_{CC}$+0.5V which, during transitions, may overshoot to $V_{CC}$+2.0V for periods <20ns.
3. Maximum DC voltage on WP#/ACC may overshoot to +13.0V for periods <20ns.
4. WP#/ACC erase/program voltage is normally 2.7V-3.6V. Applying 11.7V-12.3V to WP#/ACC during erase/program can be done for a maximum of 1,000 cycles on each block. WP#/ACC may be connected to 11.7V-12.3V for a total of 80 hours maximum.
5. Output shorted for no more than one second. No more than one output shorted at a time.

## 1.2 Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Operating Temperature | $T_A$ | -40 | +25 | +85 | °C | |
| $V_{CC}$ Supply Voltage | $V_{CC}$ | 2.7 | 3.0 | 3.6 | V | 1 |
| WP#/ACC Voltage when Used as a Logic Control | $V_{IL}$ | -0.2 | | 0.4 | V | 1 |
| | $V_{IH}$ | 2.4 | | $V_{CC}$ + 0.4 | V | |
| WP#/ACC Supply Voltage | $V_{ACCH}$ | 11.7 | 12.0 | 12.3 | V | 1, 2 |
| Block Erase Cycling: WP#/ACC=$V_{IL}$ or $V_{IH}$ | | 100,000 | | | Cycles | |
| Block Erase Cycling: WP#/ACC=$V_{ACCH}$, 80 hrs. | | | | 1,000 | Cycles | |
| Maximum WP#/ACC hours at $V_{ACCH}$ | | | | 80 | Hours | |

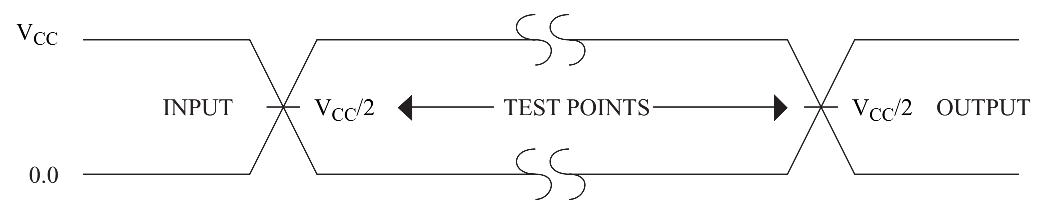
NOTES:
1. See DC Characteristics tables for voltage range-specific specification.
2. Applying WP#/ACC=11.7V-12.3V during a erase or program can be done for a maximum of 1,000 cycles on each block. A permanent connection to WP#/ACC=11.7V-12.3V is not allowed and can cause damage to the device.

### 1.2.1 Capacitance (1) ($T_A$=+25°C, f=1MHz)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0.0V | | 4 | 7 | pF |
| WP#/ACC Input Capacitance | $C_{IN}$ | $V_{IN}$=0.0V | | 18 | 22 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$=0.0V | | 6 | 10 | pF |

NOTE:
1. Sampled, not 100% tested.

### 1.2.2 AC Input/Output Test Conditions




AC test inputs are driven at $V_{CC}$(min) for a Logic "1" and 0.0V for a Logic "0".
Input timing begins, and output timing ends at $V_{CC}/2$. Input rise and fall times (10% to 90%) < 5ns.
Worst case speed conditions are when $V_{CC}=V_{CC}$(min).

Figure 4. Transient Input/Output Reference Waveform for $V_{CC}$=2.7V-3.6V

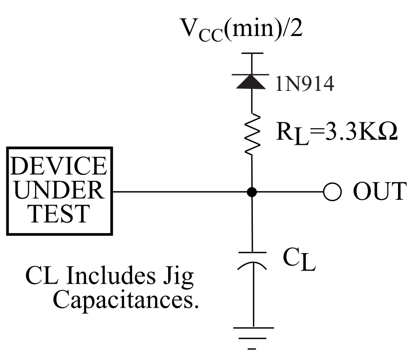



Figure 5. Transient Equivalent Testing Load Circuit

Table 9. Test Configuration Capacitance Loading Value

| Test Configuration | $C_L$ (pF) |
|---|---|
| $V_{CC}$=2.7V-3.6V | 50 |

### 1.2.3 DC Characteristics

$V_{CC}$=2.7V-3.6V

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | 1 | -1.0 | | +1.0 | µA | $V_{CC}$=$V_{CC}$Max., $V_{IN}$/$V_{OUT}$=$V_{CC}$ or GND |
| $I_{LO}$ | Output Leakage Current | 1 | -1.0 | | +1.0 | µA | |
| $I_{CCS}$ | $V_{CC}$ Standby Current | 1,6,7 | | 4 | 10 | µA | $V_{CC}$=$V_{CC}$Max., CE#=RST#= $V_{CC}$±0.2V, WP#/ACC=$V_{CC}$ or GND |
| $I_{CCAS}$ | $V_{CC}$ Automatic Power Savings Current | 1,3,6 | | 4 | 10 | µA | $V_{CC}$=$V_{CC}$Max., CE#=GND±0.2V, WP#/ACC=$V_{CC}$ or GND |
| $I_{CCD}$ | $V_{CC}$ Reset Current | 1,6 | | 4 | 10 | µA | RST#=GND±0.2V |
| $I_{CCR}$ | $V_{CC}$ Read Current | 1,6 | | | 17 | mA | $V_{CC}$=$V_{CC}$Max., CE#=$V_{IL}$, OE#=$V_{IH}$, f=5MHz |
| $I_{CCW}$ | $V_{CC}$ Program Current | 1,4,6 | | 20 | 60 | mA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,4,6 | | 10 | 20 | mA | WP#/ACC=$V_{ACCH}$ |
| $I_{CCE}$ | $V_{CC}$ Block Erase, Full Chip Erase Current | 1,4,6 | | 10 | 30 | mA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,4,6 | | 4 | 10 | mA | WP#/ACC=$V_{ACCH}$ |
| $I_{CCWS}$ $I_{CCES}$ | $V_{CC}$ Program or Block Erase Suspend Current | 1,2,6 | | 10 | 200 | µA | CE#=$V_{IH}$ |
| $I_{ACCS}$ $I_{ACCR}$ | WP#/ACC Standby or Read Current | 1,5,6 | | 2 | 5 | µA | WP#/ACC≤$V_{CC}$ |
| $I_{ACCW}$ | WP#/ACC Program Current | 1,4,5,6 | | 2 | 5 | µA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,4,5,6 | | 10 | 30 | mA | WP#/ACC=$V_{ACCH}$ |
| $I_{ACCE}$ | WP#/ACC Block Erase, Full Chip Erase Current | 1,4,5,6 | | 2 | 5 | µA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,4,5,6 | | 5 | 15 | mA | WP#/ACC=$V_{ACCH}$ |
| $I_{ACCWS}$ | WP#/ACC Program Suspend Current | 1,5,6 | | 2 | 5 | µA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,5,6 | | 10 | 200 | µA | WP#/ACC=$V_{ACCH}$ |
| $I_{ACCES}$ | WP#/ACC Block Erase Suspend Current | 1,5,6 | | 2 | 5 | µA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,5,6 | | 10 | 200 | µA | WP#/ACC=$V_{ACCH}$ |

DC Characteristics (Continued)

$V_{CC}$=2.7V-3.6V

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | 5 | -0.4 | | 0.4 | V | |
| $V_{IH}$ | Input High Voltage | 4 | 2.4 | | $V_{CC}$ + 0.4 | V | |
| $V_{OL}$ | Output Low Voltage | 4,7 | | | 0.2 | V | $V_{CC}$=$V_{CC}$Min., $I_{OL}$=100µA |
| $V_{OH}$ | Output High Voltage | 4 | $V_{CC}$ -0.2 | | | V | $V_{CC}$=$V_{CC}$Min., $I_{OH}$=-100µA |
| $V_{ACCH}$ | WP#/ACC during Block Erase, Full Chip Erase, Program or OTP Program Operations | 5 | 11.7 | 12.0 | 12.3 | V | |
| $V_{LKO}$ | $V_{CC}$ Lockout Voltage | | 1.5 | | | V | |

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values are the reference values at $V_{CC}$=3.0V and $T_A$=+25°C unless $V_{CC}$ is specified.
2. $I_{CCWS}$ and $I_{CCES}$ are specified with the device de-selected. If read or program is executed while in block erase suspend mode, the device's current draw is the sum of $I_{CCES}$ and $I_{CCR}$ or $I_{CCW}$. If read is executed while in program suspend mode, the device's current draw is the sum of $I_{CCWS}$ and $I_{CCR}$.
3. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings ($t_{AVQV}$) provide new data when addresses are changed.
4. Sampled, not 100% tested.
5. Applying 12.0V±0.3V to WP#/ACC provides fast erasing or fast programming mode. In this mode, WP#/ACC is power supply pin and supplies the memory cell current for block erasing and programming. Use similar power supply trace widths and layout considerations given to the $V_{CC}$ power bus.
   Applying 12.0V±0.3V to WP#/ACC during erase/program can only be done for a maximum of 1,000 cycles on each block. WP#/ACC may be connected to 12.0V±0.3V for a total of 80 hours maximum.
6. For all pins other than those shown in test conditions, input level is $V_{CC}$ or GND.
7. Includes RY/BY#.

### 1.2.4 AC Characteristics - Read-Only Operations[1]

$V_{CC}$=2.7V-3.6V, $T_A$=-40°C to +85°C

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{AVAV}$ | Read Cycle Time | | 90 | | ns |
| $t_{AVQV}$ | Address to Output Delay | | | 90 | ns |
| $t_{ELQV}$ | CE# to Output Delay | 3 | | 90 | ns |
| $t_{GLQV}$ | OE# to Output Delay | 3 | | 20 | ns |
| $t_{PHQV}$ | RST# High to Output Delay | | | 150 | ns |
| $t_{EHQZ}$, $t_{GHQZ}$ | CE# or OE# to Output in High Z, Whichever Occurs First | 2 | | 20 | ns |
| $t_{ELQX}$ | CE# to Output in Low Z | 2 | 0 | | ns |
| $t_{GLQX}$ | OE# to Output in Low Z | 2 | 0 | | ns |
| $t_{OH}$ | Output Hold from First Occurring Address, CE# or OE# change | 2 | 0 | | ns |

NOTES:
1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE# without impact to $t_{ELQV}$.

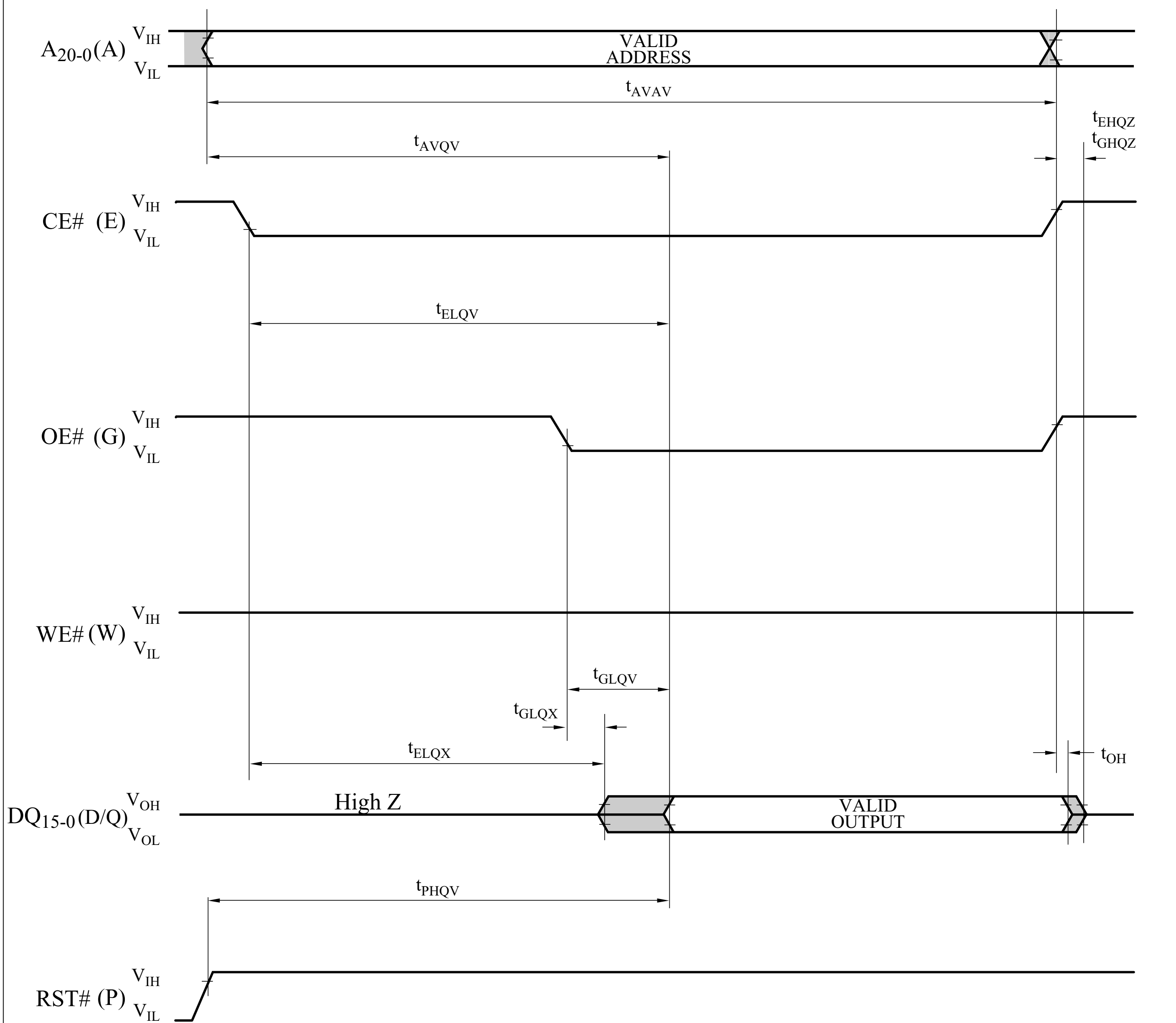


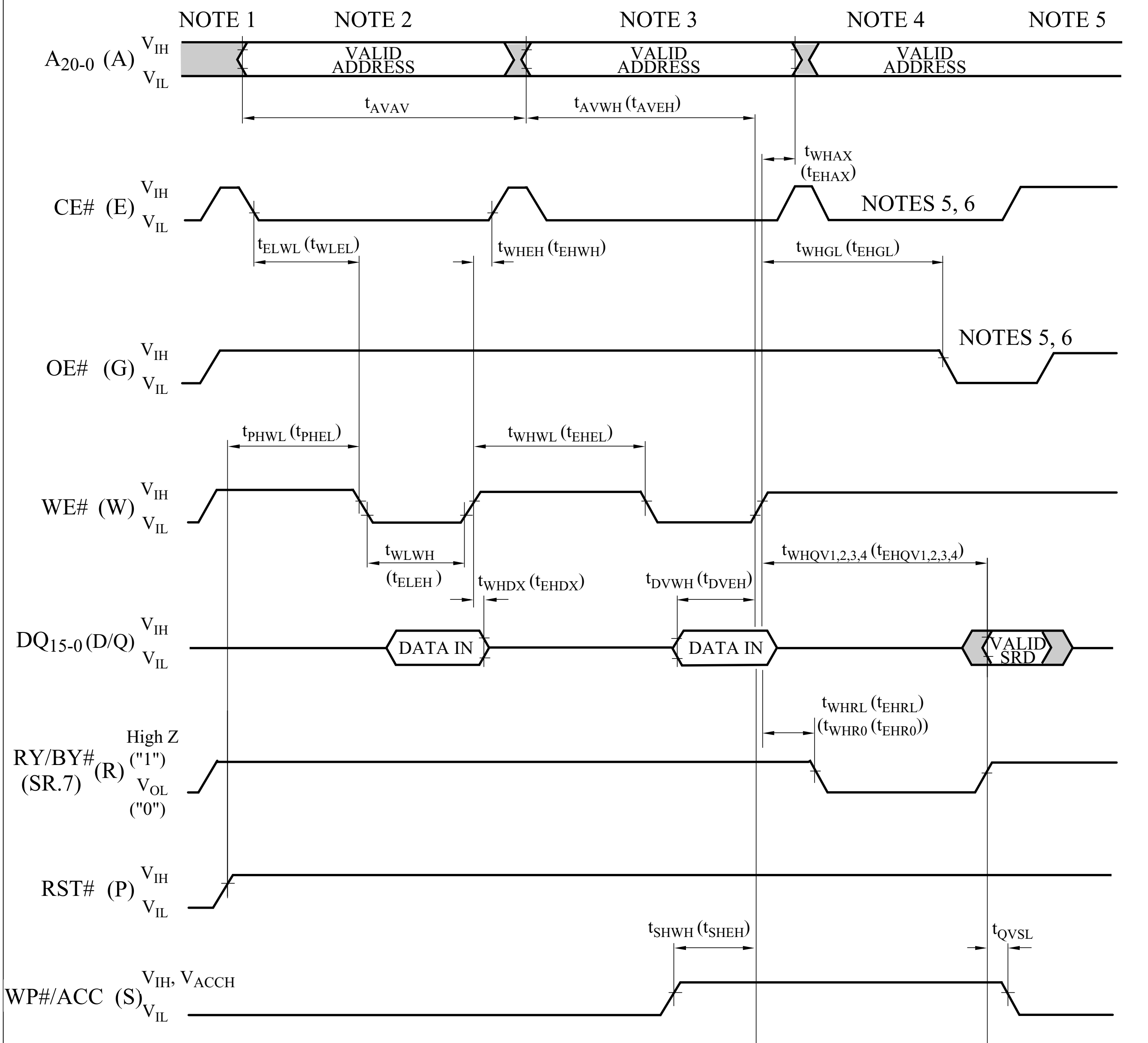

Figure 6. AC Waveform for Read Operations

## 1.2.5 AC Characteristics - Write Operations[(1), (2)]

$V_{CC}$=2.7V-3.6V, $T_A$=-40°C to +85°C

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{AVAV}$ | Write Cycle Time | | 90 | | ns |
| $t_{PHWL}$ ($t_{PHEL}$) | RST# High Recovery to WE# (CE#) Going Low | 3 | 150 | | ns |
| $t_{ELWL}$ ($t_{WLEL}$) | CE# (WE#) Setup to WE# (CE#) Going Low | | 0 | | ns |
| $t_{WLWH}$ ($t_{ELEH}$) | WE# (CE#) Pulse Width | 4 | 60 | | ns |
| $t_{DVWH}$ ($t_{DVEH}$) | Data Setup to WE# (CE#) Going High | 7 | 40 | | ns |
| $t_{AVWH}$ ($t_{AVEH}$) | Address Setup to WE# (CE#) Going High | 7 | 50 | | ns |
| $t_{WHEH}$ ($t_{EHWH}$) | CE# (WE#) Hold from WE# (CE#) High | | 0 | | ns |
| $t_{WHDX}$ ($t_{EHDX}$) | Data Hold from WE# (CE#) High | | 0 | | ns |
| $t_{WHAX}$ ($t_{EHAX}$) | Address Hold from WE# (CE#) High | | 0 | | ns |
| $t_{WHWL}$ ($t_{EHEL}$) | WE# (CE#) Pulse Width High | 5 | 30 | | ns |
| $t_{SHWH}$ ($t_{SHEH}$) | WP#/ACC High Setup to WE# (CE#) Going High: WP#/ACC=$V_{IH}$ | 3 | 0 | | ns |
| | WP#/ACC High Setup to WE# (CE#) Going High: WP#/ACC=$V_{ACCH}$ | | 200 | | |
| $t_{WHGL}$ ($t_{EHGL}$) | Write Recovery before Read | | 30 | | ns |
| $t_{QVSL}$ | WP#/ACC High Hold from Valid SRD, RY/BY# High Z | 3 | 0 | | ns |
| $t_{WHR0}$ ($t_{EHR0}$) | WE# (CE#) High to SR.7 Going "0" | 3, 6 | | $t_{AVQV}$ +50 | ns |
| $t_{WHRL}$ ($t_{EHRL}$) | WE# (CE#) High to RY/BY# Going Low | 3 | | 100 | ns |

NOTES:
1. The timing characteristics for reading the status register during block erase, full chip erase, program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width ($t_{WP}$) is defined from the falling edge of CE# or WE# (whichever goes low last) to the rising edge of CE# or WE# (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$.
5. Write pulse width high ($t_{WPH}$) is defined from the rising edge of CE# or WE# (whichever goes high first) to the falling edge of CE# or WE# (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$.
6. $t_{WHR0}$ ($t_{EHR0}$) after the Read Query or Read Identifier Codes/OTP command=$t_{AVQV}$+100ns.
7. Refer to Table 4 for valid address and data for block erase, full chip erase, program, OTP program or lock bit configuration.




NOTES:
1. $V_{CC}$ power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, OE# and CE# must be driven active, and WE# de-asserted.

Figure 7. AC Waveform for Write Operations

### 1.2.6 Reset Operations

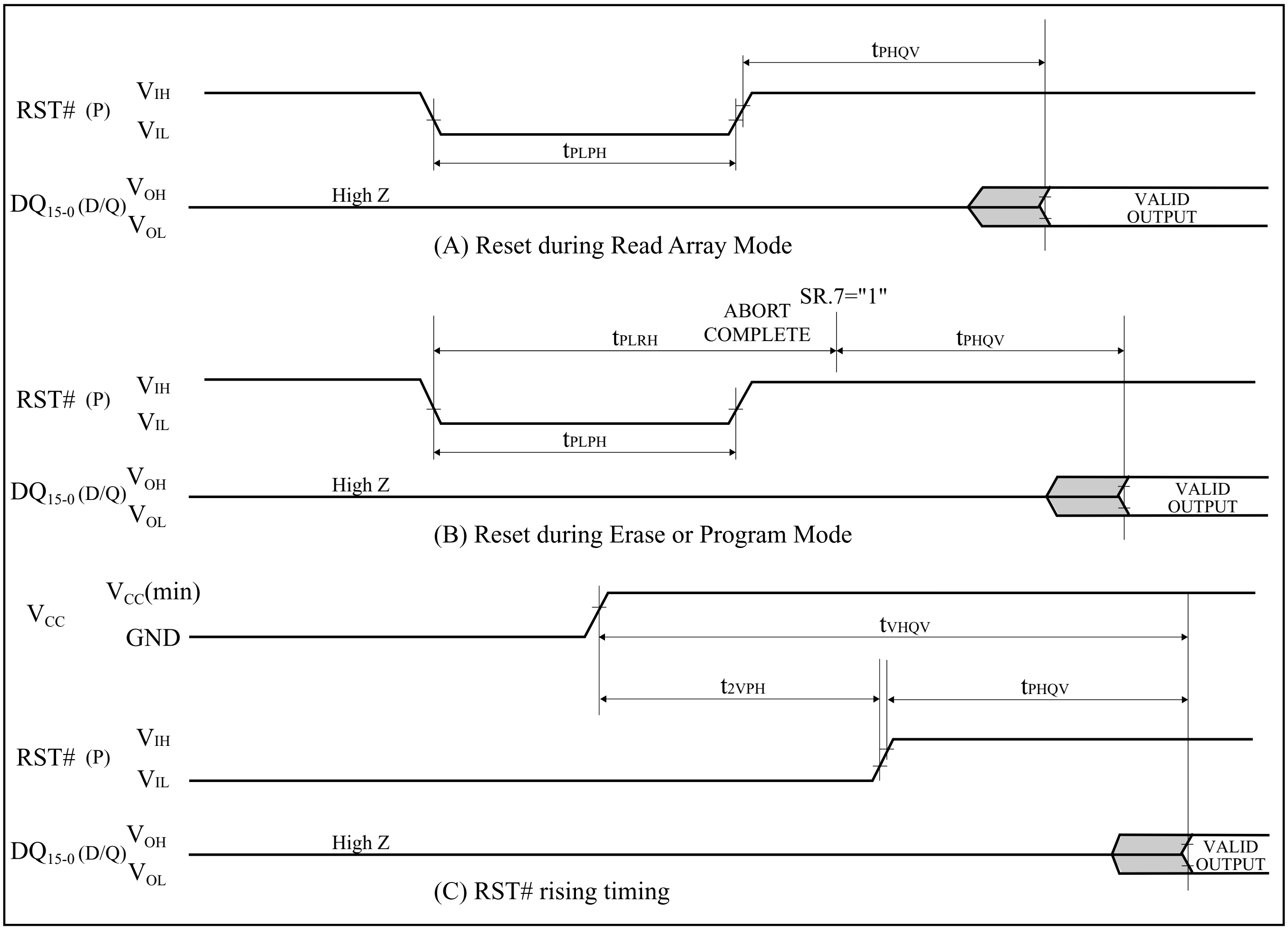



Figure 8. AC Waveform for Reset Operations

Reset AC Specifications ($V_{CC}$=2.7V-3.6V, $T_A$=-40°C to +85°C)

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{PLPH}$ | RST# Low to Reset during Read<br>(RST# should be low during power-up.) | 1, 2, 3 | 100 | | ns |
| $t_{PLRH}$ | RST# Low to Reset during Erase or Program | 1, 3, 4 | | 22 | µs |
| $t_{2VPH}$ | $V_{CC}$ 2.7V to RST# High | 1, 3, 5 | 100 | | ns |
| $t_{VHQV}$ | $V_{CC}$ 2.7V to Output Delay | 3 | | 1 | ms |

NOTES:
1. A reset time, $t_{PHQV}$, is required from the later of SR.7 (RY/BY#) going "1" (High Z) or RST# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for $t_{PHQV}$.
2. $t_{PLPH}$ is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If RST# asserted while a block erase, full chip erase, program or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding RST# low minimum 100ns is required after $V_{CC}$ has been in predefined range and also has been in stable there.