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1-Mbit (128K x 8) Static RAM

Features

- **Temperature Ranges**
 - Commercial: 0°C to 70°C
 - Industrial: -40°C to 85°C
 - Automotive-A: -40°C to 85°C
 - Automotive-E: -40°C to 125°C
- **4.5V–5.5V operation**
- **CMOS for optimum speed/power**
- **Low active power**
(70 ns Commercial, Industrial, Automotive-A)
 - 82.5 mW (max.) (15 mA)
- **Low standby power**
(55/70 ns Commercial, Industrial, Automotive-A)
 - 110 μ W (max.) (15 μ A)
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2 , and $\overline{OE}$ options**
- **Available in Pb-free and non-Pb-free 32-pin (450 mil-wide) SOIC, 32-pin STSOP and 32-pin TSOP-I**

Functional Description^[1]

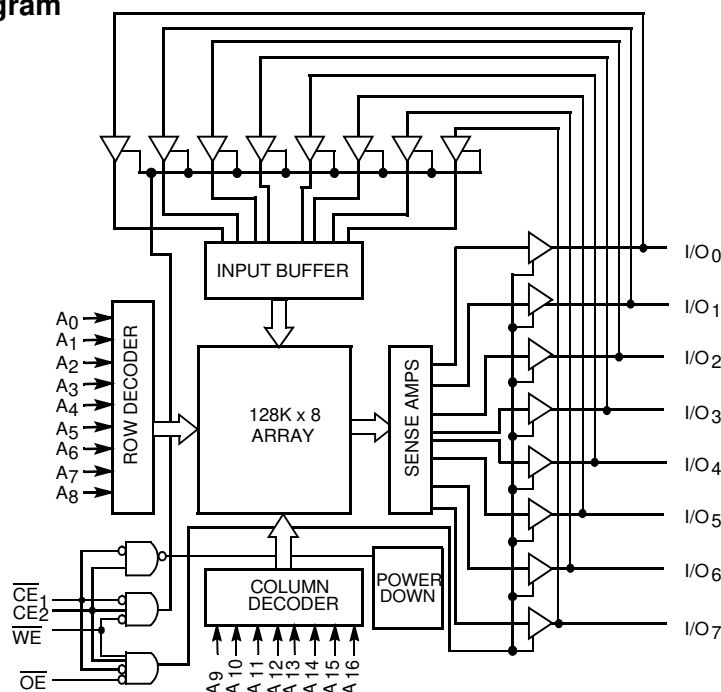
The CY62128BN is a high-performance CMOS static RAM organized as 128K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}_1$), an active HIGH Chip Enable (CE_2), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking Chip Enable One ($\overline{CE}_1$) and Write Enable (WE) inputs LOW and Chip Enable Two (CE_2) input HIGH. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₆).

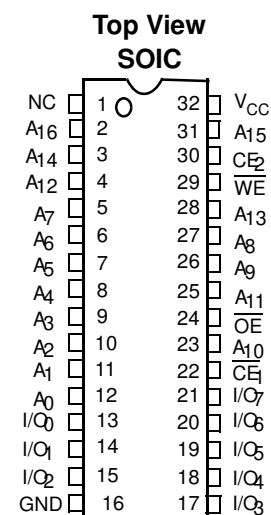
Reading from the device is accomplished by taking Chip Enable One ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable (WE) and Chip Enable Two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and WE LOW).

Logic Block Diagram



Pin Configuration



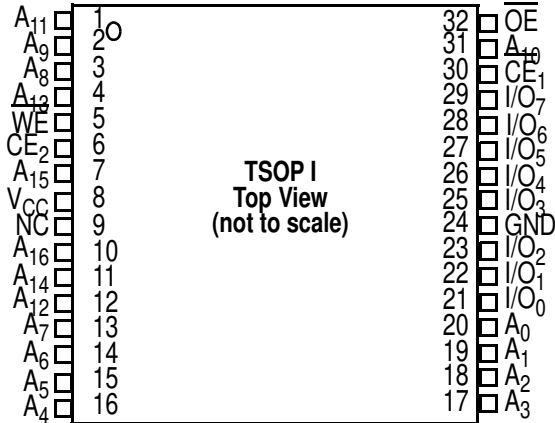
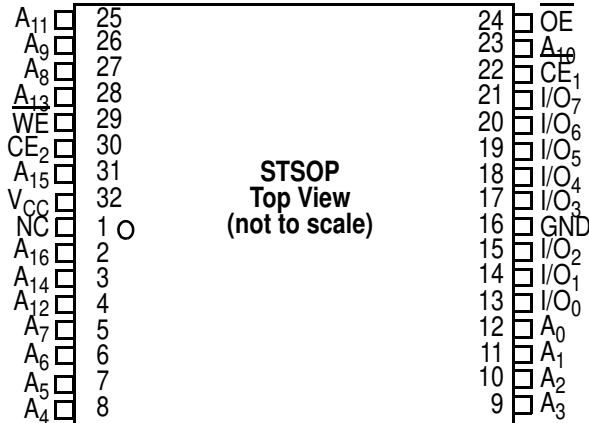
Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

Product		V _{CC} Range (V)			Speed (ns)	Power Dissipation			
						Operating, I _{CC} (mA)		Standby, I _{SB2} (μA)	
		Min.	Typ. ^[2]	Max.		Typ. ^[2]	Max.	Typ. ^[2]	Max.
CY62128BNLL	Commercial	4.5	5.0	5.5	55	7.5	20	2.5	15
					70	6	15	2.5	15
	Industrial				55	7.5	20	2.5	15
					70	6	15	2.5	15
	Automotive-A				70	6	15	2.5	15
	Automotive-E				70	6	25	2.5	25

Pin Configurations



Pin Definitions

Input	A₀–A₁₆ . Address Inputs
Input/Output	I/O₀–I/O₇ . Data lines. Used as input or output lines depending on operation
Input/Control	WE . Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/Control	CE₁ . Chip Enable 1, Active LOW.
Input/Control	CE₂ . Chip Enable 2, Active HIGH.
Input/Control	OE . Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
Ground	GND . Ground for the device
Power Supply	V_{CC} . Power supply for the device

Note:

2. Typical values are included for reference only and are not tested or guaranteed. Typical values are an average of the distribution across normal production variations as measured at V_{CC} = 5.0V, T_A = 25°C, and t_{AA} = 70 ns.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[3] -0.5V to +7.0V

DC Voltage Applied to Outputs

in High-Z State^[3] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[3] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature (T_A) ^[4]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	
Automotive-A	-40°C to +85°C	
Automotive-E	-40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-55			-70			Unit
			Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$	2.4			2.4			V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.2		$V_{CC} + 0.3$	2.2		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[3]		-0.3		0.8	-0.3		0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-1		+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-1		+1	-1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$		7.5	20		6	15	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC} , $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		0.1	2		0.1	1	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC} , $CE_1 \geq V_{CC} - 0.3V$, or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f = 0$		2.5	15		2.5	15	μA

Notes:

3. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.

4. T_A is the "Instant On" case temperature.

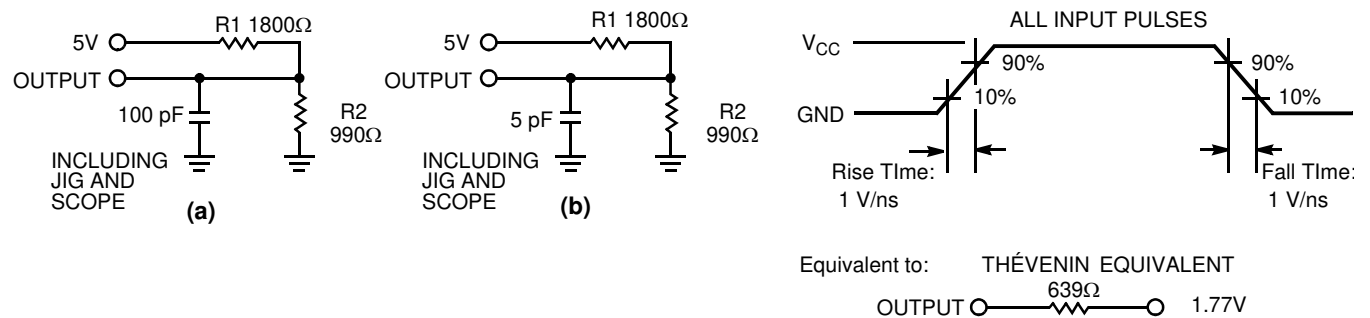
Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	9	pF
C _{OUT}	Output Capacitance		9	pF

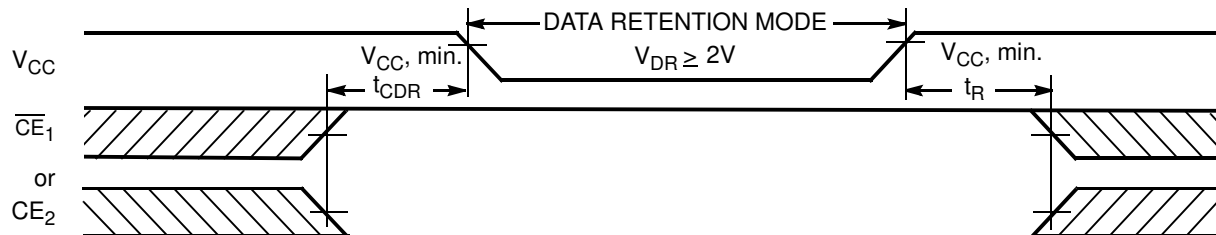
Thermal Resistance^[5]

Parameter	Description	Test Conditions	32 SOIC	32 STSOP	32 TSOP	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	66.17	105.14	97.44	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		30.87	14.09	26.05	°C/W

AC Test Loads and Waveforms



Data Retention Waveform



Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[6]	Min.	Typ.	Max.	Unit
V _{DR}	V _{CC} for Data Retention		2.0			V
I _{CCDR}	Data Retention Current	V _{CC} = V _{DR} = 2.0V, CE ₁ ≥ V _{CC} - 0.3V, or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V or, V _{IN} ≤ 0.3V		1.5	15	μA
		Commercial/ Industrial Automotive-A		1.5	25	μA
		Automotive-E		1.5	25	μA
t _{CDR}	Chip Deselect to Data Retention Time		0			ns
t _R	Operation Recovery Time		70			ns

Note:

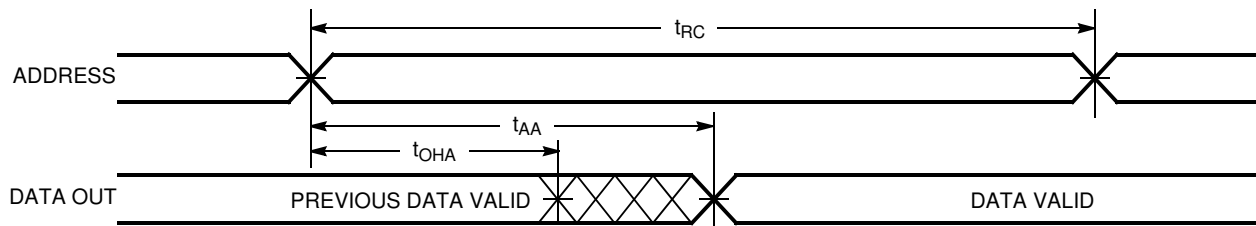
- Tested initially and after any design or process changes that may affect these parameters.
- No input may exceed V_{CC} + 0.5V.

Switching Characteristics^[7] Over the Operating Range

Parameter	Description	CY62128BN-55		CY62128BN-70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	5		5		ns
t _{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		20		35	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[7, 9]		20		25	ns
t _{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE ₂ HIGH to Low Z ^[9]	5		5		ns
t _{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE ₂ LOW to High Z ^[8, 9]		20		25	ns
t _{PU}	$\overline{CE}_1$ LOW to Power-up, CE ₂ HIGH to Power-up	0		0		ns
t _{PD}	$\overline{CE}_1$ HIGH to Power-down, CE ₂ LOW to Power-down		55		70	ns
WRITE CYCLE ^[10]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{CE}_1$ LOW to Write End, CE ₂ HIGH to Write End	45		60		ns
t _{AW}	Address Set-up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	45		50		ns
t _{SD}	Data Set-up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[9]	5		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[8, 9]		20		25	ns

Switching Waveforms

Read Cycle No.1^[11, 12]

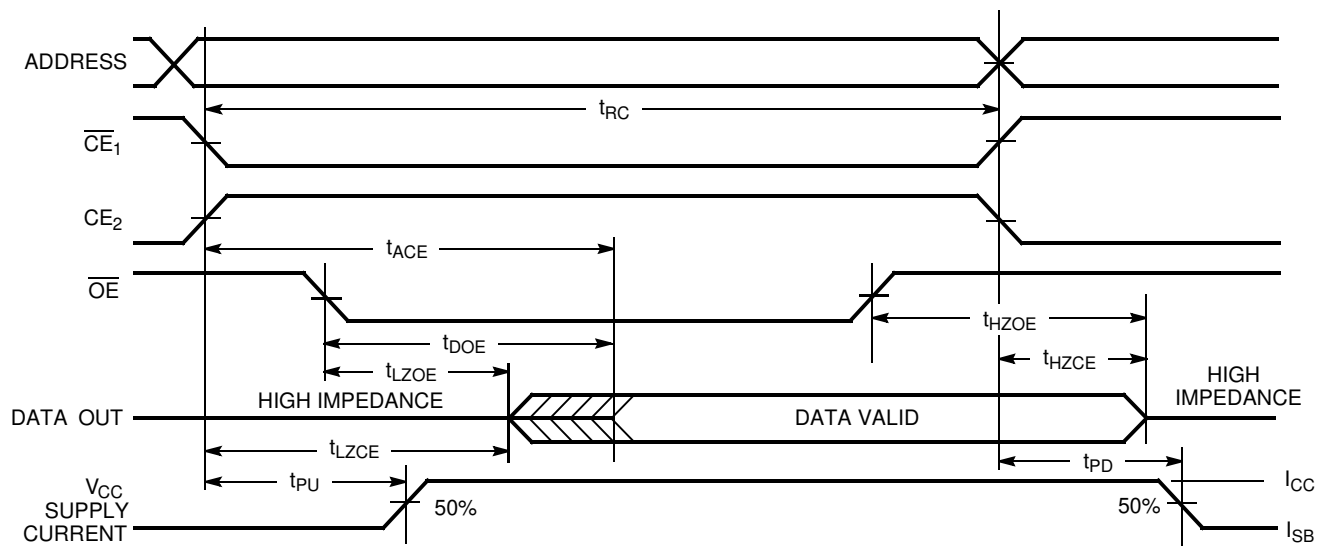


Notes:

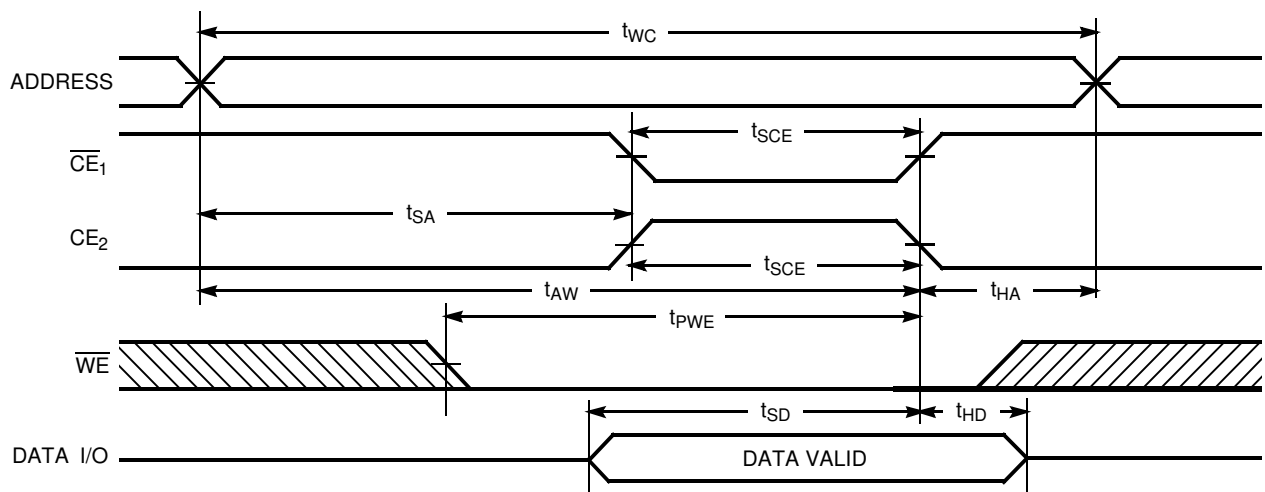
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- Device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
- $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled)^[12, 13]



Write Cycle No. 1 ($\overline{CE}_1$ or CE_2 Controlled)^[14, 15]



Notes:

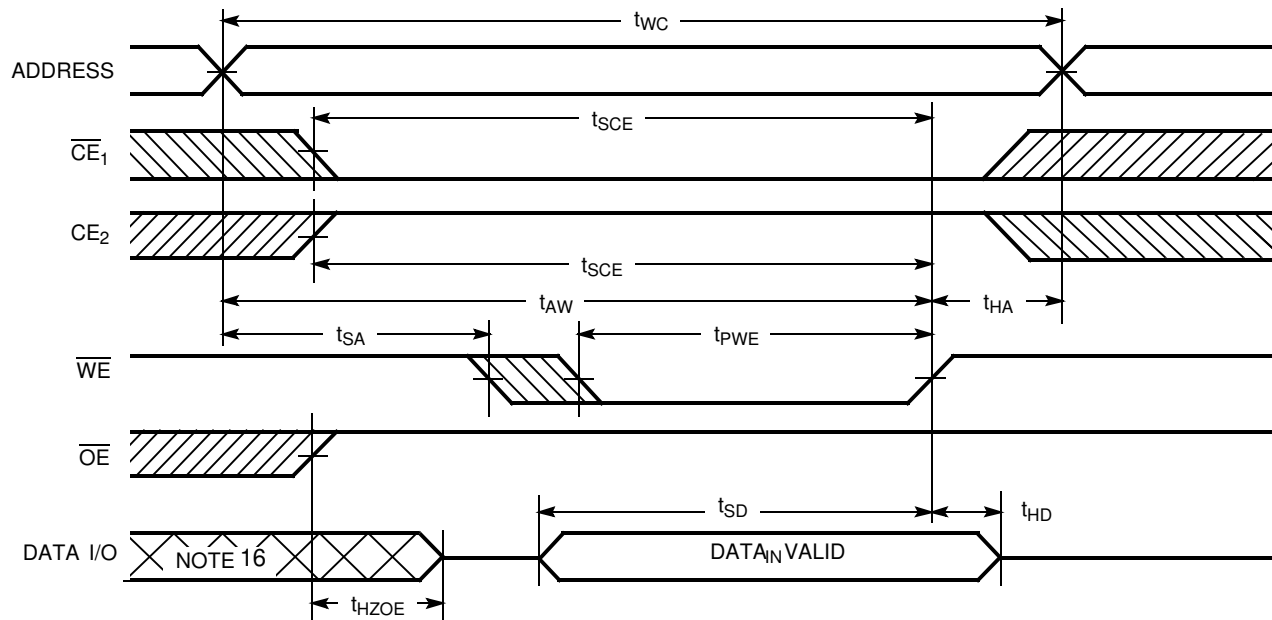
13. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

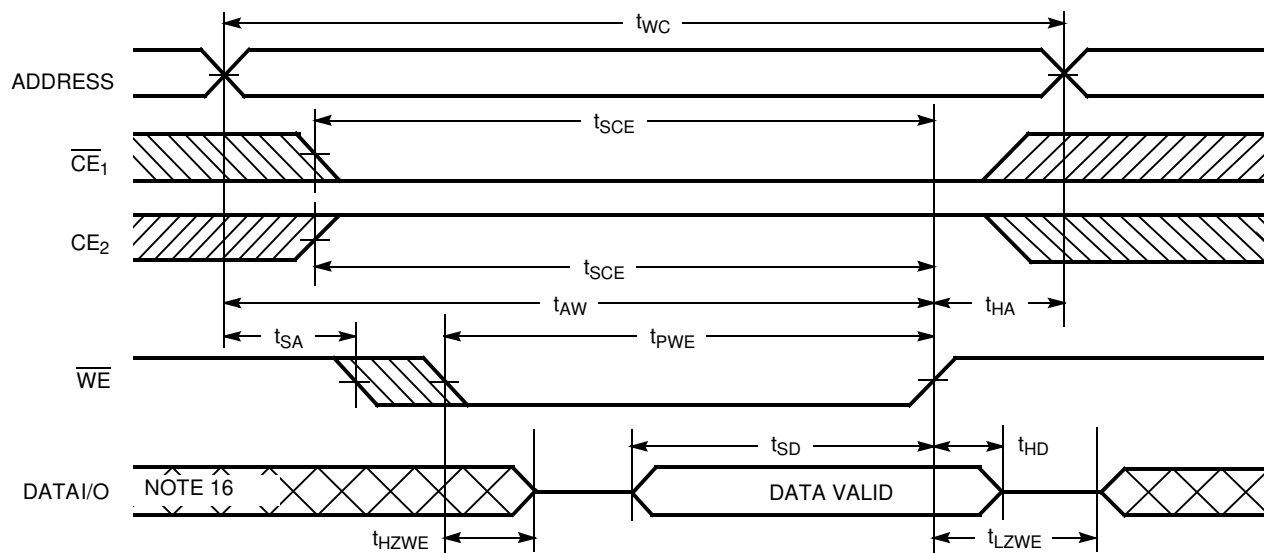
15. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)^[14, 15]



Write Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)^[14, 15]



Note:

16. During this period the I/Os are in the output state and input signals should not be applied.

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Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	I/O ₀ -I/O ₇	Mode	Power
H	X	X	X	High Z	Power-down	Standby (I _{SB})
X	L	X	X	High Z	Power-down	Standby (I _{SB})
L	H	L	H	Data Out	Read	Active (I _{CC})
L	H	X	L	Data In	Write	Active (I _{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

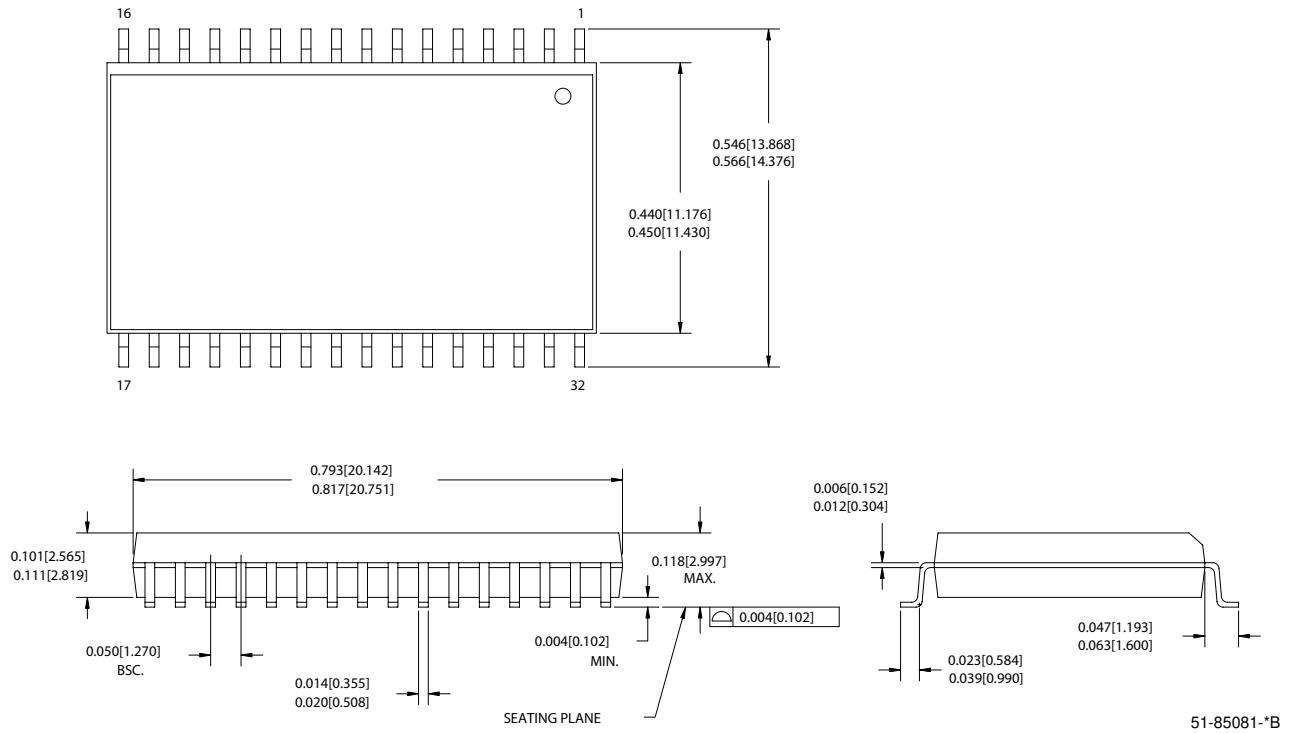
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62128BNLL-55SC	51-85081	32-pin 450-Mil SOIC	Commercial
	CY62128BNLL-55SXC		32-pin 450-Mil SOIC (Pb-Free)	
	CY62128BNLL-55SI		32-pin 450-Mil SOIC	Industrial
	CY62128BNLL-55SXI		32-pin 450-Mil SOIC (Pb-Free)	
	CY62128BNLL-55ZAI	51-85094	32-pin STSOP	
	CY62128BNLL-55ZAXI		32-pin STSOP (Pb-Free)	
	CY62128BNLL-55ZI	51-85056	32-pin TSOP Type I	
	CY62128BNLL-55ZXI		32-pin TSOP Type I (Pb-Free)	
70	CY62128BNLL-70SC	51-85081	32-pin 450-Mil SOIC	Commercial
	CY62128BNLL-70SXC		32-pin 450-Mil SOIC (Pb-Free)	
	CY62128BNLL-70ZC	51-85056	32-pin TSOP Type I	
	CY62128BNLL-70ZXC		32-pin TSOP Type I (Pb-Free)	
	CY62128BNLL-70SI	51-85081	32-pin 450-Mil SOIC	Industrial
	CY62128BNLL-70SXI		32-pin 450-Mil SOIC (Pb-Free)	
	CY62128BNLL-70ZAI	51-85094	32-pin STSOP	
	CY62128BNLL-70ZAXI		32-pin STSOP (Pb-Free)	
	CY62128BNLL-70ZI	51-85056	32-pin TSOP Type I	
	CY62128BNLL-70ZXI		32-pin TSOP Type I (Pb-Free)	
	CY62128BNLL-70ZXA	51-85056	32-pin TSOP Type I (Pb-Free)	Automotive-A
	CY62128BNLL-70SXA	51-85081	32-pin 450-Mil SOIC (Pb-Free)	
	CY62128BNLL-70SXE	51-85081	32-pin 450-Mil SOIC (Pb-Free)	Automotive-E
	CY62128BNLL-70ZAXE	51-85094	32-pin STSOP (Pb-Free)	

Please contact your local Cypress sales representative for availability of these parts

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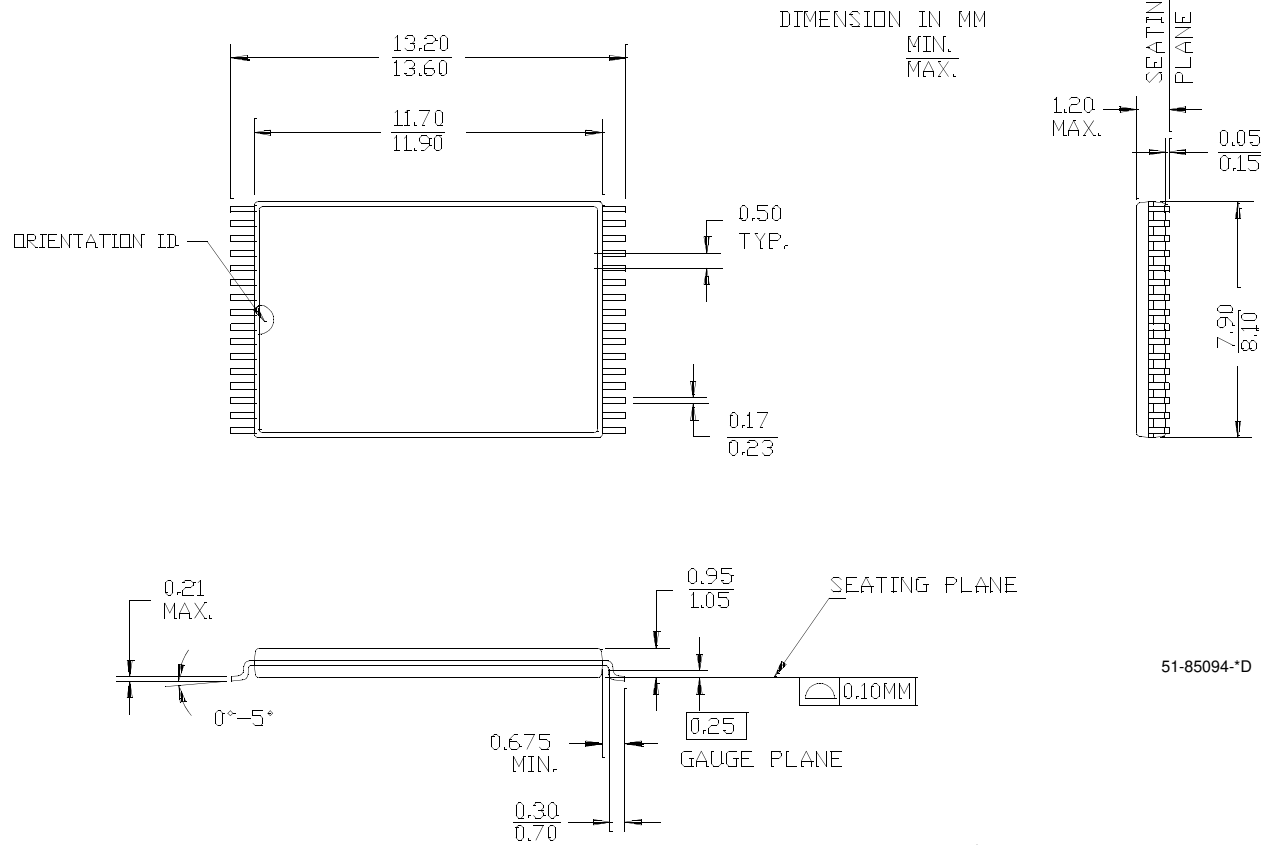
Package Diagrams

32-pin (450 Mil) Molded SOIC (51-85081)



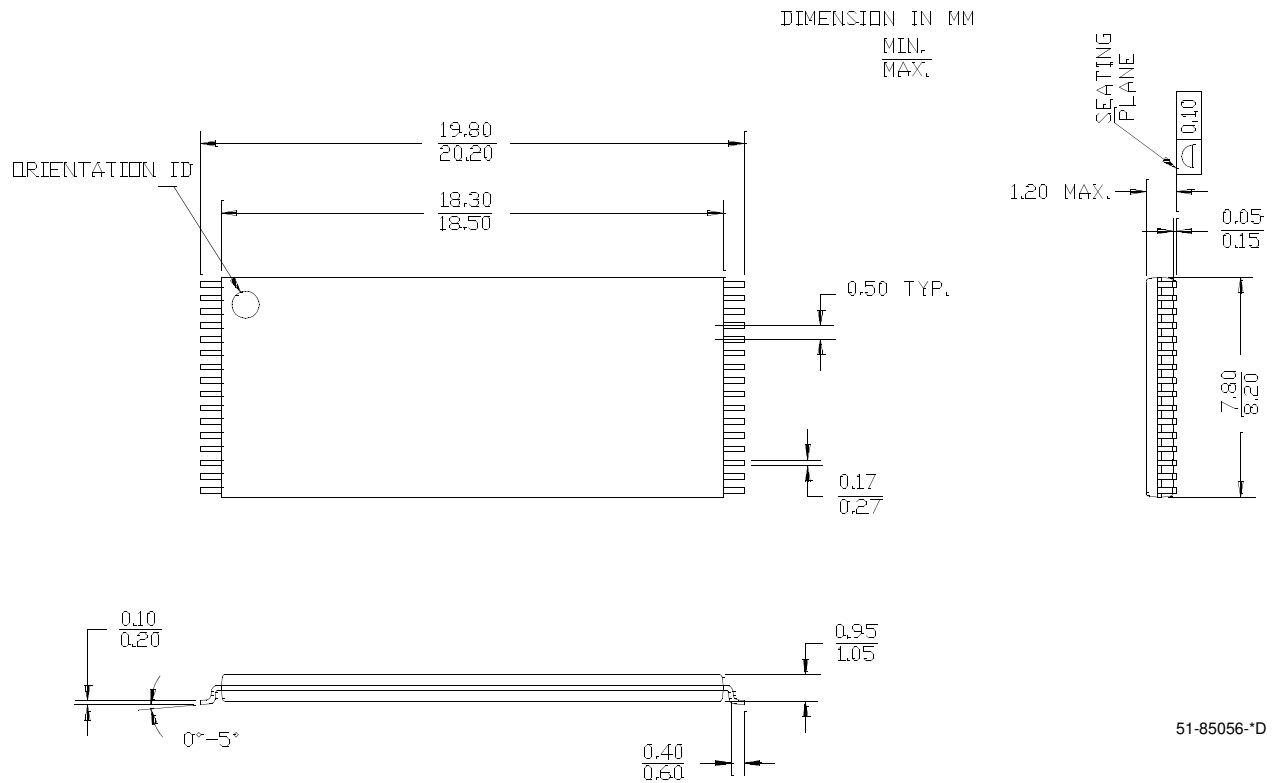
Package Diagrams (continued)

32-pin STSOP (8 x 13.4 mm) (51-85094)



Package Diagrams (continued)

32-pin TSOP Type I (8 x 20 mm) (51-85056)



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Document History Page

Document Title: CY62128BN MoBL® 1-Mbit (128K x 8) Static RAM Document Number: 001-06498				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	426503	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Removed RTSOP Package Updated ordering Information table

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