Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AT25PE40

4-Mbit DataFlash-L
Page Erase Serial Flash Memory

PRELIMINARY DATASHEET

Features

- Single 1.65V - 3.6V supply
- Serial Peripheral Interface (SPI) compatible
  - Supports SPI modes 0 and 3
  - Supports RapidS™ operation
- Continuous read capability through entire array
  - Up to 85MHz
  - Low-power read option up to 15 MHz
  - Clock-to-output time (t_V) of 6ns maximum
- User configurable page size
  - 256 bytes per page (default)
  - 264 bytes per page (customer selectable option)
- Two fully independent SRAM data buffers (256/264 bytes)
  - Allows receiving data while reprogramming the main memory array
- Flexible programming options
  - Byte/Page Program (1 to 256/264 bytes) directly into main memory
  - Buffer Write
  - Buffer to Main Memory Page Program
  - Single Command Page Read-Modify-Write Option
- Flexible erase options
  - Page Erase (256/264 bytes)
  - Block Erase (2KB)
  - Sector Erase (64KB)
  - Chip Erase (4-Mbits)
- 128-byte Security Register
  - 128 bytes factory programmed with a unique identifier
- Hardware and software controlled reset options
- JEDEC Standard Manufacturer and Device ID Read
- Low-power dissipation
  - 300nA Ultra-Deep Power-Down current (typical)
  - 5µA Deep Power-Down current (typical)
  - 25µA Standby current (typical)
  - 7mA Active Read current (typical)
- Endurance: 100,000 program/erase cycles per page minimum
- Data retention: 20 years
- Complies with full industrial temperature range
- Green (Pb/Halide-free/RoHS compliant) packaging options
  - 8-lead SOIC (0.150" wide and 0.208" wide)
  - 8-pad Ultra-thin DFN (5 x 6 x 0.6mm)

Description

The AT25PE40 is a 1.65V minimum, serial-interface sequential access Flash memory ideally suited for a wide variety of digital voice, image, program code, and data storage applications. The AT25PE40 also supports the RapidS serial interface for applications requiring very high speed operation. Its 4,194,304 bits of memory are organized as 2,048 pages of 256 bytes or 264 bytes each. In addition to the main memory, the AT25PE40 also contains two SRAM buffers of 256/264 bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Interleaving between both buffers can dramatically increase a system's ability to write a continuous data stream. In addition, the SRAM buffers can be used as additional system scratch pad memory, and E^2PROM emulation (bit or byte alterability) can be easily handled with a self-contained three step read-modify-write operation.

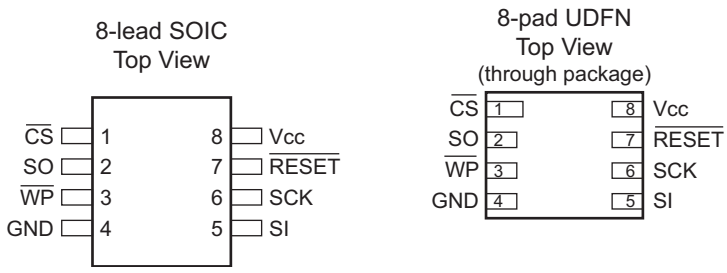
Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash-L® uses a serial interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates simplified hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage, and low-power are essential.

To allow for simple in-system re-programmability, the AT25PE40 does not require high input voltages for programming. The device operates from a single 1.65V to 3.6V power supply for the erase and program and read operations. The AT25PE40 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming and erase cycles are self-timed.

1. Pin Configurations and Pinouts

Figure 1-1. Pinouts



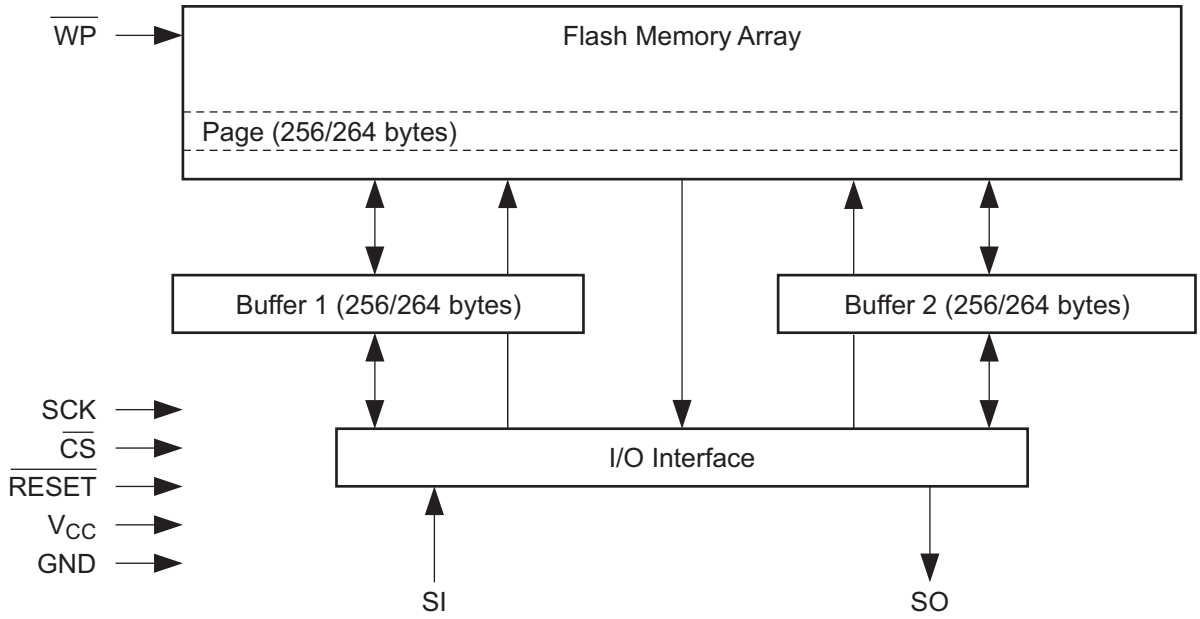
Note: 1. The metal pad on the bottom of the UDFN package is not internally connected to a voltage potential. This pad can be a “no connect” or connected to GND.

Table 1-1. Pin Configurations

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**Chip Select:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and normally be placed in the standby mode (not Deep Power-Down mode) and the output pin (SO) will be in a high-impedance state. When the device is deselected, data will not be accepted on the input pin (SI). A high-to-low transition on the $\overline{CS}$ pin is required to start an operation and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
SCK	**Serial Clock:** This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.	—	Input
SI	**Serial Input:** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched on the rising edge of SCK. Data present on the SI pin will be ignored whenever the device is deselected ($\overline{CS}$ is deasserted).	—	Input
SO	**Serial Output:** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. The SO pin will be in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	—	Output
$\overline{WP}$	**Write Protect:** When the $\overline{WP}$ pin is asserted, all sectors specified for protection by the Sector Protection Register will be protected against program and erase operations regardless of whether the Enable Sector Protection command has been issued or not. The $\overline{WP}$ pin functions independently of the software controlled protection method. After the $\overline{WP}$ pin goes low, the contents of the Sector Protection Register cannot be modified. If a program or erase command is issued to the device while the $\overline{WP}$ pin is asserted, the device will simply ignore the command and perform no operation. The device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The $\overline{WP}$ pin is internally pulled-high and may be left floating if hardware controlled protection will not be used. However, it is recommended that the $\overline{WP}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
$\overline{RESET}$	**Reset:** A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level. The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. If this pin and feature is not utilized, then it is recommended that the $\overline{RESET}$ pin be driven high externally.	Low	Input
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	—	Ground

2. Block Diagram

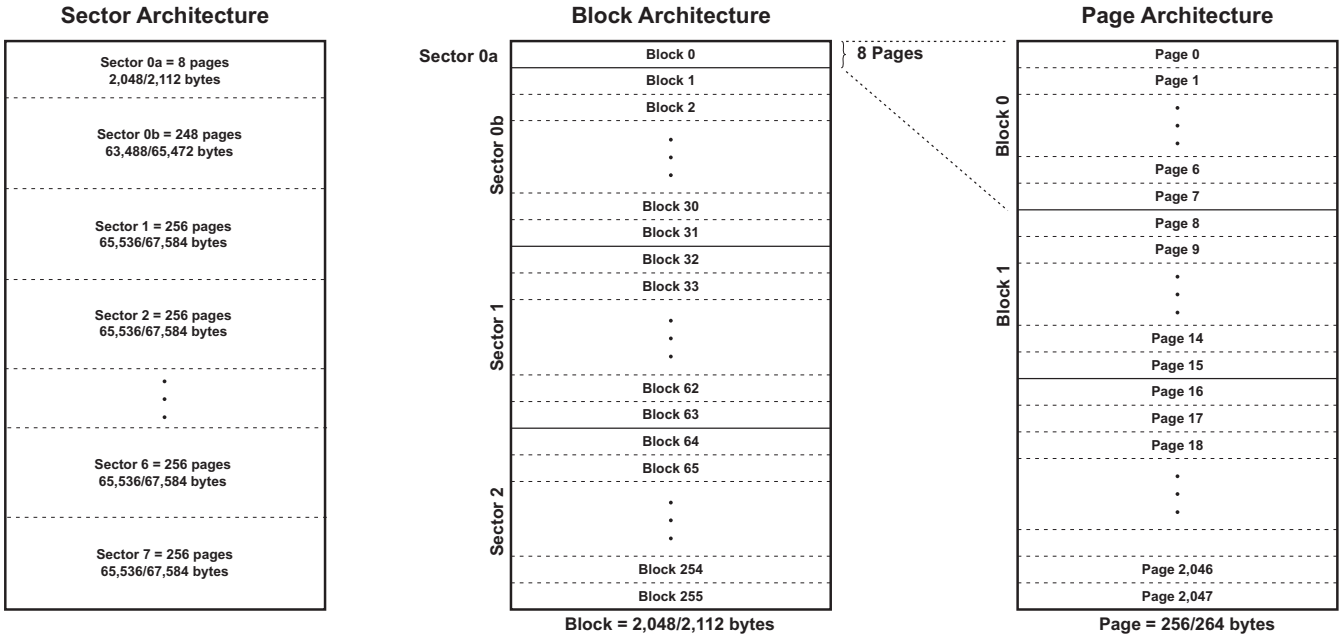
Figure 2-1. Block Diagram



3. Memory Array

To provide optimal flexibility, the AT25PE40 memory array is divided into three levels of granularity comprising of sectors, blocks, and pages. Figure 3-1, Memory Architecture Diagram illustrates the breakdown of each level and details the number of pages per sector and block. Program operations to the DataFlash-L can be done at the full page level or at the byte level (a variable number of bytes). The erase operations can be performed at the chip, sector, block, or page level.

Figure 3-1. Memory Architecture Diagram



4. Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 15-1 on page 34 through Table 15-4 on page 35. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (Serial Input) pin. All instructions, addresses, and data are transferred with the Most Significant Bit (MSB) first.

Three address bytes are used to address memory locations in either the main memory array or in one of the SRAM buffers. The three address bytes will be comprised of a number of dummy bits and a number of actual device address bits, with the number of dummy bits varying depending on the operation being performed and the selected device page size. Buffer addressing for the optional DataFlash-L page size (264 bytes) is referenced in the datasheet using the terminology BFA8 - BFA0 to denote the 9 address bits required to designate a byte address within a buffer. The main memory addressing is referenced using the terminology PA10 - PA0 and BA8 - BA0, where PA10 - PA0 denotes the 11 address bits required to designate a page address, and BA8 - BA0 denotes the 9 address bits required to designate a byte address within the page. Therefore, when using the optional DataFlash-L page size, a total of 20 address bits are used.

For the default page size (256 bytes), the buffer addressing is referenced in the datasheet using the conventional terminology BFA7 - BFA0 to denote the eight address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology A18 - A0, where A18 - A8 denotes the 11 address bits required to designate a page address, and A7 - A0 denotes the eight address bits required to designate a byte address within a page. Therefore, when using the default page size, a total of 19 address bits are used.

5. Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two SRAM data buffers. The DataFlash-L supports RapidS protocols for Mode 0 and Mode 3. Please see Section 25., Detailed Bit-level Read Waveforms: RapidS Mode 0/Mode 3 diagrams in this datasheet for details on the clock cycle sequences for each mode.

5.1 Continuous Array Read (Legacy Command: E8h Opcode)

By supplying an initial starting address for the main memory array, the Continuous Array Read command can be utilized to sequentially read a continuous stream of data from the device by simply providing a clock signal; no additional addressing information or control signals need to be provided. The DataFlash-L incorporates an internal address counter that will automatically increment on every clock cycle, allowing one continuous read from memory to be performed without the need for additional address sequences. To perform a Continuous Array Read using the optional DataFlash-L page size (264 bytes), an opcode of E8h must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence) and four dummy bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read and the last nine (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the default page size (256 bytes), an opcode of E8h must be clocked into the device followed by three address bytes and four dummy bytes. The first 11 bits (A18 - A8) of the 19-bit address sequence specify which page of the main memory array to read and the last eight bits (A7 - A0) of the 19-bit address sequence specify the starting byte address within the page. The dummy bytes that follow the address bytes are needed to initialize the read operation. Following the dummy bytes, additional clock pulses on the SCK pin will result in data being output on the SO (serial output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR1} specification. The Continuous Array Read bypasses the data buffers and leaves the contents of the buffers unchanged.

Warning: This command is not recommended for new designs.

5.2 Continuous Array Read (High Frequency Mode: 1Bh Opcode)

This command can be used to read the main memory array sequentially at the highest possible operating clock frequency up to the maximum specified by f_{CAR4}. To perform a Continuous Array Read using the optional DataFlash-L page size (264 bytes), the $\overline{CS}$ pin must first be asserted, and then an opcode of 1Bh must be clocked into the device followed by three address bytes and two dummy bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read and the last 9 bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the default page size (256 bytes), the opcode 1Bh must be clocked into the device followed by three address bytes (A18 - A0) and two dummy bytes. Following the dummy bytes, additional clock pulses on the SCK pin will result in data being output on the SO (Serial Output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR1} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.3 Continuous Array Read (High Frequency Mode: 0Bh Opcode)

This command can be used to read the main memory array sequentially at higher clock frequencies up to the maximum specified by f_{CAR1}. To perform a Continuous Array Read using the optional DataFlash-L page size (264 bytes), the $\overline{CS}$ pin must first be asserted, and then an opcode of 0Bh must be clocked into the device followed by three address bytes and one dummy byte. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read and the last 9 bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the default page size (256 bytes), the opcode 0Bh must be clocked into the device followed by three address bytes (A18 - A0) and one dummy byte. Following the dummy byte, additional clock pulses on the SCK pin will result in data being output on the SO pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy byte, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR1} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.4 Continuous Array Read (Low Frequency Mode: 03h Opcode)

This command can be used to read the main memory array sequentially at lower clock frequencies up to maximum specified by f_{CAR2}. Unlike the previously described read commands, this Continuous Array Read command for the lower clock frequencies does not require the clocking in of dummy bytes after the address byte sequence. To perform a Continuous Array Read using the optional DataFlash-L page size (264 bytes), the $\overline{CS}$ pin must first be asserted, and then an opcode of 03h must be clocked into the device followed by three address bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read and the last 9 bits (BA8 - BA0) of the address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the default page size (256 bytes), the opcode 03h must be clocked into the device followed by three address bytes (A18 - A0). Following the address bytes, additional clock pulses on the SCK pin will result in data being output on the SO pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR2} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.5 Continuous Array Read (Low Power Mode: 01h Opcode)

This command is ideal for applications that want to minimize power consumption and do not need to read the memory array at high frequencies. Like the 03h opcode, this Continuous Array Read command allows reading the main memory array sequentially without the need for dummy bytes to be clocked in after the address byte sequence. The memory can be read at clock frequencies up to maximum specified by f_{CAR3}. To perform a Continuous Array Read using the optional DataFlash-L page size (264 bytes), the $\overline{CS}$ pin must first be asserted, and then an opcode of 01h must be clocked into the device followed by three address bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which

page of the main memory array to read and the last 9 bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the default page size (256 bytes), the opcode 01h must be clocked into the device followed by three address bytes (A18 - A0). Following the address bytes, additional clock pulses on the SCK pin will result in data being output on the SO pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR3} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.6 Main Memory Page Read

A Main Memory Page Read allows the reading of data directly from a single page in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read using the optional DataFlash-L page size (264 bytes), an opcode of D2h must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence) and four dummy bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify the page in main memory to be read and the last nine bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within that page. To start a page read using the default page size (256 bytes), the opcode D2h must be clocked into the device followed by three address bytes and four dummy bytes. The first 11 bits (A18 - A8) of the 19-bit address sequence specify which page of the main memory array to read, and the last eight bits (A7 - A0) of the 19-bit address sequence specify the starting byte address within that page. The dummy bytes that follow the address bytes are sent to initialize the read operation. Following the dummy bytes, the additional pulses on SCK result in data being output on the SO (serial output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy bytes, and the reading of data. Unlike the Continuous Array Read command, when the end of a page in main memory is reached, the device will continue reading back at the beginning of the same page rather than the beginning of the next page.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Main Memory Page Read is defined by the f_{SCK} specification. The Main Memory Page Read bypasses both data buffers and leaves the contents of the buffers unchanged.

5.7 Buffer Read

The SRAM data buffers can be accessed independently from the main memory array, and utilizing the Buffer Read command allows data to be sequentially read directly from either one of the buffers. Four opcodes, D4h or D1h for Buffer 1 and D6h or D3h for Buffer 2, can be used for the Buffer Read command. The use of each opcode depends on the maximum SCK frequency that will be used to read data from the buffers. The D4h and D6h opcode can be used at any SCK frequency up to the maximum specified by f_{CAR1} while the D1h and D3h opcode can be used for lower frequency read operations up to the maximum specified by f_{CAR2}.

To perform a Buffer Read using the standard DataFlash-L buffer size (264 bytes), the opcode must be clocked into the device followed by three address bytes comprised of 15 dummy bits and 9 buffer address bits (BFA8 - BFA0). To perform a Buffer Read using the default buffer size (256 bytes), the opcode must be clocked into the device followed by three address bytes comprised of 16 dummy bits and eight buffer address bits (BFA7 - BFA0). Following the address bytes, one dummy byte must be clocked into the device to initialize the read operation if using opcodes D4h or D6h. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy byte (if using opcodes D4h or D6h), and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pin (SO).

6. Program and Erase Commands

6.1 Buffer Write

Utilizing the Buffer Write command allows data clocked in from the SI pin to be written directly into either one of the SRAM data buffers.

To load data into a buffer using the standard DataFlash-L buffer size (264 bytes), an opcode of 84h for Buffer 1 or 87h for Buffer 2 must be clocked into the device followed by three address bytes comprised of 15 dummy bits and nine buffer address bits (BFA8 - BFA0). The nine buffer address bits specify the first byte in the buffer to be written.

To load data into a buffer using the default buffer size (256 bytes), an opcode of 84h for Buffer 1 or 87h for Buffer 2, must be clocked into the device followed by 16 dummy bits and eight buffer address bits (BFA7 - BFA0). The eight buffer address bits specify the first byte in the buffer to be written.

After the last address byte has been clocked into the device, data can then be clocked in on subsequent clock cycles. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low-to-high transition is detected on the $\overline{CS}$ pin.

6.2 Buffer to Main Memory Page Program with Built-In Erase

The Buffer to Main Memory Page Program with Built-In Erase command allows data that is stored in one of the SRAM buffers to be written into an erased or programmed page in the main memory array. It is not necessary to pre-erase the page in main memory to be written because this command will automatically erase the selected page prior to the program cycle.

To perform a Buffer to Main Memory Page Program with Built-In Erase using the optional DataFlash-L page size (264 bytes), an opcode of 83h for Buffer 1 or 86h for Buffer 2 must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written, and nine dummy bits.

To perform a Buffer to Main Memory Page Program with Built-In Erase using the default page size (256 bytes), an opcode of 83h for Buffer 1 or 86h for Buffer 2 must be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written, and eight dummy bits.

When a low-to-high transition occurs on the $\overline{CS}$ pin, the device will first erase the selected page in main memory (the erased state is a Logic 1) and then program the data stored in the appropriate buffer into that same page in main memory. Both the erasing and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent erase and program algorithm that can detect when a byte location fails to erase or program properly. If an erase or programming error arises, it will be indicated by the EPE bit in the Status Register.

6.3 Buffer to Main Memory Page Program without Built-In Erase

The Buffer to Main Memory Page Program without Built-In Erase command allows data that is stored in one of the SRAM buffers to be written into a pre-erased page in the main memory array. It is necessary that the page in main memory to be written be previously erased in order to avoid programming errors.

To perform a Buffer to Main Memory Page Program without Built-In Erase using the optional DataFlash-L page size (264 bytes), an opcode of 88h for Buffer 1 or 89h for Buffer 2 must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written, and nine dummy bits.

To perform a Buffer to Main Memory Page Program using the default page size (256 bytes), an opcode of 88h for Buffer 1 or 89h for Buffer 2 must be clocked into the device followed by three address bytes comprised of three dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written, and eight dummy bits.

When a low-to-high transition occurs on the $\overline{CS}$ pin, the device will program the data stored in the appropriate buffer into the specified page in the main memory. The page in main memory that is being programmed must have been previously erased using one of the erase commands (Page Erase, Block Erase, Sector Erase, or Chip Erase). The programming of the page is internally self-timed and should take place in a maximum time of t_P. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it will be indicated by the EPE bit in the Status Register.

6.4 Main Memory Page Program through Buffer with Built-In Erase

The Main Memory Page Program through Buffer with Built-In Erase command combines the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations into a single operation to help simplify application firmware development. With the Main Memory Page Program through Buffer with Built-In Erase command, data is first clocked into either Buffer 1 or Buffer 2, the addressed page in memory is then automatically erased, and then the contents of the appropriate buffer are programmed into the just-erased main memory page.

To perform a Main Memory Page Program through Buffer using the optional DataFlash-L page size (264 bytes), an opcode of 82h for Buffer 1 or 85h for Buffer 2 must first be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written, and nine buffer address bits (BFA8 - BFA0) that select the first byte in the buffer to be written.

To perform a Main Memory Page Program through Buffer using the default page size (256 bytes), an opcode of 82h for Buffer 1 or 85h for Buffer 2 must first be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written, and eight buffer address bits (BFA7 - BFA0) that select the first byte in the buffer to be written.

After all address bytes have been clocked in, the device will take data from the input pin (SI) and store it in the specified data buffer. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low-to-high transition on the $\overline{CS}$ pin, the device will first erase the selected page in main memory (the erased state is a Logic 1) and then program the data stored in the buffer into that main memory page. Both the erasing and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent erase and programming algorithm that can detect when a byte location fails to erase or program properly. If an erase or program error arises, it will be indicated by the EPE bit in the Status Register.

6.5 Main Memory Byte/Page Program through Buffer 1 without Built-In Erase

The Main Memory Byte/Page Program through Buffer 1 without Built-In Erase command combines both the Buffer Write and Buffer to Main Memory Program without Built-In Erase operations to allow any number of bytes (1 to 256/264 bytes) to be programmed directly into previously erased locations in the main memory array. With the Main Memory Byte/Page Program through Buffer 1 without Built-In Erase command, data is first clocked into Buffer 1, and then only the bytes clocked into the buffer are programmed into the pre-erased byte locations in main memory. Multiple bytes up to the page size can be entered with one command sequence.

To perform a Main Memory Byte/Page Program through Buffer 1 using the optional DataFlash-L page size (264 bytes), an opcode of 02h must first be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written, and nine buffer address bits (BFA8 - BFA0) that select the first byte in the buffer to be written. After all address bytes are clocked in, the device will take data from the input pin (SI) and store it in Buffer 1. Any number of bytes (1 to 264) can be entered. If the end of the buffer is reached, then the device will wrap around back to the beginning of the buffer.

To perform a Main Memory Byte/Page Program through Buffer 1 using the default page size (256 bytes), an opcode of 02h for Buffer 1 using must first be clocked into the device followed by three address bytes comprised of three dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written, and eight buffer address bits (BFA7 - BFA0) that selects the first byte in the buffer to be written. After all address bytes are clocked in, the device will take data from the input pin (SI) and store it in Buffer 1. Any number of bytes (1 to 256) can be entered. If the end of the

buffer is reached, then the device will wrap around back to the beginning of the buffer. When using the default page size, the page and buffer address bits correspond to a 19-bit logical address (A18-A0) in the main memory.

After all data bytes have been clocked into the device, a low-to-high transition on the $\overline{CS}$ pin will start the program operation in which the device will program the data stored in Buffer 1 into the main memory array. Only the data bytes that were clocked into the device will be programmed into the main memory.

Example: If only two data bytes were clocked into the device, then only two bytes will be programmed into main memory and the remaining bytes in the memory page will remain in their previous state.

The $\overline{CS}$ pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, the operation will be aborted and no data will be programmed. The programming of the data bytes is internally self-timed and should take place in a maximum time of t_P (the program time will be a multiple of the t_{BP} time depending on the number of bytes being programmed). During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it will be indicated by the EPE bit in the Status Register.

6.6 Read-Modify-Write

A completely self-contained read-modify-write operation can be performed to reprogram any number of sequential bytes in a page in the main memory array without affecting the rest of the bytes in the same page. This command allows the device to easily emulate an EEPROM by providing a method to modify a single byte or more in the main memory in a single operation, without the need for pre-erasing the memory or the need for any external RAM buffers. The Read-Modify-Write command is essentially a combination of the Main Memory Page to Buffer Transfer, Buffer Write, and Buffer to Main Memory Page Program with Built-in Erase commands.

To perform a Read-Modify-Write using the optional DataFlash-L page size (264 bytes), an opcode of 58h for Buffer 1 or 59h for Buffer 2 must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written, and nine byte address bits (BA8 - BA0) that designate the starting byte address within the page to reprogram.

To perform a Read-Modify-Write using the default page size (256 bytes), an opcode of 58h for Buffer 1 or 59h for Buffer 2 must be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written, and eight byte address bits (A7 - A0) designate the starting byte address within the page to reprogram.

After the address bytes have been clocked in, any number of sequential data bytes from one to 256/264 bytes can be clocked into the device. If the end of the buffer is reached when clocking in the data, then the device will wrap around back to the beginning of the buffer. After all data bytes have been clocked into the device, a low-to-high transition on the CS pin will start the self-contained, internal read-modify-write operation. Only the data bytes that were clocked into the device will be reprogrammed in the main memory.

Example: If only one data byte was clocked into the device, then only one byte in main memory will be reprogrammed and the remaining bytes in the main memory page will remain in their previous state.

The $\overline{CS}$ pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, the operation will be aborted and no data will be programmed. The reprogramming of the data bytes is internally self-timed and should take place in a maximum time of t_P. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent erase and programming algorithm that can detect when a byte location fails to erase or program properly. If an erase or program error arises, it will be indicated by the EPE bit in the Status Register.

Note: The Read-Modify-Write command uses the same opcodes as the Auto Page Rewrite command. If no data bytes are clocked into the device, then the device will perform an Auto Page Rewrite operation. See the Auto Page Rewrite command description on page 22 for more details.

6.7 Page Erase

The Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-In Erase command or the Main Memory Byte/Page Program through Buffer 1 command to be utilized at a later time.

To perform a Page Erase with the optional DataFlash-L page size (264 bytes), an opcode of 81h must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be erased, and nine dummy bits.

To perform a Page Erase with the default page size (256 bytes), an opcode of 81h must be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be erased, and eight dummy bits.

When a low-to-high transition occurs on the $\overline{CS}$ pin, the device will erase the selected page (the erased state is a Logic 1). The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it will be indicated by the EPE bit in the Status Register.

6.8 Block Erase

The Block Erase command can be used to erase a block of eight pages at one time. This command is useful when needing to pre-erase larger amounts of memory and is more efficient than issuing eight separate Page Erase commands.

To perform a Block Erase with the optional DataFlash-L page size (264 bytes), an opcode of 50h must be clocked into the device followed by three address bytes comprised of four dummy bits, eight page address bits (PA10 - PA3), and 12 dummy bits. The eight page address bits are used to specify which block of eight pages is to be erased.

To perform a Block Erase with the default page size (256 bytes), an opcode of 50h must be clocked into the device followed by three address bytes comprised of five dummy bits, eight page address bits (A18 - A11), and 11 dummy bits. The eight page address bits are used to specify which block of eight pages is to be erased.

When a low-to-high transition occurs on the $\overline{CS}$ pin, the device will erase the selected block of eight pages. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it will be indicated by the EPE bit in the Status Register.

Table 6-1. Block Erase Addressing

PA10/ A18	PA9/ A17	PA8/ A16	PA7/ A15	PA6/ A14	PA5/ A13	PA4/ A12	PA3/ A11	PA2/ A10	PA1/ A9	PA0/ A8	Block
0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	1	1	X	X	X	3
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	1	1	1	1	1	0	0	X	X	X	252
1	1	1	1	1	1	0	1	X	X	X	253
1	1	1	1	1	1	1	0	X	X	X	254
1	1	1	1	1	1	1	1	X	X	X	255

6.9 Sector Erase

The Sector Erase command can be used to individually erase any sector in the main memory.

The main memory array is comprised of nine sectors, and only one sector can be erased at a time. To perform an erase of Sector 0a or Sector 0b with the optional DataFlash-L page size (264 bytes), an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of four dummy bits, eight page address bits (PA10 - PA3), and 12 dummy bits. To perform a Sector 1-7 erase, an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of four dummy bits, three page address bits (PA10 - PA8), and 17 dummy bits.

To perform a Sector 0a or Sector 0b erase with the default page size (256 bytes), an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of five dummy bits, eight page address bits (A18 - A11), and 11 dummy bits. To perform a Sector 1-7 erase, an opcode of 7Ch must be clocked into the device followed by three dummy bits, three page address bits (A18 - A16), and 16 dummy bits.

The page address bits are used to specify any valid address location within the sector to be erased. When a low-to high transition occurs on the $\overline{CS}$ pin, the device will erase the selected sector. The erase operation is internally self-timed and should take place in a maximum time of t_{SE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it will be indicated by the EPE bit in the Status Register.

Table 6-2. Sector Erase Addressing

PA10/ A18	PA9/ A17	PA8/ A16	PA7/ A15	PA6/ A14	PA5/ A13	PA4/ A12	PA3/ A11	PA2/ A10	PA1/ A9	PA0/ A8	Sector
0	0	0	0	0	0	0	0	X	X	X	0a
0	0	0	0	0	0	0	1	X	X	X	0b
0	0	1	X	X	X	X	X	X	X	X	1
0	1	0	X	X	X	X	X	X	X	X	2
0	1	1	X	X	X	X	X	X	X	X	3
1	0	0	X	X	X	X	X	X	X	X	4
1	0	1	X	X	X	X	X	X	X	X	5
1	1	0	X	X	X	X	X	X	X	X	6
1	1	1	X	X	X	X	X	X	X	X	7

6.10 Chip Erase

The Chip Erase command allows the entire main memory array to be erased can be erased at one time.

To execute the Chip Erase command, a 4-byte command sequence of C7h, 94h, 80h, and 9Ah must be clocked into the device. Since the entire memory array is to be erased, no address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to start the erase process. The erase operation is internally self-timed and should take place in a time of t_{CE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy.

The Chip Erase command will not affect sectors that are protected or locked down; the contents of those sectors will remain unchanged. Only those sectors that are not protected or locked down will be erased.

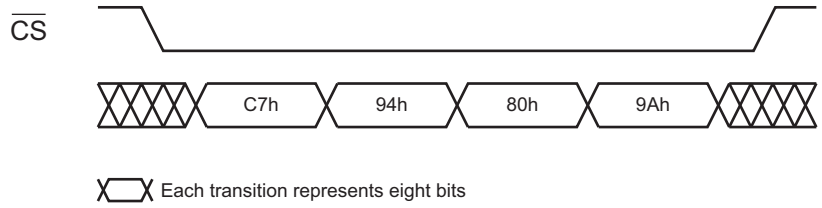
The $\overline{WP}$ pin can be asserted while the device is erasing, but protection will not be activated until the internal erase cycle completes.

The device also incorporates an intelligent algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it will be indicated by the EPE bit in the Status Register.

Table 6-3. Chip Erase Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Chip Erase	C7h	94h	80h	9Ah

Figure 6-1. Chip Erase



7. Sector Protection

Two protection methods, hardware and software controlled, are provided for protection against inadvertent or erroneous program and erase cycles. The software controlled method relies on the use of software commands to enable and disable sector protection while the hardware controlled method employs the use of the Write Protect ($\overline{WP}$) pin. The selection of which sectors that are to be protected or unprotected against program and erase operations is specified in the Nonvolatile Sector Protection Register. The status of whether or not sector protection has been enabled or disabled by either the software or the hardware controlled methods can be determined by checking the Status Register.

7.1 Software Sector Protection

Software controlled protection is useful in applications in which the $\overline{WP}$ pin is not or cannot be controlled by a host processor. In such instances, the $\overline{WP}$ pin may be left floating (the $\overline{WP}$ pin is internally pulled high) and sector protection can be controlled using the Enable Sector Protection and Disable Sector Protection commands.

If the device is power cycled, then the software controlled protection will be disabled. Once the device is powered up, the Enable Sector Protection command should be reissued if sector protection is desired and if the $\overline{WP}$ pin is not used.

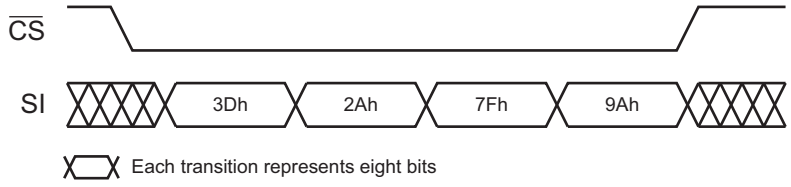
7.1.1 Enable Sector Protection

Sectors specified for protection in the Sector Protection Register can be protected from program and erase operations by issuing the Enable Sector Protection command. To enable the sector protection, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and A9h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to enable the Sector Protection.

Table 7-1. Enable Sector Protection Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Enable Sector Protection	3Dh	2Ah	7Fh	A9h

Figure 7-1. Enable Sector Protection



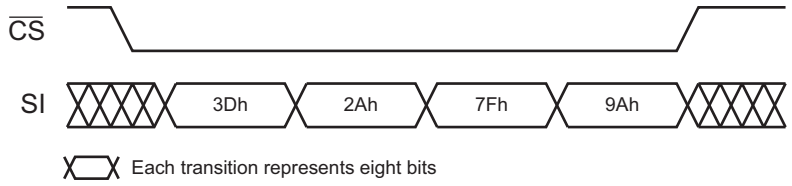
7.1.2 Disable Sector Protection

To disable the sector protection, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and 9Ah must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to disable the sector protection.

Table 7-2. Disable Sector Protection Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Disable Sector Protection	3Dh	2Ah	7Fh	9Ah

Figure 7-2. Disable Sector Protection



7.2 Hardware Controlled Protection

Sectors specified for protection in the Sector Protection Register and the Sector Protection Register itself can be protected from program and erase operations by asserting the $\overline{WP}$ pin and keeping the pin in its asserted state. The Sector Protection Register and any sector specified for protection cannot be erased or programmed as long as the $\overline{WP}$ pin is asserted. In order to modify the Sector Protection Register, the $\overline{WP}$ pin must be deasserted. If the $\overline{WP}$ pin is permanently connected to GND, then the contents of the Sector Protection Register cannot be changed. If the $\overline{WP}$ pin is deasserted or permanently connected to V_{CC}, then the contents of the Sector Protection Register can be modified.

The $\overline{WP}$ pin will override the software controlled protection method but only for protecting the sectors.

Example: If the sectors were not previously protected by the Enable Sector Protection command, then simply asserting the $\overline{WP}$ pin would enable the sector protection within the maximum specified t_{WPE} time. When the $\overline{WP}$ pin is deasserted, however, the sector protection would no longer be enabled (after the maximum specified t_{WPD} time) as long as the Enable Sector Protection command was not issued while the $\overline{WP}$ pin was asserted. If the Enable Sector Protection command was issued before or while the $\overline{WP}$ pin was asserted, then simply deasserting the $\overline{WP}$ pin would not disable the sector protection. In this case, the Disable Sector Protection command would need to be issued while the $\overline{WP}$ pin is deasserted to disable the sector protection. The Disable Sector Protection command is also ignored whenever the $\overline{WP}$ pin is asserted.

A noise filter is incorporated to help protect against spurious noise that may inadvertently assert or deassert the $\overline{WP}$ pin.

Figures 7-3 and Table 7-3 detail the sector protection status for various scenarios of the $\overline{WP}$ pin, the Enable Sector Protection command, and the Disable Sector Protection command.

Figure 7-3. $\overline{WP}$ Pin and Protection Status

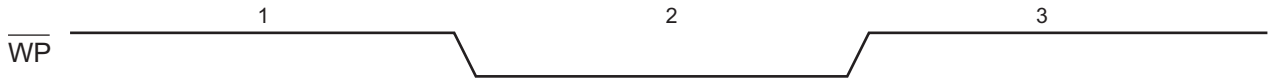


Table 7-3. $\overline{WP}$ Pin and Protection Status

Time Period	$\overline{WP}$ Pin	Enable Sector Protection Command	Disable Sector Protection Command	Sector Protection Status	Sector Protection Register
1	High	Command Not Issued Previously	X	Disabled	Read/Write
		—	Issue Command	Disabled	Read/Write
		Issue Command	—	Enabled	Read/Write
2	Low	X	X	Enabled	Read
3	High	Command Issued During Period 1 or 2	Not Issued Yet	Enabled	Read/Write
		—	Issue Command	Disabled	Read/Write
		Issue Command	—	Enabled	Read/Write

7.3 Sector Protection Register

The nonvolatile Sector Protection Register specifies which sectors are to be protected or unprotected with either the software or hardware controlled protection methods. The Sector Protection Register contains eight bytes of data, of which byte locations zero through seven contain values that specify whether Sectors 0 through 7 will be protected or unprotected. The Sector Protection Register is user modifiable and must be erased before it can be reprogrammed. Table 7-4 illustrates the format of the Sector Protection Register.

Table 7-4. Sector Protection Register

Sector Number	0 (0a, 0b)	1 to 7
Protected	See Table 7-5	FFh
Unprotected		00h

Note: 1. The default values for bytes 0 through 7 are 00h when shipped from Adesto.

Table 7-5. Sector 0 (0a, 0b) Sector Protection Register Byte Value

	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0	
	Sector 0a (Page 0-7)	Sector 0b (Page 8-15)	N/A	N/A	Data Value
Sectors 0a and 0b Unprotected	00	00	XX	XX	0xh
Protect Sector 0a	11	00	XX	XX	Cxh
Protect Sector 0b	00	11	XX	XX	3xh
Protect Sectors 0a and 0b	11	11	XX	XX	Fxh

Note: 1. x = Don't care

7.3.1 Erase Sector Protection Register

In order to modify and change the values of the Sector Protection Register, it must first be erased using the Erase Sector Protection Register command.

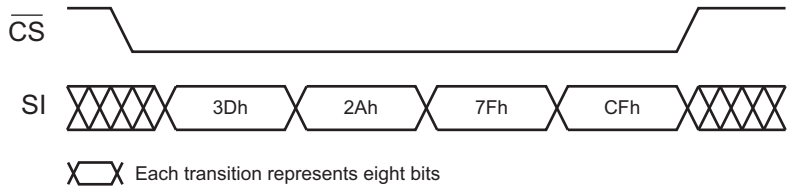
To erase the Sector Protection Register, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and CFh must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed erase cycle. The erasing of the Sector Protection Register should take place in a maximum time of t_{PE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy. If the device is powered-down before the completion of the erase cycle, then the contents of the Sector Protection Register cannot be guaranteed.

The Sector Protection Register can be erased with sector protection enabled or disabled. Since the erased state (FFh) of each byte in the Sector Protection Register is used to indicate that a sector is specified for protection, leaving the sector protection enabled during the erasing of the register allows the protection scheme to be more effective in the prevention of accidental programming or erasing of the device. If for some reason an erroneous program or erase command is sent to the device immediately after erasing the Sector Protection Register and before the register can be reprogrammed, then the erroneous program or erase command will not be processed because all sectors would be protected.

Table 7-6. Erase Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Erase Sector Protection Register	3Dh	2Ah	7Fh	CFh

Figure 7-4. Erase Sector Protection Register



7.3.2 Program Sector Protection Register

Once the Sector Protection Register has been erased, it can be reprogrammed using the Program Sector Protection Register command.

To program the Sector Protection Register, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and FCh must be clocked into the device followed by eight bytes of data corresponding to Sectors 0 through 7. After the last bit of the opcode sequence and data have been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the Sector Protection Register should take place in a maximum time of t_P. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy. If the device is powered-down before the completion of the erase cycle, then the contents of the Sector Protection Register cannot be guaranteed.

If the proper number of data bytes is not clocked in before the $\overline{CS}$ pin is deasserted, then the protection status of the sectors corresponding to the bytes not clocked in cannot be guaranteed.

Example: If only the first two bytes are clocked in instead of the complete eight bytes, then the protection status of the last 14 sectors cannot be guaranteed. Furthermore, if more than eight bytes of data is clocked into the device, then the data will wrap back around to the beginning of the register. For instance, if nine bytes of data are clocked in, then the ninth byte will be stored at byte location 0 of the Sector Protection Register.

The data bytes clocked into the Sector Protection Register need to be valid values (0xh, 3xh, Cxh, and Fxh for Sector 0a or Sector 0b, and 00h or FFh for other sectors) in order for the protection to function correctly. If a non-valid value is clocked into a byte location of the Sector Protection Register, then the protection status of the sector corresponding to that byte location cannot be guaranteed.

Example: If a value of 17h is clocked into byte location 2 of the Sector Protection Register, then the protection status of Sector 2 cannot be guaranteed.

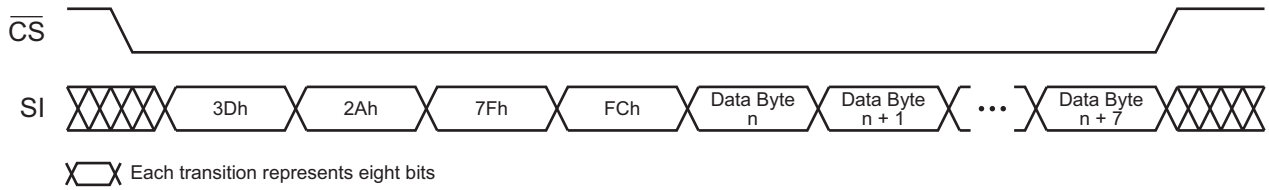
The Sector Protection Register can be reprogrammed while the sector protection is enabled or disabled. Being able to reprogram the Sector Protection Register with the sector protection enabled allows the user to temporarily disable the sector protection to an individual sector rather than disabling sector protection completely.

The Program Sector Protection Register command utilizes Buffer 1 for processing. Therefore, the contents of Buffer 1 will be altered from its previous state when this command is issued.

Table 7-7. Program Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Program Sector Protection Register	3Dh	2Ah	7Fh	FCh

Figure 7-5. Program Sector Protection Register



7.3.3 Read Sector Protection Register

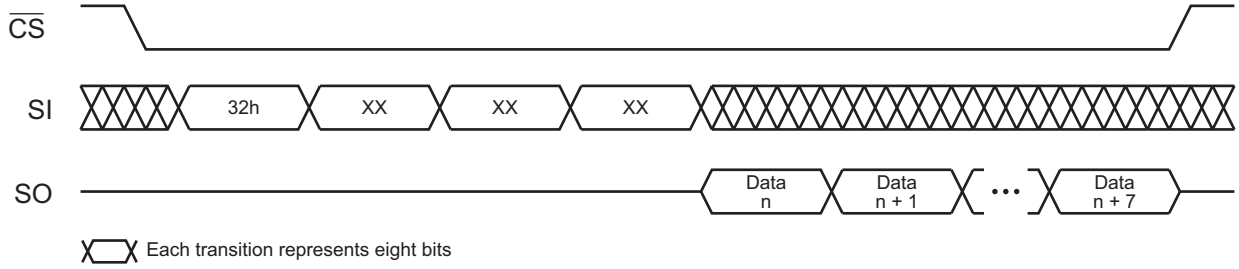
To read the Sector Protection Register, an opcode of 32h and three dummy bytes must be clocked into the device. After the last bit of the opcode and dummy bytes have been clocked in, any additional clock pulses on the SCK pin will result in the Sector Protection Register contents being output on the SO pin. The first byte (byte location 0) corresponds to Sector 0 (0a and 0b), the second byte corresponds to Sector 1, and the last byte (byte location 7) corresponds to Sector 7. Once the last byte of the Sector Protection Register has been clocked out, any additional clock pulses will result in undefined data being output on the SO pin. The $\overline{CS}$ pin must be deasserted to terminate the Read Sector Protection Register operation and put the output into a high-impedance state.

Table 7-8. Read Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Protection Register	32h	XXh	XXh	XXh

Note: 1. XX = Dummy byte

Figure 7-6. Read Sector Protection Register



7.3.4 About the Sector Protection Register

The Sector Protection Register is subject to a limit of 10,000 erase/program cycles. Users are encouraged to carefully evaluate the number of times the Sector Protection Register will be modified during the course of the application's life cycle. If the application requires that the Security Protection Register be modified more than the specified limit of 10,000 cycles because the application needs to temporarily unprotect individual sectors (sector protection remains enabled while the Sector Protection Register is reprogrammed), then the application will need to limit this practice. Instead, a combination of temporarily unprotecting individual sectors along with disabling sector protection completely will need to be implemented by the application to ensure that the limit of 10,000 cycles is not exceeded.

8. Security Features

8.1 Security Register

The device contains a specialized Security Register that can be used for purposes such as unique device serialization or locked key storage. The register is comprised of a total of 128 bytes (byte locations 0 through 127). All 128 bytes of the Security Register are factory programmed by Adesto and will contain a unique value for each device. The factory programmed data is fixed and cannot be changed.

Table 8-1. Security Register

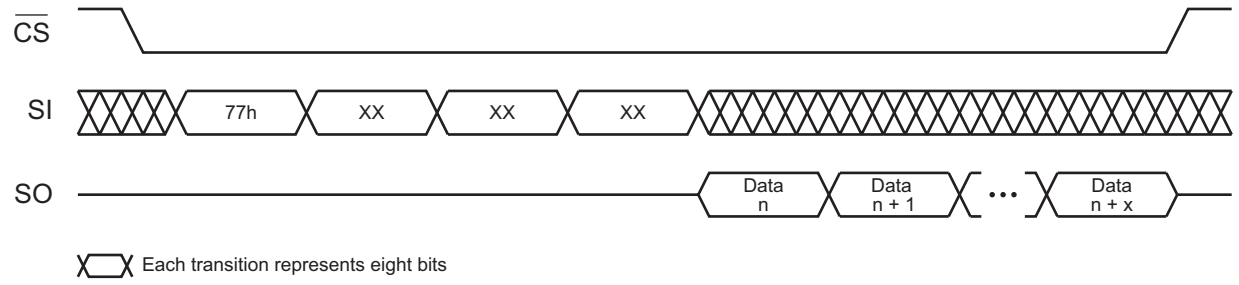
	Security Register Byte Number							
	0	1	. . .		. . .		. . .	127
Data Type	Factory Programmed by Adesto							

8.1.1 Reading the Security Register

To read the Security Register, an opcode of 77h and three dummy bytes must be clocked into the device. After the last dummy bit has been clocked in, the contents of the Security Register can be clocked out on the SO pin. After the last byte of the Security Register has been read, additional pulses on the SCK pin will result in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin will terminate the Read Security Register operation and put the SO pin into a high-impedance state.

Figure 8-1. Read Security Register



9. Additional Commands

9.1 Main Memory Page to Buffer Transfer

A page of data can be transferred from the main memory to either Buffer 1 or Buffer 2. To transfer a page of data using the optional DataFlash-L page size (264 bytes), an opcode of 53h for Buffer 1 or 55h for Buffer 2 must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) which specify the page in main memory to be transferred, and nine dummy bits. To transfer a page of data using the default page size (256 bytes), an opcode of 53h for Buffer 1 and 55h for Buffer 2 must be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) which specify the page in the main memory to be transferred, and eight dummy bits.

The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode and the three address bytes from the input pin (SI). The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the page transfer time (t_{XFR}), the RDY/$\overline{BUSY}$ bit in the Status Register can be read to determine whether or not the transfer has been completed.

9.2 Main Memory Page to Buffer Compare

A page of data in main memory can be compared to the data in Buffer 1 or Buffer 2 as a method to ensure that data was successfully programmed after a Buffer to Main Memory Page Program command. To compare a page of data with the optional DataFlash-L page size (264 bytes), an opcode of 60h for Buffer 1 or 61h for Buffer 2 must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) which specify the page in the main memory to be compared to the buffer, and nine dummy bits. To compare a page of data with the default page size (256 bytes), an opcode of 60h for Buffer 1 or 61h for Buffer 2 must be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) which specify the page in the main memory to be compared to the buffer, and eight dummy bits.

The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode and the address bytes from the input pin (SI). On the low-to-high transition of the $\overline{CS}$ pin, the data bytes in the selected Main Memory Page will be compared with the data bytes in Buffer 1 or Buffer 2. During the compare time (t_{COMP}), the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the part is busy. On completion of the compare operation, bit 6 of the Status Register will be updated with the result of the compare.

9.3 Auto Page Rewrite

This command only needs to be used if the possibility exists that static (non-changing) data may be stored in a page or pages of a sector and the other pages of the same sector are erased and programmed a large number of times. Applications that modify data in a random fashion within a sector may fall into this category. To preserve data integrity of a sector, each page within a sector must be updated/rewritten at least once within every 50,000 cumulative page erase/program operations within that sector. The Auto Page Rewrite command provides a simple and efficient method to “refresh” a page in the main memory array in a single operation.

The Auto Page Rewrite command is a combination of the Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase commands. With the Auto Page Rewrite command, a page of data is first transferred from the main memory to Buffer 1 or Buffer 2 and then the same data (from Buffer 1 or Buffer 2) is programmed back into the same page of main memory, essentially “refreshing” the contents of that page. To start the Auto Page Rewrite operation with the optional DataFlash-L page size (264 bytes), a 1-byte opcode, 58H for Buffer 1 or 59H for Buffer 2, must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10-PA0) that specify the page in main memory to be rewritten, and nine dummy bits.

To initiate an Auto Page Rewrite with the a default page size (256 bytes), the opcode 58H for Buffer 1 or 59H for Buffer 2, must be clocked into the device followed by three address bytes consisting of five dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory that is to be rewritten, and eight dummy bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the RDY/$\overline{BUSY}$ Status Register will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page and the possibility does not exist that there will be a page or pages of static data, then the programming algorithm shown in Figure 26-1 on page 55 is recommended. Otherwise, if there is a chance that there may be a page or pages of a sector that will contain static data, then the programming algorithm shown in Figure 26-2 on page 56 is recommended.

Note: The Auto Page Rewrite command uses the same opcodes as the Read-Modify-Write command. If data bytes are clocked into the device, then the device will perform a Read-Modify-Write operation. See the Read-Modify-Write command description on page 12 for more details.

9.4 Status Register Read

The 2-byte Status Register can be used to determine the device's ready/busy status, page size, a Main Memory Page to Buffer Compare operation result, the sector protection status, erase/program error status, and the device density. The Status Register can be read at any time, including during an internally self-timed program or erase operation.

To read the Status Register, the $\overline{CS}$ pin must first be asserted and then the opcode D7h must be clocked into the device. After the opcode has been clocked in, the device will begin outputting Status Register data on the SO pin during every subsequent clock cycle. After the second byte of the Status Register has been clocked out, the sequence will repeat itself, starting again with the first byte of the Status Register, as long as the $\overline{CS}$ pin remains asserted and the clock pin is being pulsed. The data in the Status Register is constantly being updated, so each repeating sequence may output new data. The RDY/$\overline{BUSY}$ status is available for both bytes of the Status Register and is updated for each byte.

Deasserting the $\overline{CS}$ pin will terminate the Status Register Read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Table 9-1. Status Register Format – Byte 1

Bit	Name		Type[1]	Description	
7	RDY/$\overline{BUSY}$	Ready/Busy Status	R	0	Device is busy with an internal operation.
				1	Device is ready.
6	COMP	Compare Result	R	0	Main memory page data matches buffer data.
				1	Main memory page data does not match buffer data.
5:2	DENSITY	Density Code	R	0111	4-Mbit
1	PROTECT	Sector Protection Status	R	0	Sector protection is disabled.
				1	Sector protection is enabled.
0	PAGE SIZE	Page Size Configuration	R	0	Device is configured for optional DataFlash-L page size (264 bytes).
				1	Device is configured for default page size (256 bytes).

Note: 1. R = Readable only

Table 9-2. Status Register Format – Byte 2

Bit	Name		Type[1]	Description	
7	RDY/$\overline{\text{BUSY}}$	Ready/Busy Status	R	0	Device is busy with an internal operation.
				1	Device is ready.
6	RES	*Reserved for Future Use*	R	0	*Reserved for future use.*
5	EPE	Erase/Program Error	R	0	Erase or program operation was successful.
				1	Erase or program error detected.
4	RES	*Reserved for Future Use*	R	0	*Reserved for future use.*
3	RES	*Reserved for Future Use*	R	0	*Reserved for future use.*
2	RES	*Reserved for Future Use*	R	x	*Reserved for future use.*
1	RES	*Reserved for Future Use*	R	x	*Reserved for future use.*
0	RES	*Reserved for Future Use*	R	x	*Reserved for future use.*

Note: 1. R = Readable only

2. x = “Don’t care”. Can be “0” or “1”.

9.4.1 RDY/$\overline{\text{BUSY}}$ Bit

The RDY/$\overline{\text{BUSY}}$ bit is used to determine whether or not an internal operation, such as a program or erase, is in progress. To poll the RDY/$\overline{\text{BUSY}}$ bit to detect the completion of an internally timed operation, new Status Register data must be continually clocked out of the device until the state of the RDY/$\overline{\text{BUSY}}$ bit changes from a Logic 0 to a Logic 1.

9.4.2 COMP Bit

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using the COMP bit. If the COMP bit is a Logic 1, then at least one bit of the data in the Main Memory Page does not match the data in the buffer.

9.4.3 DENSITY Bits

The device density is indicated using the DENSITY bits. For the AT25PE40, the four bit binary value is 0111. The decimal value of these four binary bits does not actually equate to the device density; the four bits represent a combinational code relating to differing densities of DataFlash-L devices. The DENSITY bits are not the same as the density code indicated in the JEDEC Device ID information. The DENSITY bits are provided only for backward compatibility to older generation DataFlash-L devices.

9.4.4 PROTECT Bit

The PROTECT bit provides information to the user on whether or not the sector protection has been enabled or disabled, either by the software-controlled method or the hardware-controlled method.

9.4.5 PAGE SIZE Bit

The PAGE SIZE bit indicates whether the buffer size and the page size of the main memory array is configured for the default page size (256 bytes) or the optional DataFlash-L page size (264 bytes).

9.4.6 EPE Bit

The EPE bit indicates whether the last erase or program operation completed successfully or not. If at least one byte during the erase or program operation did not erase or program properly, then the EPE bit will be set to the Logic 1 state. The EPE bit will not be set if an erase or program operation aborts for any reason.. The EPE bit is updated after every erase and program operation.

10. Deep Power-Down

During normal operation, the device will be placed in the standby mode to consume less power as long as the $\overline{CS}$ pin remains deasserted and no internal operation is in progress. The Deep Power-Down command offers the ability to place the device into an even lower power consumption state called the Deep Power-Down mode.

When the device is in the Deep Power-Down mode, all commands including the Status Register Read command will be ignored with the exception of the Resume from Deep Power-Down command. Since all commands will be ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Deep Power-Down mode is accomplished by simply asserting the $\overline{CS}$ pin, clocking in the opcode B9h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the device will enter the Deep Power-Down mode within the maximum time of t_{EDPD}.

The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device will abort the operation and return to the standby mode once the $\overline{CS}$ pin is deasserted. In addition, the device will default to the standby mode after a power cycle.

The Deep Power-Down command will be ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Deep Power-Down mode.

Figure 10-1. Deep Power-Down