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AT25SL128A

128-Mbit, 1.7V Minimum
SPI Serial Flash Memory with Dual I/O, Quad I/O and QPI Support

Features

- Single 1.7V - 2.0V Supply
- Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI) Compatible
  - Supports SPI Modes 0 and 3
  - Supports Dual Output Read and Quad I/O Program and Read
  - Supports QPI Program and Read
  - 104 MHz* Maximum Operating Frequency
  - Clock-to-Output (t_{V1}) of 6 ns
  - Up tp 52MB/S continuous data transfer rate
- Full Chip Erase
- Flexible, Optimized Erase Architecture for Code and Data Storage Applications
  - 0.6 ms Typical Page Program (256 Bytes) Time
  - 60 ms Typical 4-Kbyte Block Erase Time
  - 200 ms Typical 32-Kbyte Block Erase Time
  - 350 ms Typical 64-Kbyte Block Erase Time
- Hardware Controlled Locking of Status Registers via $\overline{WP}$ Pin
- 4K-bit secured One-Time Programmable Security Register
- Hardware Write Protection
- Serial Flash Discoverable Parameters (SFDP) Register
- Flexible Programming
  - Byte/Page Program (1 to 256 Bytes)
  - Dual or Quad Input Byte/Page Program (1 to 256 Bytes)
- Erase/Program Suspend and Resume
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
  - 2µA Deep Power-Down Current (Typical)
  - 10µA Standby current (Typical)
  - 5mA Active Read Current (Typical)
- Endurance: 100,000 program/erase cycles (4KB, 32KB or 64KB blocks)
- Data Retention: 20 Years
- Industrial Temperature Range: -40°C to +85°C
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
  - 8-lead SOIC (208-mil)
  - 8-pad DFN (6 x 5 x 0.6 mm)
  - 21-ball die Ball Grid Array (dBGA - WLCSP)
  - Die in Wafer Form

1. Introduction

The Adesto® AT25SL128A is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT25SL128A is ideal for data storage as well, eliminating the need for additional data storage devices.

The erase block sizes of the AT25SL128A have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz for Dual Output and 416MHz for Quad Output when using the QPI and Fast Read Dual/Quad I/O instructions.The AT25SL128A array is organized into 65,536 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instructions. Pages can be erased 4KB Block, 32KB Block, 64KB Block or the entire chip.

The devices operate on a single 1.7V to 2.0V power supply with current consumption as low as 5mA active and 3µA for Deep Power Down. All devices offered in space-saving packages. The device supports JEDEC standard manufacturer and device identification with a 4K-bit Secured OTP.

2. Pinouts and Pin Descriptions

The following figures show the available package types.

Figure 1-1. 8-SOIC (Top View)

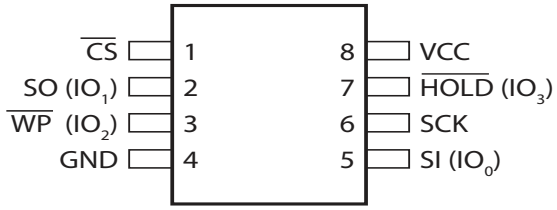


Figure 1-2. 8-UDFN (Top View)

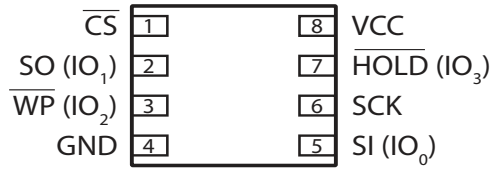
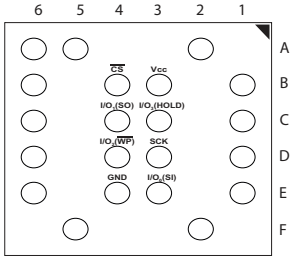


Figure 1-3. 21-WLCSP (Bottom View)



During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC} (min) to V_{CC} (max).
All of the input and output signals must be held high or low (according to voltages of VIH, VOH, VIL or VOL.

Table 1-1. Pin Descriptions

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**CHIP SELECT** When this input signal is high, the device is deselected and serial data output pins are at high impedance. Unless an internal program, erase or write status register cycle is in progress, the device will be in the standby power mode (this is not the deep power down mode). Driving Chip Select ($\overline{CS}$) low enables the device, placing it in the active power mode. After power-up, a falling edge on Chip Select ($\overline{CS}$) is required prior to the start of any instruction.	Low	Input
SCK	**SERIAL CLOCK** This input signal provides the timing for the serial interface. Instructions, addresses, or data present at serial data input are latched on the rising edge of Serial Clock (SCK). Data are shifted out on the falling edge of the Serial Clock (SCK).	-	Input
SI (I/O_0)	**SERIAL INPUT** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched in on the rising edge of SCK. With the Dual-Output and Quad-Output Read commands, the SI Pin becomes an output pin (I/O_0) in conjunction with other pins to allow two or four bits of data on (I/O_{3-0}) to be clocked in on every falling edge of SCK To maintain consistency with the SPI nomenclature, the SI (I/O_0) pin is referenced as the SI pin unless specifically addressing the Dual-I/O and Quad-I/O modes in which case it is referenced as I/O_0. Data present on the SI pin is ignored whenever the device is deselected ($\overline{CS}$ is deasserted).	-	Input/Output
SO (I/O_1)	**SERIAL OUTPUT** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. With the Dual-Output Read commands, the SO Pin remains an output pin (I/O0) in conjunction with other pins to allow two bits of data on (I/O_{1-0}) to be clocked in on every falling edge of SCK To maintain consistency with the SPI nomenclature, the SO (I/O_1) pin is referenced as the SO pin unless specifically addressing the Dual-I/O modes in which case it is referenced as I/O_1. The SO pin is in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	-	Input/Output
$\overline{WP}$ (I/O_2)	**WRITE PROTECT** The Write Protect ($\overline{WP}$) pin can be used to protect the Status Register against data modification. Used in company with the Status Register's Block Protect (SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect SRP) bits, a portion or the entire memory array can be hardware protected. The $\overline{WP}$ pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the $\overline{WP}$ pin (Hardware Write Protect) function is not available since this pin is used for IO_2. See figures 1-1, 1-2, and 1-3 for the pin configuration of Quad I/O and QPI operation.	-	Input/Output

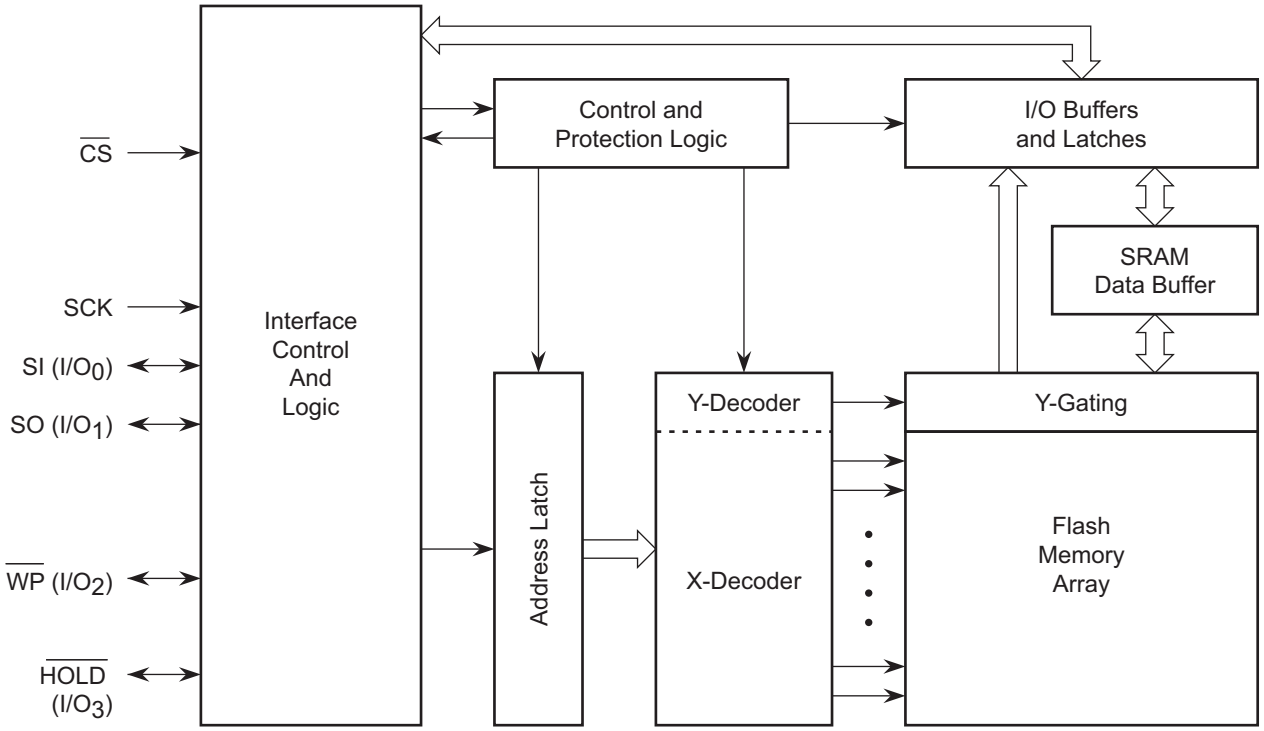
Table 1-1. Pin Descriptions (Continued)

Symbol	Name and Function	Asserted State	Type
$\overline{HOLD}$ (I/O_3)	**HOLD** The $\overline{HOLD}$ pin is used to temporarily pause serial communication without deselecting or resetting the device. While the $\overline{HOLD}$ pin is asserted, transitions on the SCK pin and data on the SI pin are ignored and the SO pin is placed in a high-impedance state. The $\overline{CS}$ pin must be asserted, and the SCK pin must be in the low state in order for a Hold condition to start. A Hold condition pauses serial communication only and does not have an effect on internally self-timed operations such as a program or erase cycle. With the Quad-Input Byte/Page Program command, the $\overline{HOLD}$ pin becomes an input pin (I/O_3) and with other pins, allows four bits (on I/O_{3-0}) of data to be clocked in on every rising edge of SCK. With the Quad-Output Read commands, the $\overline{HOLD}$ Pin becomes an output pin (I/O_3) in conjunction with other pins to allow four bits of data on ($I/O3_{3-0}$) to be clocked in on every falling edge of SCK. To maintain consistency with SPI nomenclature, the $\overline{HOLD}$ (I/O_3) pin is referenced as the $\overline{HOLD}$ pin unless specifically addressing the Quad-I/O modes in which case it is referenced as I/O_3. The $\overline{HOLD}$ pin is internally pulled-high and may be left floating if the Hold function is not used. However, it is recommended that the $\overline{HOLD}$ pin also be externally connected to V_{CC} whenever possible. See figures 1-1, 1-2, and 1-3 for the pin configuration of Quad I/O and QPI operation.	-	Input/Output
V_{CC}	**DEVICE POWER SUPPLY:** V_{CC} is the supply voltage. It is the single voltage used for all device functions including read, program, and erase. The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	-	Power
GND	**GROUND:** V_{SS} is the reference for the V_{CC} supply voltage. The ground reference for the power supply. GND should be connected to the system ground.	-	Power

2. Block Diagram

Figure 2-1 shows a block diagram of the AT25SL128A serial Flash.

Figure 2-1. AT25SL128A Block Diagram



Note: I/O_{3-0} pin naming convention is used for Dual-I/O and Quad-I/O commands.

3. Memory Array

To provide the greatest flexibility, the memory array of the AT25SL128A can be erased in four levels of granularity including a full chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions. The Memory Architecture Diagram illustrates the breakdown of each erase level.

Figure 3-1. Memory Architecture Diagram

Block Erase Detail				Page Program Detail	
64KB	32KB	4KB	Block Address Range	1-256 Byte	Page Address Range
Sector 255	Block 511	4KB	FFFFFFh – FFF000h	256 Bytes	FFFFFFh – FFFF00h
		4KB	FFEFFFh – FFE000h	256 Bytes	FFFEFFh – FFFE00h
		4KB	FFDFFFh – FFD000h	256 Bytes	FFFDFFh - FFFD00h
		4KB	FFCFFFh – FFC000h	256 Bytes	FFFCFFh – FFFC00h
		4KB	FFBFFFh – FFB000h	256 Bytes	FFFBFFh – FFFB00h
		4KB	FFAFFFh – FFA000h	256 Bytes	FFFAFFh – FFFA00h
		4KB	FF9FFFh – FF9000h	256 Bytes	FFF9FFh – FFF900h
		4KB	FF8FFFh – FF8000h	256 Bytes	FFF8FFh – FFF800h
	Block 510	4KB	FF7FFFh – FF7000h	256 Bytes	FFF7FFh – FFF700h
		4KB	FF6FFFh – FF6000h	256 Bytes	FFF6FFh – FFF600h
		4KB	FF5FFFh – FF5000h	256 Bytes	FFF5FFh – FFF500h
		4KB	FF4FFFh – FF4000h	256 Bytes	FFF4FFh – FFF400h
		4KB	FF3FFFh – FF3000h	256 Bytes	FFF3FFh – FFF300h
		4KB	FF2FFFh – FF2000h	256 Bytes	FFF2FFh – FFF200h
		4KB	FF1FFFh – FF1000h	256 Bytes	FFF1FFh – FFF100h
		4KB	FF0FFFh – FF0000h	256 Bytes	FFF0FFh – FFF000h
Sector 254	Block 509	4KB	FEFFFFh – FEF000h	256 Bytes	FFEFFFh – FFEF00h
		4KB	FEEFFFh – FEE000h	256 Bytes	FFEEFFh – FFEE00h
		4KB	FEDFFFh – FED000h	256 Bytes	FFEDFFh – FFED00h
		4KB	FECFFFh – FEC000h	256 Bytes	FFECFFh – FFEC00h
		4KB	FEBFFFh – FEB000h	256 Bytes	FFEBFFh – FFEB00h
		4KB	FEAFFFh – FEA000h	256 Bytes	FFEAFFh – FFEA00h
		4KB	FE9FFFh – FE9000h	256 Bytes	FFE9FFh – FFE900h
		4KB	FE8FFFh – FE8000h	256 Bytes	FFE8FFh – FFE800h
	Block 508	4KB	FE7FFFh – FE7000h	⋮	
		4KB	FE6FFFh – FE6000h		
		4KB	FE5FFFh – FE5000h		
		4KB	FE4FFFh – FE4000h	256 Bytes	0017FFh – 001700h
		4KB	FE3FFFh – FE3000h	256 Bytes	0016FFh – 001600h
		4KB	FE2FFFh – FE2000h	256 Bytes	0015FFh – 001500h
		4KB	FE1FFFh – FE1000h	256 Bytes	0014FFh – 001400h
		4KB	FE0FFFh – FE0000h	256 Bytes	0013FFh – 001300h
⋮	⋮	⋮		256 Bytes	0012FFh – 001200h
				256 Bytes	0011FFh – 001100h
				256 Bytes	0010FFh – 001000h
Sector 0	Block 1	4KB	00FFFFh – 00F000h	256 Bytes	000FFFh – 000F00h
		4KB	00EFFFh – 00E000h	256 Bytes	000EFFh – 000E00h
		4KB	00DFFFh – 00D000h	256 Bytes	000DFFh – 000D00h
		4KB	00CFFFh – 00C000h	256 Bytes	000CFFh – 000C00h
		4KB	00BFFFh – 00B000h	256 Bytes	000BFFh – 000B00h
		4KB	00AFFFh – 00A000h	256 Bytes	000AFFh – 000A00h
		4KB	009FFFh – 009000h	256 Bytes	0009FFh – 000900h
		4KB	008FFFh – 008000h	256 Bytes	0008FFh – 000800h
	Block 0	4KB	007FFFh – 007000h	256 Bytes	0007FFh – 000700h
		4KB	006FFFh – 006000h	256 Bytes	0006FFh – 000600h
		4KB	005FFFh – 005000h	256 Bytes	0005FFh – 000500h
		4KB	004FFFh – 004000h	256 Bytes	0004FFh – 000400h
		4KB	003FFFh – 003000h	256 Bytes	0003FFh – 000300h
		4KB	002FFFh – 002000h	256 Bytes	0002FFh – 000200h
		4KB	001FFFh – 001000h	256 Bytes	0001FFh – 000100h
		4KB	000FFFh – 000000h	256 Bytes	0000FFh – 000000h

4. Device Operation

4.1 Standard SPI Operation

The AT25SL128A features a serial peripheral interface on four signals: Serial Clock (SCK). Chip Select ($\overline{CS}$), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI instructions use the SI input pin to serially write instructions, addresses or data to the device on the rising edge of SCK. The SO output pin is used to read data or status from the device on the falling edge of SCK.

SPI bus operation Modes 0 (0, 0) and 3 (1, 1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the SCK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the SCK signal is normally low on the falling and rising edges of $\overline{CS}$. For Mode 3 the SCK signal is normally high on the falling and rising edges of $\overline{CS}$.

4.2 Dual SPI Operation

The AT25SL128A supports Dual SPI operation. This instruction allows data to be transferred to or from the device at two times the rate of the standard SPI. The Dual Read instruction is ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XIP). When using Dual SPI instructions the SI and SO pins become bidirectional I/0 pins; IO_0 and IO_1.

4.3 Quad SPI Operation

The AT25SL128A supports Quad SPI operation. This instruction allows data to be transferred to or from the device at four times the rate of the standard SPI. The Quad Read instruction offers a significant improvement in continuous and random access transfer rates allowing fast code- shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instruction the SI and SO pins become bidirectional IO_0 and IO_1, and the $\overline{WP}$ and $\overline{HOLD}$ pins become IO_2 and IO_3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

4.4 QPI Operation

The AT25SL128A supports Quad Peripheral Interface (QPI) operation when the device is switched from Standard/ Dual/ Quad SPI mode to QPI mode using the “Enable QPI (38h)” instruction. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the SI and SO pins become bidirectional IO0 and IO1, and the $\overline{WP}$ and $\overline{HOLD}$ pins become IO_2 and IO_3 respectively.

The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via SI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/ Dual/ Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time, “Enable QPI” and “Disable QPI/ Disable QPI 2” instructions are used to switch between these two modes. Upon power-up or after software reset using “Reset (99h) instruction, the default state of the device is Standard/ Dual/ Quad SPI mode.

5. Write Protection

To protect inadvertent writes by the possible noise, several means of protection are applied to the Flash memory.

5.1 Write Protect Features

- While Power-on reset, all operations are disabled and no instruction is recognized.
- An internal time delay of tPUW can protect the data against inadvertent changes while the power supply is outside the operating specification. This includes the Write Enable, Page program, Block Erase, Chip Erase, Write Security Register and the Write Status Register instructions.
- For data changes, Write Enable instruction must be issued to set the Write Enable Latch (WEL) bit to “0”. Power-up, Completion of Write Disable, Write Status Register, Page program, Block Erase and Chip Erase are subjected to this condition.
- Using setting the Status Register protect (SRP) and Block protect (SEC, TB, BP2, BP1, and BP0) bits a portion of memory can be configured as reading only called software protection.
- Write Protect ($\overline{WP}$) pin can control to change the Status Register under hardware control.
- The Deep Power Down mode provides extra protection from unexpected data changes as all instructions are ignored under this status except for Release Deep Power Down instruction.

6. Status Register

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled the state of write protection and the Quad SPI setting. The Write Status Register instruction can be used to configure the devices writes protection features and Quad SPI setting. Write access to the Status Register is controlled by in some cases of the $\overline{WP}$ pin.

Table 6-1. Status Register-1

S7	S6	S5	S4	S3	S2	S1	S0
SRP	SEC	TB	BP2	BP1	BP0	WEL	BUSY
Status Register Protect 0 (Non-Volatile)	Sector Protect (Non-Volatile)	Top/Bottom Write Protect (Non-Volatile)	Block Protect (Non-Volatile)	Block Protect (Non-Volatile)	Block Protect (Non-Volatile)	Write Enable Latch	Erase or Write in Progress

Table 6-2. Status Register-2

S15	S14	S13	S12	S11	S10	S9	S8
SUS	CMP	(R)	(R)	(R)	(R)	QE	SRP1
Suspend Status	Complement Protect (Non-Volatile)	Reserved	Reserved	Reserved	Reserved	Quad Enable (Non- Volatile)	Register Protect 1 (Non- Volatile)

6.1 Busy

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Erase, Write Status Register or Write Security Register instruction. During this time the device will ignore further instruction except for the Read Status Register and Erase / Program Suspend instruction (see tW, tPP, tSE, tBE1, tBE2 and tCE in AC Characteristics). When the Program, Erase, Write Status Register or Write Security Register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

6.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable instruction. The WEL status bit is cleared to a 0 when device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Erase and Write Status Register.

6.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide write protection control and status. Block protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

6.4 Top/Bottom Block protect (TB)

The Top/Bottom bit (TB) is non-volatile bits in the status register (S5) that controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

6.5 Sector/Block Protect (SEC)

The Sector protect bit (SEC) is non-volatile bits in the status register (S6) that controls if the Block Protect Bits (BP2, BP1, BP0) protect 4KB Sectors (SEC=1)or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory protection table. The default setting is SEC=0.

6.6 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

SRP1	SRP0	$\overline{WP}$	Status Register	Description
0	0	X	Software Protection	$\overline{WP}$ pin no control. The register can be written to After a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When $\overline{WP}$ pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When $\overline{WP}$ pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power down, power-up cycle(1)
1	1	X	One Time Program	Status Register is permanently protected and cannot be written to.

Note: 1. When SRP1, SRP0=(1,0), a power down, power-up cycle will change SRP1, SRP0 to(0,0) state.

6.7 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad operation. When the QE bit is set to a 0 state (factory default) the $\overline{WP}$ pin and $\overline{HOLD}$ are enabled. When the QE pin is set to a 1 the Quad IO2 and IO3 pins are enabled. **WARNING : The QE bit should never be set to a 1 during standard SPI or Dual SPI operation if the $\overline{WP}$ or $\overline{HOLD}$ pins are tied directly to the power supply or ground.**

6.8 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4KB sector can be protected while the rest of the array is not; when CMP=1, the top 4KB sector will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

6.9 Erase/Program Suspend Status (SUS)

The Suspend Status bit (SUS) is a read only bit in the status register (S15) that is set to 1 after executing an Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power down, power-up cycle.

Table 6-3. Status Register Memory Protection (CMP = 0)

STATUS REGISTER					MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	SECTOR(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 thru 255	FC0000h-FFFFFFh	256KB	Upper 1/64
0	0	0	1	0	248 thru 255	F80000h-FFFFFFh	512KB	Upper 1/32
0	0	0	1	1	240 thru 255	F00000h-FFFFFFh	1MB	Upper 1/16
0	0	1	0	0	224 thru 255	E00000h-FFFFFFh	2MB	Upper 1/8
0	0	1	0	1	192 thru 255	C00000h-FFFFFFh	4MB	Upper 1/4
0	0	1	1	0	128 thru 255	800000h-FFFFFFh	8MB	Upper 1/2
0	1	0	0	1	0 thru 3	000000h-03FFFFh	256KB	Lower 1/64
0	1	0	1	0	0 thru 7	000000h-07FFFFh	512KB	Lower 1/32
0	1	0	1	1	0 thru 15	000000h-0FFFFFh	1MB	Lower 1/16
0	1	1	0	0	0 thru 31	000000h-1FFFFFh	2MB	Lower 1/8
0	1	1	0	1	0 thru 63	000000h-3FFFFFh	4MB	Lower 1/4
0	1	1	1	0	0 thru 127	000000h-7FFFFFh	8MB	Lower 1/2
X	X	1	1	1	0 thru 255	000000h-FFFFFFh	16MB	ALL
1	0	0	0	1	255	FFF000h-FFFFFFh	4KB	U – 1/4096 (See Note 4)
1	0	0	1	0	255	FFE000h-FFFFFFh	8KB	U – 1/2048
1	0	0	1	1	255	FFC000h-FFFFFFh	16KB	U – 1/1024
1	0	1	0	X	255	FF8000h-FFFFFFh	32KB	U – 1/512
1	1	0	0	1	0	000000h-000FFFh	4KB	L – 1/4096
1	1	0	1	0	0	000000h-001FFFh	8KB	L – 1/2048
1	1	0	1	1	0	000000h-003FFFh	16KB	L – 1/1024
1	1	1	0	X	0	000000h-007FFFh	32KB	L – 1/512

Note:

1. X = Don't care
2. L = Lower; U = Upper
3. If any Erase or Program instruction specifies a memory region that contains protected data portion, this instruction will be ignored.
4. Note 3 does not apply to this Status Register Bit setting. See Errata 1 in Appendix A for details.

Table 6-4. Status Register Memory Protection (CMP = 1)

STATUS REGISTER					MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	SECTOR(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	0 thru 255	000000h - FFFFFFh	16MB	ALL
0	0	0	0	1	0 thru 251	000000h – FBFFFFh	16,128KB	Lower 63/64
0	0	0	1	0	0 and 247	000000h – F7FFFFh	15,872KB	Lower 31/32
0	0	0	1	1	0 thru 239	000000h – EFFFFFh	15MB	Lower 15/16
0	0	1	0	0	0 thru 223	000000h – DFFFFFh	14MB	Lower 7/8
0	0	1	0	1	0 thru 191	000000h – BFFFFFh	12MB	Lower 3/4
0	0	1	1	0	0 thru 127	000000h – 7FFFFFh	8MB	Lower 1/2
0	1	0	0	1	4 thru 255	040000h - FFFFFFh	16,128KB	Upper 63/64
0	1	0	1	0	8 and 255	080000h - FFFFFFh	15,872KB	Upper 31/32
0	1	0	1	1	16 thru 255	100000h - FFFFFFh	15MB	Upper 15/16
0	1	1	0	0	32 thru 255	200000h - FFFFFFh	14MB	Upper 7/8
0	1	1	0	1	64 thru 255	400000h - FFFFFFh	12MB	Upper 3/4
0	1	1	1	0	128 thru 255	800000h - FFFFFFh	8MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 255	000000h - FFEFFFh	16,380KB	L – 4095/4096
1	0	0	1	0	0 thru 255	000000h - FFDFFFh	16,376KB	L – 2047/2048
1	0	0	1	1	0 thru 255	000000h - FFBFFFh	16,368KB	L – 1023/1024
1	0	1	0	X	0 thru 255	000000h - FF7FFFh	16,352KB	L – 511/512
1	1	0	0	1	0 thru 255	001000h - FFFFFFh	16,380KB	U – 4095/4096 (See Note 4)
1	1	0	1	0	0 thru 255	002000h - FFFFFFh	16,376KB	U – 2047/2048
1	1	0	1	1	0 thru 255	004000h - FFFFFFh	16,368KB	U – 1023/1024
1	1	1	0	X	0 thru 255	008000h - FFFFFFh	16,352KB	U – 511/512

Note:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program instruction specifies a memory region that contains protected data portion, this instruction will be ignored.
4. Note 3 does not apply to this Status Register Bit setting. See Errata 2 in Appendix A for details.

7. Instructions

The SPI instruction set of the AT25SL128A consists of thirty eight basic instructions and the QPI instruction set of the AT25SL128A consists of thirty one basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select ($\overline{CS}$). The first byte of data clocked into the input pins (SI or IO [3:0]) provides the instruction code. Data on the SI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions are completed with the rising edge of edge $\overline{CS}$. Clock relative timing diagrams for each instruction are included in figures 8-1 through 8-66 All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte ($\overline{CS}$ driven high after a full 8-bit have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Register will be ignored until the program or erase cycle has completed.

Table 7-1. Manufacturer and Device Identification

		ID code	Instruction
Manufacturer ID	Adesto	1Fh	90h, 92h, 94h, 9Fh
Device ID	AT25SL128A	17h	90h, 92h, 94h, ABh
Memory Type ID	SPI / QPI	42h	9Fh
Capacity Type ID	128M	18h	9Fh

7.1 Instruction Set Tables

Table 7-2. Instruction Set Table 1 (SPI instruction)(1)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
(CLOCK NUMBER)	(0 – 7)	(8 - 15)	(16 - 23)	(24 - 31)	(32 - 39)	(40 - 47)
Write Enable	**06h**					
Write Enable For Volatile Status Register	**50h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(SR7-SR0)(2)				
Read Status Register-2	**35h**	(SR15-SR8)(2)				
Write Status Register-1	**01h**	(SR7-SR0)	(SR15-SR8)			
Write Status Register-2	**31h**	(SR15-SR8)				
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read Data	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Page Program	**02h**	A23-A16	A15-A8	A7-A0	(D7-D0)(3)	
Enable QPI	**38h**					
Block Erase(4KB)	**20h**	A23-A16	A15-A8	A7-A0		

7.1 Instruction Set Tables

Table 7-2. Instruction Set Table 1 (SPI instruction)[1]

Block Erase(32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase(64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Chip Erase	**60h/C7h**					
Erase/Program Suspend	**75h**					
Erase/Program Resume	**7Ah**					
Deep Power Down	**B9h**					
Release Deep power down/ Device ID[4]	**ABh**	dummy	dummy	dummy	(ID7-ID0)[2]	
Read Manufacturer/ Device ID[4]	**90h**	00h	00h	00h or 01h	(MID7-MID0)	(DID7-DID0)
Read JEDEC ID	**9Fh**	(MID7-MID0)	(D7-D0)	(D7-D0)		
Reset Enable	**66h**					
Reset	**99h**					
Enter Secured OTP	**B1h**					
Exit Secured OTP	**C1h**					
Read Security Register	**2Bh**	(SC7-SC0) [10]				
Write Security Register	**2Fh**					
Read Serial Flash Discovery Parameter	**5Ah**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)

Table 7-3. Instruction Set Table 2 (Dual SPI Instruction)

INSTRUCTION (CLOCK NUMBER)	(0 – 7)	(8 - 15)	(16 - 23)	(24 - 31)	(32 - 39)	(40 - 47)
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)[6]
Fast Read Dual I/O	**BBh**	A23-A8[5]	A7-A0,	(D7-D0, …)[6]		
Read Dual Manufacturer/ Device ID[4]	**92h**	0000h	(00h, xxxx) or (01h, xxxx)	(MID7-MID0) (DID7-DID0)[6]		

Table 7-4. Instruction Set Table 3 (Quad SPI Instruction)

INSTRUCTION (CLOCK NUMBER)	(0 – 7)	(8 - 15)	(16 - 23)	(24 - 31)	(32 - 39)	(40 - 47)
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) [8]
Fast Read Quad I/O	**EBh**	A23-A0, M7-M0[7]	(xxx, D7-D0,…)[9]	(D7-D0, …)[8]		
Quad Page Program	**33h**	A23-A0 (D7-D0, …)[8]				

Table 7-4. Instruction Set Table 3 (Quad SPI Instruction)

Read Quad Manufacturer /Device ID[4]	**94h**	(00_0000h, xx) or (00_0001h, xx)	(xxxx, MID7-MID0) (xxxx, DID7-DID0)[9]		
Word Read Quad I/O	**E7h**	A23-A0, M7-M0[7]	(xx, D7-D0..)	(D7-D0)[8]	
Set Burst with Wrap	**77h**	xxxxxx, W6-W4[7]			

Table 7-5. Instruction Set Table 4 (QPI instruction)

INSTRUCTION		BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8	BYTE 9
(CLOCK NUMBER)		(0 , 1)	(2 , 3)	(4 , 5)	(6 , 7)	(8 , 9)	(10 , 11)	(12 , 13)	(14 , 15)	(16 , 17)
Write Enable		**06h**								
Write Enable for Volatile		**50h**								
Write Disable		**04h**								
Read Status Register-1		**05h**	(SR7-SR0)[2]							
Read Status Register-2		**35h**	(SR15-SR8)[2]							
Write Status Register-1[5]		**01h**	(SR7-SR0)	(SR15-SR8)						
Write Status Register-2		**31h**	(SR15-SR8)							
Fast Read Data	>80MHz	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)		
	>104MHz		A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	(D7-D0)	
Page Program		**02h**	A23-A16	A15-A8	A7-A0	(D7-D0)[3]				
Block Erase(4KB)		**20h**	A23-A16	A15-A8	A7-A0					
Block Erase(32KB)		**52h**	A23-A16	A15-A8	A7-A0					
Block Erase(64KB)		**D8h**	A23-A16	A15-A8	A7-A0					
Chip Erase		**60h/ C7h**								
Erase/Program Suspend		**75h**								
Erase/Program Resume		**7Ah**								
Deep Power Down		**B9h**								
Release Deep Power Down		**ABh**								
Read Manufacturer/Device ID[4]		**90h**	00h	00h	00h or 01h	(MID7-MID0)	(DID7-DID0)			
Read JEDEC ID[4]		**9Fh**	(MID7-MID0) Manufacturer	(D7-D0) Memory Type	(D7-D0) Capacity Type					
Enter Security		**B1h**								
Exit Security		**C1h**								

Table 7-5. Instruction Set Table 4 (QPI instruction)

Read Security Register		**2Bh**	(SC7-SC0) (10)							
Write Security Register		**2Fh**								
Fast Read Quad I/O	>80MHz	**EBh**	A23-A16	A15-A8	A7-A0	(M7-M0)	dummy	(D7-D0)		
	>104MHz		A23-A16	A15-A8	A7-A0	(M7-M0)	dummy	dummy	(D7-D0)	
Reset Enable		**66h**								
Reset		**99h**								
Disable QPI		**FFh**								
Burst Read with Wrap	>80MHz	**0Ch**	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)		
	>104MHz		A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	(D7-D0)	
Set Read Parameter		**C0h**	P7-P0							
Quad Page Program		**33h**	A23-A16	A15-A8	A7-A0	(D7-D0)				

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data being read from the device on the IO pin.
2. SR = status register, The Status Register contents and Device ID will repeat continuously until $\overline{CS}$ terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Register, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. See Manufacturer and Device Identification table for Device ID information.
5. Dual Input Address
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
6. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
7. Quad Input Address

   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

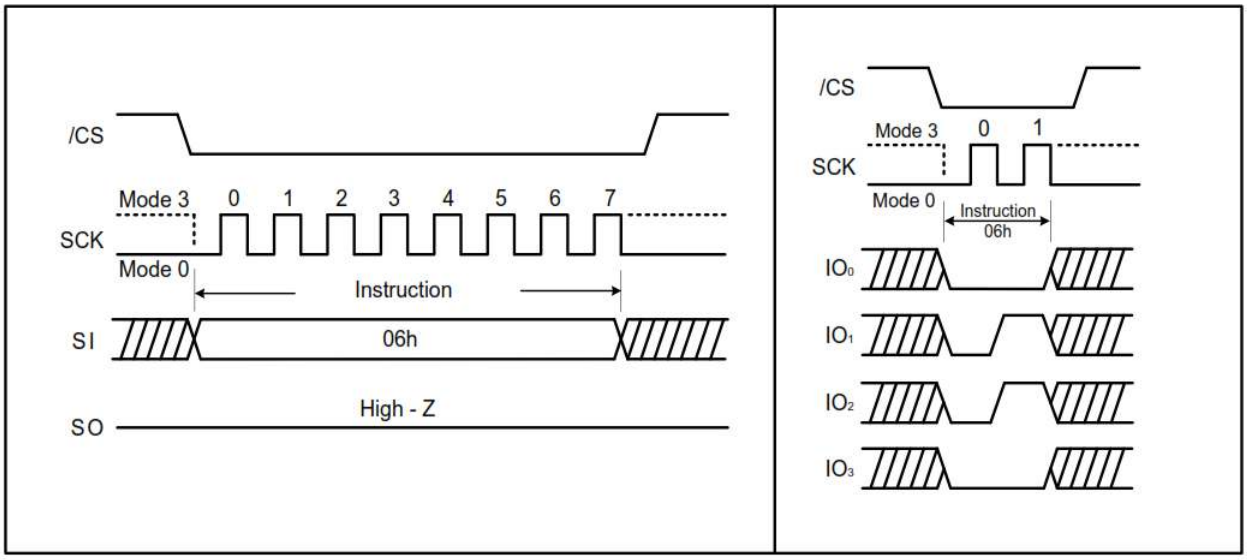
   Set Burst with Wrap Input

   IO0 = x, x, x, x, x, x, W4, x
   IO1 = x, x, x, x, x, x, W5, x
   IO2 = x, x, x, x, x, x, W6, x
   IO3 = x, x, x, x, x, x, x x
8. Quad Input/ Output Data
   IO0 = (D4, D0…)
   IO1 = (D5, D1…)
   IO2 = (D6, D2…)
   IO3 = (D7, D3…)
9. Fast Read Quad I/O Data Output
   IO0 = (x, x, x, x, D4, D0…)
   IO1 = (x, x, x, x, D5, D1…)
   IO2 = (x, x, x, x, D6, D2…)
   IO3 = (x, x, x, x, D7, D3…)
10. SC = security register

7.2 Write Enable (06h)

Write Enable instruction is for setting the Write Enable Latch (WEL) bit in the Status Register. The WEL bit must be set prior to every Program, Erase and Write Status Register instruction. To enter the Write Enable instruction, $\overline{CS}$ goes low prior to the instruction "06h" into Data Input (SI) pin on the rising edge of SCK, and then driving $\overline{CS}$ high.

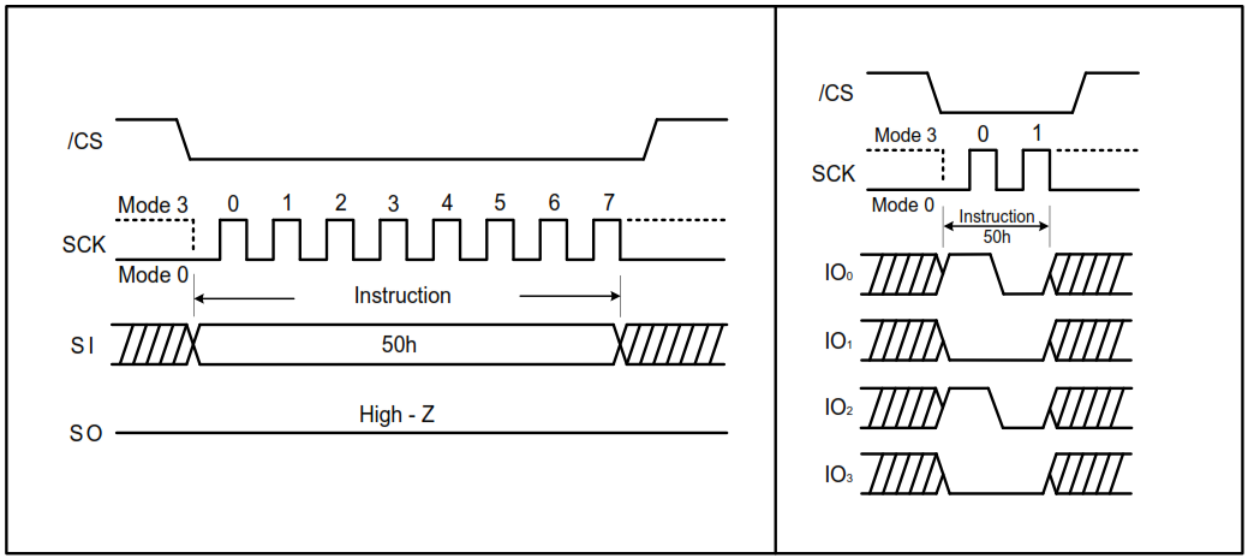
Figure 7-1. Write Enable Instruction for SPI Mode (left) and QPI Mode (right)



7.3 Write Enable for Volatile Status Register (50h)

This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 7-2) will not set the Write Enable Latch (WEL) bit. Once Write Enable for Volatile Status Register is set, a Write Enable instruction should not have been issued prior to setting Write Status Register instruction (01h or 31h). When Write Enable for Volatile Status Register (50h) is set in QPI Mode, the SUS bit (S15) and Reserved bits (S13, S12, S11 and S10) of the Status Register-2 must be driven to high after Write Status Register instruction(01h).Once Read Status Register (05h or 31h) is issued the read values of SUS bit (S15) and Reserved bits (S13, S12, S11 and S10) of the Status Register-2 are ignored.

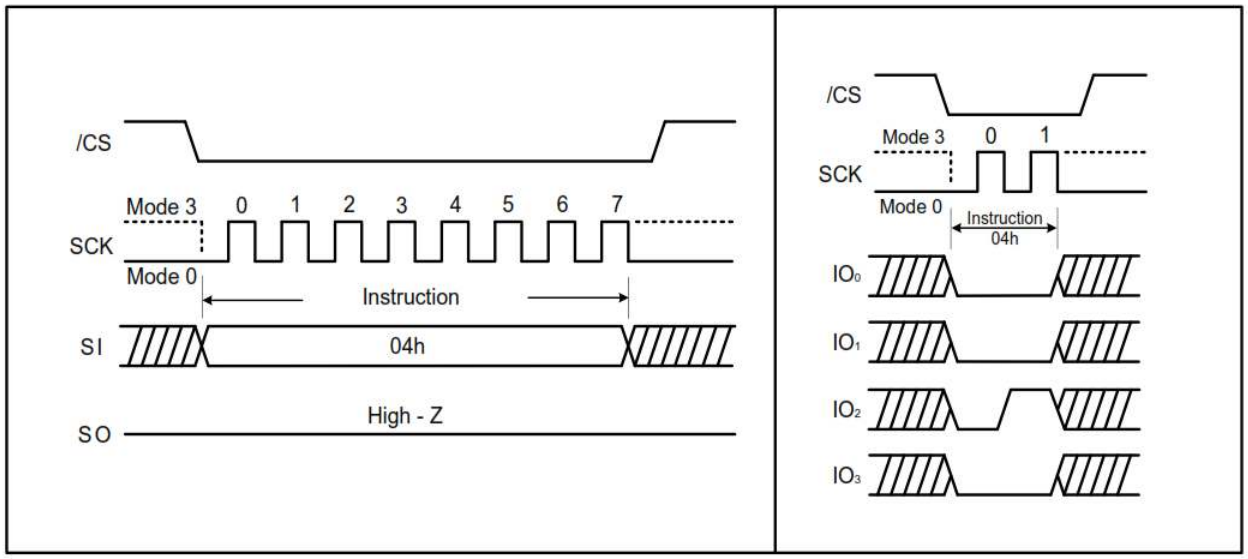
Figure 7-2. Write Enable for Volatile Status Register Instruction for SPI Mode (left) and QPI Mode (right)



7.4 Write Disable (04h)

The Write Disable instruction is to reset the Write Enable Latch (WEL) bit in the Status Register. To enter the Write Disable instruction, $\overline{CS}$ goes low prior to the instruction “04h” into Data Input (SI) pin on the rising edge of SCK, and then driving $\overline{CS}$ high. WEL bit is automatically reset write- disable status of “0” after Power-up and upon completion of the every Program, Erase and Write Status Register instructions.

Figure 7-3. Write Disable Instruction for SPI Mode (left) and QPI Mode (right)



7.5 Read Status Register-1 (05h) and Read Status Register-2 (35h)

The Read Status Register instructions are to read the Status Register. The Read Status Register can be read at any time (even in program/erase/write Status Register and Write Security Register condition). It is recommended to check the BUSY bit before sending a new instruction when a Program, Erase, Write Status Register or Write Status Register operation is in progress.

The instruction is entered by driving $\overline{CS}$ low and sending the instruction code “05h” for Status Register-1 or “35h” for Status Register-2 into the SI pin on the rising edge of SCK. The status register bits are then shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first as shown in (Figure 7-4 and Figure 7-5). The Status Register can be read continuously. The instruction is completed by driving $\overline{CS}$ high.

Figure 7-4. Read Status Register Instruction (SPI Mode)

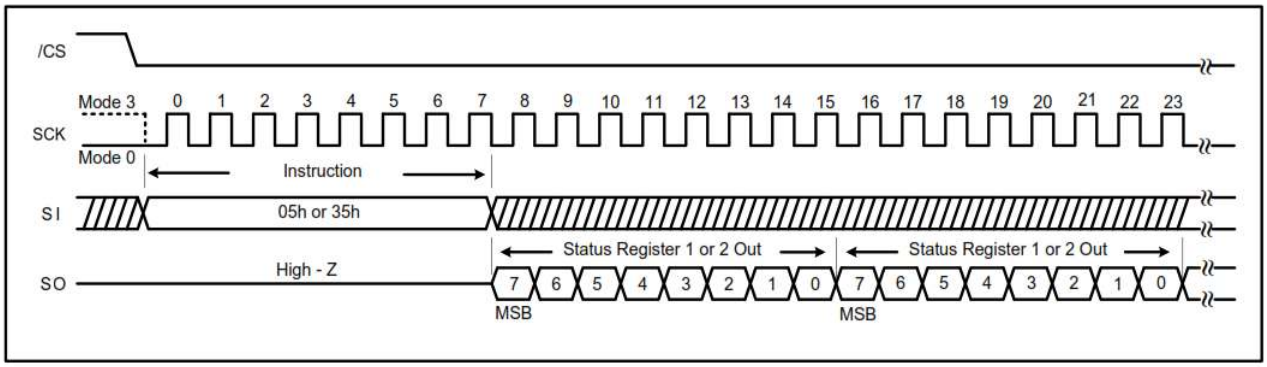
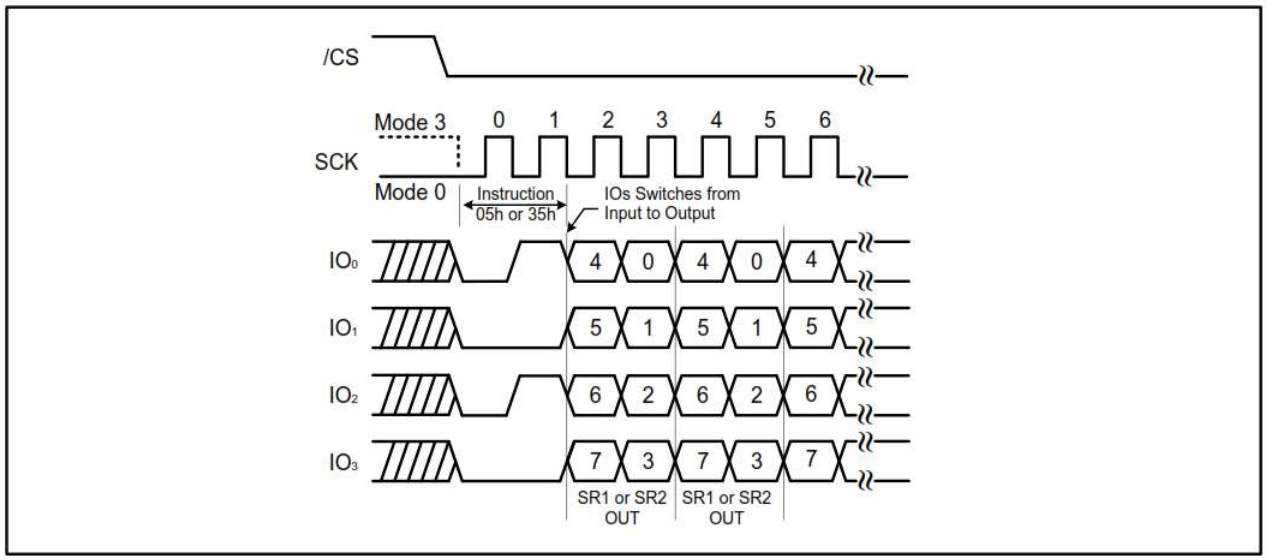


Figure 7-5. Read Status Register Instruction (QPI Mode)



7.6 Write Status Register (01h)

The Write Status Register instruction is to write only non-volatile Status Register-1 bits (SRP0) and Status Register-2 bits (QE and SRP1). All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

A Write Enable instruction must previously have been issued prior to setting Write Status Register Instruction (Status Register bit WEL must equal 1). Once write is enabled, the instruction is entered by driving $\overline{CS}$ low, sending the instruction code, and then writing the status register data byte as illustrated in Figure 7-6 and Figure 7-7.

The $\overline{CS}$ pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done the Write Status Register instruction will not be executed. If $\overline{CS}$ is driven high after the eighth clock, the QE and SRP1 bits will be cleared to 0. After $\overline{CS}$ is driven high, the self- timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics).

While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in Status Register will be cleared to 0.

Figure 7-6. Write Status Register Instruction (SPI Mode)

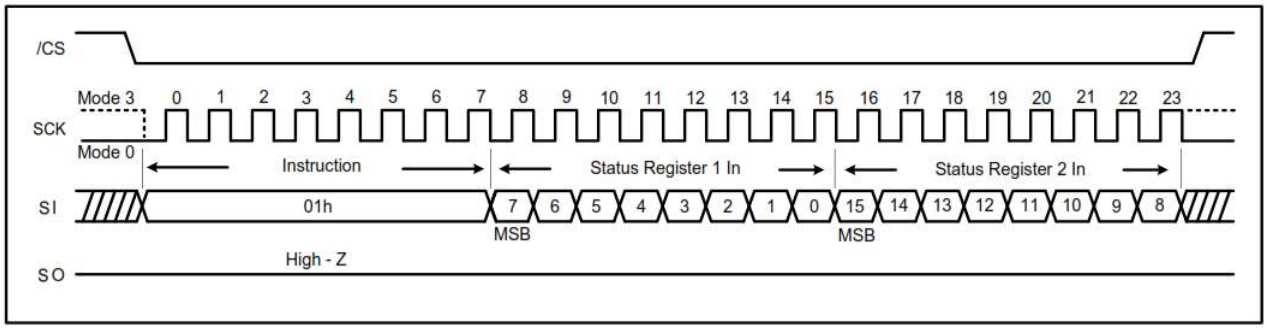
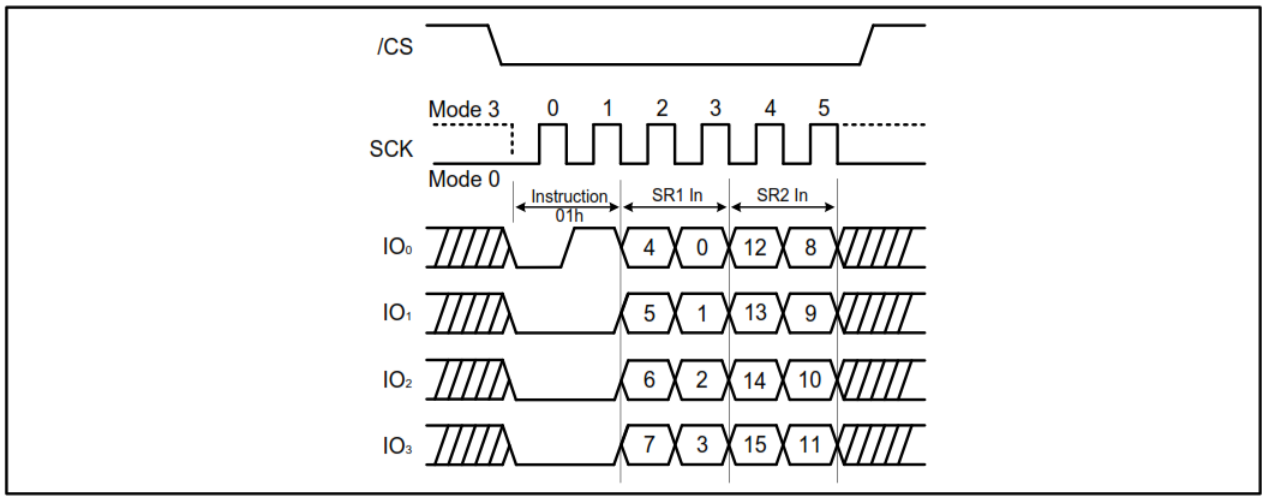


Figure 7-7. Write Status Register Instruction (QPI Mode)



7.7 Write Status Register-2 (31h)

The Write Status Register-2 instruction is to write only non-volatile Status Register-2 bits (QE and SRP1).

A Write Enable instruction must previously have been issued prior to setting Write Status Register Instruction (Status Register bit WEL must equal 1). Once write is enabled, the instruction is entered by driving $\overline{CS}$ low, sending the instruction code, and then writing the status register data byte as illustrated in Figure 7-8 and Figure 7-9.

Using Write Status Register-2 (31h) instruction, software can individually access each one-byte status registers via different instructions.

Figure 7-8. Write Status Register-2 Instruction (SPI Mode)

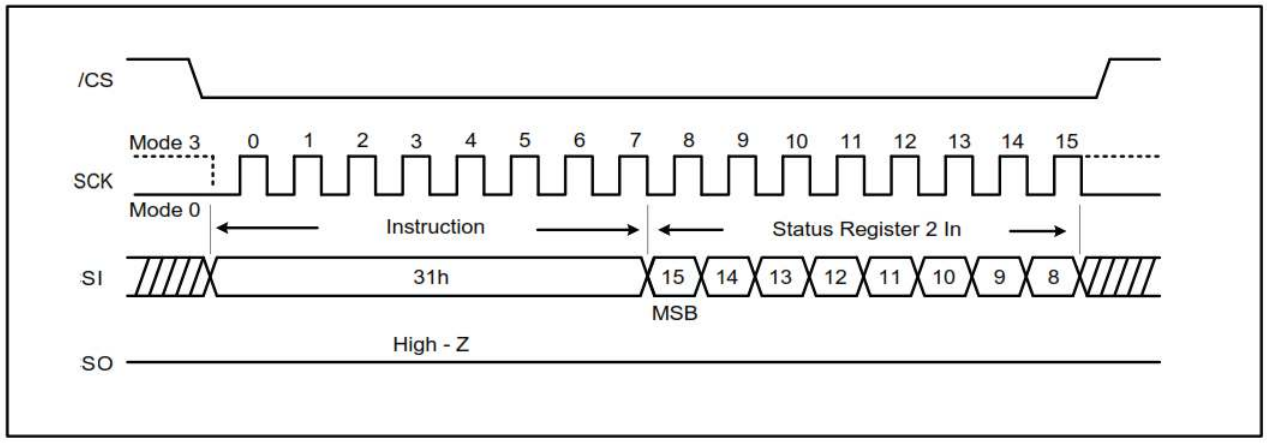
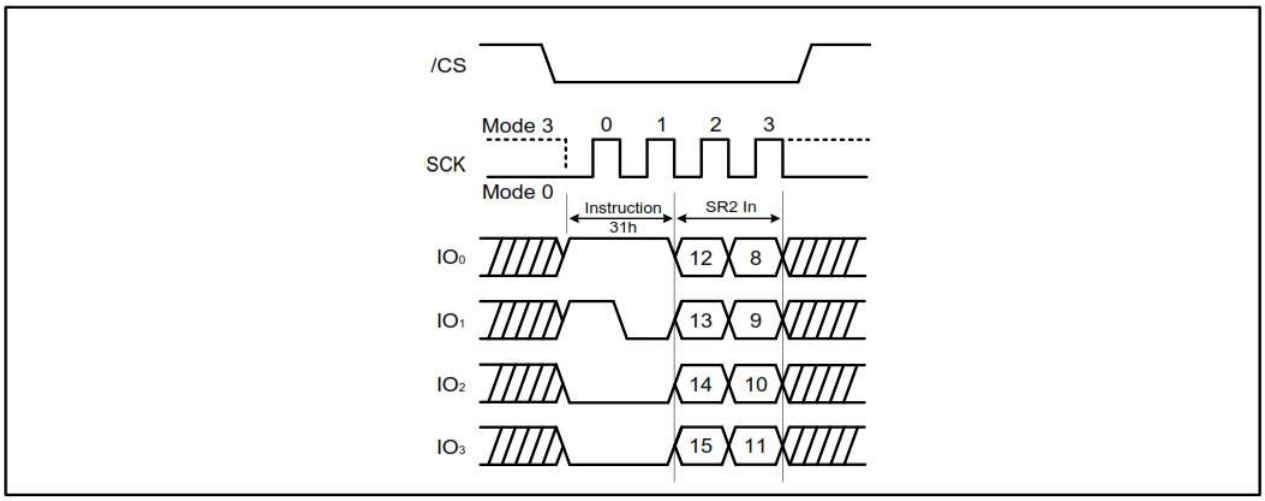


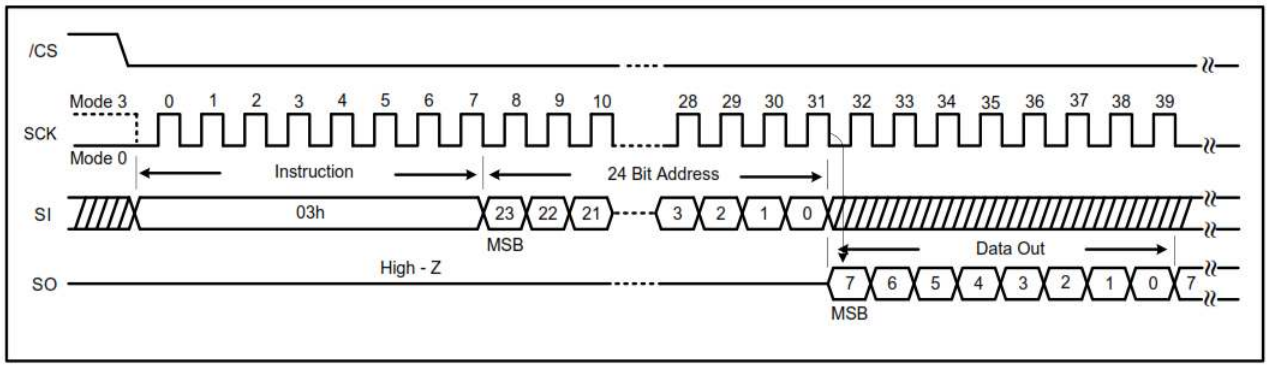
Figure 7-9. Write Status Register-2 Instruction (QPI Mode)



7.8 Read Data (03h)

The Read Data instruction is to read data out from the device. The instruction is initiated by driving the $\overline{CS}$ pin low and then sending the instruction code “03h” with following a 24-bit address (A23- A0) into the SI pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving $\overline{CS}$ high. The Read Data instruction sequence is shown in Figure 7-10. If a Read Data instruction is issued while an Erase, Program or Write Status Register cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C to a maximum of f_R (see AC Electrical Characteristics).

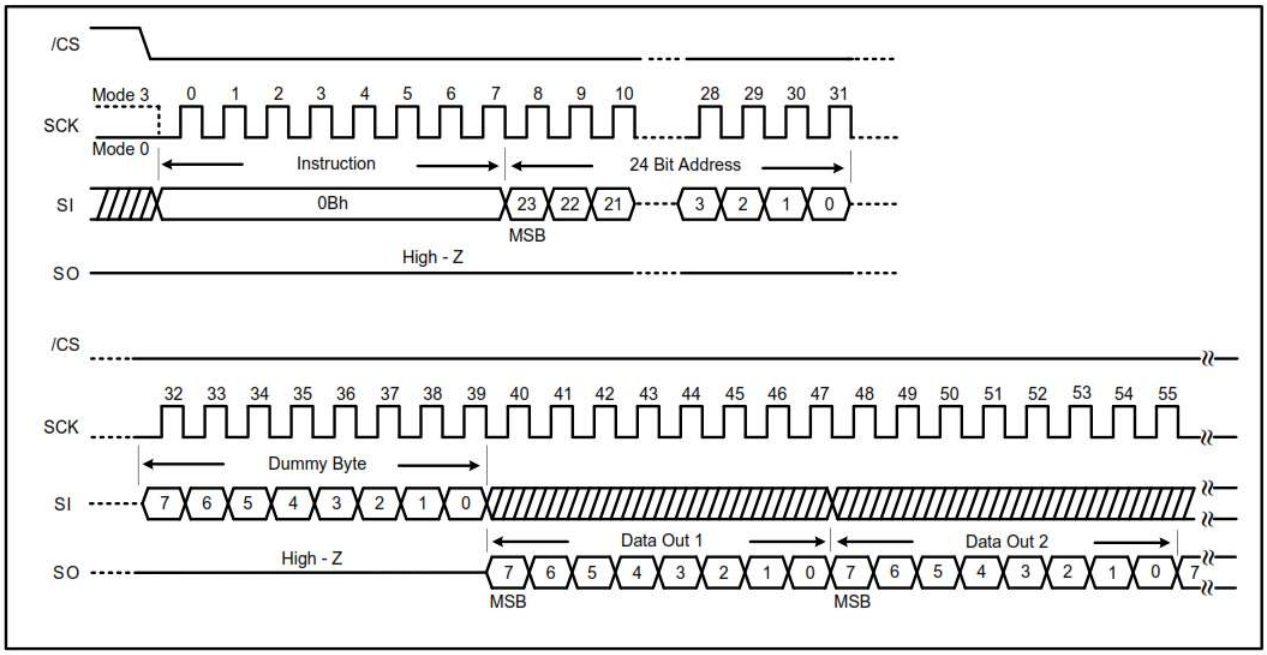
Figure 7-10. Read Data Instruction



7.9 Fast Read (0Bh)

The Fast Read instruction is high speed reading mode that it can operate at the highest possible frequency of F_R. The address is latched on the rising edge of the SCK. After the 24-bit address, this is accomplished by adding “dummy” clocks as shown in Figure 7-11. The dummy clocks means the internal circuits require time to set up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. Data of each bit shifts out on the falling edge of SCK.

Figure 7-11. Fast Read Instruction (SPI Mode)



7.10 Fast Read in QPI Mode

When QPI mode is enabled, the number of dummy clock is configured by the “Set Read Parameters (C0h)” instruction to accommodate wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bit P[4] and P[5] setting, the number of dummy clocks can be configured as either 4, or 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 4. (Please refer to Figure 7-12, Figure 7-13 and Figure 7.11).

Figure 7-12. Fast Read instruction (QPI Mode, 80MHz)

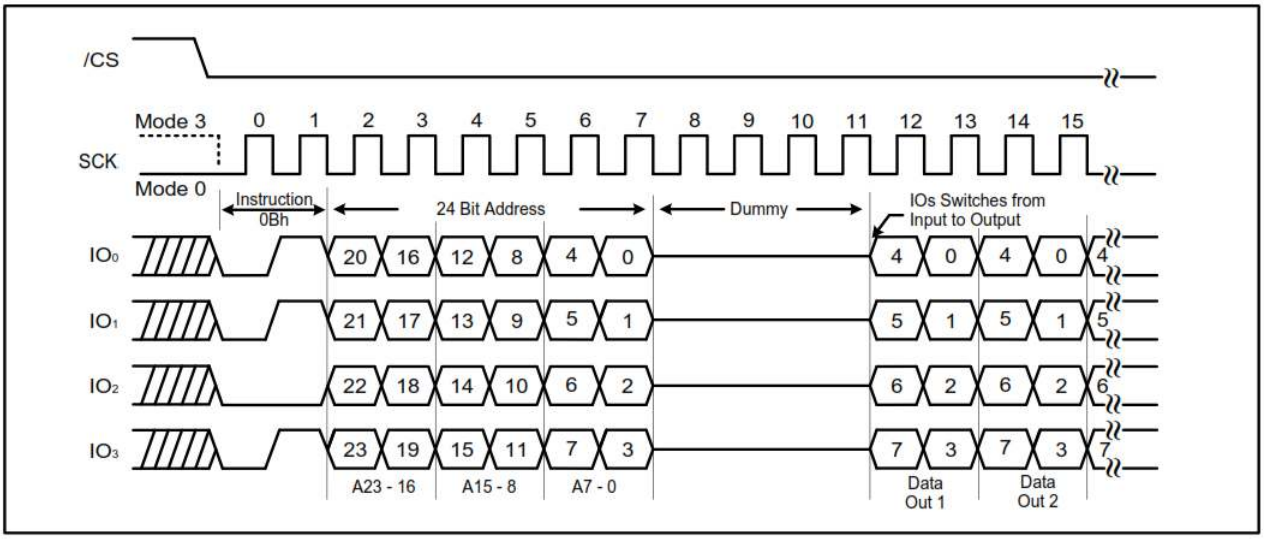
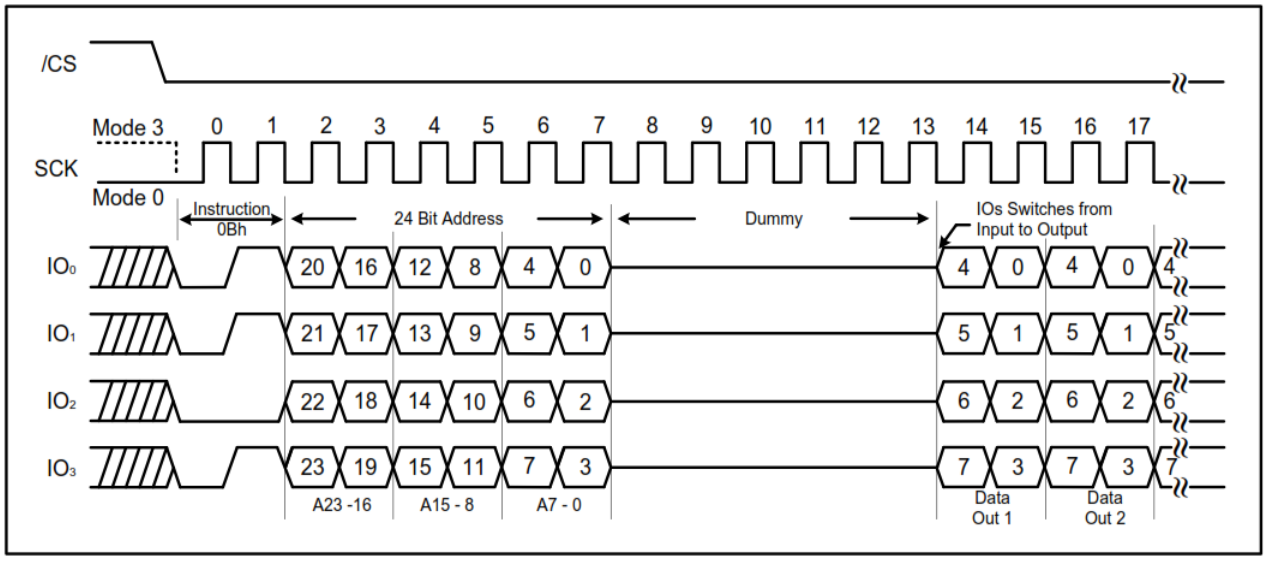


Figure 7-13. Fast Read instruction (QPI Mode, 104MHz)

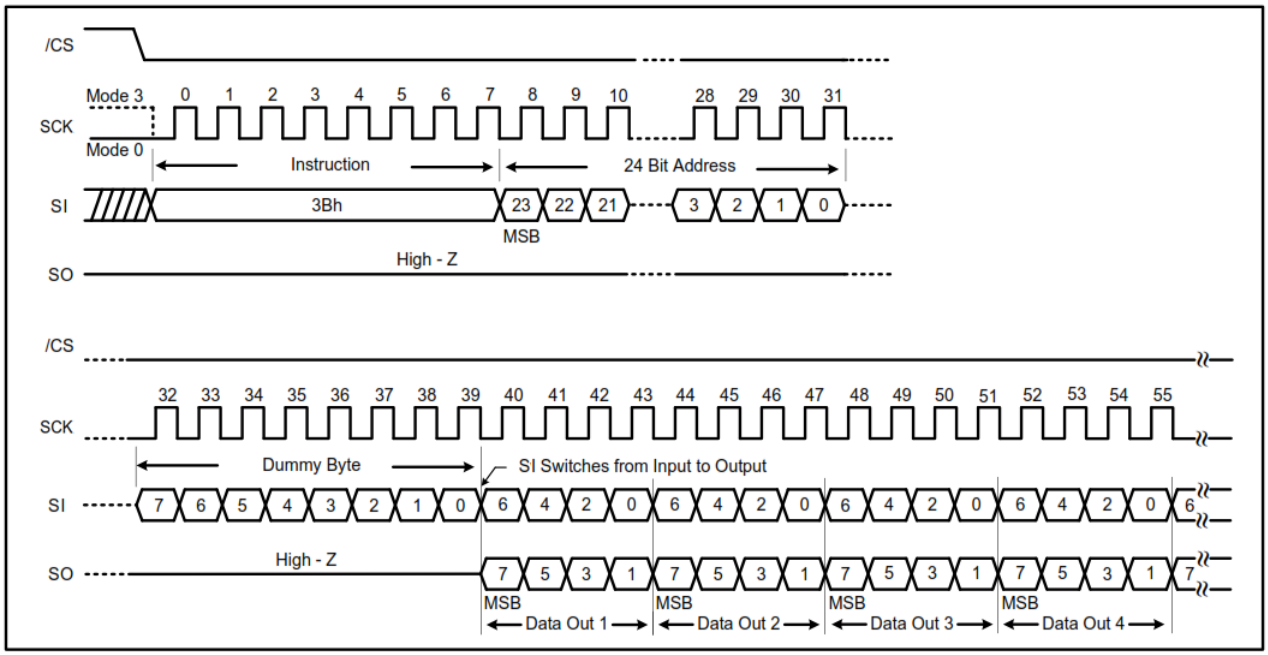


7.11 Fast Read Dual Output (3Bh)

By using two pins (IO_0 and IO_1, instead of just IO_0), The Fast Read Dual Output instruction allows data to be transferred from the AT25SL128A at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for application that cache code-segments to RAM for execution.

The Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). After the 24-bit address, this is accomplished by adding eight “dummy” clocks as shown in Figure 7-14. The dummy clocks allow the internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

Figure 7-14. Fast Read Dual Output instruction (SPI Mode)



7.12 Fast Read Quad Output (6Bh)

By using four pins (IO_0, IO_1, IO_2, and IO_3), The Fast Read Quad Output instruction allows data to be transferred from the AT25SL128A at four times the rate of standard SPI devices. A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output instruction (Status Register bit QE must equal 1).

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24- bit address as shown in Figure 7-15. The dummy clocks allow the internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.